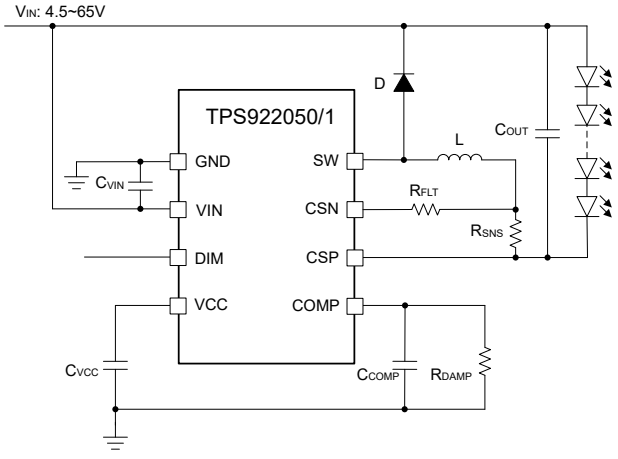
TPS922050/1 65V 1A/2A 降圧 LED ドライバ、PWM / アナログ調光付き

1 特長

- 広い入力電圧範囲 4.5V ～ 65V
- LED は、コモン アノード接続に対応
- 300mΩ MOSFET を内蔵:
  - 標準電流制限 (1.6A / 3.2A)
  - スイッチング周波数 (400kHz / 1MHz)
- 高度な調光オプション:
  - アナログ調光 (200:1)
  - 高速 PWM 調光 (パルス幅 50ns)
- 包括的な保護機能を搭載:
  - LED の断線 / 短絡保護
  - スイッチング FET の断線 / 短絡保護
  - 外部部品の障害保護
  - サイクル単位の電流制限
  - サーマル シャットダウン
- パッケージ:WSON-8、HVSSOP-8、SOT583

2 アプリケーション

- 常時照明:
  - 屋内および屋外照明
  - 家電照明
  - 冷間 / 温間 WLED 照明
  - 緊急用 / サイネージ用照明
  - セキュリティ フラッドライト
  - LED 電球およびランプ
  - LCD バックライト
- 瞬間照明:
  - マシン ビジョンおよびカメラ フラッシュ
  - 火災報知器およびストロボ



概略回路図

3 概要

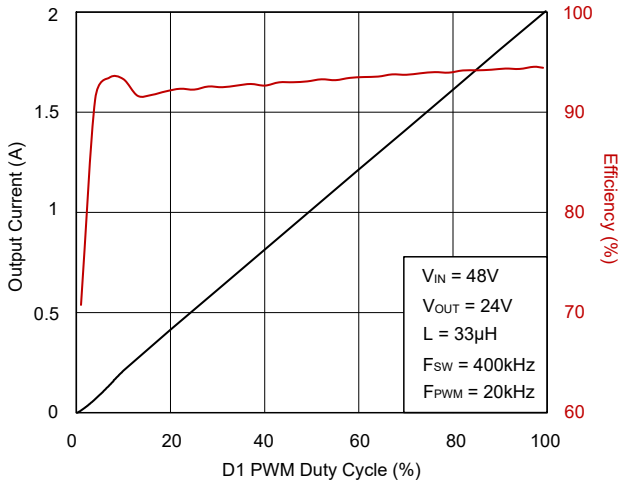
TPS92205x ファミリは、4.5V～65V の広い入力電圧範囲に対応した 1A/2A 非同期昇圧 / 昇降圧 LED ドライバです。ローサイド NMOS を内蔵することにより、このデバイスは高電力密度および高効率で LED を駆動できます。また、このデバイスは、コモン アノード アノード接続および単層 PCB もサポートしています。スイッチング周波数は 400kHz または 1MHz に設定します。

TPS92205x ファミリは、DIM 入力ピンを使用して単純な High 信号と Low 信号を構成することで、PWM 調光をサポートしています。TPS92205x ファミリは、DIM 入力ピンを使用してアナログ電圧信号を構成することで、アナログ調光をサポートしています。このデバイスは、適応型オフ時間電流モード制御とスマートで正確なサンプリングにより、高速 PWM 調光を可能にし、高い調光比を実現します。

TPS92205x ファミリは、LED の断線と短絡、スイッチング FET の断線と短絡、センス抵抗の開放と短絡、サーマル シャットダウンなど、複数の系統的な保護機能も提供します。

製品情報

部品番号	パッケージ	本体サイズ (公称)
TPS922050 TPS922051	WSON (8)	2.0 mm × 2.0mm
	HVSSOP (8)	3.0 mm × 3.0mm
TPS922050	SOT583 (8)	2.0 mm × 1.2mm



調光の直線性と効率

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4 Device Comparison Table

Part Number	Package	Typical Current Limit	Switching Frequency	LED Dimming	Junction Temperature
TPS922051D1DSGR	WSON (8)	3A	400kHz	PWM	-40°C to 125°C
TPS922051D2DSGR	WSON (8)	3A	400kHz	Analog	-40°C to 125°C
TPS922051D1DGNR	HVSSOP (8)	3A	400kHz	PWM	-40°C to 125°C
TPS922051D2DGNR	HVSSOP (8)	3A	400kHz	Analog	-40°C to 125°C
TPS922050D1DSGR	WSON (8)	1.5A	1MHz	PWM	-40°C to 125°C
TPS922050D2DSGR	WSON (8)	1.5A	1MHz	Analog	-40°C to 125°C
TPS922050D1DGNR	HVSSOP (8)	1.5A	1MHz	PWM	-40°C to 125°C
TPS922050D2DGNR	HVSSOP (8)	1.5A	1MHz	Analog	-40°C to 125°C
TPS922050D1DRLR	SOT583 (8)	1.5A	400kHz	PWM	-40°C to 125°C
TPS922050D2DRLR	SOT583 (8)	1.5A	400kHz	Analog	-40°C to 125°C

5 Pin Configuration and Functions

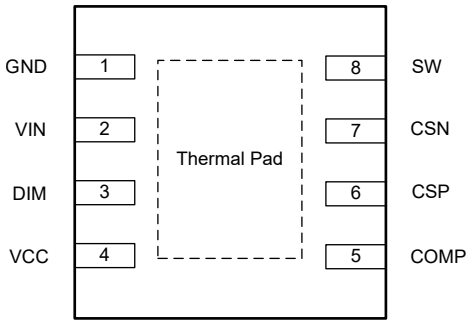


図 5-1. 8-Pin WSON Top View

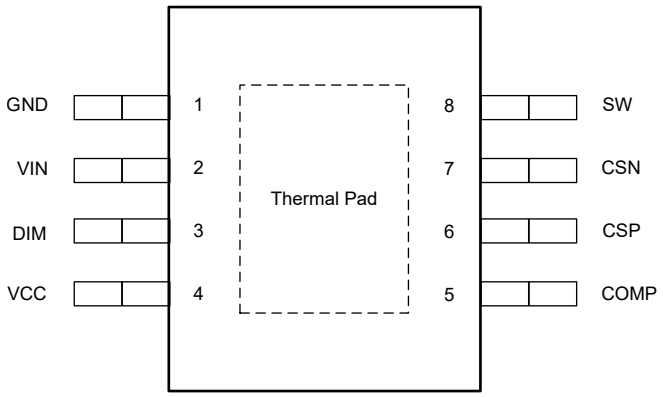


図 5-2. 8-Pin HVSSOP Top View

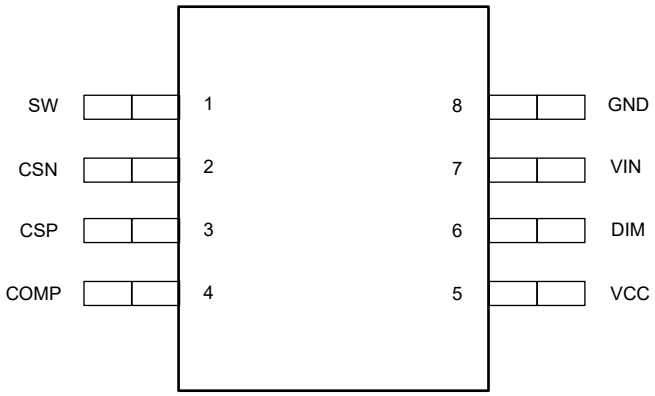


図 5-3. 8-Pin SOT583 Top View

表 5-1. Pin Functions

PIN				TYPE(1)	DESCRIPTION
NAME	WSON Package	SOP Package	SOT Package		
GND	1	1	8	G	Ground pin.
VIN	2	2	7	P	Input power pin.
DIM	3	3	6	I	PWM dimming pin for D1 version. Input PWM signal for PWM dimming. Analog dimming pin for D2 version. Input analog signal for analog dimming.
VCC	4	4	5	P	Internal LDO output pin. Connect with a 16V, 1µF capacitor to GND.
COMP	5	5	4	I/O	Error-amilifier output. Connect capacitors to GND. Different capacitor values determine different softstart times and bandwidths.
CSP	6	6	3	I	LED current sense positive pin.
CSN	7	7	2	I	LED current sense negative pin.
SW	8	8	1	P	Switching node pin. Internally connected to the low-side MOSFET. Connect with the power inductor and the schottky diode.
Thermal Pad	Y	Y	N/A	NC	No connection.

(1) I = Input, O = Output, P = Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins VIN, CSP, CSN, SW		–0.3	65	V
Voltage on pins VCC, DIM, COMP		–0.3	5.5	V
T_J	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage range	4.5	63	V
V_{SW}	Switching node voltage range	0	63	V
V_{CSP}, V_{CSN}	Sense common-mode voltage range	0	63	V
V_{VCC}	LDO output voltage range	0	5	V
V_{DIM}	Dimming voltage range	0	5	V
V_{COMP}	Compensation capacitor voltage range	0	5	V
T_A	Operating ambient temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS922050/1 WSON 8 PINS	TPS922050/1 HVSSOP 8 PINS	TPS922050 SOT 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.9	47.8	113.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.2	74.1	41.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.1	20.4	24.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	4.6	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.1	20.4	23.6	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics*application report, SPRA953.

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containingit. T_J = –40°C to +125°C, V_{IN} = 7V, (unlessotherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN_UVLO}	V_{IN} undervoltage lockout	Rising V_{IN}	3.0	3.2	3.4	V
		Falling V_{IN}	2.8	3.0	3.2	V
	Hysteresis			0.2		V
I_{OFF}	PWM off quiesent current from V_{IN}	V_{DIM} = 0V, device enabled		1.0	1.3	mA
I_{OP}	Normal operating current	400kHz switching frequency		2.3		mA
I_{OP}	Normal operating current	1MHz switching frequency		3.5		mA
V_{VCC}	Internal LDO output voltage	I_{VCC} = 5mA	5.0	5.15	5.3	V
I_{VCC_LIM}	Internal LDO output current limit		15	20	26	mA
DIMMING						
V_{PWM_L}	DIM low-level input voltage (D1 version)				0.4	V
V_{PWM_H}	DIM high-level input voltage (D1 version)		1.2			V
$t_{PWM\_OUT\_ON}$	PWM output minimum on time (D1 version)				100	ns
$t_{PWM\_IN\_ON}$	PWM input minimum on time (D1 verison)				100	ns
V_{ADIM}	DIM input voltage range (D2 version)		0		2.2	V
FEEDBACK AND ERROR AMPLIFIER						
$g_{M(ea)}$	Transconductance gain	V_{DIM} = 2V, $V_{CSP-CSN}$ = 200mV	205	265	325	µA/V
I_{COMP}	Source/sink current	V_{DIM} = 2V, $V_{CSP-CSN}$ = 200mV ± 200mV	±24	±40	±56	µA
V_{REF}	CSP-CSN pin voltage	V_{DIM} = 2V	193	200	207	mV
V_{REF}	CSP-CSN pin voltage	V_{DIM} = 0.2V	18.5	20	21.5	mV
$I_{LEAK\_CSP/N}$	CSP+CSN pin leakage current	V_{IN} = 60V, V_{DIM} = 2V			48	µA
$I_{LEAK\_CSP/N}$	CSP+CSN pin leakage current	V_{IN} = 60V, V_{DIM} = 0V			15	µA
POWER STAGE						
R_{DSON}	Switching FET on resistance	V_{IN} ≥ 5V		300		mΩ
t_{min_ON}	Switching FET minimum on time			140	160	ns
t_{min_OFF}	Switching FET minimum off time			140	160	ns
f_{SW}	Switching FET frequency (TPS922051, TPS922050DRLR)			0.4		MHz
f_{SW}	Switching FET frequency (TPS922050DSGR, TPS922050DGNR)			1.0		MHz
CURRENT LIMIT						
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS922050)		1.4	1.6	1.8	A
I_{LIM}	Switching FET cycle-by-cycle current limit (TPS922051)		2.8	3.2	3.6	A
THERMAL PROTECTION						
T_{TSD}	Thermal shutdown temperature			165		°C
	Hysteresis			15		°C

6.6 Typical Characteristics

V_{IN} = 24V, LED count = 4, F_{SW} = 400kHz, L = 33µH, unless otherwise specified

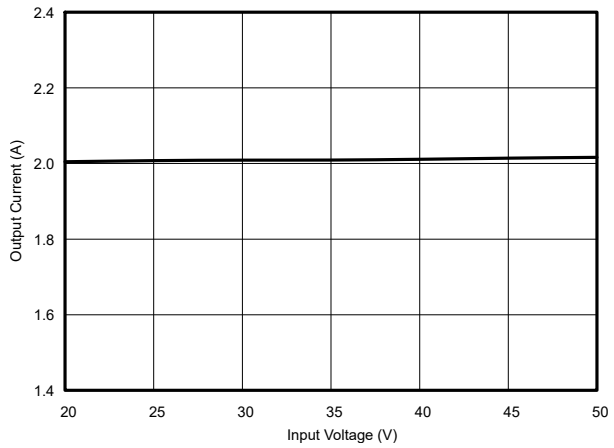


図 6-1. Output Current vs. Input Voltage

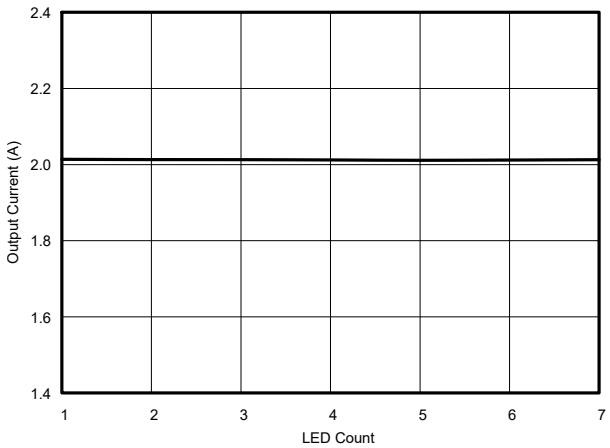


図 6-2. Output Current vs. LED Count

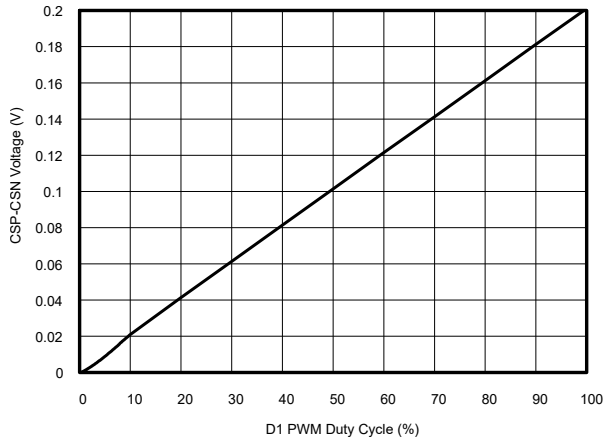


図 6-3. D1 PWM Duty Cycle vs. CSP-CSN Voltage at 20kHz PWM

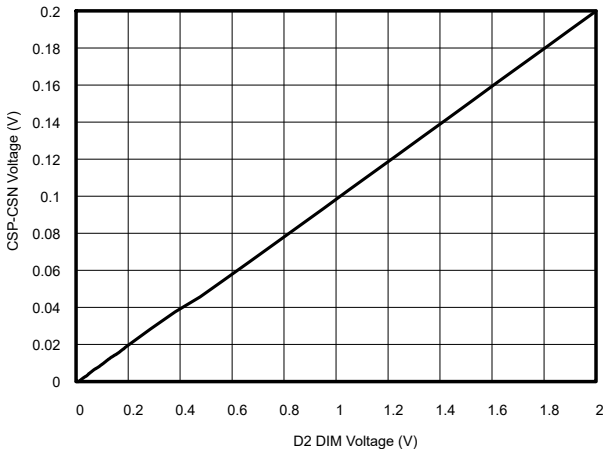


図 6-4. D2 Analog Voltage vs. CSP-CSN Voltage

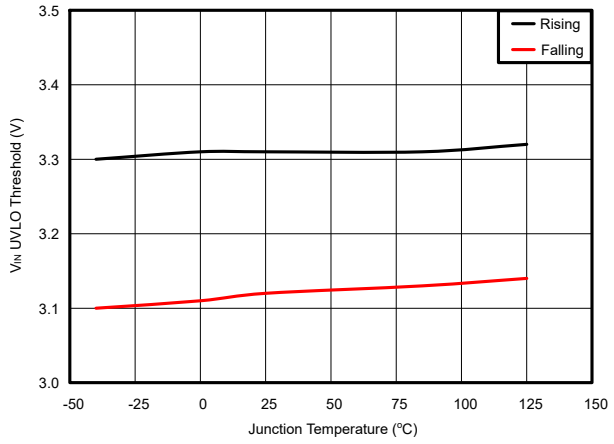


図 6-5. VIN UVLO Threshold vs. Junction Temperature

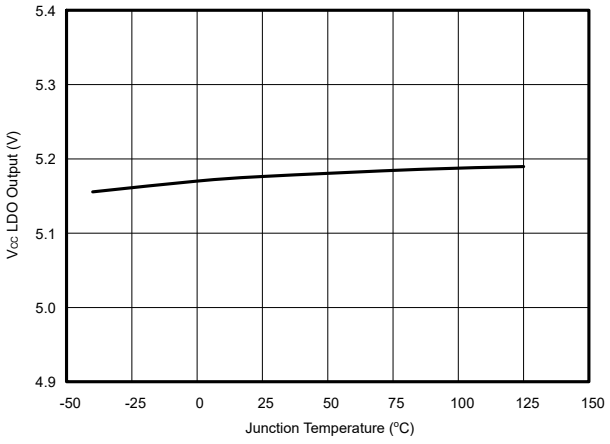


図 6-6. Internal LDO Output vs. Junction Temperature

6.6 Typical Characteristics (continued)

V_{IN} = 24V, LED count = 4, F_{SW} = 400kHz, L = 33µH, unless otherwise specified

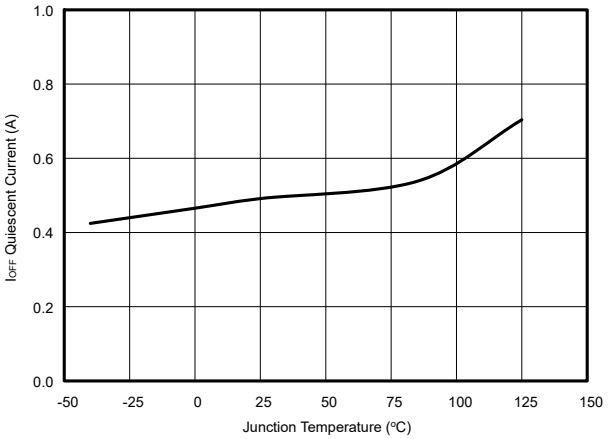


図 6-7. VIN Quiescent Current vs. Junction Temperature

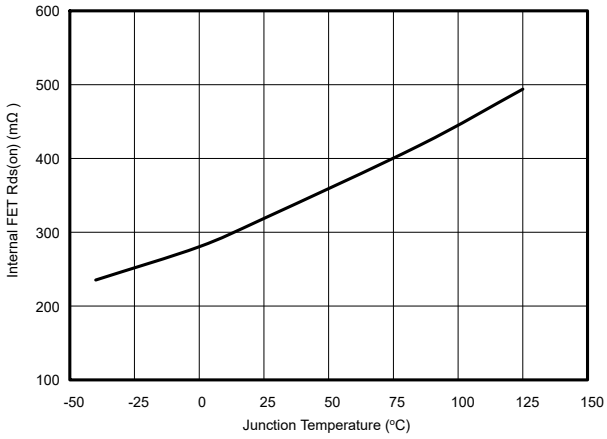


図 6-8. Switching FET Rdson vs. Junction Temperature

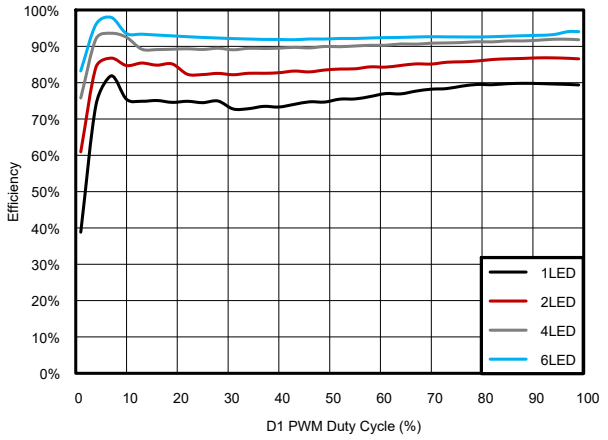


図 6-9. D1 Efficiency at 24V Input Voltage, 2A Output Current, 20kHz PWM

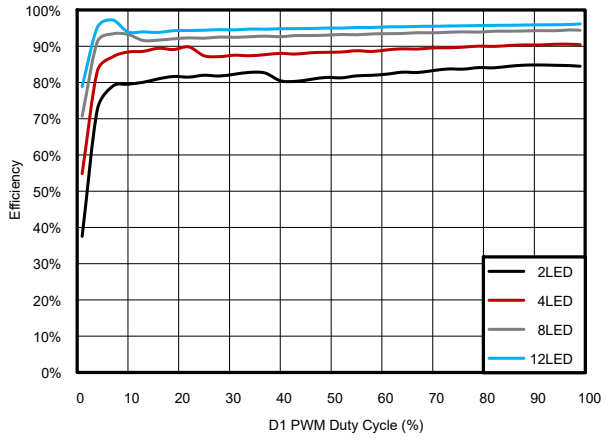


図 6-10. D1 Efficiency at 48V Input Voltage, 2A Output Current, 20kHz PWM

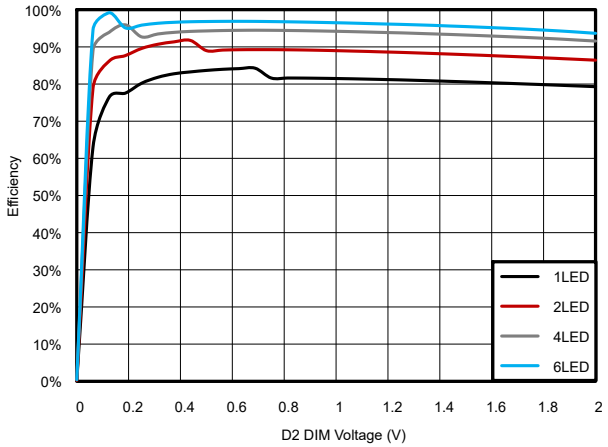


図 6-11. D2 Efficiency at 24V Input Voltage, 2A Output Current

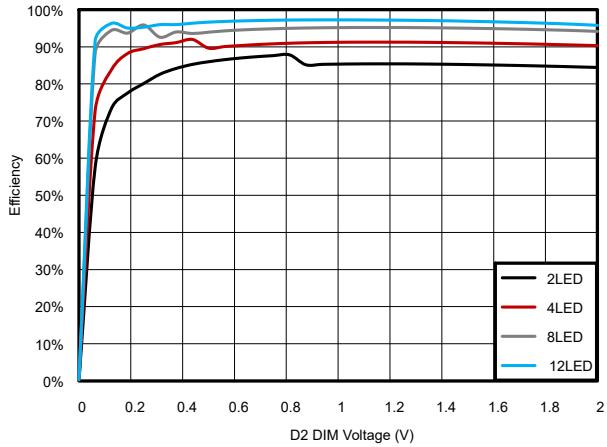


図 6-12. D2 Efficiency at 48V Input Voltage, 2A Output Current

7 Detailed Description

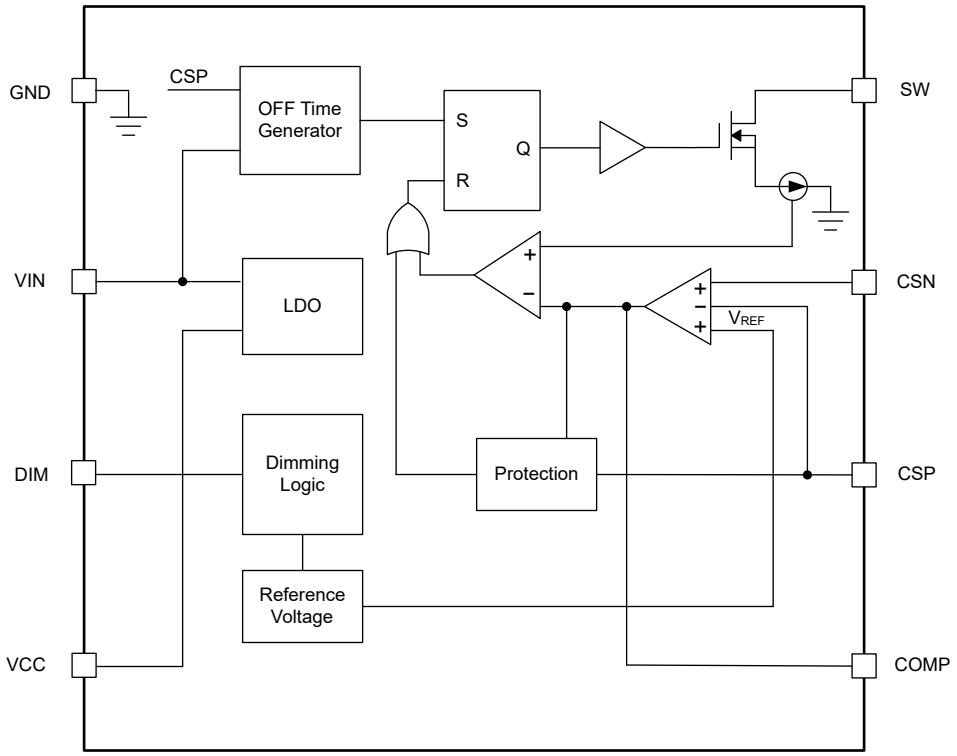
7.1 Overview

The TPS92205x ファミリ is a 1A / 2A non-synchronous 降圧 LED driver with 4.5V to 65V wide input range. By integrating the low-side NMOS switch with constant current control, the device is capable of driving LEDs with high power density and high efficiency. The device also supports common アノード connection and single layer PCB design, hence saving cost of connector, harness and PCB. The switching frequency is at 400kHz or 1MHz.

The TPS92205x ファミリ support PWM dimming by configuring through the DIM input pins by means of simple high and low signals. The TPS92205x ファミリ support analog dimming by configuring through the DIM input pins by means of analog signals. In PWM dimming, LED is turned on and off corresponding to on and off of the PWM input signal at DIM input pin. The PWM dimming mode supports ultra-narrow pulse width down to 50ns. In analog dimming, LED current is regulated corresponding to the analog voltage of the input signal at DIM input pin. The device adopts an adaptive off-time current mode control along with smart and accurate sampling to enable fast PWM dimming and achieve high dimming ratio. The compensation bandwidth can be adjusted through an external capacitor based on system requirement.

For safety and protection, the devices support full systematic protections including LED open and short, switching FET open and short, sense resistor open and short, and thermal shutdown protection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive Off-Time Current Mode Control

The TPS922050/1 device adopts an adaptive off-time current mode control to support fast transient response over a wide range of operation. The switching frequency is set at 400kHz or 1MHz.

For average output current regulation, the sensed voltage across the sensing resistor between the CSP and CSN pins is compared with the internal voltage reference, V_{REF} , through the error amplifier. The output of the error amplifier, V_{COMP}, passes through an external compensation network and is then compared with the peak current feedback at the PWM comparator. During each switching cycle, when the internal NMOS FET is turned on, the peak currernt is sensed through the internal FET. When the sensed value of peak current reaches V_{COMP} at the input of PWM comparator, the NMOS FET is turned off and the adaptive off-time counter starts counting. Once the adaptive off-time counter stops counting, the counter is reset until when the NMOS FET stays off. The counting off time is determined by the external resistor connected to the FSET pin and the input/output feedforward. Thus, the device is able to maintain a nearly constant switching frequnecy at steady state and regulate the output average current at a desired value.

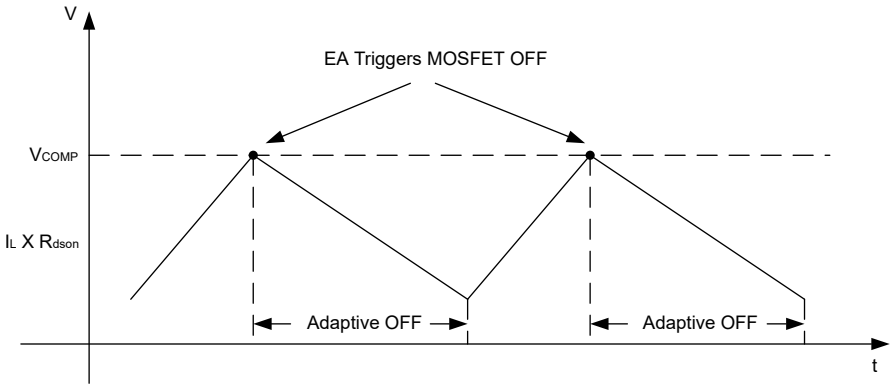


図 7-1. Adaptive off-time current mode control method

7.3.2 Setting LED Current

The LED current is set by the external sensing resistor between CSP and CSN pins. The internal voltage reference, V_{REF}, for instance, is set at 200mV for full-scale LED current, I_{LED_FS}, and the sensing resistor can be calculated using the equation below.

$$R_{SENSE} = \frac{V_{REF}}{I_{LED\_FS}} \quad (1)$$

where

- V_{REF} = 200mV

An offset on V_{REF} need to be considered due to voltage drop on R_{FLT} with common-mode leakage current of CSP and CSN pins.

7.3.3 Internal Soft Start

The TPS922050/1 implements the internal soft-start function. Once V_{IN} rises above V_{VIN_MIN}, the internal LDO starts to charge V_{CC} capacitor. It takes approximately 800µs for V_{CC} to rise above V_{VIN_UVLO} if a 1µF capacitor is connected to V_{CC} pin. The POR is enabled right after V_{CC} above V_{VIN_UVLO}. In this case, if using 1µF V_{CC} capacitor, it is recommended to wait for 1ms to start dimming after V_{IN} rises above V_{VIN_MIN}.

If DIM pin starts to rise or has the first PWM pulse appearing after V_{CC} rises above V_{VIN_UVLO}, the device starts switching right away. For D1 version, the initial PWM pulse can be as small as 50ns at DIM input pin to start dimming.

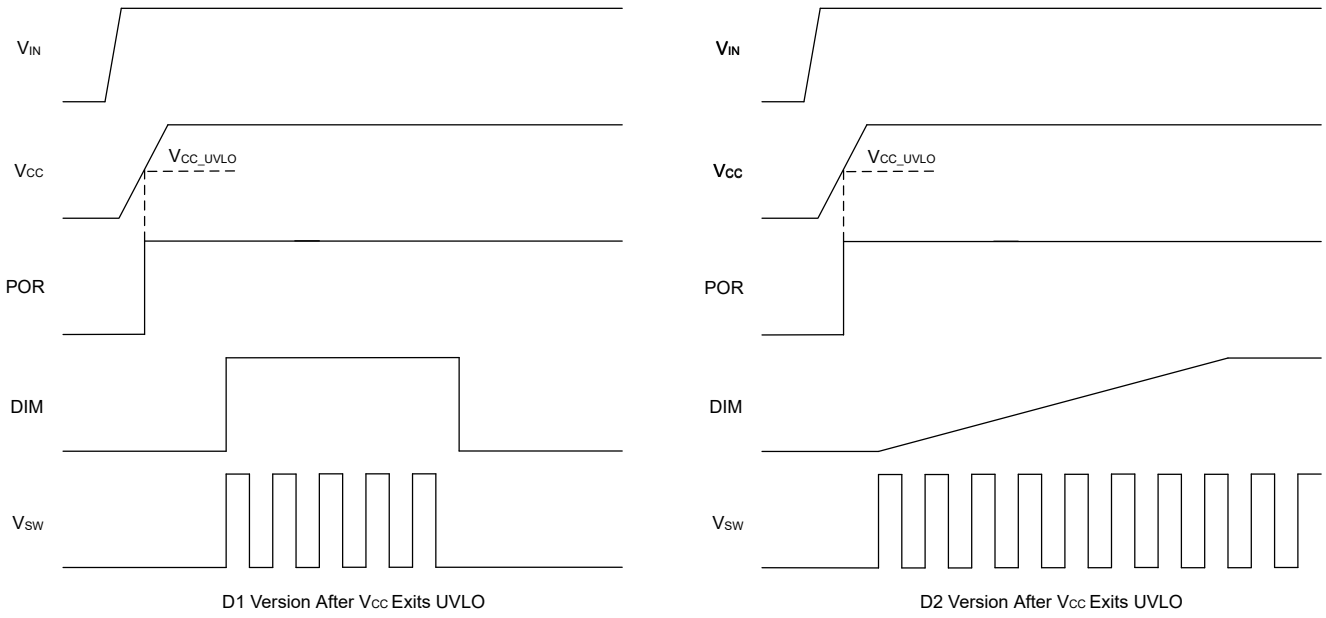


図 7-2. Startup Sequence

7.3.4 Dimming Mode

The TPS922050D1 and TPS922051D1 devices enable PWM dimming mode. The TPS922050D2 and TPS922051D2 devices enable analog dimming mode.

The configuration to dimming modes are shown as below

表 7-1. Dimming Mode Configuration

Dimming Mode	Version	DIM Pin
PWM Dimming	D1	PWM signal
Analog Dimming	D2	Analog signal

7.3.4.1 PWM Dimming

The TPS922050D1 and TPS922051D1 support PWM input signals with ultra-narrow pulse width down to 50-ns for direct PWM dimming. The PWM dimming starts when the DIM input pin is configured by a PWM input signal.

When the PWM input signal at the DIM pin turns from low to high, the internal NMOS FET starts switching and the inductor current rises to the determined value set by sense resistor. The LED current is then regulated at the determined value as long as the PWM input signal stays high. When the PWM input signal turns from high to low, the internal FET is turned off causing the inductor current falling to zero. The internal FET maintains off and the LED current stays zero as long as the PWM input signal stays low.

7.3.4.2 Analog Dimming

The TPS922050D2 and TPS922051D2 support analog dimming which regulates the LED current through the analog input signal at the DIM pin.

The internal voltage reference, V_{REF}, starts to rise after the device exit UVLO. Once an analog voltage appears at the DIM pin, V_{REF} continues to increase until changing to the desired value in proportion to the analog voltage.

V_{REF} is 200mV when the analog input signal at the DIM pin is 2V, for instance, and V_{REF} is 20mV when the analog input signal is 0.2V. V_{REF} is clamped at 220mV when the analog input signal at the DIM pin is higher than 2.2V. V_{REF} is 0V and the device stops switching when the analog input signal is lower than 10mV. The circuit is able to respond to the voltage change of the analog input signal with micro-seconds delay.

7.3.5 Fault Protection

The TPS922050/1 is able to provide fault protections in many fault conditions, including LED open, LED ± short, LED short to GND, sense resistor open and short, internal switching FET open and short, and thermal shutdown.

表 7-2. Protections

TYPE	CRITERION	BEHAVIOR
LED open load	V_{CSP} < 1V	The device keeps switching with minimum on time.
LED+ and LED- short circuit	V_{IN} - V_{CSP} < 100mV	The device keeps switching.
LED- short to GND	V_{CSP} < 1V	The device keeps switching with minimum on time.
Sense-resistor open circuit	V_{CSP} - V_{CSN} > 300mV	The device stops switching and recovers when fault is removed.
Sense-resistor short circuit	COMP pin is clamped high	The device keeps switching under the cycle-by-cycle current limit.
Switching FET open circuit	COMP pin is clamped high	The device stops switching and recovers when fault is removed.
Switching FET short circuit	V_{CSP} - V_{CSN} > 300mV	The device stops switching and recovers when fault is removed.
Thermal shutdown	T_J > T_{TSD}	The device stops switching and recovers when T_J falls below the hysteresis level.

8 Application and Implementation

8.1 Application Information

The TPS922050/1 is typically used as a Buck converter to drive one or more LEDs from an input from 4.5V to 63V range.

8.2 Typical Application

8.2.1 TPS922051D2 24V Input, 2A Output, 4-piece WLED Driver With Analog Dimming

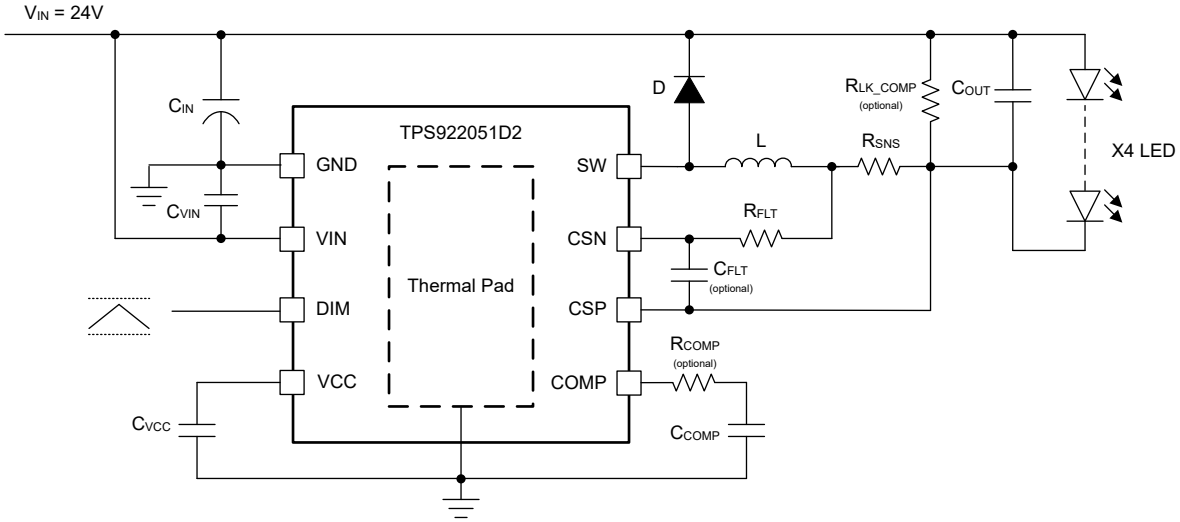


図 8-1. 24V Input, 2A Output, 4-piece WLED, Analog Dimming Reference Design

8.2.1.1 Design Requirements

For this design example, use the parameters in the following table.

表 8-1. Design Parameters

PARAMETER	VALUE
Input voltage range	24V ±10%
LED forward voltage	3.0V
Output voltage	12V (3.0V × 4)
Maximum LED current	2A
Inductor current ripple	30% of maximum LED current
LED current ripple	20mA or less
Input voltage ripple	200mV or less
Dimming type	Analog dimming with TPS922051D2: 0V to 2V analog input at the DIM pin

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

For this design, the input voltage is a 24V rail with 10% variation. The output is 4 white LEDs in series and the inductor current ripple by requirement is less than 30% of maximum inductor current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in full-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use the equation below to calculate the recommended value of the output inductor L.

$$L = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (2)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current.
- $I_{L(max)}$ is the maximum inductor current.
- f_{SW} is the switching frequency.
- $V_{IN(max)}$ is the maximum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using the equation below.

$$I_{L(ripple)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L \times f_{SW}} \quad (3)$$

The ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in the equations below .

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (4)$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^{2} + \frac{I_{L(ripple)}^{2}}{12}} \quad (5)$$

In this design, $V_{IN(max)}$ = 24V, V_{OUT} = 12V, I_{LED} = 2A, f_{SW} = 400kHz, choose K_{IND} = 0.3, the calculated inductance is 25µH. A 33µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 0.45A, 2.2A, and 2.01A, respectively.

8.2.1.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 10µF ceramic capacitor along with a 0.1µF capacitor from VIN to GND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use the equation below to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = I_{L(max)} \times \left(\frac{V_{OUT}}{K_{DR} \times C_{IN} \times f_{SW} \times V_{IN(max)}} + ESR_{CIN}\right) \quad (6)$$

In this design, 68µF, 100V electrolytic capacitor, a 22µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen, yielding around 160mV input ripple voltage.

8.2.1.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's datasheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See the equation below.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{7}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(ripple)} - I_{LED(ripple)}} \tag{8}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{9}$$

Once the output capacitor is chosen, the equation below can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(ripple)}}{Z_{COUT} + R_{LED}} \tag{10}$$

Osram WLED is used here. The dynamic resistance of the LED is 0.67Ω at 2A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, a 4.7µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 14mA.

8.2.1.2.4 Sense Resistor Selection

The maximum LED current is 2A at 2V analog input and the corresponding V_{REF} is 200mV. By using , the sense resistance is calculated as 100mΩ.

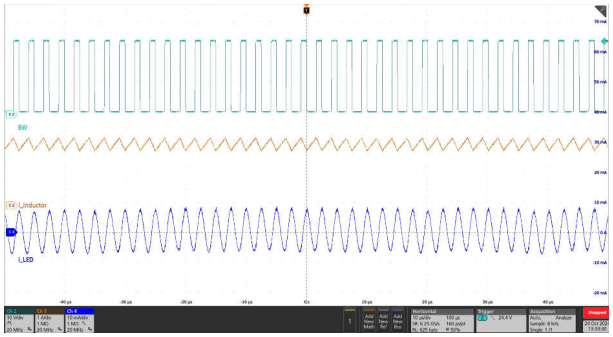
Note that the power consumption of the sense resistor is 400mW, requiring enough margin of the resistor's power rating in selection.

8.2.1.2.5 Other External Components Selection

In this design, a 100Ω resistor is recommended for R_{FLT} at CSN pin to avoid noise injection and increase robustness. An optional 1nF, 50V X7R ceramic capacitor is chosen for C_{FLT} across CSP-CSN pins to filter high-frequency noise of sense feedback.

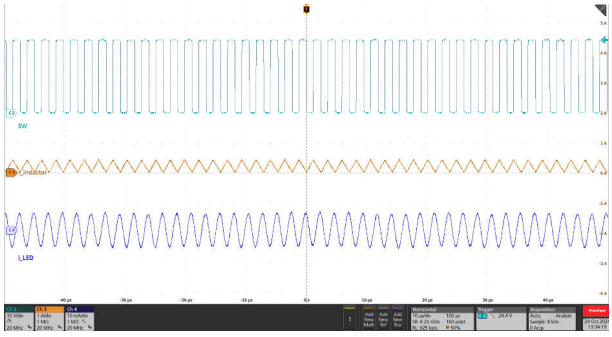
For loop stability, it is recommended to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and an optional 100Ω resistor for R_{COMP} . An optional resistor is chosen for R_{LK_COMP} to compensate the CSP+CSN common-mode leakage current and avoid it passing through LEDs.

8.2.1.3 Application Curves



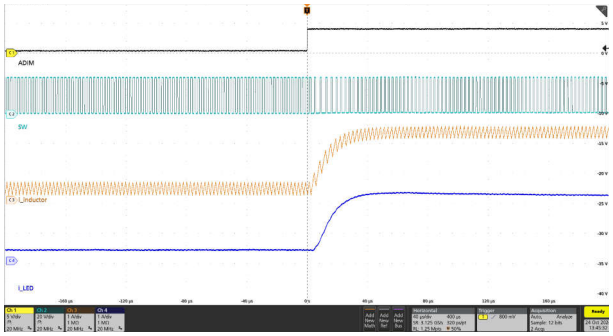
Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current Ripple (AC)

図 8-2. LED Current Ripple at DIM_{Analog} = 2V and F_{SW} = 400kHz



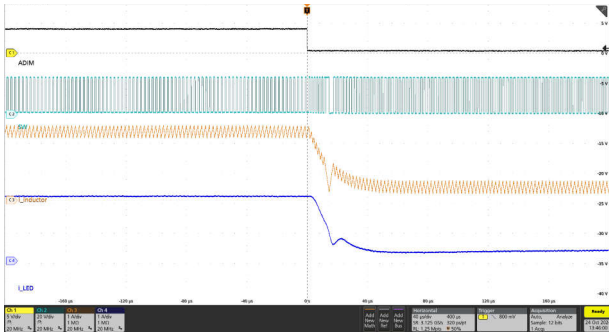
Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current Ripple (AC)

図 8-3. LED Current Ripple at DIM_{Analog} = 0.2V and F_{SW} = 400kHz



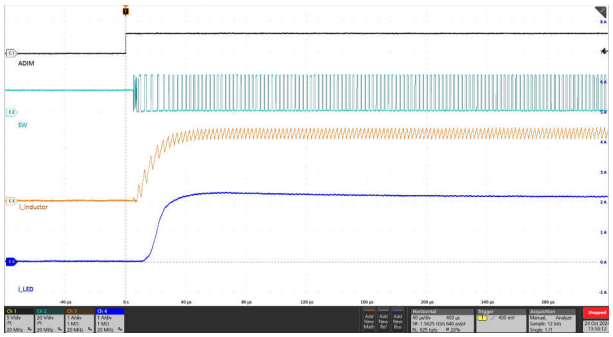
Black: DIM_{Analog}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-4. LED Current Transient for a DIM_{Analog} Transition from 0.2V to 2V



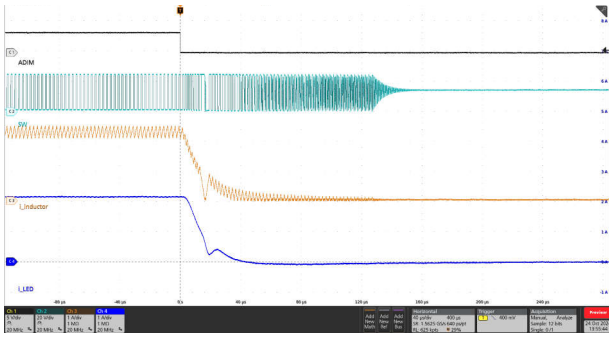
Black: DIM_{Analog}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-5. LED Current Transient for a DIM_{Analog} Transition from 2V to 0.2V



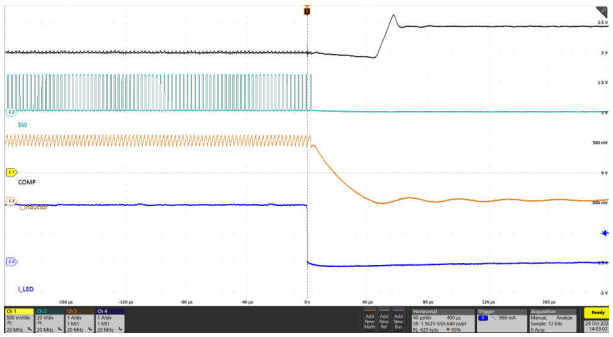
Black: DIM_{Analog}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-6. Start-Up at DIM_{Analog} = 2V



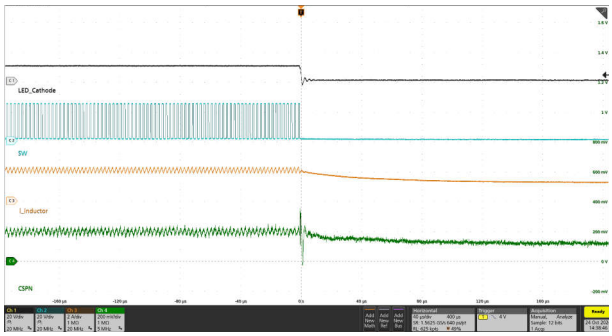
Black: DIM_{Analog}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-7. Shutdown at DIM_{Analog} = 2V



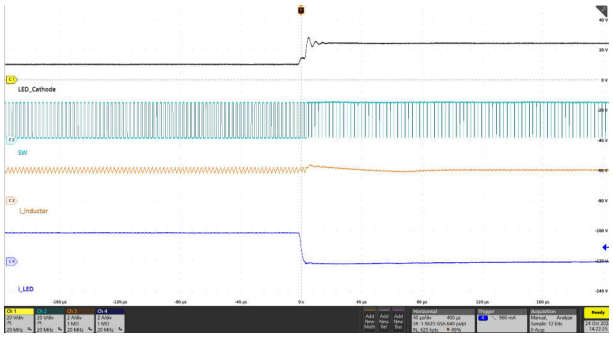
Black: LED–, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-8. LED Open-Load Protection



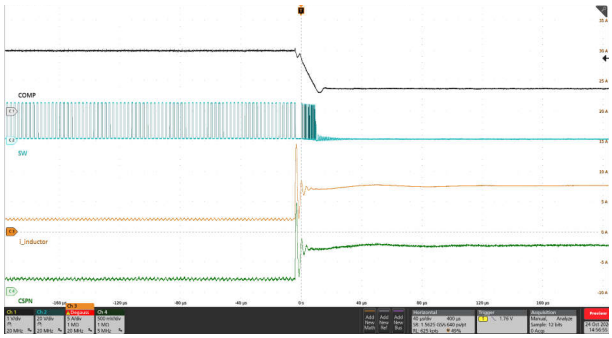
Black: LED–, Light Blue: SW, Orange: Inductor Current, Green: CSN

図 8-9. LED– Short-to-GND Protection



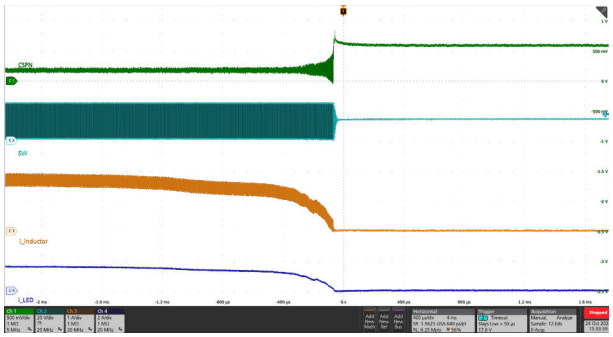
Black: LED–, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-10. LED+ and LED– Short-Circuit Protection



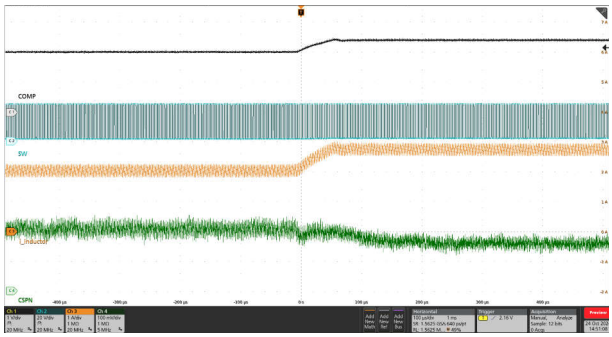
Black: COMP, Light Blue: SW, Orange: Inductor Current, Green: CSN

図 8-11. Switching FET Short-Circuit Protection



Green: CSN, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-12. Sense-Resistor Open Protection



Black: COMP, Light Blue: SW, Orange: Inductor Current, Green: CSN

図 8-13. Sense-Resistor Short-Circuit Protection

8.2.2 TPS922050D1 48V Input, 1A Output, 12-piece WLED Driver with PWM Dimming

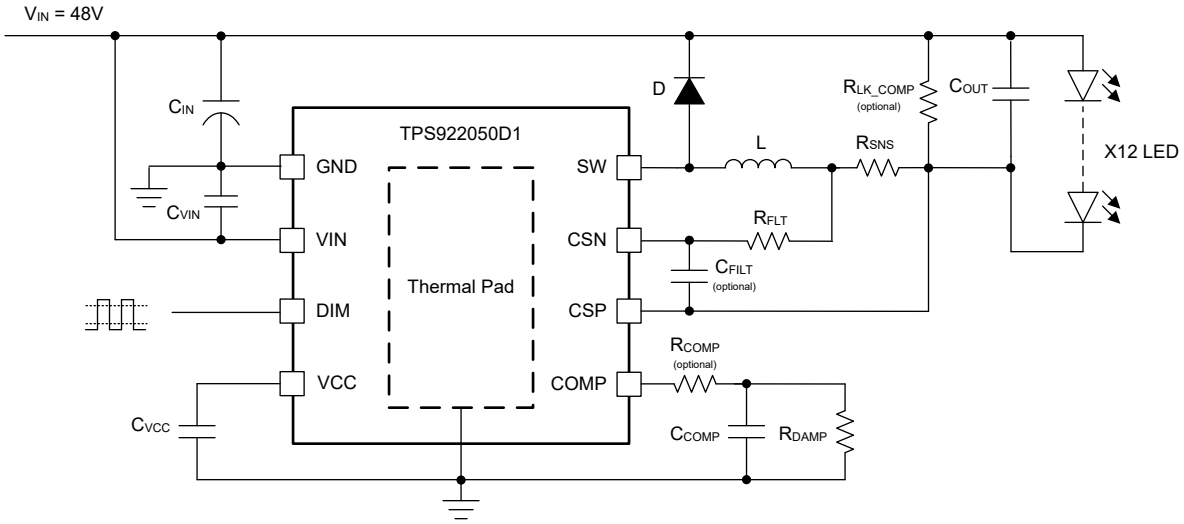


図 8-14. 48V Input, 1A Output, 12-piece WLED, PWM Dimming Reference Design

8.2.2.1 Design Requirements

For this design example, use the parameters in the following table.

表 8-2. Design Parameters

PARAMETER	VALUE
Input voltage range	48V ±10%
LED forward voltage	3.0V
Output voltage	36V (3.0V × 12)
Maximum LED current	1A
Inductor current ripple	30% of maximum LED current
LED current ripple	20mA or less
Input voltage ripple	400mV or less
Dimming type	PWM dimming with TPS922050D1: 0% to 100%, 20kHz PWM input at the DIM pin

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Inductor Selection

For this design, the input voltage is a 48V rail with 10% variation. The output is 12 white LEDs in series and the inductor current ripple by requirement is less than 30% of maximum inductor current. To choose a proper peak-to-peak inductor current ripple, the low-side FET current limit should not be violated when the converter works in no-load condition. This requires half of the peak-to-peak inductor current ripple to be lower than that limit. Another consideration is to ensure reasonable inductor core loss and copper loss caused by the peak-to-peak current ripple. Once this peak-to-peak inductor current ripple is chosen, use the equation below to calculate the recommended value of the output inductor L.

$$L = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{L(max)} \times f_{SW}} \quad (11)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum LED current.
- $I_{L(max)}$ is the maximum inductor current.
- f_{SW} is the switching frequency.
- $V_{IN(max)}$ is the maximum input voltage.
- V_{OUT} is the sum of the voltage across LED load and the voltage across sense resistor.

With the chosen inductor value, the user can calculate the actual inductor current ripple using the equation below.

$$I_{L(ripple)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L \times f_{SW}} \quad (12)$$

The ratings of inductor RMS current and saturation current must be greater than those seen in the system requirement. This is to ensure no inductor overheat or saturation occurring. During power up, transient conditions or fault conditions, the inductor current may exceed its normal operating current and reach the current limit. Therefore, it is preferred to select a saturation current rating equal to or greater than the converter current limit. The peak-inductor-current and RMS current equations are shown in the equations below.

$$I_{L(peak)} = I_{L(max)} + \frac{I_{L(ripple)}}{2} \quad (13)$$

$$I_{L(rms)} = \sqrt{I_{L(max)}^{2} + \frac{I_{L(ripple)}^{2}}{12}} \quad (14)$$

In this design, $V_{IN(max)}$ = 48V, V_{OUT} = 36V, I_{LED} = 1A, f_{SW} = 1MHz, choose K_{IND} = 0.3, the calculated inductance is 30µH. A 33µH inductor is chosen. With this inductor, the ripple, peak, and rms currents of the inductor are 0.27A, 1.14A, and 1.01A, respectively.

8.2.2.2.2 Input Capacitor Selection

An input capacitor is required to reduce the surge current drawn from the input supply and the switching noise coming from the device. Electrolytic capacitors are recommended for energy storage. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, it is recommended to place a 10µF capacitor along with a 0.1µF capacitor from VIN to GND to provide high-frequency filtering. The input capacitor voltage rating must be greater than the maximum input voltage. Use the equation below to calculate the input ripple voltage, where ESR_{CIN} is the ESR of input capacitor, and K_{DR} is the derating coefficient of ceramic capacitance at the applied DC voltage.

$$V_{IN(ripple)} = \frac{I_{L(max)}}{2\pi \times f_{PWM} \times C_{OUT}} \quad (15)$$

In this design, a 10µF, 100V electrolytic capacitor, a 22µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen, yielding around 360mV input ripple voltage.

8.2.2.2.3 Output Capacitor Selection

The output capacitor reduces the high-frequency current ripple through the LED string. Excessive current ripple increases the RMS current in the LED string, therefore increasing the LED temperature.

1. Calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's datasheet.

2. Calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, $I_{LED(ripple)}$. $I_{L(ripple)}$ is the peak-to-peak inductor ripple current as calculated with the selected inductor.

3. Calculate the minimum effective output capacitance required.

4. Increase the output capacitance appropriately due to the derating effect of applied DC voltage.

See the equations below.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ of\ LEDs \tag{16}$$

$$Z_{COUT} = \frac{R_{LED} \times I_{LED(ripple)}}{I_{L(ripple)} - I_{LED(ripple)}} \tag{17}$$

$$C_{COUT} = \frac{1}{2\pi \times f_{SW} \times Z_{COUT}} \tag{18}$$

Once the output capacitor is chosen, the equation below can be used to estimate the peak-to-peak ripple current through the LED string.

$$I_{LED(ripple)} = \frac{Z_{COUT} \times I_{L(ripple)}}{Z_{COUT} + R_{LED}} \tag{19}$$

Osram WLED is used here. The dynamic resistance of the LED is 0.67Ω at 1A forward current. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. In this design, a 1µF, 100V X7R ceramic capacitor and a 0.1µF, 100V X7R ceramic capacitor are chosen. The calculated ripple current of the LED is about 6mA.

8.2.2.2.4 Sense Resistor Selection

The maximum LED current is 1A at 100% PWM duty and the corresponding V_{REF} is 200mV. By using the equation below, the sense resistance is calculated as 200mΩ.

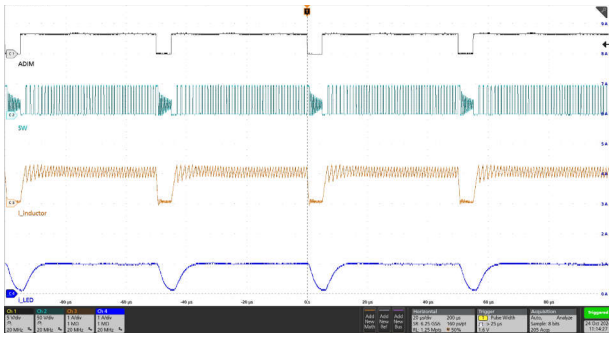
Note that the power consumption of the sense resistor is 200mW, requiring enough margin of the resistor's power rating in selection.

8.2.2.2.5 Other External Components Selection

In this design, a 100Ω resistor is recommended for R_{FLT} at CSN pin to avoid noise injection and increase robustness. An optional 1nF, 50V X7R ceramic capacitor is chosen for C_{FLT} across CSP-CSN pins to filter high-frequency noise of sense feedback.

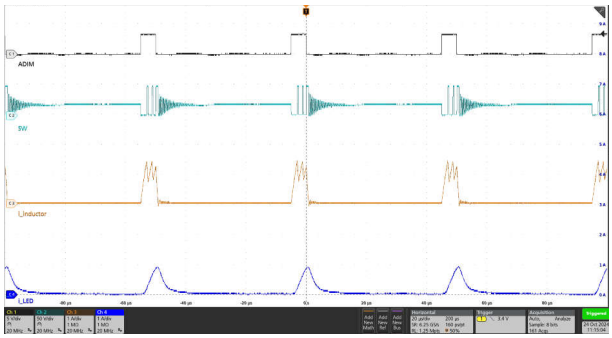
For loop stability, it is recommended to select a 1nF, 10V X7R ceramic capacitor for C_{COMP} and an optional 100Ω resistor for R_{COMP} . A 20MΩ resistor is chosen for R_{DAMP} to suppress the overshoot current at rising edge of PWM on. An optional resistor is chosen for R_{LK_COMP} to compensate the CSP+CSN common-mode leakage current and avoid it passing through LEDs.

8.2.2.3 Application Curves



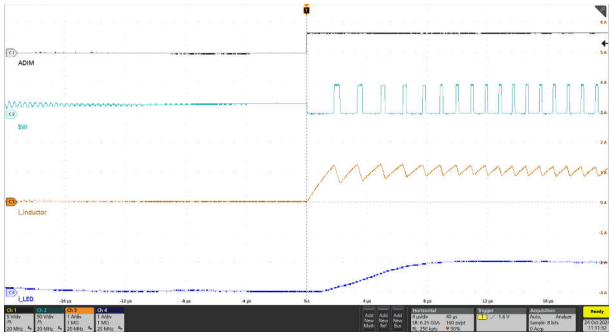
Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-15. LED Current at DIM_{PWM} = 90%, 20kHz and F_{SW} = 1MHz



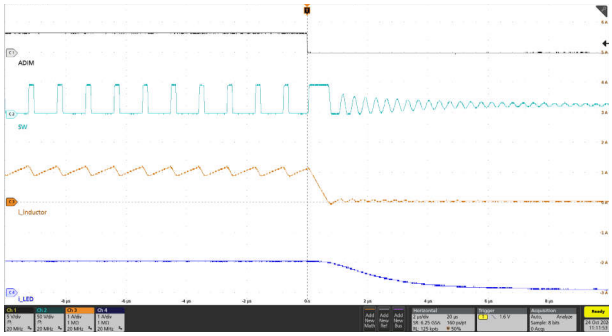
Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-16. LED Current at DIM_{PWM} = 10%, 20kHz and F_{SW} = 1MHz



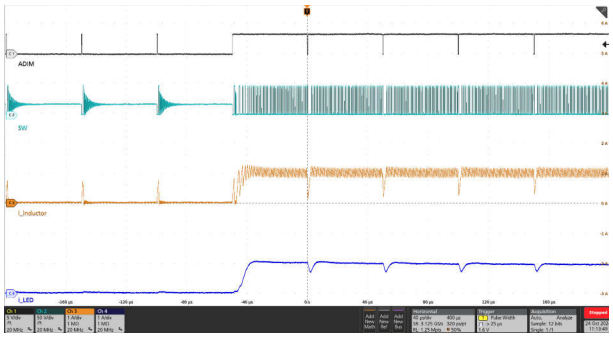
Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-17. LED PWM Dimming Rising Edge at DIM_{PWM} = 50%, 20kHz



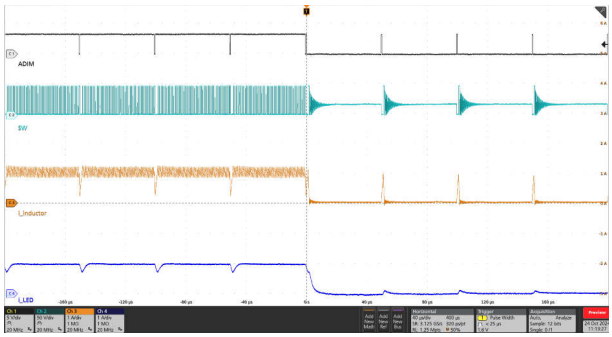
Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-18. LED PWM Dimming Falling Edge at DIM_{PWM} = 50%, 20kHz



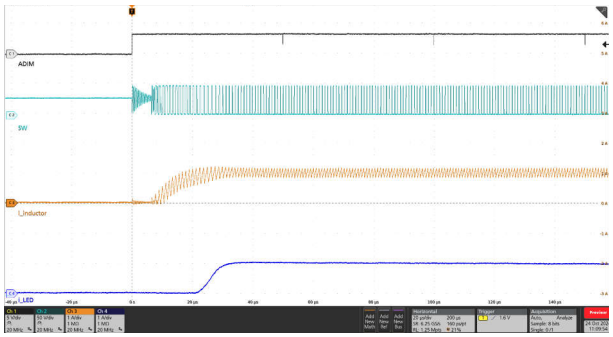
Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-19. LED Current Transient for a DIM_{PWM} Transition from 1% to 99%, 20kHz



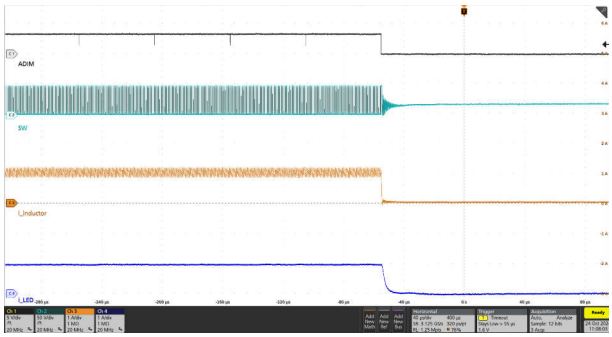
Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-20. LED Current Transient for a DIM_{PWM} Transition from 99% to 1%, 20kHz



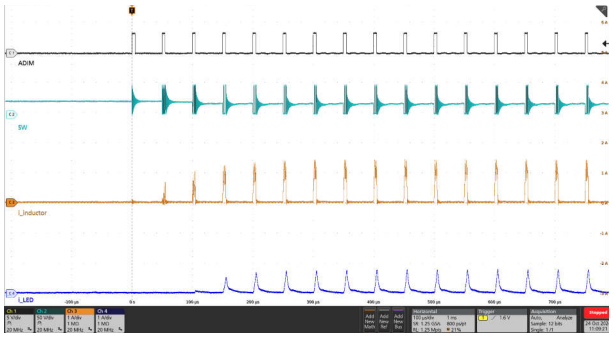
Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-21. Start-Up at DIM_{PWM} = 100%, 20kHz



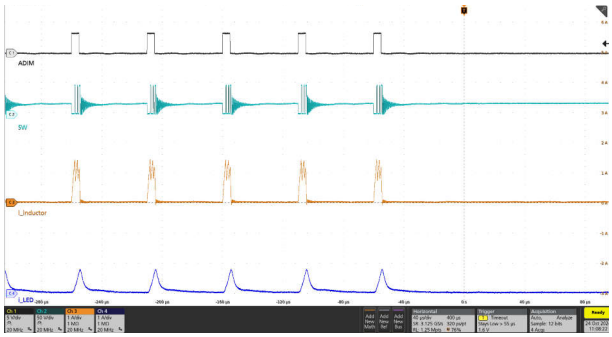
Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-22. Shutdown at DIM_{PWM} = 100%, 20kHz



Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-23. Start-Up at DIM_{PWM} = 10%, 20kHz



Black: DIM_{PWM}, Light Blue: SW, Orange: Inductor Current, Deep Blue: LED Current

図 8-24. Shutdown at DIM_{PWM} = 10%, 20kHz

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging between 4.5V and 63V. This input supply must be well regulated. The device requires an input capacitor to reduce the surge current drawn from the input supply and the switching noise from the device. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is enough.

8.4 Layout

The TPS922050/1 requires a proper layout for optimal performance. The following section gives some guidelines to ensure a proper layout.

8.4.1 Layout Guidelines

An example of a proper layout for the TPS922050/1 device is shown in 8-Pin WSON Top View Layout Example.

- Creating a large GND plane for good electrical and thermal performance is important.
- The VIN and GND traces should be as wide as possible to reduce trace impedance. Wide traces have the additional advantage of providing excellent heat dissipation.
- Thermal vias can be used to connect the top-side GND plane to additional printed-circuit board (PCB) layers for heat dissipation and grounding.
- The input capacitors must be located as close as possible to the VIN pin and the GND pin.
- The VCC capacitor should be placed as close as possible to VCC pin to ensure stable LDO output voltage.
- The SW trace must be kept as short as possible to reduce parasitic inductance and thereby reduce transient voltage spikes. Short SW trace also reduces radiated noise and EMI.
- Do not allow switching current to flow under the device.
- The routing of CSN and CSP traces are recommended to be in parallel and kept as short as possible and placed away from the high-voltage switching trace and the ground shield.
- The compensation capacitor must be placed as close as possible to COMP pin so as to prevent oscillation and system instability.

8.4.2 Layout Example

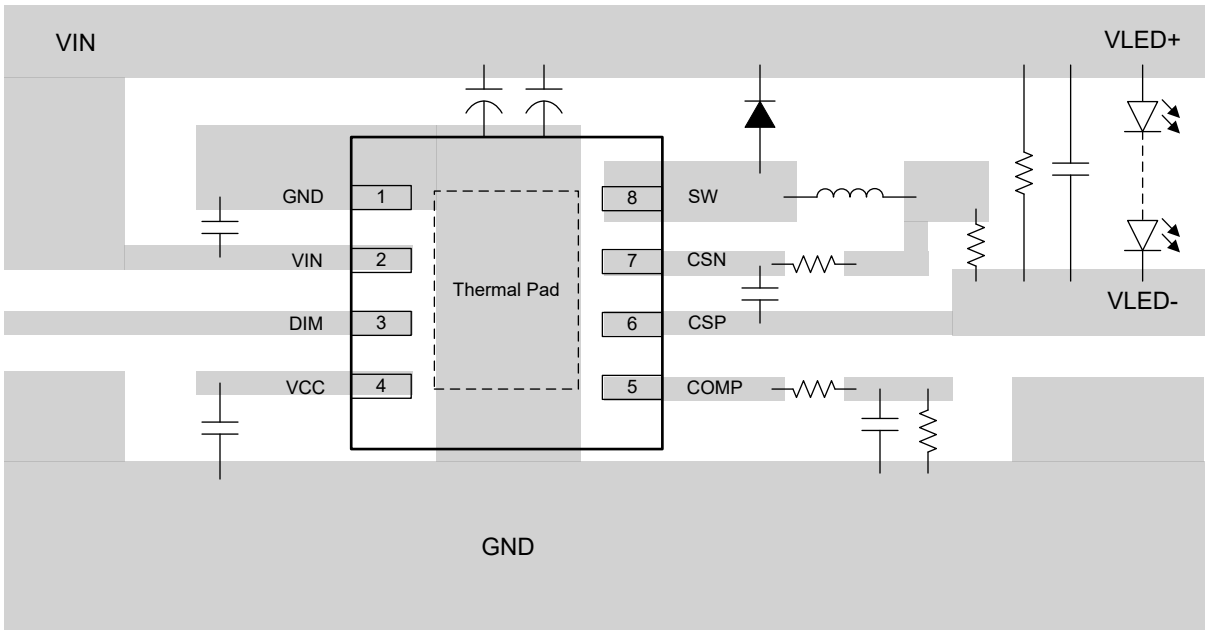


図 8-25. 8-Pin WSON Top View Layout Example

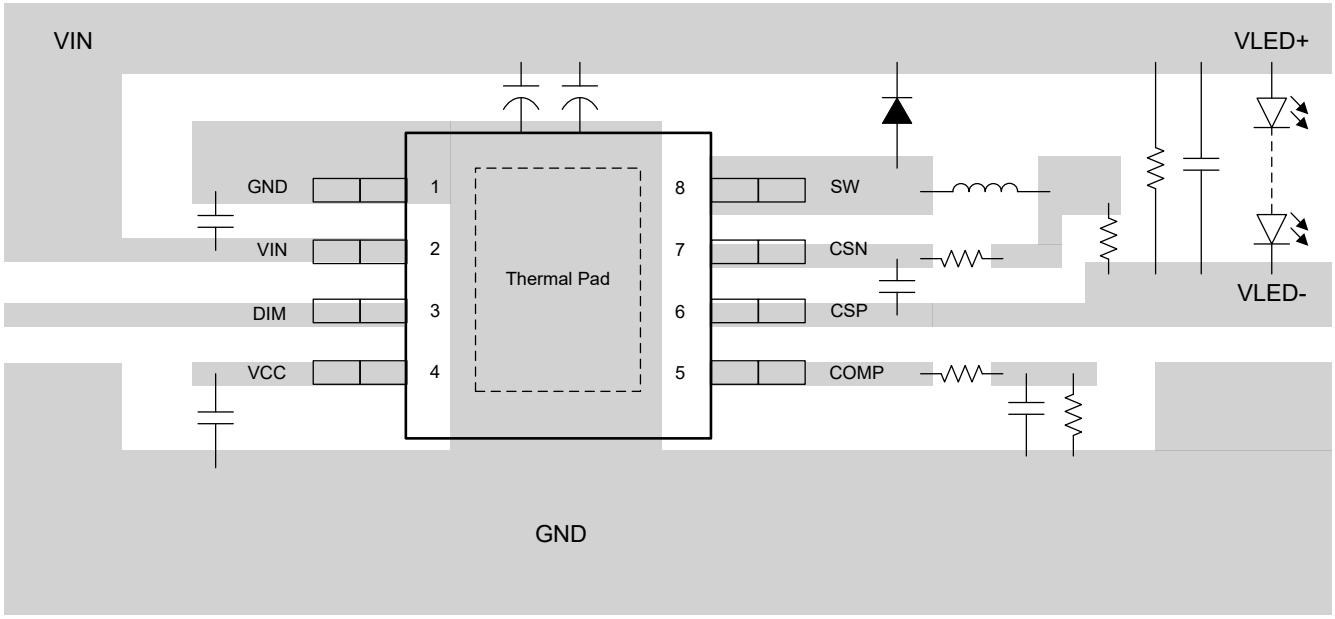


図 8-26. 8-Pin HVSSOP Top View Layout Example

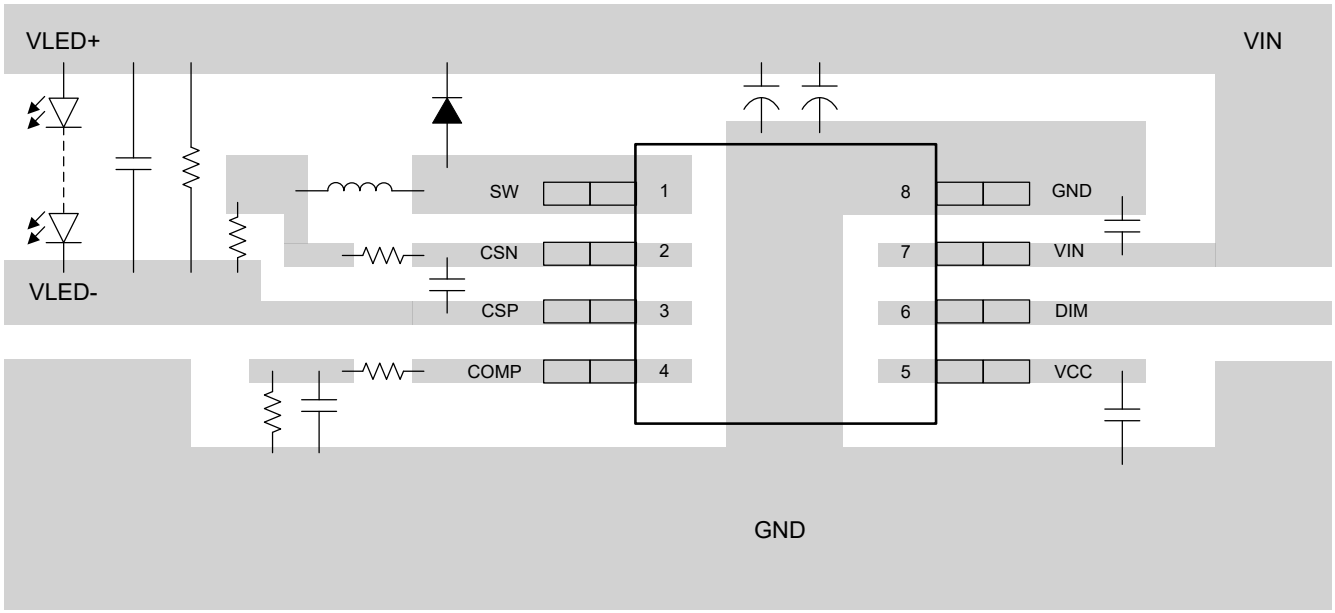


図 8-27. 8-Pin SOT583 Top View Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

DATE	REVISION	NOTES
November 2024	*	Initial release.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

11.1 Package Option Addendum

Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TPS922051D1DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2211
TPS922051D2DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2212
TPS922051D1DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2211

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TPS922051D2DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2212
TPS922050D1DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2201
TPS922050D2DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2202
TPS922050D1DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2201
TPS922050D2DGNR	ACTIVE	HVSSOP	DGN	8	2500	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2202
TPS922050D1DRLR	ACTIVE	SOT583	DRL	8	4000	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2201
TPS922050D2DRLR	ACTIVE	SOT583	DRL	8	4000	Green (RoHS and no Sb/Br)	Cu NiPdAu	LEVEL1-260C-UNLIM	-40 to 85	2202

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

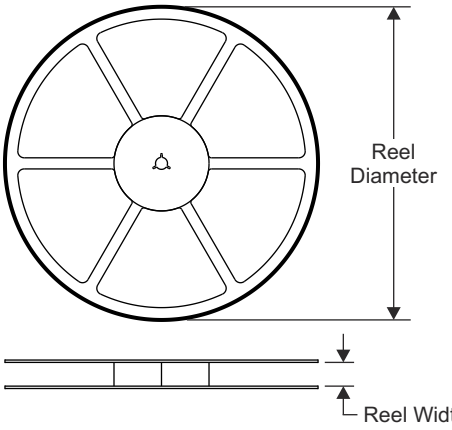
(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

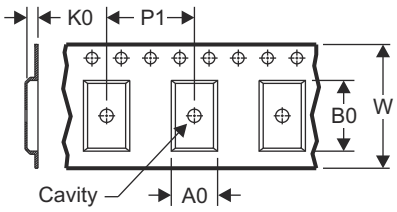
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

11.2 Tape and Reel Information

REEL DIMENSIONS

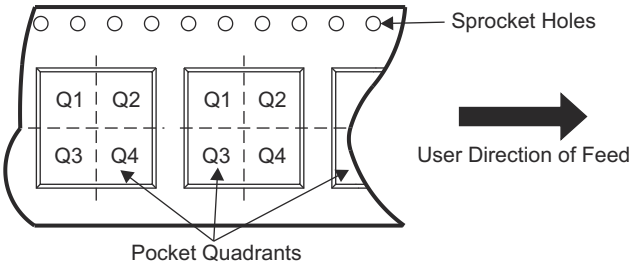


TAPE DIMENSIONS



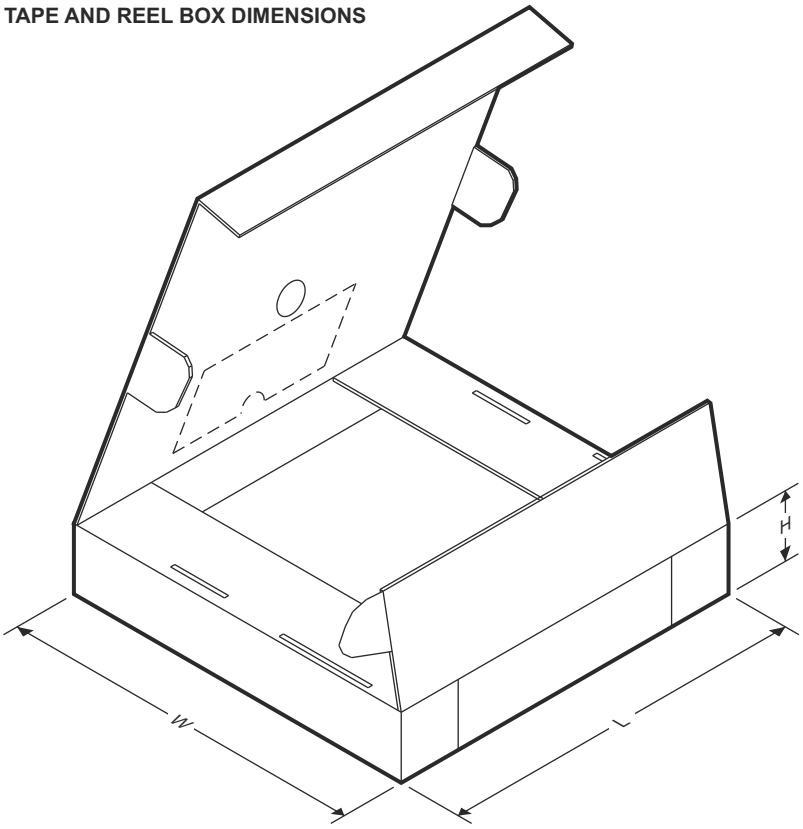
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS922051D1DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS922051D2DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS922051D1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS922051D2DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS922050D1DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS922050D2DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS922050D1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS922050D2DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS922050D1DRLR	SOT583	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS922050D2DRLR	SOT583	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



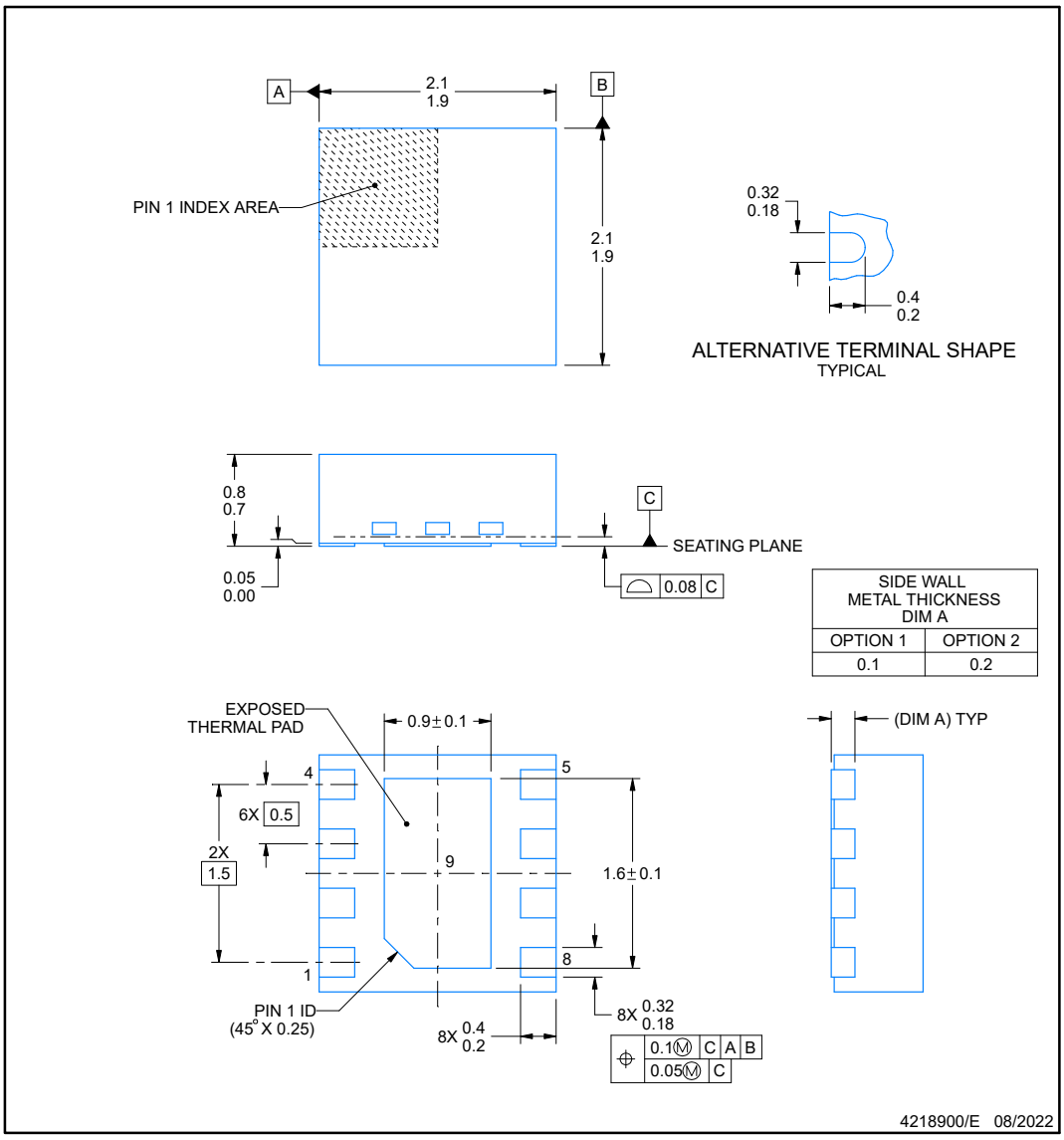
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS922051D1DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS922051D2DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS922051D1DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS922051D2DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS922050D1DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS922050D2DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS922050D1DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS922050D2DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS922050D1DRLR	SOT583	DRL	8	4000	210.0	185.0	35.0
TPS922050D2DRLR	SOT583	DRL	8	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



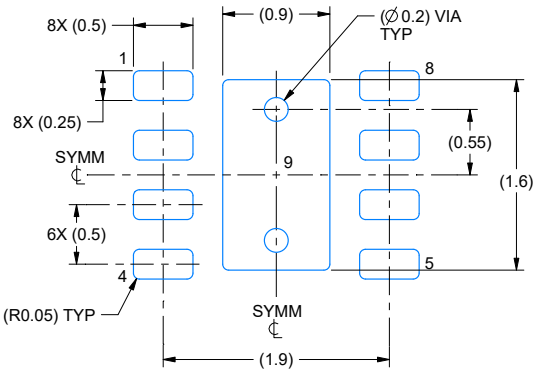
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

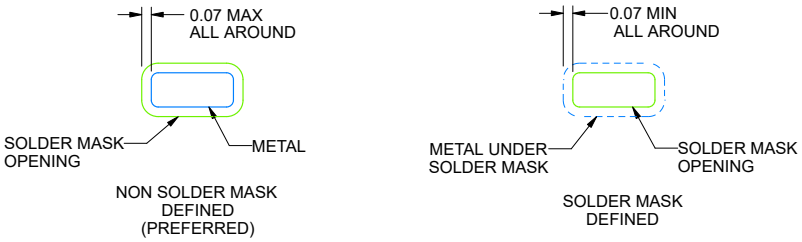
EXAMPLE BOARD LAYOUT

DSG0008A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

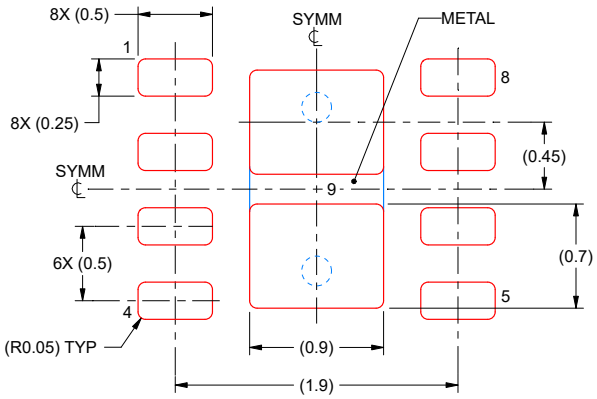
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A — **WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

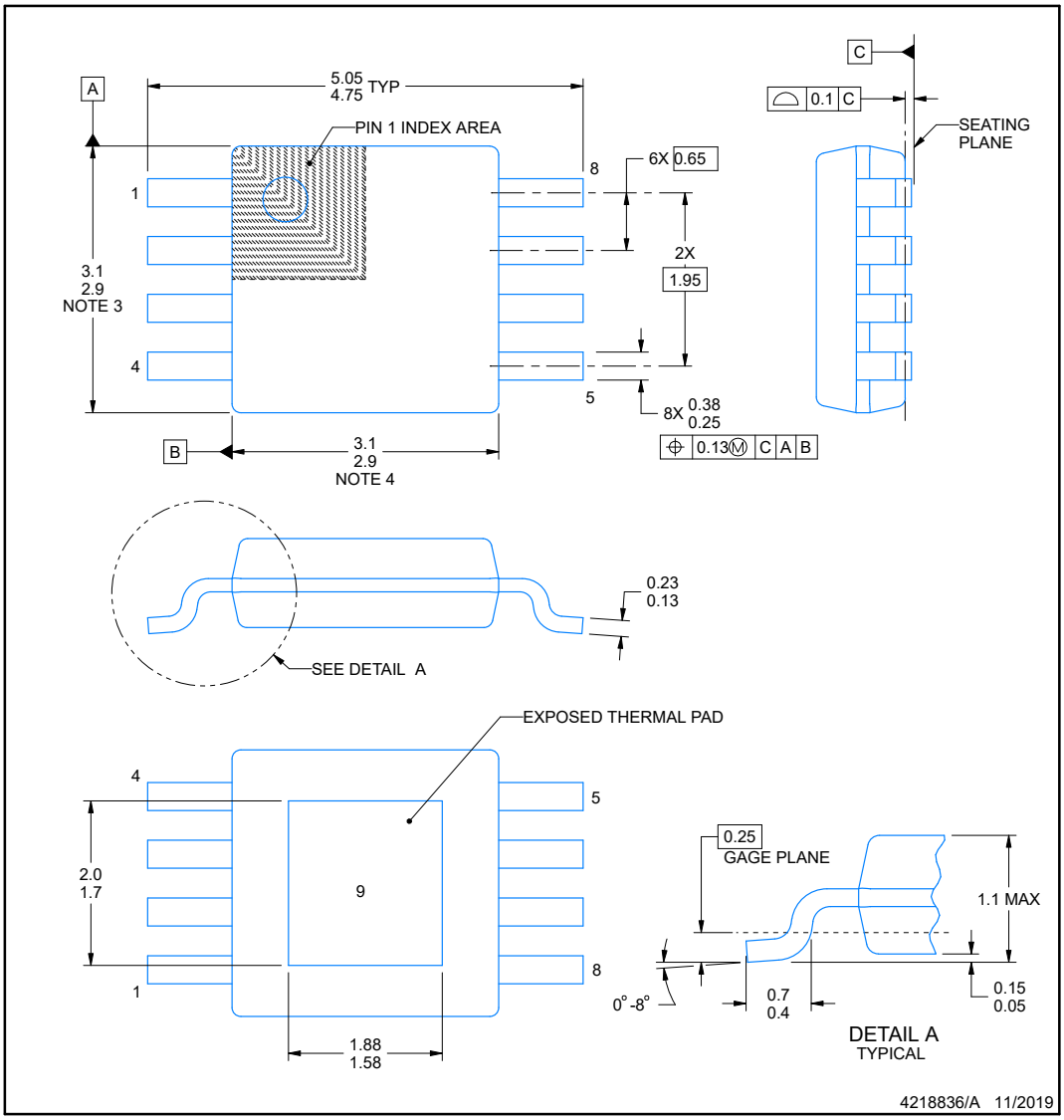
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DGN0008A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

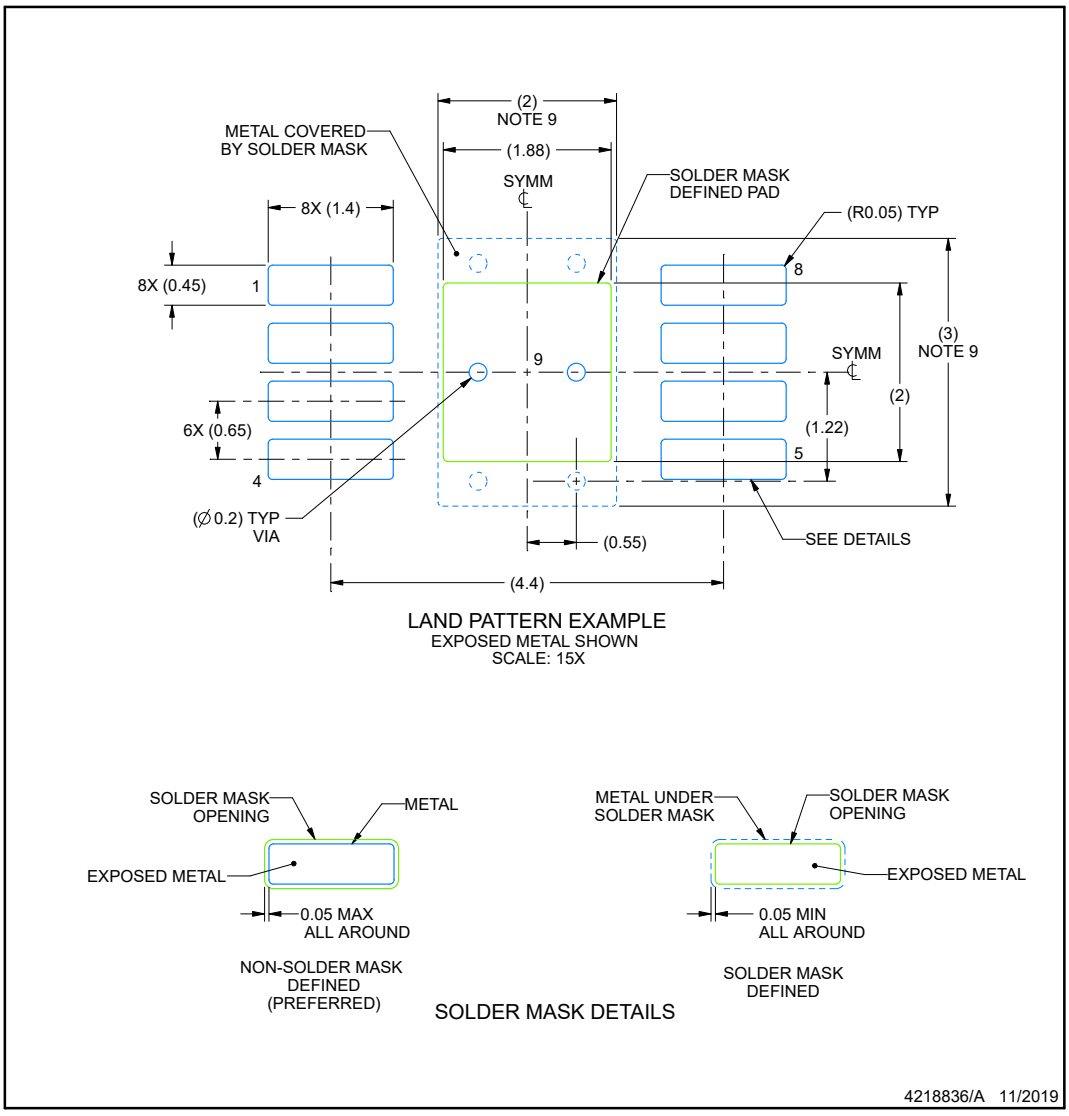
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

www.ti.com

EXAMPLE BOARD LAYOUT

DGN0008A — **PowerPAD™ VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



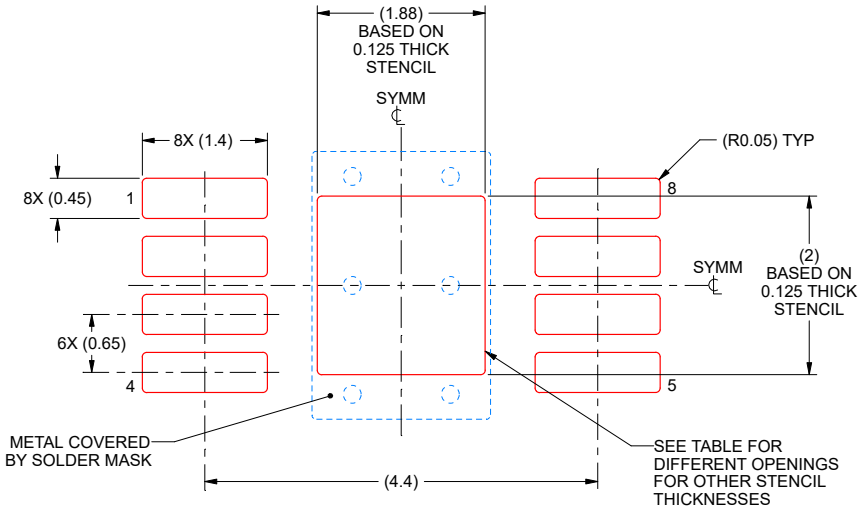
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008A — **PowerPAD™ VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

4218836/A 11/2019

NOTES: (continued)

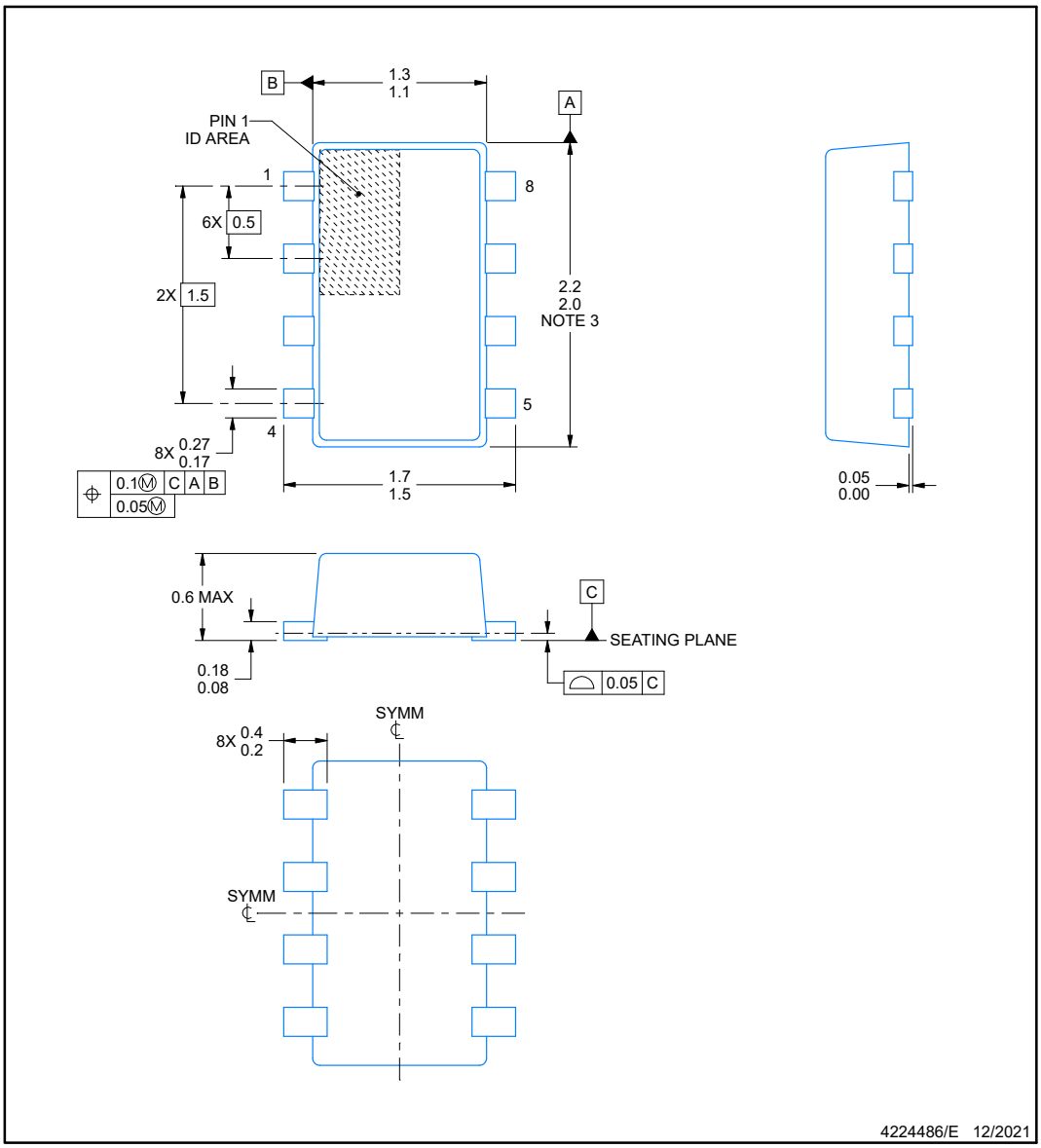
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

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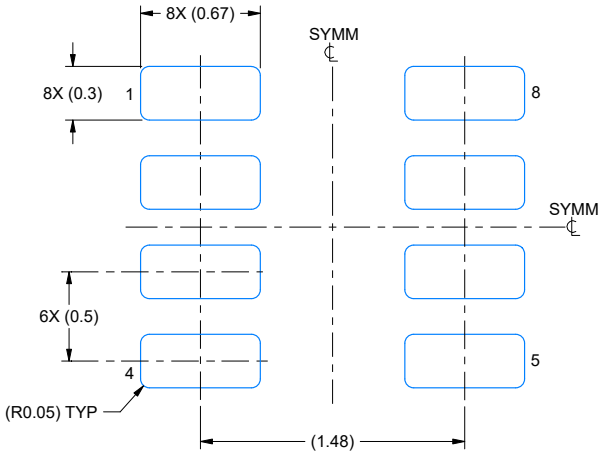
EXAMPLE BOARD LAYOUT

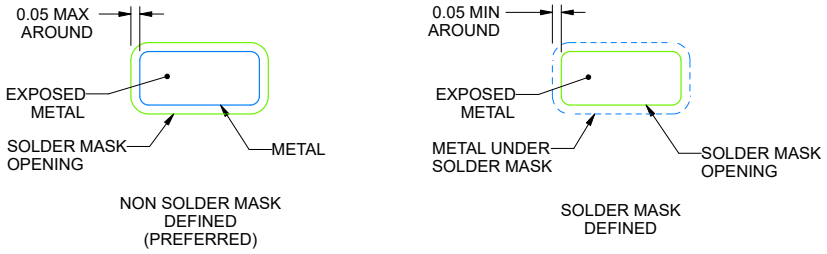
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/E 12/2021

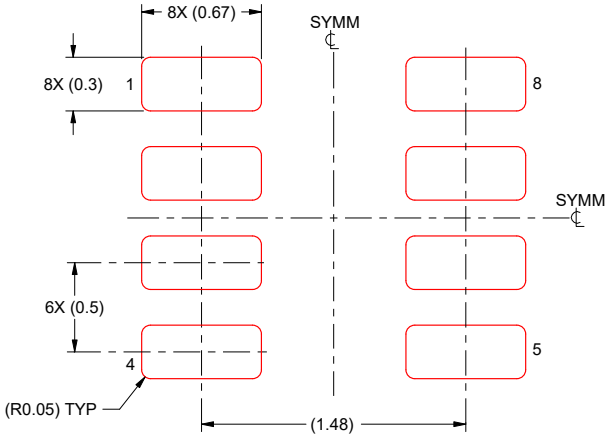
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A — **SOT-5X3 - 0.6 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/E 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS922050D1DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2201
TPS922050D1DRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2201
TPS922050D1DRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2201
TPS922050D1DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2201
TPS922050D1DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2201
TPS922050D2DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2202
TPS922050D2DRLR	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2202
TPS922050D2DRLR.A	Active	Production	SOT-5X3 (DRL) | 8	4000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	2202
TPS922050D2DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2202
TPS922050D2DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2202
TPS922051D1DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2211
TPS922051D1DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2211
TPS922051D1DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2211
TPS922051D2DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2212
TPS922051D2DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2212
TPS922051D2DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2212

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

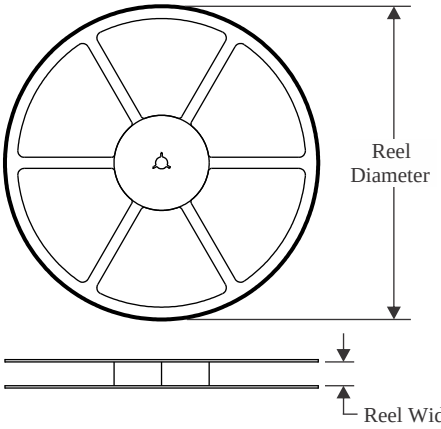
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

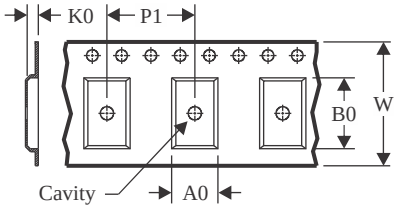
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

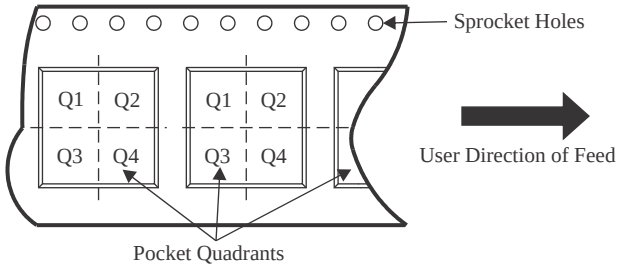


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

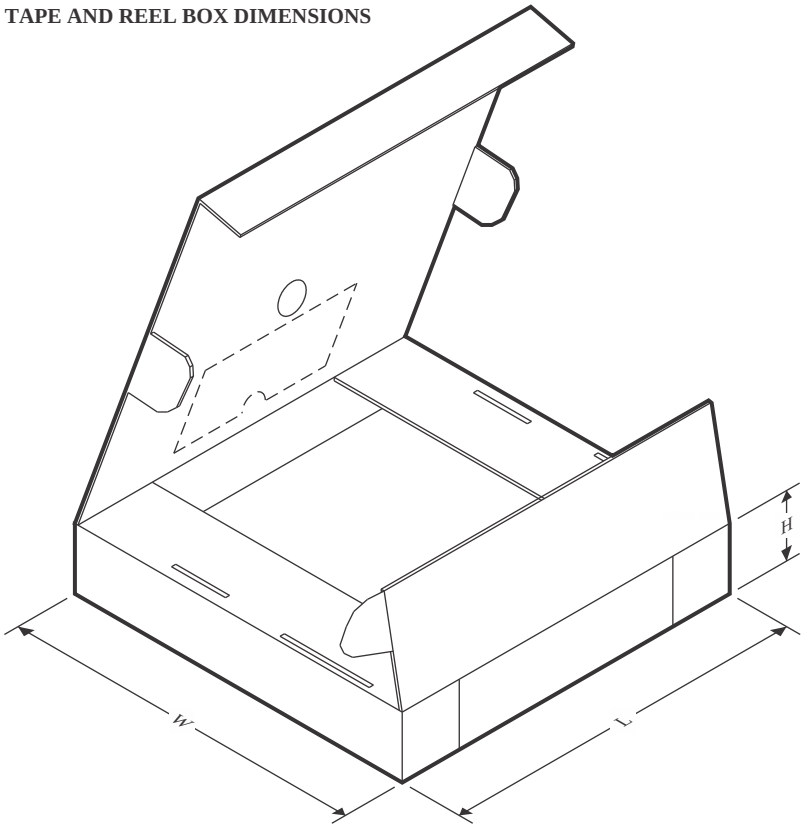
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS922050D1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS922050D1DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS922050D1DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS922050D2DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS922050D2DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS922050D2DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS922051D1DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS922051D1DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS922051D2DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS922051D2DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS922050D1DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS922050D1DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS922050D1DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS922050D2DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS922050D2DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS922050D2DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS922051D1DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS922051D1DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS922051D2DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
TPS922051D2DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

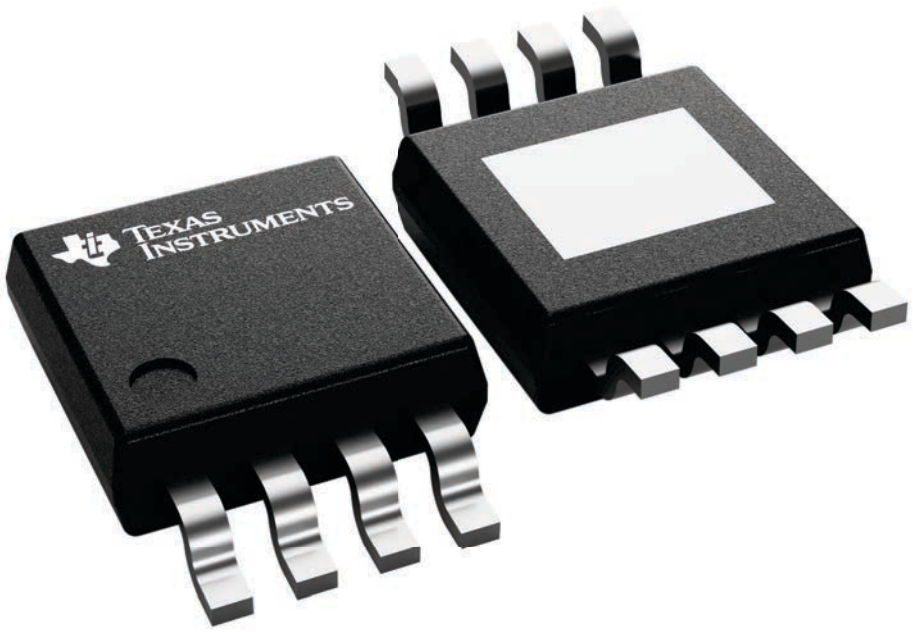
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

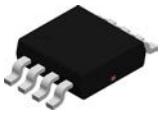
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

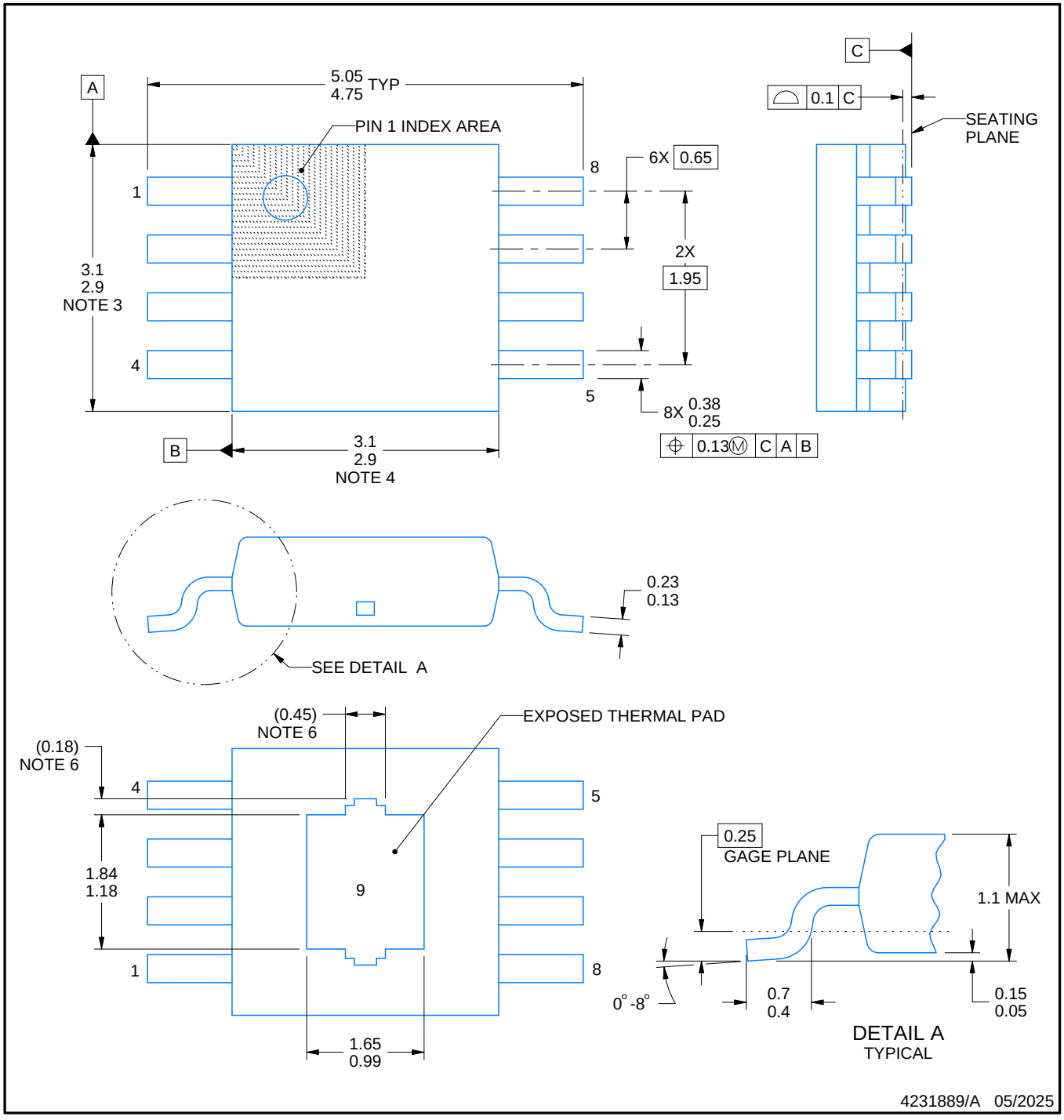
PACKAGE OUTLINE

DGN0008K



PowerPAD™ VSSOP - 1.1 mm max height

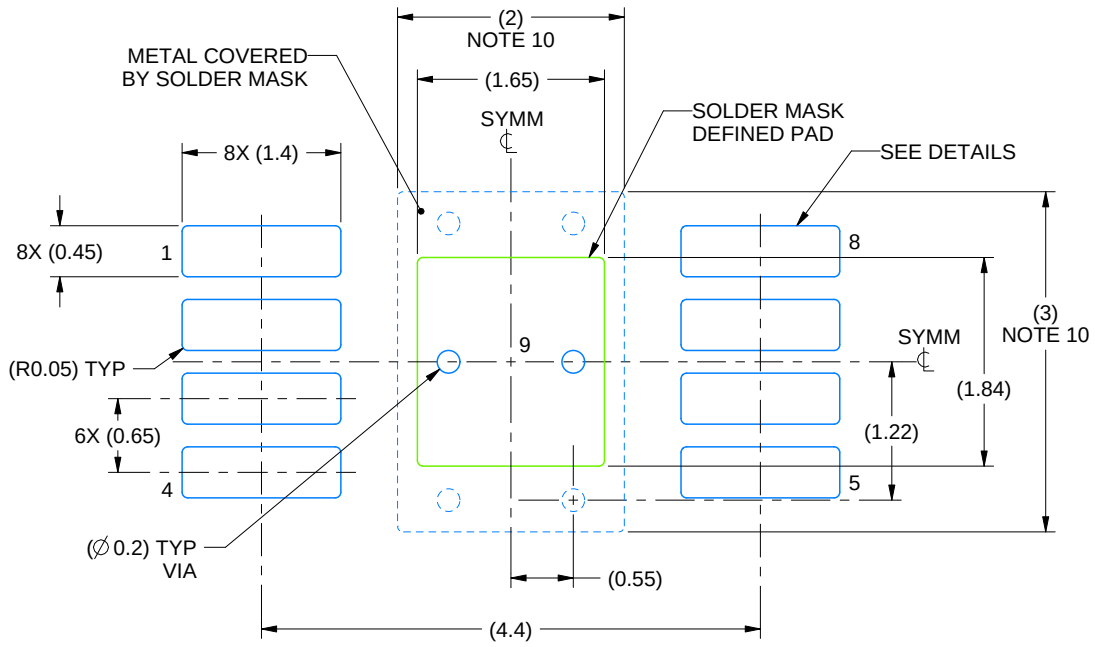
SMALL OUTLINE PACKAGE



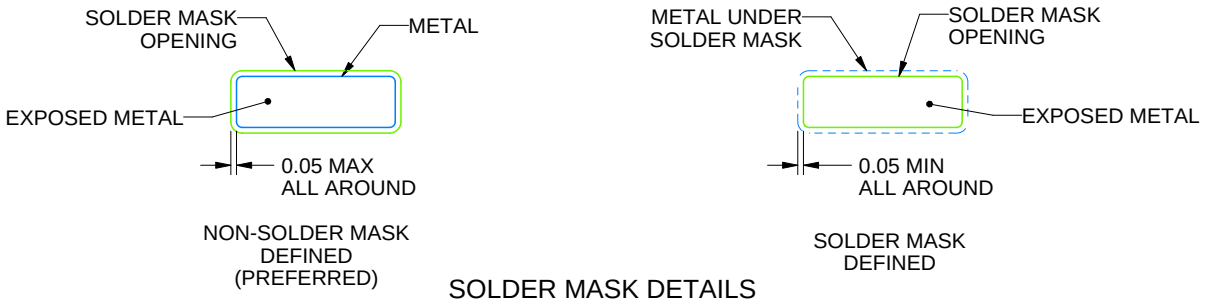
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

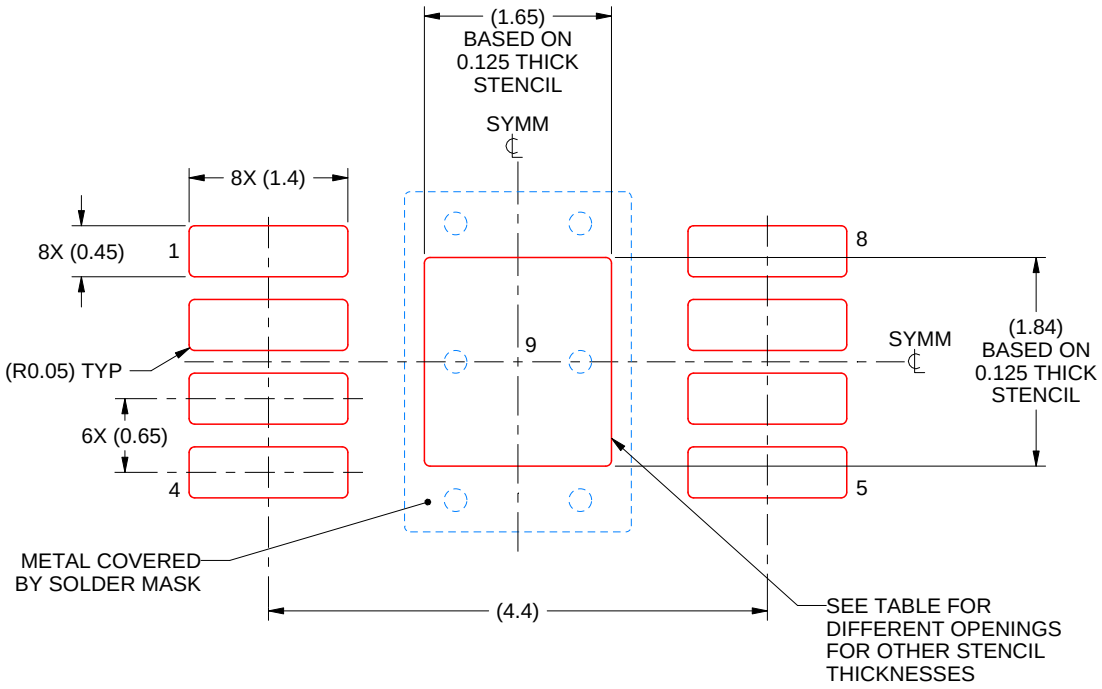


SOLDER MASK DETAILS

4231889/A 05/2025

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.84 X 2.06
0.125	1.65 X 1.84 (SHOWN)
0.15	1.51 X 1.68
0.175	1.39 X 1.56

4231889/A 05/2025

NOTES: (continued)

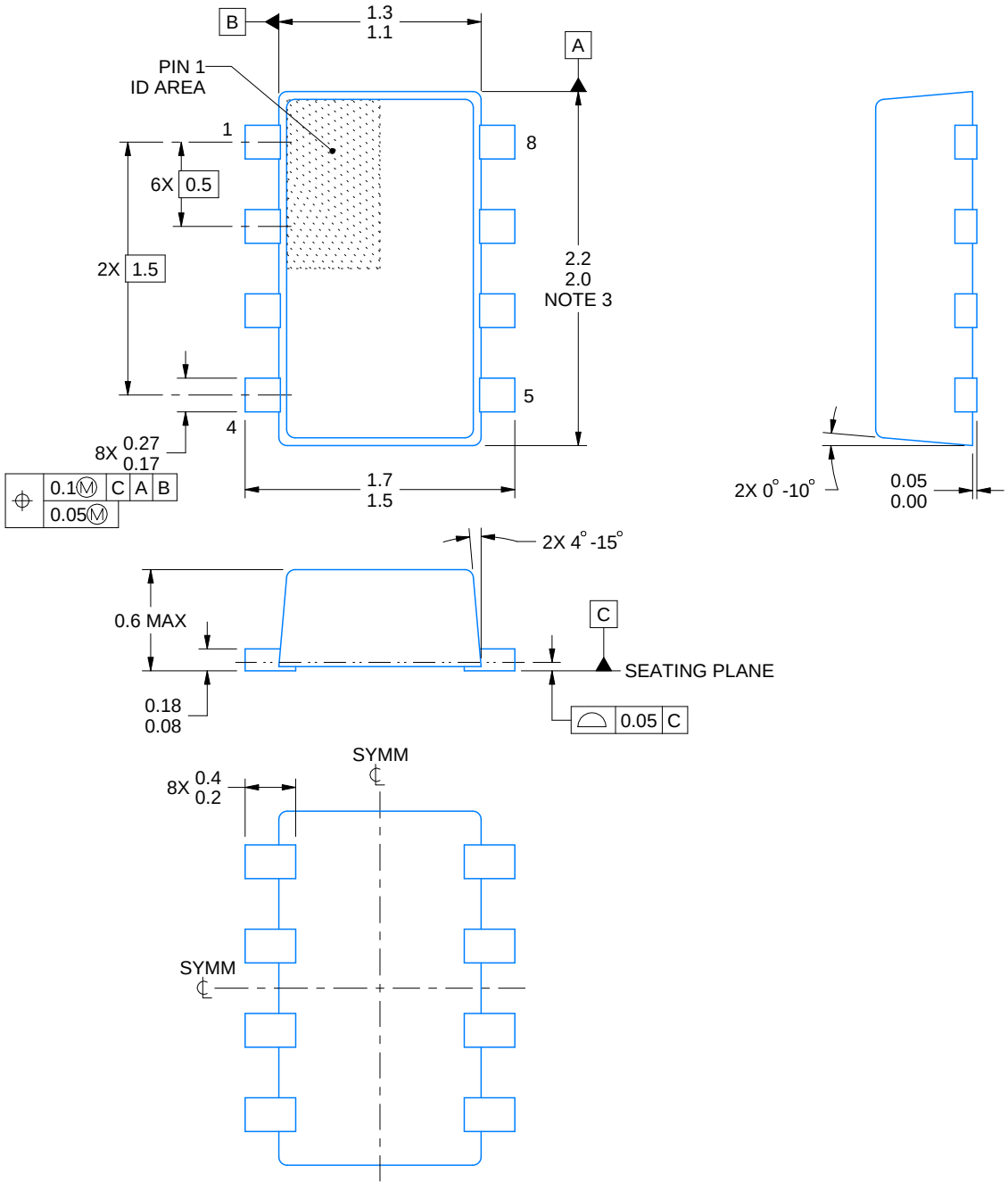
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/G 11/2024

NOTES:

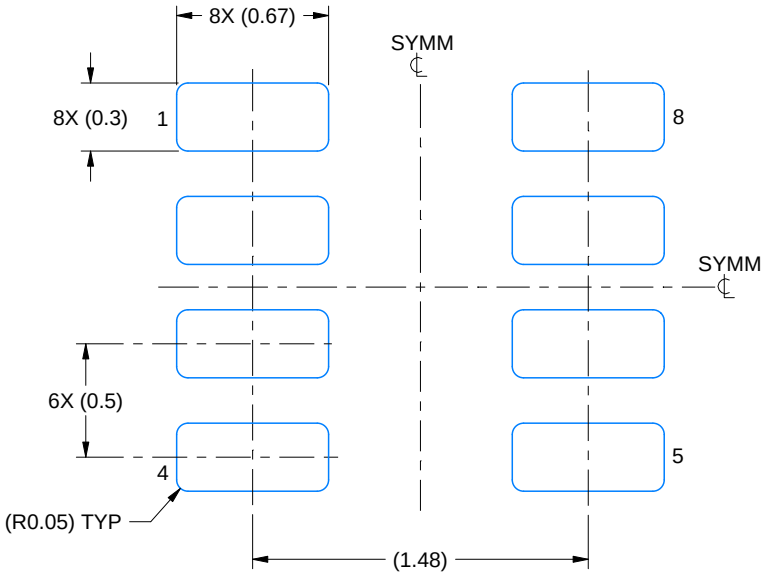
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

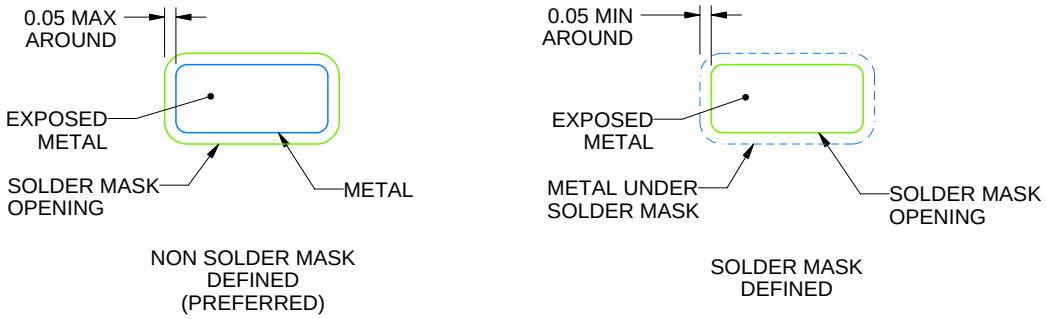
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

4224486/G 11/2024

NOTES: (continued)

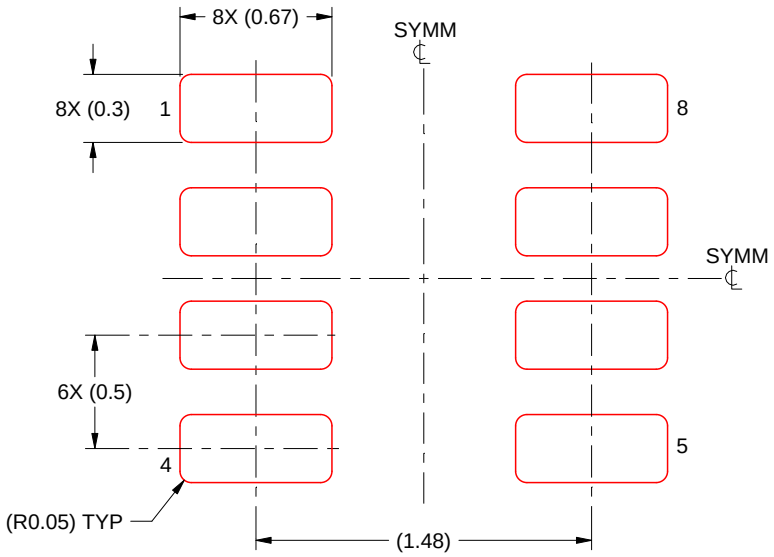
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

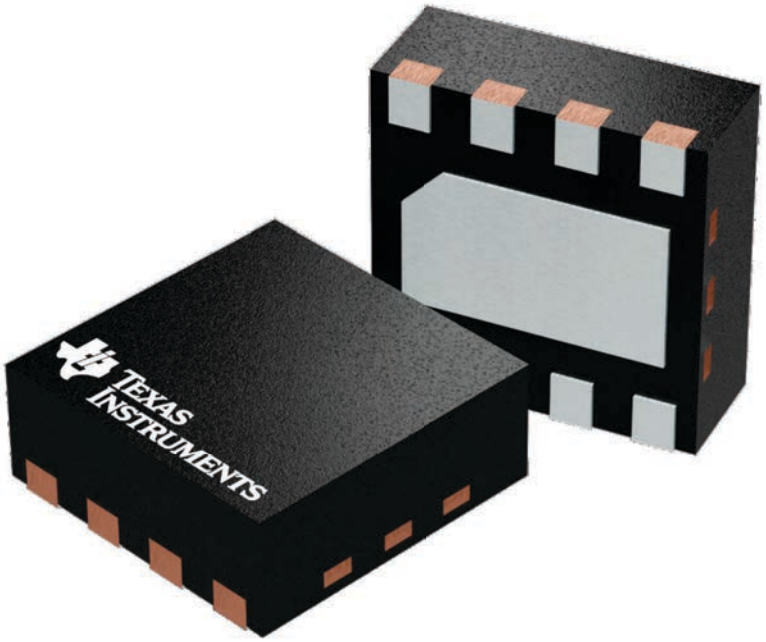
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



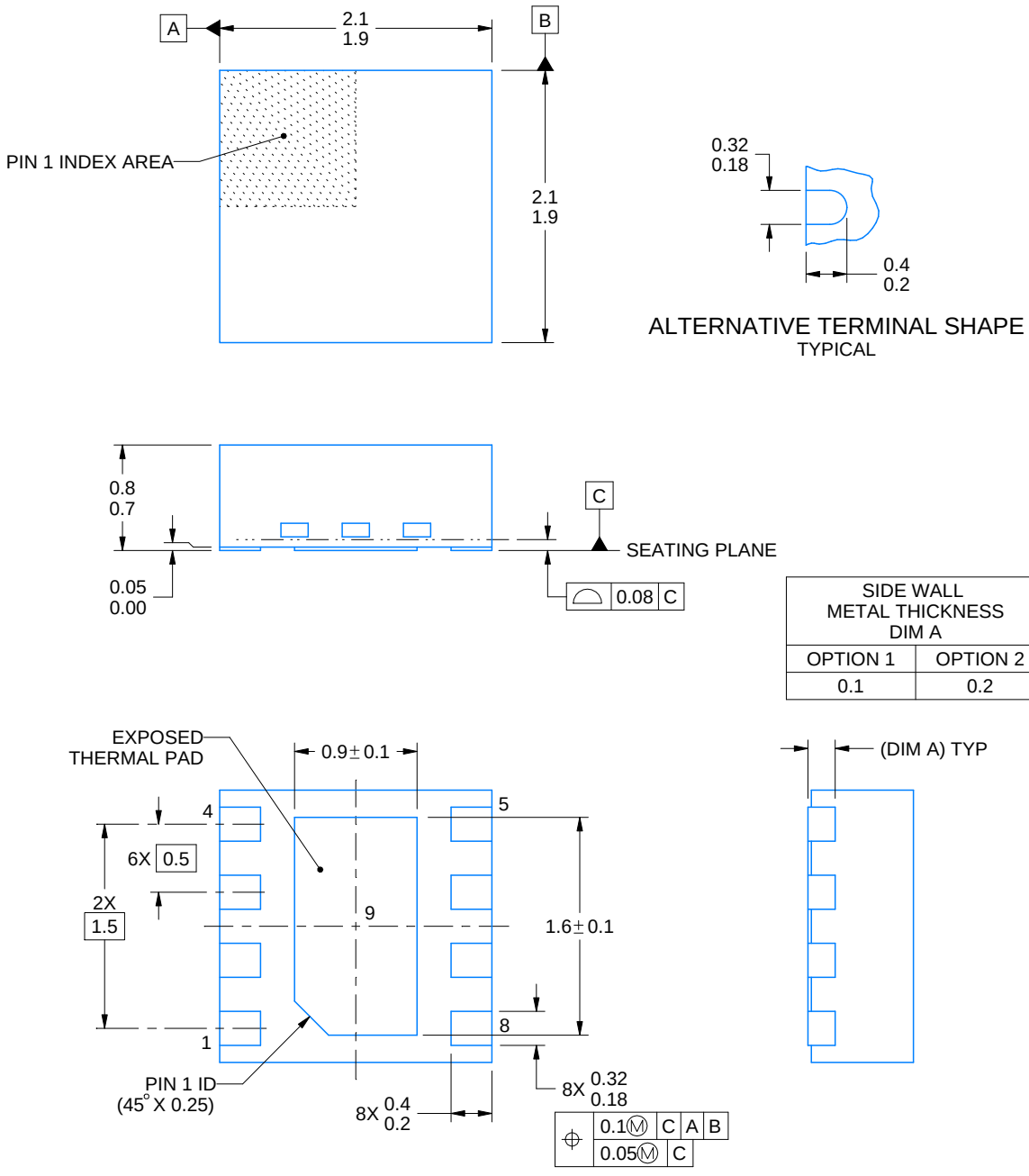
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

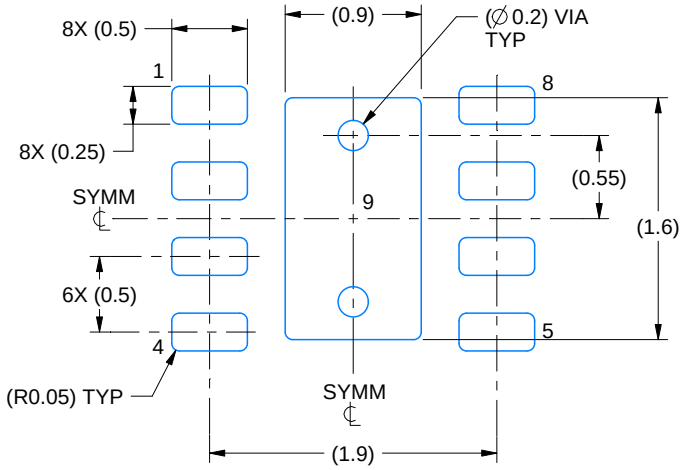
PLASTIC SMALL OUTLINE - NO LEAD



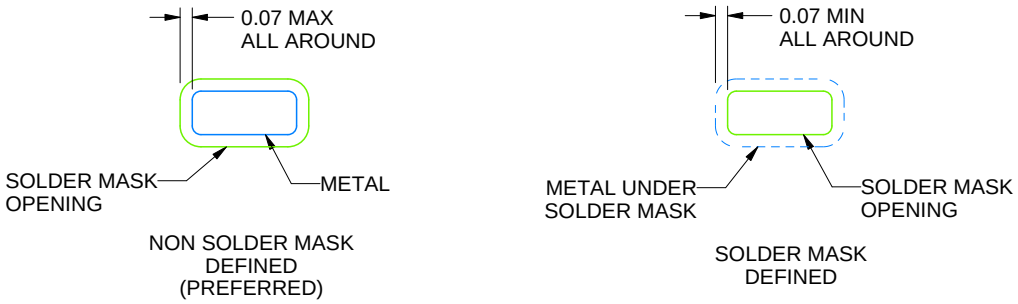
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

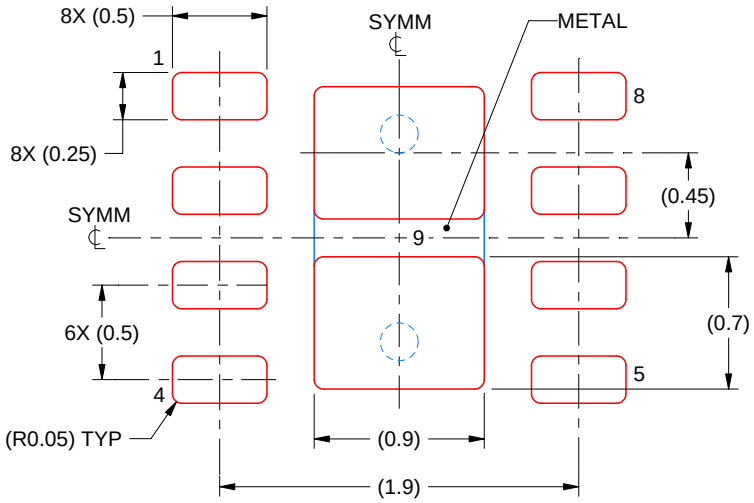


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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