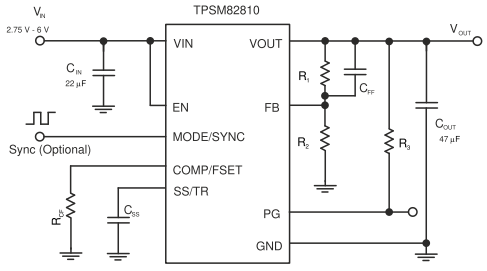
# TPSM8281x 2.75V～6V 入力、1A から 4A の降圧パワー モジュール、インダクタ内蔵、周波数同期機能付き、MicroSiP™ および MagPack™ パッケージ

## 1 特長

- 1.8MHz～4MHz の調整可能で同期可能なスイッチング周波数
- 2 つのパッケージ タイプが供給可能
  - MagPack パッケージ (シールド インダクタと IC) 13 ピン、高さ 2.0mm 未満
  - µSIL 14 ピン、高さ 2.4mm 未満
- 低 EMI 要件に対して最適化
  - フリップチップ ダイ マウント (ボンド ワイヤなし)
  - 最適化されたピン配置によるレイアウトの簡素化
- 拡散スペクトラム クロック バージョンを利用可能
- 強制 PWM または PFM/PWM 動作を選択可能
- 出力電圧精度 ±1% (PWM 動作)
- 入力電圧範囲:2.75V～6V
- 出力電圧範囲:0.6V ～ 5.5V
- 調整可能なソフト スタートまたはトラッキング
- ウィンドウ コンパレータによるパワー グッド出力
- 高精度の ENABLE 入力が可能
  - ユーザー定義の低電圧誤動作防止機能
  - 正確なシーケンシング
- 100% デューティ サイクル
- 出力放電
- 静止電流 15µA (標準値)
- 優れた放熱特性
- –40°C～125°Cの動作温度範囲
- ピン互換の 6A バージョン、高さ 1.6mm:TPSM82816
- WEBENCH® Power Designer により、TPSM8281x を使用するカスタム設計を作成

## 2 アプリケーション

- 光モジュール、データ センターの相互接続
- 試験 / 測定機器
- メディカル モニタと診断
- ワイヤレス インフラ
- 航空宇宙 / 防衛




回路図

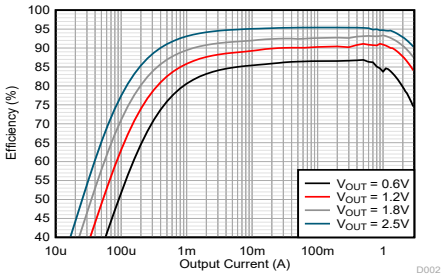
## 3 概要

TPSM8281x はピン互換で、高効率で使いやすい、出力電流範囲が 1A から最大 4A のインダクタ内蔵の同期整流降圧型 DC/DC パワー モジュールのファミリです。これらのデバイスは、固定周波数のピーク電流モード制御トポロジを使用しており、通信、試験および測定、医療用アプリケーションの高い電力密度要件に対応しています。抵抗値の低いスイッチにより、高い周囲温度でも最大 4A の連続出力電流を供給できます。スイッチング周波数は 1.8MHz～4MHz の範囲で変更でき、外部クロックと同期させることもできます。PFM/PWM モードでは、TPSM8281x は負荷範囲全体にわたって高い効率を維持します。これらのデバイスは PWM モードで 1% の出力電圧精度を実現するため、高精度の電源を簡単に設計できます。SS/TR ピンを使用して、正確なスタートアップ ランプによって突入電流を制限したり、このピンに印加される外部電圧に出力電圧をトラッキングすることでシーケンシングを行うことができます。

**製品情報**

| 部品番号 (3) | 出力電流 | パッケージ (1) | 本体サイズ (2) (公称) |
|---|---|---|---|
| TPSM82810 | 4A | SIL (µSiL、14) | 3.0mm × 4.0mm × 2.4mm |
| TPSM82813 | 3A | SIL (µSiL、14) | 3.0mm × 4.0mm × 2.4mm |
| | | VCA (QFN、13) | 2.5mm × 3.0mm × 1.95mm |
| TPSM82812 (4) | 2A | VCA (QFN、13) | 2.5mm × 3.0mm × 1.95mm |
| TPSM82811 (4) | 1A | | |

(1) 詳細については、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅 × 高さ) は公称値であり、該当する場合はピンも含まれます。
(3) デバイス比較表を参照してください。
(4) プレビュー情報 (量産データではありません)。




TPSM82813PVCAR の効率 ($V_{IN}$ = 3.3V)

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## 4 Device Comparison Table

| DEVICE NUMBER | OUTPUT CURRENT | SPREAD SPECTRUM CLOCKING |
|---|---|---|
| TPSM8281**0**SILR | 4A | OFF |
| TPSM8281**0S**SILR | 4A | ON |
| TPSM8281**3**SILR | 3A | OFF |
| TPSM8281**3S**SILR | 3A | ON |
| TPSM8281**3P**VCAR | 3A | OFF |
| TPSM8281**2P**VCAR(1) | 2A | OFF |
| TPSM8281**1P**VCAR(1) | 1A | OFF |

(1) Preview information (not production data).

# 5 Pin Configuration and Functions

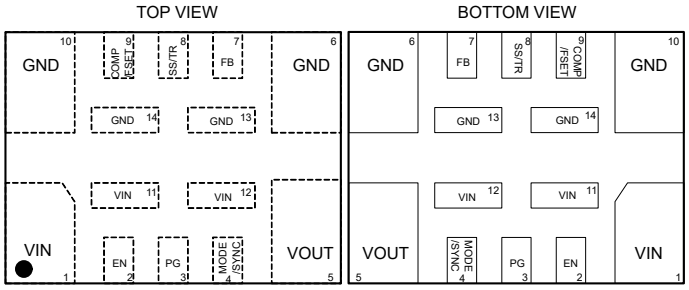



**図 5-1. SIL Package, 14-Pin µSiL**

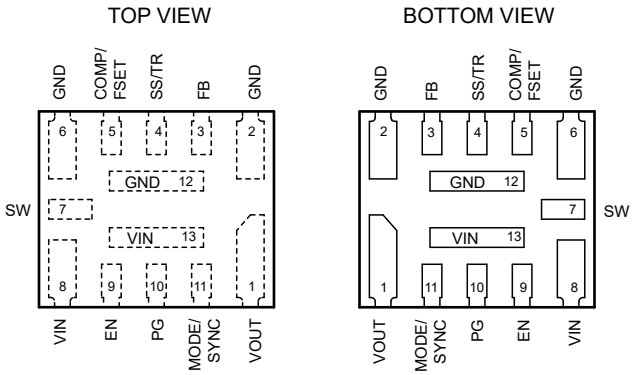



**図 5-2. VCA Package, 13-Pin QFN**

**表 5-1. Pin Functions**

| PIN | | | TYPE (1) | DESCRIPTION |
|---|---|---|---|---|
| NAME | SIL | VCA | | |
| EN | 2 | 9 | I | This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected. |
| FB | 7 | 3 | I | Voltage feedback input. Connect the output voltage resistor divider to this pin. |
| GND | 6, 10, 13, 14 | 2, 6, 12 | | Ground pin |
| MODE / SYNC | 4 | 11 | I | The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The MODE/SYNC pin can also be used to synchronize the device to an external frequency. See *セクション 9.3.2*. |
| COMP /FSET | 9 | 5 | I | Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. The switching frequency is set to 2.25 MHz if the pin is tied to GND or VIN. See 表 8-1. Do not leave this pin unconnected. |
| PG | 3 | 10 | O | Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used. A pullup resistor can be connected to any voltage not larger than VIN. |
| SS/TR | 8 | 4 | I | Soft-start, tracking pin. A capacitor connected from this pin to GND defines the output voltage rise time. The pin can also be used as an input for tracking and sequencing - see *Voltage Tracking*. |
| VOUT | 5 | 1 | | Output voltage pin. This pin is internally connected to the integrated inductor. |
| VIN | 1, 11, 12 | 8, 13 | | Power supply input. Connect the input capacitor as close as possible between the VIN and GND pins. |
| SW | — | 7 | O | This pin is the switch pin of the converter. This pin is connected to the internal power MOSFET and the inductor. Leave this pin unconnected for best EMI performance. |

(1) I = input, O = output

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage(2) | VIN, EN, MODE/SYNC | –0.3 | 6.5 | V |
| | SW (VCA package only) | –0.3 | $V_{IN}$+0.3 | V |
| | SW (transient for less than 10 ns, VCA package only, while switching) | –3 | 10 | V |
| | FB | –0.3 | 4 | V |
| | COMP/FSET, PG, SS/TR, VOUT | –0.3 | $V_{IN}$+0.3 | V |
| $I_{SINK\_PG}$ | Sink current at PG pin | | 10 | mA |
| $T_J$ | Operating junction temperature | –40 | 125 | °C |
| $T_{stg}$ | Storage temperature | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply voltage range | 2.75 | | 6 | V |
| $V_{OUT}$ | Output voltage range | 0.6 | | 5.5 | V |
| $C_{OUT}$ | Effective output capacitance(1) | 27 | 47 | 470 | µF |
| $C_{IN}$ | Effective input capacitance(1) | 5 | 10 | | µF |
| $R_{CF}$ | | 4.5 | | 100 | kΩ |
| $T_J$ | Operating junction temperature | -40 | | 125 | °C |

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied. Please see Section 9.3.3 about the output capacitance vs compensation setting and output voltage.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPSM8281x | | | | UNIT |
|---|---|---|---|---|---|---|
| | | VCA (13 PINS) | | µSIL (14 PINS) | | |
| | | EVM | JEDEC 51-7 | EVM | JEDEC 51-5 | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 27.4 | 73.0 | 35.0 | 52.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | n/a(3) | 34.1 | n/a(3) | 52.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | n/a(3) | 20.9 | n/a(3) | 16.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | (–3)(2) | (–1.4)(2) | 11.1 | 12.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 10.2 | 20.6 | 14.8 | 16.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report and Thermal Consideration.
(2) Case top temperature can be higher than temperature of active circuit because of inductor power dissipation. This results in a negative Junction-to-top characterization parameter.
(3) Not applicable to an EVM

## 6.5 Electrical Characteristics

Over operating junction temperature ($T_J$ = -40 °C to +125 °C) and $V_{IN}$ = 2.75 V to 6 V. Typical values at $V_{IN}$ = 5 V and $T_J$ = 25 °C. (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_Q$ | Operating Quiescent Current | EN = high, $I_{OUT}$ = 0mA, Device not switching | | 15 | 21 | µA |
| $I_{SD}$ | Shutdown Current | EN = 0V | | 0.11 | 18 | µA |
| $V_{UVLO}$ | Undervoltage Lockout Threshold | Rising Input Voltage | 2.5 | 2.6 | 2.75 | V |
| | | Falling Input Voltage | 2.25 | 2.5 | 2.6 | V |
| $T_{SD}$ | Thermal Shutdown Temperature | Rising Junction Temperature | | 170 | | °C |
| | Thermal Shutdown Hysteresis | | | 15 | | |
| **CONTROL (EN, SS/TR, PG, MODE/SYNC)** | | | | | | |
| $V_{IH}$ | High Level Input Voltage for MODE/SYNC Pin | | 1.1 | | | V |
| $V_{IL}$ | Low Level Input Voltage for MODE/SYNC Pin | | | | 0.3 | V |
| $f_{SYNC}$ | Frequency Range on MODE/SYNC Pin for Synchronization | | 1.8 | | 4 | MHz |
| | Duty Cycle of Synchronization Signal at MODE/SYNC Pin | | 40% | 50% | 60% | |
| $V_{IH}$ | Input Threshold Voltage for EN pin | Rising EN | 1.06 | 1.1 | 1.15 | V |
| $V_{IL}$ | Input Threshold Voltage for EN pin | Falling EN | 0.96 | 1.0 | 1.05 | V |
| $I_{LKG}$ | Input Leakage Current for EN, MODE/SYNC Pins | EN, MODE/SYNC = $V_{IN}$ or GND | | | 150 | nA |
| $V_{TH\_PG}$ | UVP Power Good Threshold | Rising (%$V_{FB}$) | 92% | 95% | 98% | |
| | UVP Power Good Threshold | Falling (%$V_{FB}$) | 87% | 90% | 93% | |
| | OVP Power Good Threshold | Rising (%$V_{FB}$) | 107% | 110% | 113% | |
| | OVP Power Good Threshold | Falling (%$V_{FB}$) | 104% | 107% | 111% | |
| | Power Good De-glitch Time | for a high level to low level transition on power good | | 40 | | µs |
| $V_{OL\_PG}$ | Power Good Output Low Voltage | $I_{PG}$ = 2mA | | 0.07 | 0.3 | V |
| $I_{LKG\_PG}$ | Input Leakage Current for PG Pin | $V_{PG}$ = 5V | | | 100 | nA |
| $I_{SS/TR}$ | SS/TR Pin Source Current | | 2.1 | 2.5 | 2.8 | µA |
| $t_{delay}$ | Start-up Delay Time | Time from EN=high to start switching; $V_{IN}$ applied already | 135 | 200 | 450 | µs |
| $t_{ramp}$ | Ramp time; SS/TR Pin Open | Time from first switching pulse until 95% of nominal output voltage | 100 | 150 | 200 | µs |
| | Tracking Gain | $V_{FB}/V_{SS/TR}$ | | 1 | | |
| | Tracking Offset | FB pin with $V_{SS/TR}$ = 0V | | 17 | | mV |
| **POWER SWITCH** | | | | | | |
| $R_{DS(ON)}$ | High-Side MOSFET ON-Resistance | $V_{IN}$ ≥ 5V | | 37 | 60 | mΩ |
| $R_{DS(ON)}$ | Low-Side MOSFET ON-Resistance | $V_{IN}$ ≥ 5V | | 15 | 35 | mΩ |
| $R_{DP}$ | Dropout resistance | 100% mode. Maximum value at $V_{IN}$ = 3.3V, $T_J$ = 85°C | | 50 | 90 | mΩ |
| $I_{LIMH}$ | High-Side MOSFET Current Limit (1) | TPSM82810; $V_{IN}$ = 3V to 6V | 4.8 | 5.6 | 6.55 | A |
| $I_{LIMH}$ | High-Side MOSFET Current Limit(1) | TPSM82813; $V_{IN}$ = 3V to 6V | 3.9 | 4.5 | 5.25 | A |
| $I_{LIMNEG}$ | Negative Current Limit (1) | MODE/SYNC = HIGH | | –1.8 | | A |
| $f_S$ | PWM Switching Frequency Range | | 1.8 | 2.25 | 4 | MHz |
| $f_S$ | PWM Switching Frequency | with COMP/FSET tied to VIN or GND | 2.025 | 2.25 | 2.475 | MHz |
| | PWM Switching Frequency Tolerance | using a resistor from COMP/FSET to GND | –19% | | 18% | |

## 6.5 Electrical Characteristics (続き)

Over operating junction temperature ($T_J$ = -40 °C to +125 °C) and $V_{IN}$ = 2.75 V to 6 V. Typical values at $V_{IN}$ = 5 V and $T_J$ = 25 °C. (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{on,min}$ | Minimum on-time | $V_{IN}$ = 3.3V | | 50 | 75 | ns |
| $t_{off,min}$ | Minimum off-time | $V_{IN}$ = 3.3V | | 30 | | ns |
| **OUTPUT** | | | | | | |
| $V_{FB}$ | Feedback Voltage Accuracy | $V_{IN} \geq V_{OUT}$ + 1V; PWM mode | 594 | 600 | 606 | mV |
| | | $V_{IN} \geq V_{OUT}$ + 1V; PFM mode<br>$V_{OUT} \geq$ 1.5V; $C_{OUT,eff} \geq$ 27µF | 594 | 600 | 612 | mV |
| | | 1 V ≤ $V_{OUT}$ < 1.5V; PFM mode<br>$C_{OUT,eff} \geq$ 47µF | 594 | 600 | 615 | mV |
| $I_{LKG\_FB}$ | Input Leakage Current (FB pin) | $V_{FB}$ = 0.6V | | 1 | 70 | nA |
| $V_{FB}$ | Feedback Voltage Accuracy with Voltage Tracking | $V_{IN} \geq V_{OUT}$ + 1V; PWM mode<br>$V_{SS/TR}$ = 0.3V | 297 | 300 | 321 | mV |
| $R_{dis}$ | Output Discharge Resistance | | | 30 | 50 | Ω |

(1) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see Current Limit And Short Circuit Protection section).

## 6.6 Typical Characteristics

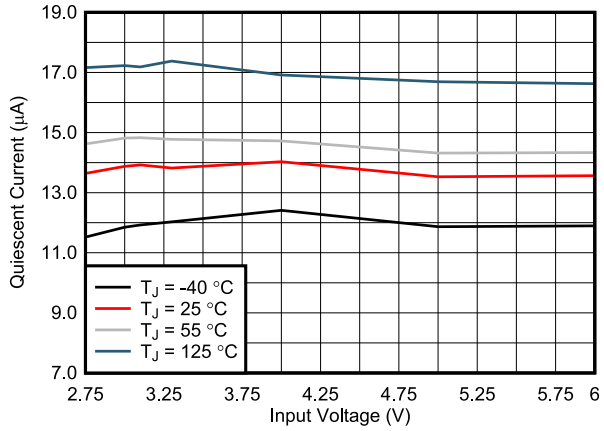



図 6-1. Quiescent Current

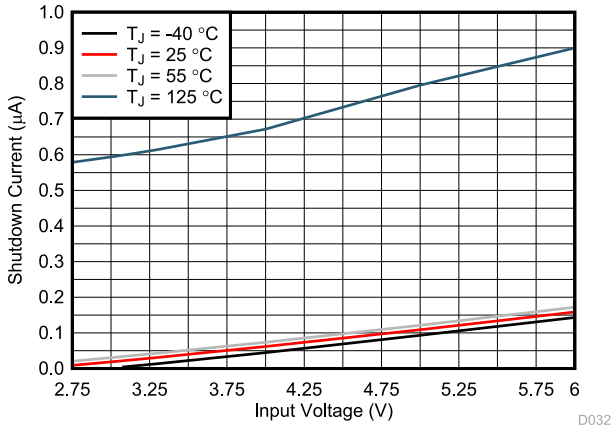



図 6-2. Shutdown Current

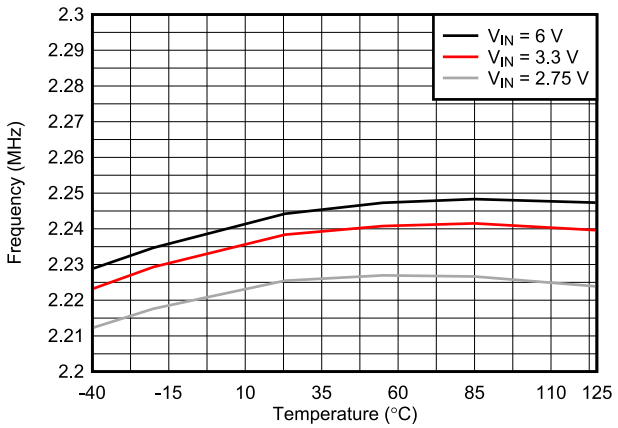



図 6-3. Oscillator Frequency vs Temperature (COMP/FSET tied to VIN or GND)

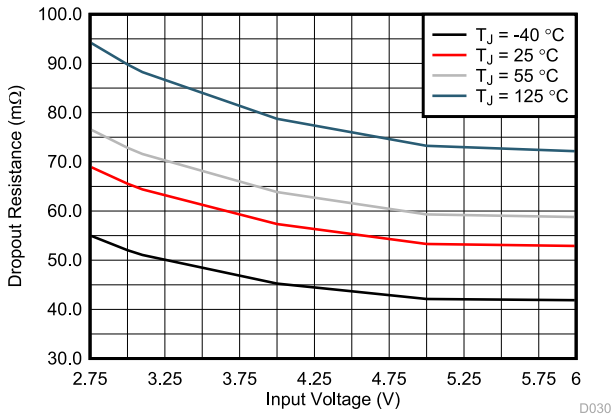



図 6-4. Dropout Resistance

# 7 Parameter Measurement Information

## 7.1 Schematic

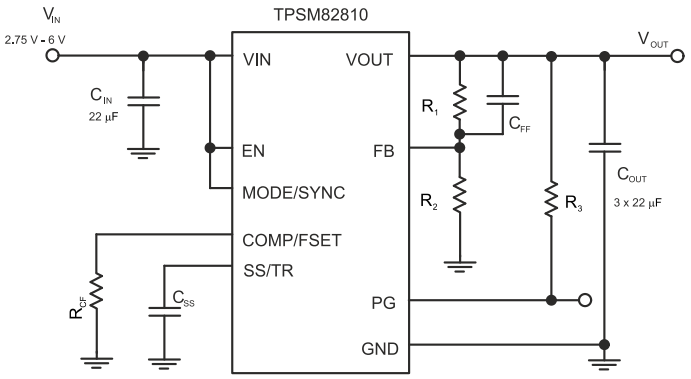



**図 7-1. Measurement Setup for TPSM8281x**

**表 7-1. List of Components for the TPSM8281xSILR**

| REFERENCE | DESCRIPTION | MANUFACTURER (1) |
|---|---|---|
| IC | TPSM82810 or TPSM82813 | Texas Instruments |
| $C_{IN}$ | 22µF / X7T / 10V; GRM21BD71A226ME44 | Murata |
| $C_{OUT}$ | 3 x 22µF / X7T / 10V; GRM21BD71A226ME44 | Murata |
| $C_{SS}$ | 4.7nF | Any |
| $R_{CF}$ | 10kΩ | Any |
| $C_{FF}$ | 10pF | Any |
| $R_1$ | Depending on VOUT | Any |
| $R_2$ | Depending on VOUT | Any |
| $R_3$ | 100kΩ | Any |

**表 7-2. List of Components for the TPSM8281xPVCAR**

| REFERENCE | DESCRIPTION | MANUFACTURER (1) |
|---|---|---|
| IC | TPSM82811PVCAR, TPSM82812PVCAR, TPSM82813PVCAR | Texas Instruments |
| $C_{IN}$ | 22µF / X7R / 10V; GRM21BZ1A226ME15L | Murata |
| $C_{OUT}$ | 2x 47uF / X6S / 6.3V; GRM21BC80J476ME01L | Murata |
| $C_{SS}$ | 4.7nF | Any |
| $R_{CF}$ | 10kΩ | Any |
| $C_{FF}$ | 10pF | Any |
| $R_1$ | Depending on VOUT | Any |
| $R_2$ | Depending on VOUT | Any |
| $R_3$ | 100kΩ | Any |

(1) See the *Third-party Products Disclaimer*.

注

The input and output capacitor part numbers in each table above indicate the BOM used for parameter measurement. Both designs work in either configuration.

# 8 Detailed Description

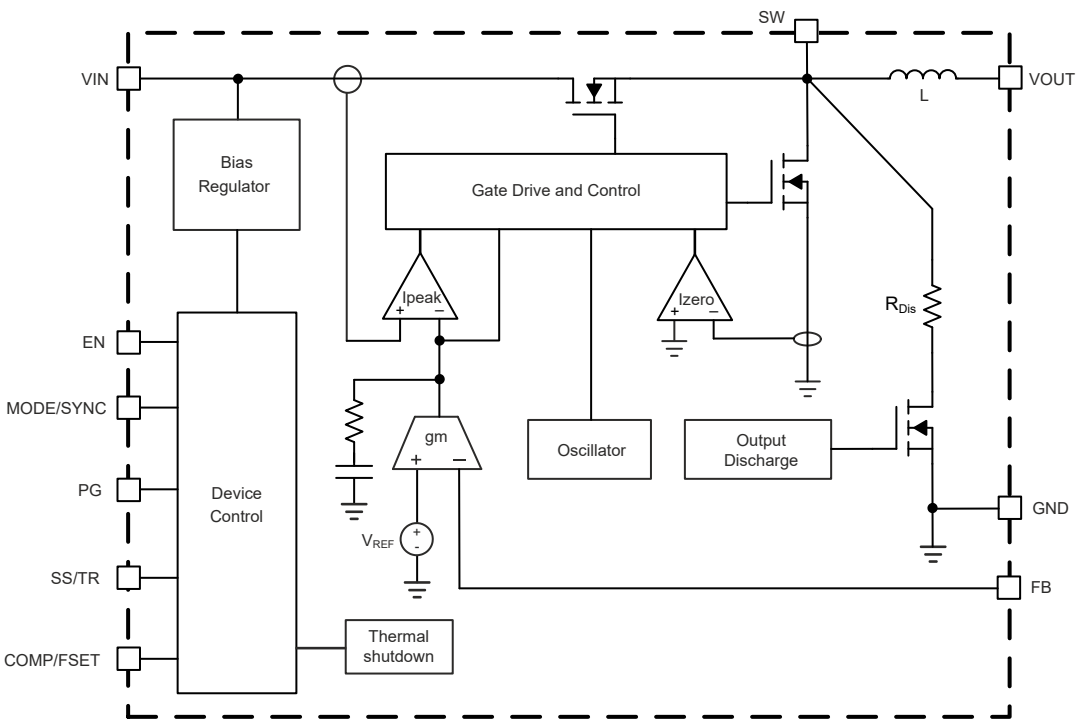
## 8.1 Overview

The TPSM8281x synchronous switch mode DC/DC converter power modules are based on a fixed-frequency peak current-mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with the TPSM8281x, one of three internal compensation settings can be selected. See *セクション 8.3.3*. The compensation setting is selected either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors.

The devices support fixed-frequency forced PWM operation with the MODE/SYNC pin tied to a logic high level. When the MODE/SYNC pin is set to a logic low level, the device operates in power save mode (PFM) at low-output currents and automatically transitions to fixed-frequency PWM mode at higher output currents. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output currents. The device can be synchronized to an external clock signal in a range from 1.8MHz to 4MHz applied to the MODE/SYNC pin.

The TPSM8281xP versions in the VCA package use MagPack technology to deliver the highest-performance power module design. Leveraging Texas Instruments' proprietary integrated-magnetics packaging technology, MagPack (magnetics in package) power modules deliver industry-leading power density, high efficiency and good thermal performance, ease of use, and reduced EMI emissions.

## 8.2 Functional Block Diagram




注

SW is only accessable with the VCA package

## 8.3 Feature Description

### *8.3.1 Precise Enable (EN)*

The TPSM8281x starts operation when the rising EN threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this

mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off. The voltage applied at the EN pin of the TPSM8281x is compared to a fixed threshold of 1.1V for a rising voltage.

The enable input threshold for a falling edge is typically 100mV lower than the rising edge threshold. The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the EN pin. The Precise Enable input also allows you to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. See the *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold* analog design journal for more details.

### *8.3.2 Output Discharge*

The purpose of the discharge function is to make sure of a defined down-ramp of the output voltage when the device is disabled and keep the output voltage close to 0V when the device is off. The output discharge feature is only active after the TPSM8281x has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 1V.

### *8.3.3 COMP/FSET*

This pin sets two different parameters independently:

- Internal compensation settings for the control loop (three settings available)
- The switching frequency in PWM mode from 1.8MHz to 4MHz

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation adapts the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is set after enabling the converter, so a change in the resistor during operation only has an effect on the switching frequency but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined switching frequency and compensation. Do not leave the pin floating.

The switching frequency must be selected based on the maximum input voltage and the output voltage to meet the specifications for the minimum on-time.

Example: $V_{IN}$ = 5.5 V, $V_{OUT}$ = 1 V

$$f_{Sw,max} = \frac{V_{OUT}}{V_{IN} \times t_{ON,min}} = \frac{1\,V}{5.5\,V \times 75\,ns} = 2.42\,MHz \quad (1)$$

The compensation range has to be chosen based on the minimum effective capacitance used. The capacitance can be increased from the minimum value as given in 表 8-1 up to the maximum of 470µF in all of the three compensation ranges. The higher compensation settings give better load transient response, when larger output capacitances are used. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1:

$$R_{CF}(k\Omega) = \frac{18MHz \times k\Omega}{f_S(MHz)} \quad (2)$$

For compensation (comp) setting 2:

$$R_{CF}(k\Omega) = \frac{60MHz \times k\Omega}{f_S(MHz)} \quad (3)$$

For compensation (comp) setting 3:

$$R_{CF}(k\Omega) = \frac{180MHz \times k\Omega}{f_S(MHz)} \quad (4)$$

**表 8-1. Switching Frequency and Compensation**

| COMPENSATION | $R_{CF}$ | SWITCHING FREQUENCY | MINIMUM OUTPUT CAPACITANCE FOR VOUT < 1V | MINIMUM OUTPUT CAPACITANCE FOR 1V ≤ VOUT < 3.3V | MINIMUM OUTPUT CAPACITANCE FOR VOUT ≥ 3.3V |
|---|---|---|---|---|---|
| for smallest output capacitance (comp setting 1) | 10kΩ ... 4.5kΩ | 1.8MHz (10kΩ) ... 4MHz (4.5kΩ) according to Equation 3 | 53µF | 32µF | 27µF |
| for medium output capacitance (comp setting 2) | 33kΩ ... 15kΩ | 1.8MHz (33kΩ) ... 4MHz (15kΩ) according to Equation 4 | 100µF | 60µF | 50µF |
| for large output capacitance (comp setting 3) | 100kΩ ... 45kΩ | 1.8MHz (100kΩ) ... 4MHz (45kΩ) according to Equation 5 | 200µF | 120µF | 100µF |
| for smallest output capacitance (comp setting 1) | tied to GND | internally fixed 2.25MHz | 53µF | 32µF | 27µF |
| for large output capacitance (comp setting 3) | tied to $V_{IN}$ | internally fixed 2.25MHz | 200µF | 120µF | 100µF |

Refer to *セクション 9.2.2.5* for further details on the output capacitance required depending on the output voltage. All values are the effective value of capacitance.

A too high resistor value for $R_{CF}$ is read as "tied to $V_{IN}$", and a value below the lowest range as "tied to GND". The minimum output capacitance in 表 8-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

### *8.3.4 MODE/SYNC*

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin forces PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8MHz to 4MHz for external synchronization. When an external clock is applied, the device operates in PWM mode. As with the switching frequency selection, the specification for the minimum on-time has to be observed when applying the external clock signal. When using external synchronization, TI recommends to set the switching frequency as set by $R_{CF}$ to a similar value as the externally applied clock. This ensures that the switching frequency stays in the same range when the external clock fails and the settling time to the internal clock is reduced. When there is no resistor from COMP/FSET to GND, but the pin is pulled high or low, external synchronization is not possible. An internal PLL allows you to change from an internal clock to external clock during operation. The synchronization to the external clock is done on the falling edge of the applied clock to the rising edge of the internal SW pin. The MODE/SYNC pin can be changed during operation. See セクション 9.3.2 for more details.

### *8.3.5 Spread Spectrum Clocking (SSC) - TPSM8281xS*

These devices offer spread spectrum clocking, where the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288kHz above the nominal switching frequency. When the device is externally synchronized, the TPSM8281xS follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

### *8.3.6 Undervoltage Lockout (UVLO)*

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the MOSFETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage goes below the falling threshold.

### 8.3.7 Power-Good Output (PG)

The device has a power good output with window comparator. The PG pin goes high impedance after the FB pin voltage is above 95% and less than 107% of the nominal voltage, and is driven low after the voltage falls below typically 90% or higher than 110% of the nominal voltage. 表 8-2 shows the typical PG pin logic. The PG pin is an open-drain output and is specified to sink up to 2mA. The power good output requires a pullup resistor connected to any voltage rail less than VIN. The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. If not used, the PG pin can be left floating or connected to GND.

**表 8-2. Power Good Pin Logic**

| DEVICE STATE | | PG LOGIC STATUS | |
|---|---|---|---|
| | | HIGH IMPEDANCE | LOW |
| Enabled (EN = High) | $0.57V \le V_{FB} \le 0.642V$ | √ | |
| | $V_{FB} < 0.54V$ or $V_{FB} > 0.66V$ | | √ |
| Shutdown (EN = Low) | | | √ |
| UVLO | $2V \le V_{IN} < V_{UVLO}$ | | √ |
| Thermal Shutdown | $T_J > T_{JSD}$ | | √ |
| Power Supply Removal | $V_{IN} < 2V$ | √ | |

The PG pin has a 40µs deglitch time on the falling edge.

### 8.3.8 Thermal Shutdown

The junction temperature ($T_J$) of the device is monitored by an internal temperature sensor. If $T_J$ exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When $T_J$ decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During PFM, the thermal shutdown is not active.

## 8.4 Device Functional Modes

### 8.4.1 Pulse Width Modulation (PWM) Operation

The TPSM8281x has two operating modes: Forced PWM mode and PFM/PWM mode.

With the MODE/SYNC pin set to high, the TPSM8281x operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP/FSET pin to GND or by an external clock signal applied to the MODE/SYNC pin.

### 8.4.2 Power Save Mode Operation (PFM/PWM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 1.2A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses.

In power save mode, the switching frequency decreases linearly with the load current to maintain high efficiency. The linear behavior of the switching frequency in power save mode is shown in 図 8-1.

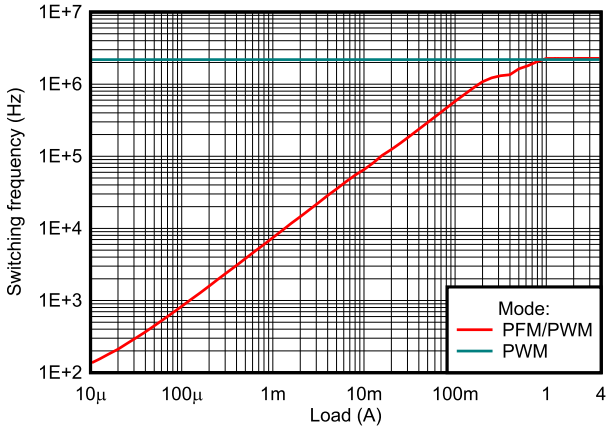



**図 8-1. Switching Frequency versus Output Current ($V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $R_{CF}$ = 8.06kΩ)**

### *8.4.3 100% Duty-Cycle Operation*

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. When the minimum off-time of typically 30ns is reached, the TPSM8281x skips switching cycles while approaching 100% mode. In 100% mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN\ (min)} = V_{OUT\ (min)} + I_{OUT} \times R_{DP} \quad (5)$$

where

- $R_{DP}$ is the resistance from $V_{IN}$ to $V_{OUT}$, which includes the high-side MOSFET on-resistance and DC resistance of the inductor
- $V_{OUT\ (min)}$ is the minimum output voltage the load can accept

### *8.4.4 Current Limit and Short Circuit Protection*

The TPSM8281x is protected against overload and short circuit events. If the inductor current exceeds the current limit $I_{LIMH}$, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. Due to internal propagation delays, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \cdot t_{PD} \quad (6)$$

where

- $I_{LIMH}$ is the static current limit, as specified in the electrical characteristics
- L is the effective inductance (typically 470nH)
- $V_L$ is the voltage across the inductor ($V_{IN}$ - $V_{OUT}$)
- $t_{PD}$ is the internal propagation delay of typically 50ns

The dynamic peak current is calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \cdot 50ns \quad (7)$$

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned

off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in Forced PWM mode.

### *8.4.5 Soft Start / Tracking (SS/TR)*

The internal soft-start circuitry controls the output voltage slope during start-up. This control avoids excessive inrush current and makes sure of a controlled output voltage rise time. This control also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high, the device starts switching after a delay of about 200µs. Then $V_{OUT}$ rises with a slope controlled by an external capacitor connected to the SS/TR pin.

A capacitor connected from SS/TR to GND is charged with 2.5µA by an internal current source during soft start until the capacitor reaches the reference voltage of 0.6V. After reaching 0.6V, the SS/TR pin voltage is clamped internally while the SS/TR pin voltage keeps rising to a maximum of about 3.3V. The capacitance required to set a certain ramp-time ($t_{ramp}$) is:

$$C_{SS}\left[nF\right] = \frac{2.5\mu A \cdot t_{ramp}\left[ms\right]}{0.6V} \tag{8}$$

Leaving the SS/TR pin un-connected provides the fastest start-up ramp of 150µs typically. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin to GND tomake sure of a proper low level. Returning from those states causes a new start-up sequence.

A voltage applied at the SS/TR pin can also be used to track a controller voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current. An external voltage applied on SS/TR is internally clamped to the feedback voltage (0.6V). TI recommends to set the final value of the external voltage on SS/TR to be slightly above 0.6V to make sure the device operates with the internal reference voltage when the power-up sequencing is finished. See *セクション 9.3.1*.

# 9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 9.1 Application Information

The TPSM8281x are synchronous step-down converter power modules. The required power inductor is integrated inside the TPSM8281x. The inductor is shielded and has an inductance of 470 nH with approximately a ±20% tolerance.

The VCA MagPack package includes a 470nH shielded inductor and shields the entire IC for better EMI performance. The smaller size and lower height provide higher power density compared to the SIL package.

The 1A, 2A, and 3A VCA versions have the same efficiency and performance, differing only in the output current rating. The versions are pin-to-pin compatible with higher-current versions: TPSM82814PVCAR (4A) and TPSM82816PVCAR (6A).

The 3A SIL version has the same efficiency and performance as the 4A SIL version. Both versions differ only in the output current rating. The versions are pin-to-pin compatible with the higher-current TPSM82816SIER (6A) version.

## 9.2 Typical Application

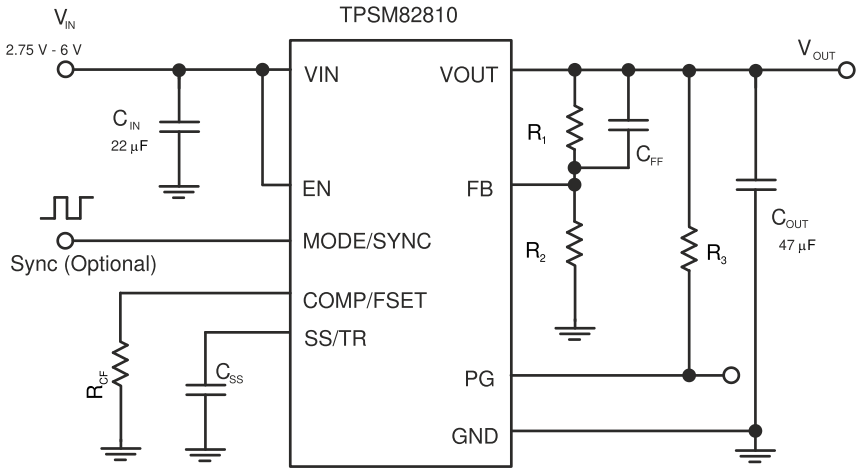



**図 9-1. Typical Application Schematic**

### *9.2.1 Design Requirements*

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

### *9.2.2 Detailed Design Procedure*

#### 9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM8281x device with the WEBENCH® Power Designer.

1. In the part number field start entering the part number if you have a preference and wait until a part list will appear and populate. If there is no preference leave this field blank.
2. In the next section (auto-filled if you started with a part number) enter the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
3. In the "Design Considerations" section select your design priorities.

4. View your design proposal and compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools here: Design and simulation tools.

#### 9.2.2.2 Setting the Output Voltage

The output voltage of the TPSM8281x is adjustable. Choose resistors R1 and R2 to set the output voltage within a range of 0.6V to 5.5V according to Equation 10. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100kΩ to have at least 6µA of current in the voltage divider.

$$R1 = R2 \times \left( \frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left( \frac{V_{OUT}}{0.6V} - 1 \right) \tag{9}$$

Lower values of FB resistors achieve better noise immunity at the expense of reduced light load efficiency. Details about optimizing feedback resistor networks can be found in the analog design journal article Design considerations for a resistive feedback divider in a DC/DC converter.

#### 9.2.2.3 Feedforward capacitor

A feedforward capacitor ($C_{FF}$) is recommended in parallel with $R_1$ in order to improve the transient response. Regardless of the FB resistor values, the $C_{FF}$ value must always be 10pF.

#### 9.2.2.4 Input Capacitor

For most applications, a 22µF nominal ceramic capacitor is recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A X7R or X7T multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For applications with ambient temperatures below 85°C, a capacitor with X5R dielectric can be used. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating. The minimum required input capacitance is 5µF.

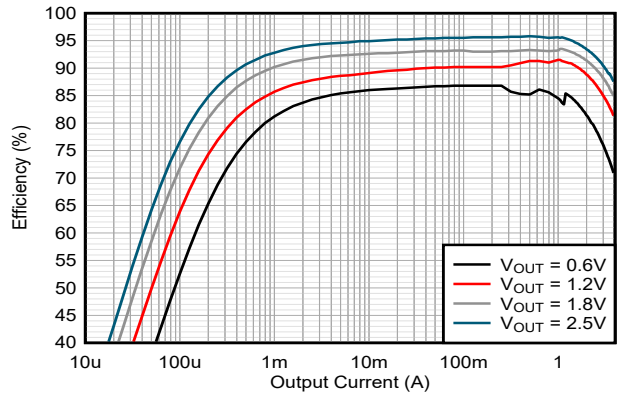
#### 9.2.2.5 Output Capacitor

The architecture of the TPSM8281x allows the use of ceramic output capacitors which have low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the low resistance up to high frequencies and to get a narrow capacitance variation with temperature, TI recommends to use an X7R or X7T dielectric. At temperatures below 85°C, an X5R dielectric can be used.

Using a higher capacitance value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode. By changing the device compensation with a resistor from COMP/FSET to GND, the device can be compensated in three steps based on the minimum capacitance used on the output. The maximum capacitance is 470µF in any of the compensation settings. The minimum capacitance required on the output depends on the compensation setting and output voltage as shown in 表 8-1. For output voltages below 1V, the minimum required capacitance increases linearly from 32µF at 1V to 53µF at 0.6V with the compensation setting for smallest output capacitance. Other compensation settings scale the same. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating.

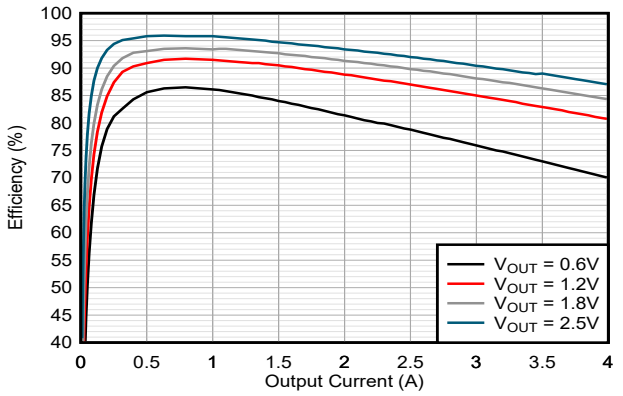
### 9.2.3 Application Curves

$T_A$ = 25°C, $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, 1.8MHz, PWM mode, BOM = 表 7-1 unless otherwise noted.



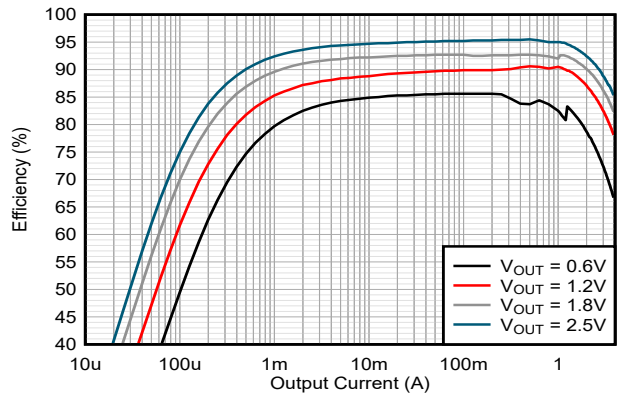

$V_{IN}$ = 3.3V PFM, SIL Package $T_A$ = 25°C

**図 9-2. Efficiency vs Output Current**



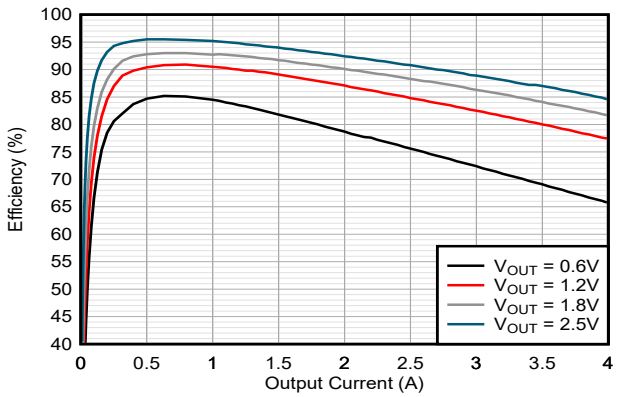

$V_{IN}$ = 3.3V PWM, SIL Package $T_A$ = 25°C

**図 9-3. Efficiency vs Output Current**



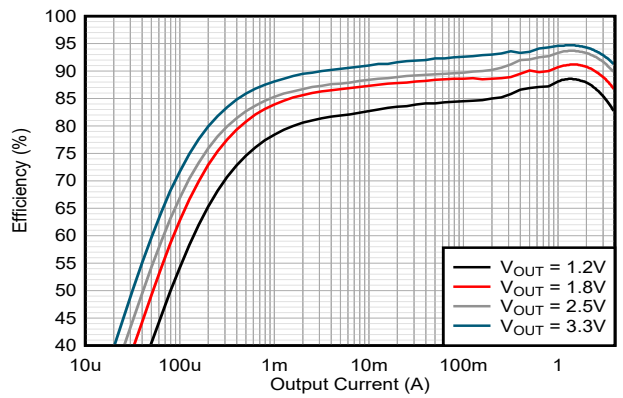

$V_{IN}$ = 3.3V PFM, SIL Package $T_A$ = 85°C

**図 9-4. Efficiency vs Output Current**



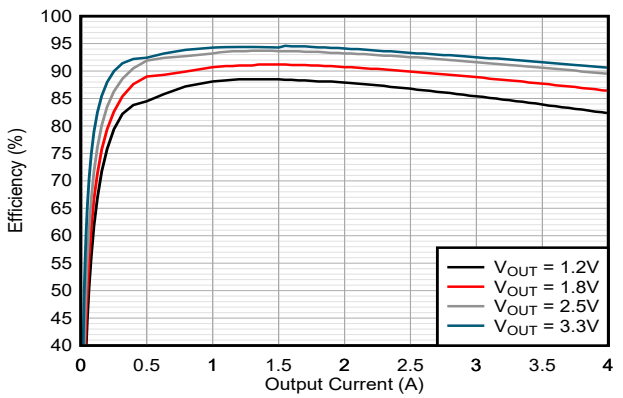

$V_{IN}$ = 3.3V PWM, SIL Package $T_A$ = 85°C

**図 9-5. Efficiency vs Output Current**



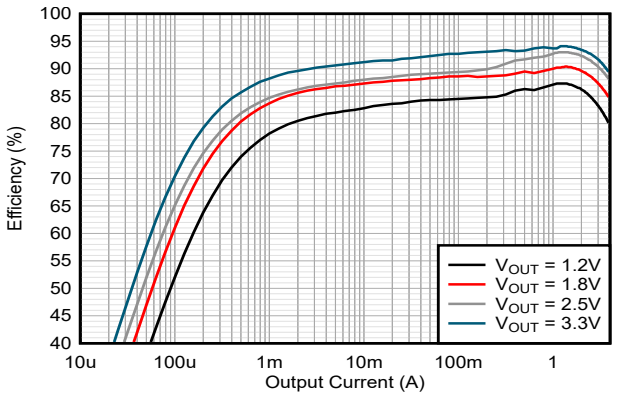

$V_{IN}$ = 5V PFM, SIL Package $T_A$ = 25°C

**図 9-6. Efficiency vs Output Current**



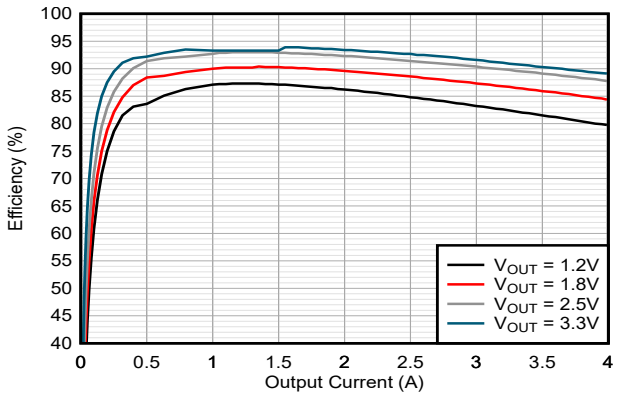

$V_{IN}$ = 5V PWM, SIL Package $T_A$ = 25°C

**図 9-7. Efficiency vs Output Current**



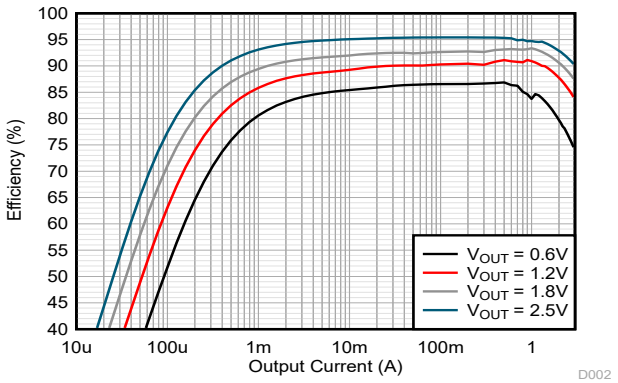

$V_{IN}$ = 5V PFM, SIL Package $T_A$ = 85°C

**図 9-8. Efficiency vs Output Current**



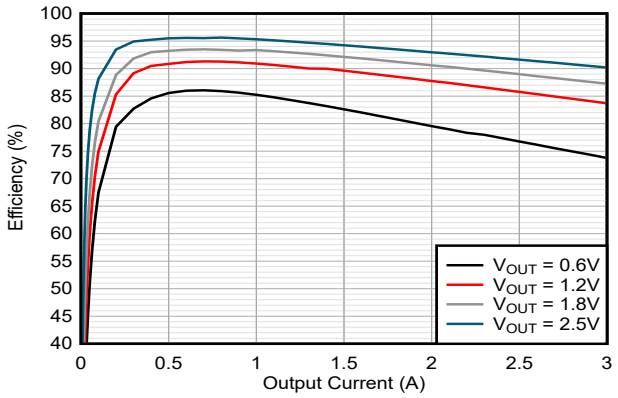

$V_{IN}$ = 5V PWM, SIL Package $T_A$ = 85°C

**図 9-9. Efficiency vs Output Current**



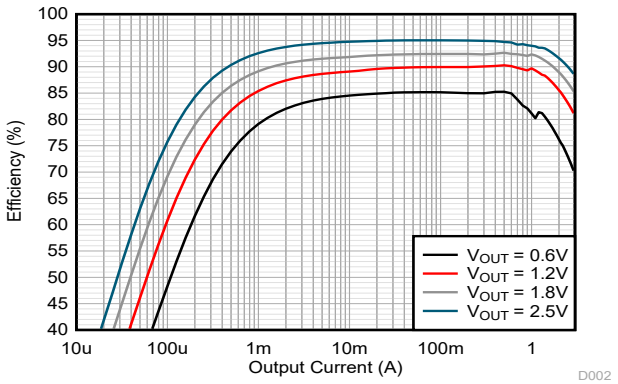

$V_{IN}$ = 3.3V PFM, VCA Package $T_A$ = 25°C

**図 9-10. Efficiency vs Output Current**



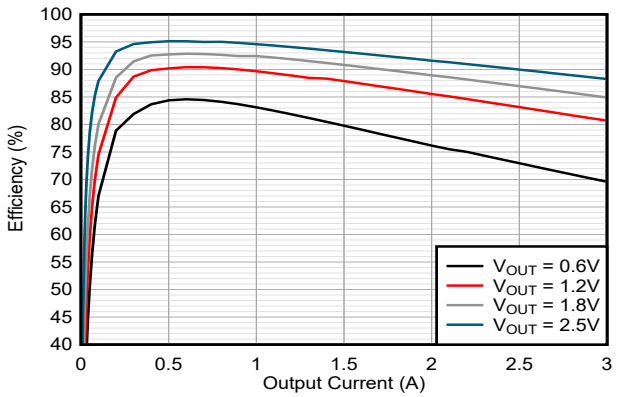

$V_{IN}$ = 3.3V PWM, VCA Package $T_A$ = 25°C

**図 9-11. Efficiency vs Output Current**



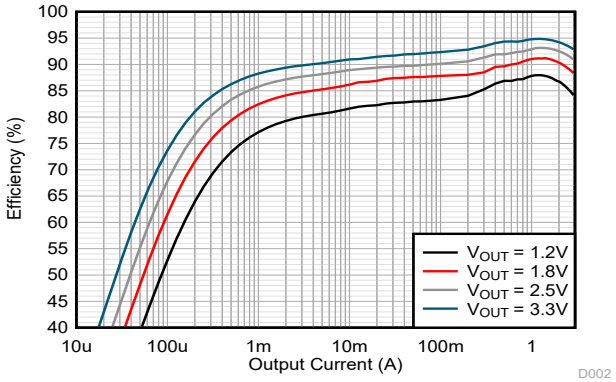

$V_{IN}$ = 3.3V PFM, VCA Package $T_A$ = 85°C

**図 9-12. Efficiency vs Output Current**



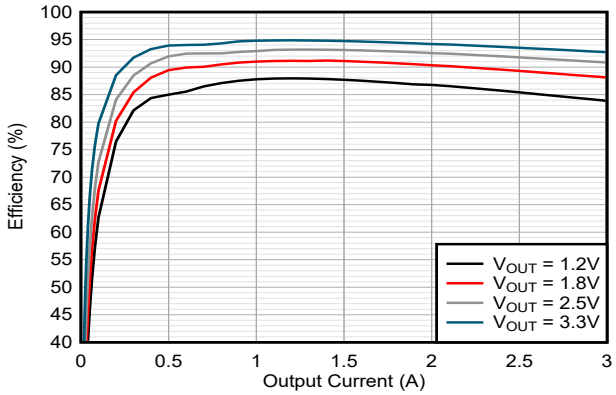

$V_{IN}$ = 3.3V PWM, VCA Package $T_A$ = 85°C

**図 9-13. Efficiency vs Output Current**



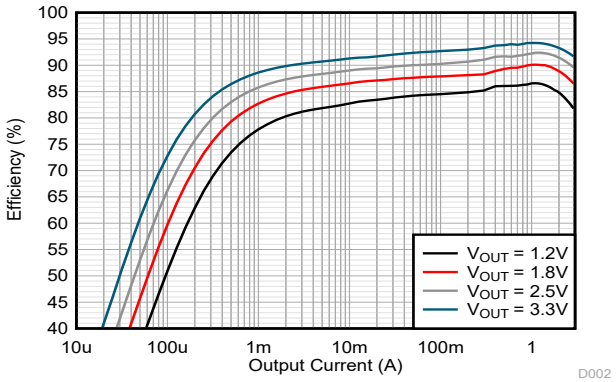

$V_{IN}$ = 5V PFM, VCA $T_A$ = 25°C
Package

**図 9-14. Efficiency vs Output Current**



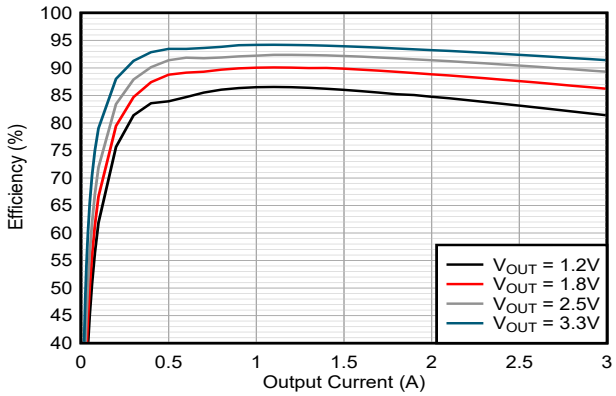

$V_{IN}$ = 5V PWM, VCA $T_A$ = 25°C
Package

**図 9-15. Efficiency vs Output Current**



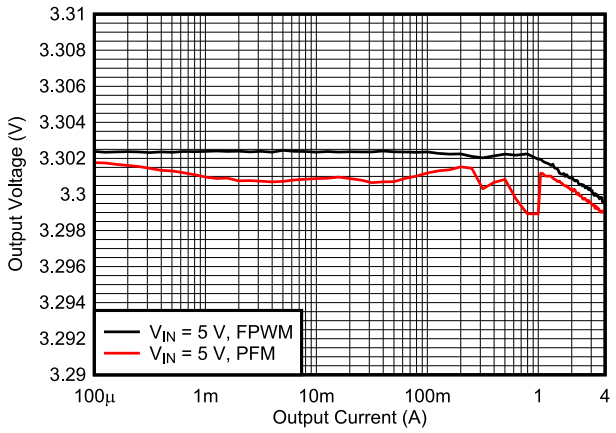

$V_{IN}$ = 5V PFM, VCA $T_A$ = 85°C
Package

**図 9-16. Efficiency vs Output Current**



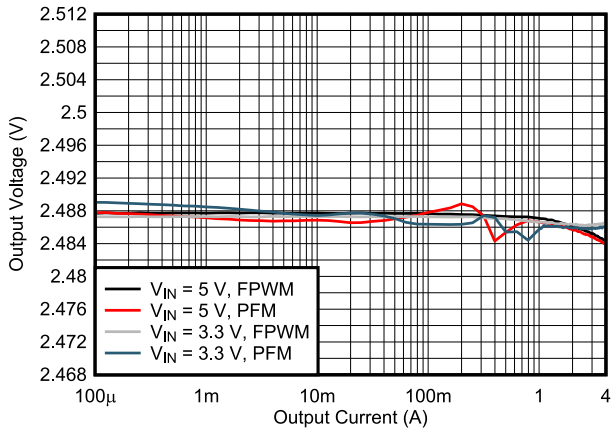

$V_{IN}$ = 5V PWM, VCA $T_A$ = 85°C
Package

**図 9-17. Efficiency vs Output Current**



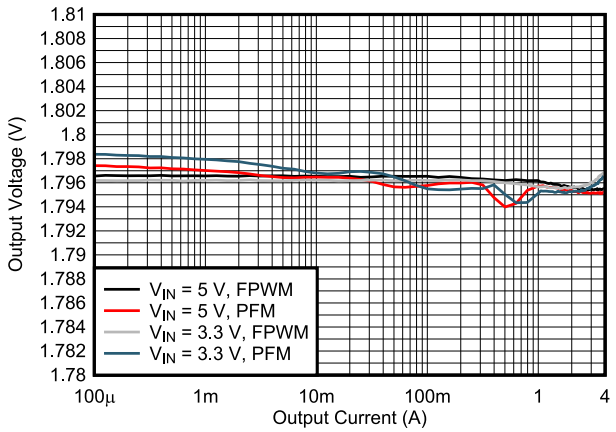

$V_{OUT}$ = 3.3V $T_A$ = 25°C

**図 9-18. Output Voltage vs Output Current**



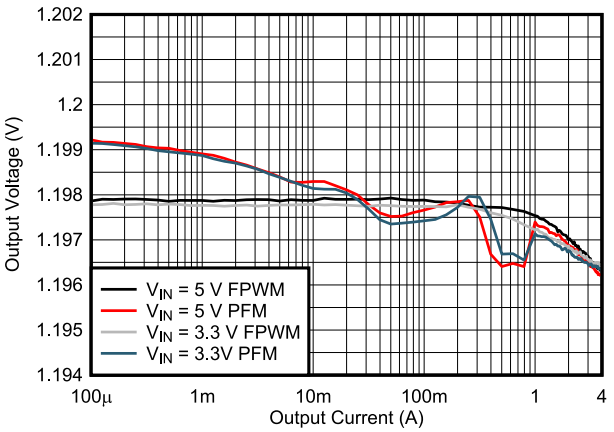

$V_{OUT}$ = 2.5V $T_A$ = 25°C

**図 9-19. Output Voltage vs Output Current**



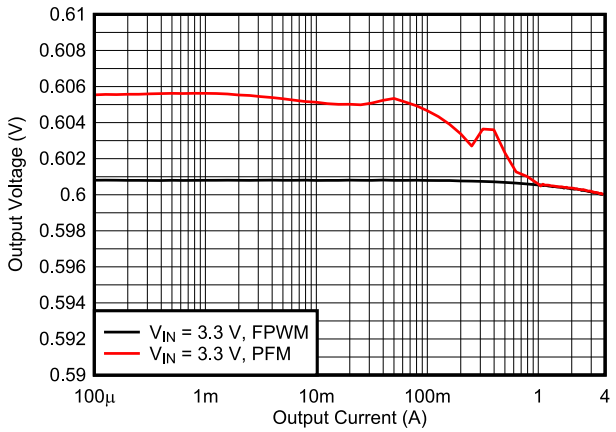

$V_{OUT}$ = 1.8V $T_A$ = 25°C

**図 9-20. Output Voltage vs Output Current**



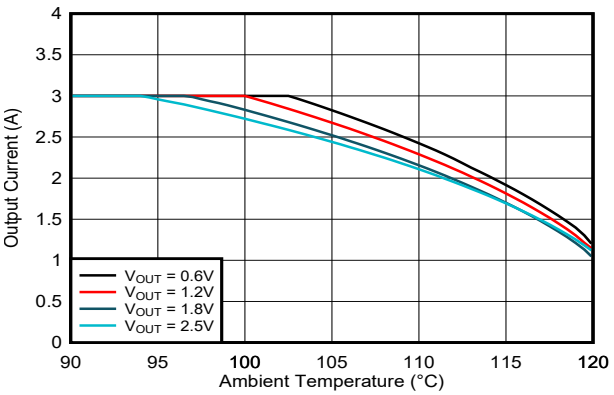

$V_{OUT}$ = 1.2V $T_A$ = 25°C

**図 9-21. Output Voltage vs Output Current**



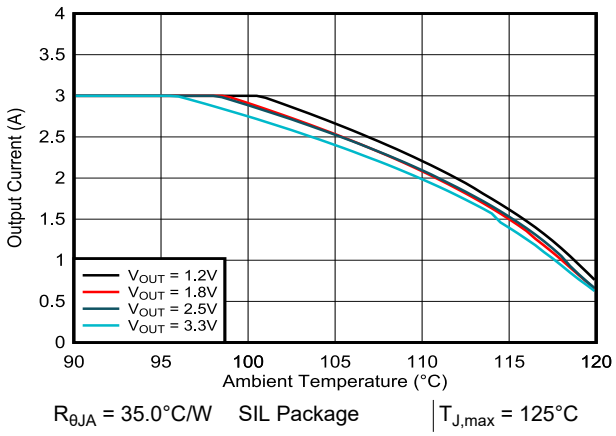

$V_{OUT}$ = 0.6V $T_A$ = 25°C

**図 9-22. Output Voltage vs Output Current**



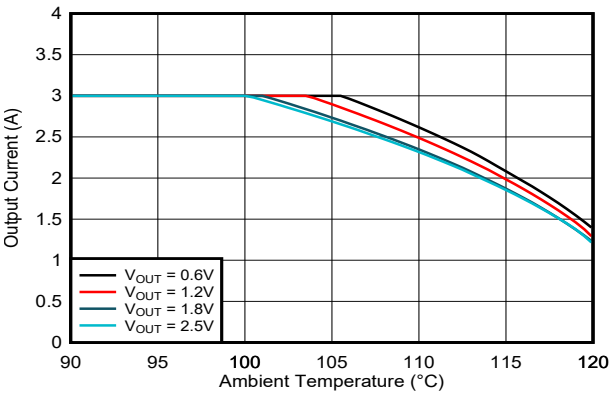

$R_{\theta JA}$ = 35.0°C/W SIL Package $T_{J,max}$ = 125°C

**図 9-23. Safe Operating Area $V_{IN}$ = 3.3V**



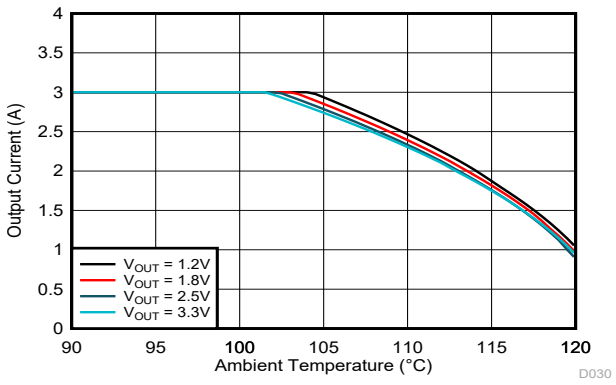

$R_{\theta JA}$ = 35.0°C/W SIL Package $T_{J,max}$ = 125°C

**図 9-24. Safe Operating Area $V_{IN}$ = 5.0V**



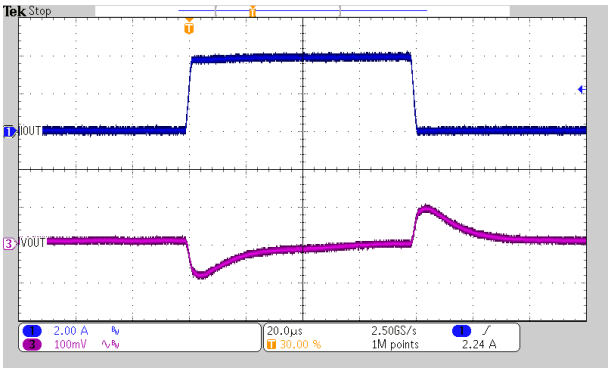

$R_{\theta JA}$ = 27.4°C/W VCA Package $T_{J,max}$ = 125°C

**図 9-25. Safe Operating Area $V_{IN}$ = 3.3V**



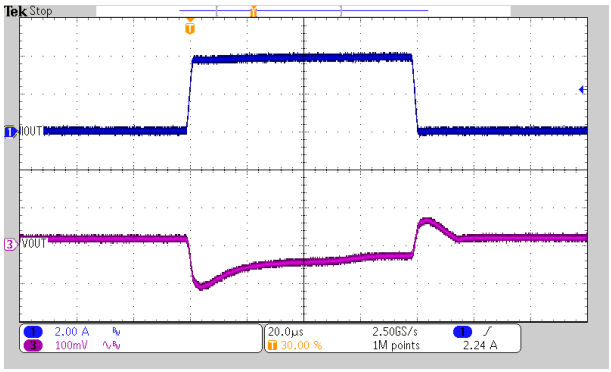

$R_{\theta JA}$ = 27.4°C/W VCA Package | $T_{J,max}$ = 125°C

**図 9-26. Safe Operating Area $V_{IN}$ = 5.0V**



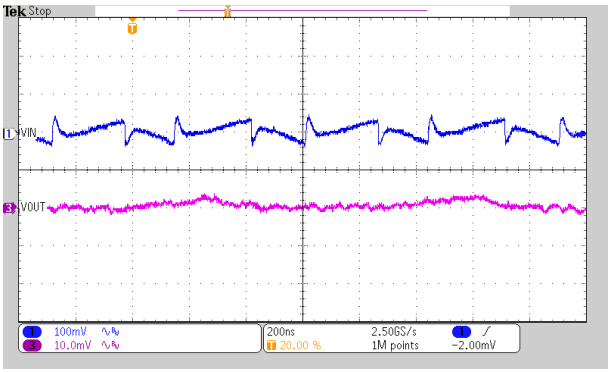

$V_{OUT}$ = 1.8V PWM $T_A$ = 25°C
$V_{IN}$ = 5.0V $I_{OUT}$ = 0A to 4A to 0A

**図 9-27. Load Transient Response**



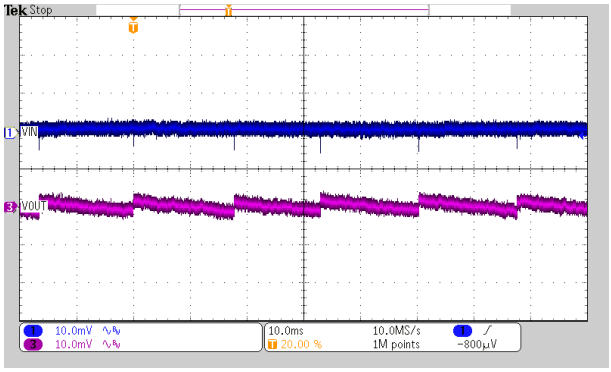

$V_{OUT}$ = 1.8V PFM $T_A$ = 25°C
$V_{IN}$ = 5.0V $I_{OUT}$ = 0A to 4A to 0A

**図 9-28. Load Transient Response**



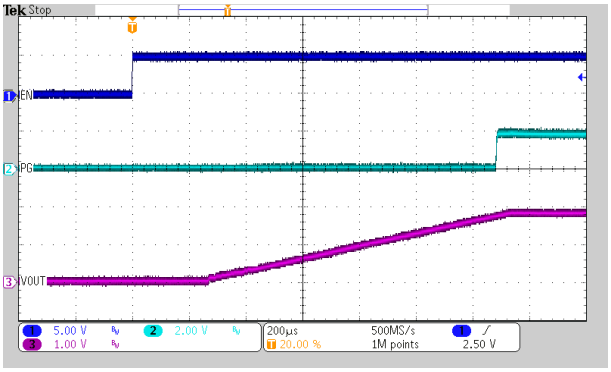

$V_{OUT}$ = 1.8V PWM $T_A$ = 25 °C
$I_{OUT}$ = 4A $V_{IN}$ = 5.0V BW = 20MHz

**図 9-29. Output and Input Voltage Ripple**



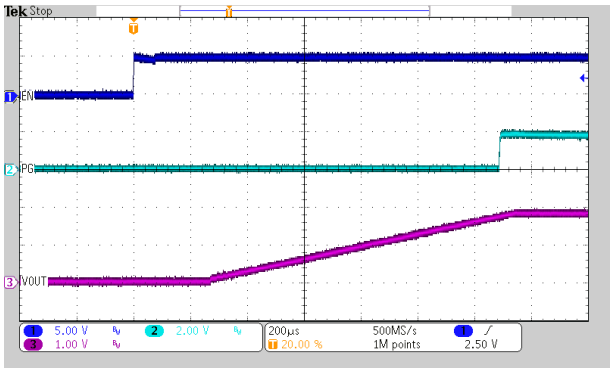

$V_{OUT}$ = 1.8V PFM $T_A$ = 25°C
$I_{OUT}$ = 0A $V_{IN}$ = 5.0V BW = 20MHz

**図 9-30. Output and Input Voltage Ripple**




$V_{OUT}$ = 1.8V PWM $T_A$ = 25°C
$I_{OUT}$ = 4A $V_{IN}$ = 5V $C_{SS}$ = 4.7nF

**図 9-31. Start-Up Timing**




$V_{OUT}$ = 1.8V　　PFM　　$T_A$ = 25°C
$I_{OUT}$ = 0A　　$V_{IN}$ = 5V　　$C_{SS}$ = 4.7nF

**図 9-32. Start-Up Timing**

## 9.3 System Examples

### *9.3.1 Voltage Tracking*

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 図 9-33. From 0V to 0.6V, the internal reference voltage to the internal error amplifier follows the SS/TR pin voltage. When the SS/TR pin voltage is above 0.6V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.6V. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in 図 9-34.

The R2 value must be set properly to achieve accurate voltage tracking by taking the 2.5µA charging current into account. 1kΩ or smaller is a sufficient value for R2. For decreasing SS/TR pin voltage, the device does not sink current from the output when the device is in PFM mode. The resulting decrease of the output voltage can be slower than the SS/TR pin voltage if the load is light.

When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is VIN+0.3V.

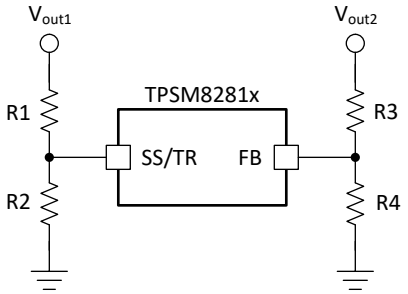



**図 9-33. Schematic for Output Voltage Tracking**

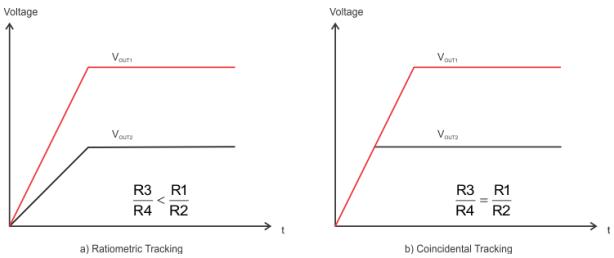



**図 9-34. Output Voltage Tracking**

### 9.3.2 Synchronizing to an External Clock

The TPSM8281x can be synchronized by applying a clock on the MODE/SYNC pin. There is no need for any additional circuitry. See 図 9-35. The clock can be applied, changed, and removed during operation. The value of the $R_{CF}$ resistor is recommended to be chosen such that the internally defined frequency and the externally-applied frequency are close to each other to have a fast settling time to the external clock. Synchronizing to a clock is not possible, if the COMP/FSET pin is connected to Vin or GND. 図 9-36 and 図 9-37 show the external clock being applied and removed. When an external clock is applied, the device operates in PWM mode.

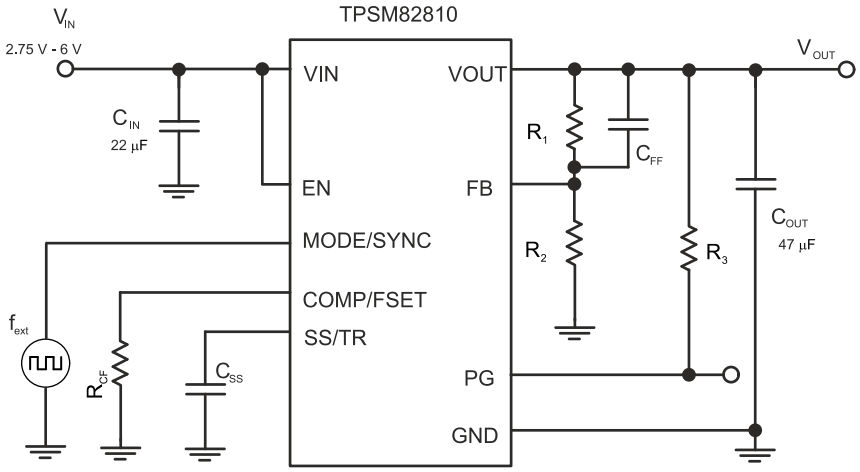
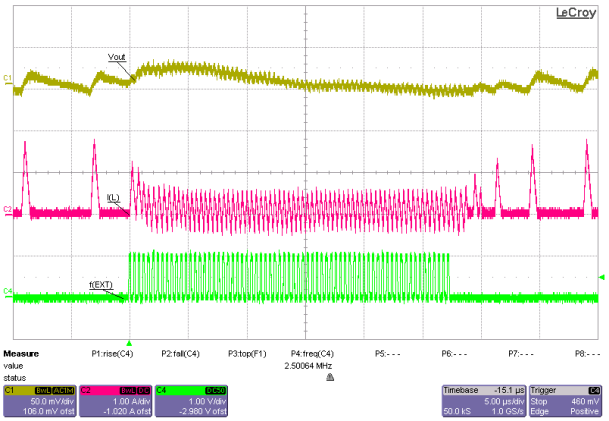
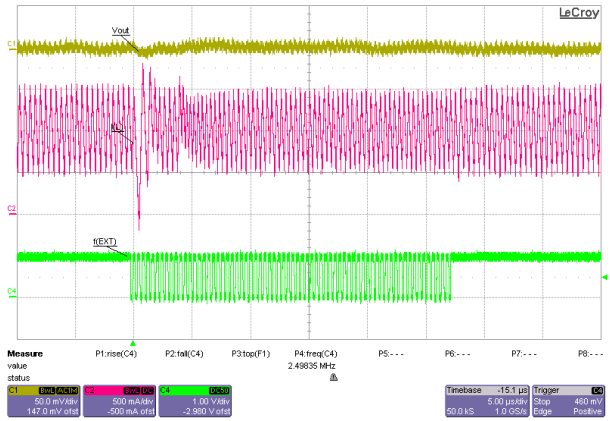



**図 9-35. Frequency Synchronization**




$V_{IN}$ = 5V $R_{CF}$ = 8.06kΩ $I_{OUT}$ = 0.1A
$V_{OUT}$ = 1.8V $f_{EXT}$ = 2.5MHz

**図 9-36. Applying and Removing the Synchronization Signal (PFM)**




$V_{IN}$ = 5V $R_{CF}$ = 8.06kΩ $I_{OUT}$ = 1A
$V_{OUT}$ = 1.8V $f_{EXT}$ = 2.5MHz

**図 9-37. Applying and Removing the Synchronization Signal (FPWM)**

## 9.4 Power Supply Recommendations

The TPSM8281x device family has no special requirements for the input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPSM8281x.

## 9.5 Layout

### 9.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8281x demands careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- The input capacitor must be placed as close as possible to the VIN and GND pins of the device. This is the most critical component placement. Route the input capacitor directly to the VIN and GND pins avoiding vias.
- Place the output capacitor ground close to the VOUT and GND pins and route directly avoiding vias.
- Place the FB resistors, R1 and R2, and the feedforward capacitor $C_{FF}$ close to the FB pin and place $C_{SS}$ close to the SS/TR pin to minimize noise pickup.
- Place the $R_{CF}$ resistor close to the COMP/FSET pin to minimize the parasitic capacitance.
- The recommended layout is implemented on the EVM and shown in the *EVM User's Guide* and in *セクション 9.5.2*.
- The recommended land pattern for the TPSM8281x is shown at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD), when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

### 9.5.2 Layout Examples

The example below shows a cut-out from the layout of the MagPack evaluation module. To further reduce EMI, current loops are kept small and noisy traces kept short.

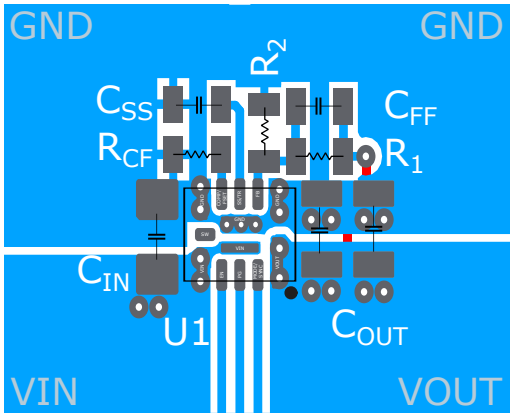



**図 9-38. Example Layout VCA Package**

The same rules also apply to the layout with the SIL package. The pin-outs of both the SIL and the VCA package are optimized for short connections between the device and input or output capacitors. The copper keepout (only for the SIL package) is for top copper layer only. Other PCBs layers can enter this keepout.

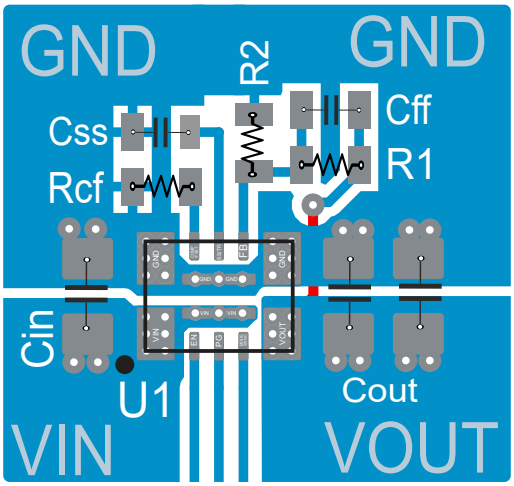



**図 9-39. Example Layout SIL Package**

#### 9.5.2.1 Thermal Consideration

The TPSM8281x module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM8281x, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

The thermal values in *Thermal Information* used the recommended land pattern, shown at the end of this data sheet, including the 18 vias as shown. The TPSM8281x was simulated on a PCB defined by JEDEC 51-7. The 9 vias on the GND pins were connected to copper on other PCB layers, while the remaining 9 vias were not connected to other layers.

# 10 Device and Documentation Support

## 10.1 Device Support

### *10.1.1 サード・パーティ製品に関する免責事項*

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

### *10.1.2 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TPSM8281x device with the WEBENCH® Power Designer.

1. In the part number field start entering the part number if you have a preference and wait until a part list will appear and populate. If there is no preference leave this field blank.
2. In the next section (auto-filled if you started with a part number) enter the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
3. In the "Design Considerations" section select your design priorities.
4. View your design proposal and compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools here: Design and simulation tools.

## 10.2 Documentation Support

### *10.2.1 Related Documentation*

For related documentation see the following:

- Texas Instruments, *TPSM82810EVM-089 Evaluation Module* user's guide
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal
- Texas Instruments, *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold* analog design journal

## 10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 10.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

### 10.5 Trademarks

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### 10.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 10.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision B (July 2024) to Revision C (December 2024)** — **Page**

- 「QFN」を「MicroSiP」に変更してドキュメントのタイトルを更新 ..... 1
- WEBENCH の箇条書き項目のデバイス名を更新、箇条書きの順序を更新、「特長」の EMI コンテキストで「ボンド ワイヤなし」というフレーズを追加 ..... 1
- 「アプリケーション」の壊れているリンクをすべて更新 ..... 1
- TPSM82813、VCA (QFN、13) パッケージから事前情報の注記を削除 ..... 1
- Deleted the Advance Information note from TPSM82813**P**VCAR ..... 2
- Added separate VCA and SIL *Thermal Information* tables into one table and added SIL EVM thermal data ..... 4
- Added transient switch node spec to the *Absolute Maximum Ratings* table and updated table entries to match device family members data sheets ..... 4
- Added BOM table for VCA MagPack package device as different capacitors were used for parameter measurements ..... 8
- Added VCA MagPack package description to the *Overview* ..... 9
- Updated block diagram to match TPSM82816 in *Functional Block Diagram* ..... 9
- Updated equation and calculation example in *COMP/FSET* ..... 10
- Added paragraph about pin and function compatibility between the different members of the device family in *Application Information* ..... 15
- Updated paragraph about WEBENCH tools to match the latest version issued by Texas Instruments in *Custom Design With WEBENCH® Tools* ..... 15
- Added more detail to the feedback divider design procedure in *Setting the Output Voltage* ..... 16
- Added SOA curves for the VCA package and the SIL package to the *Application Curves* ..... 17
- Updated SIL package based layout example to the latest EVM version and added descriptive text to both of the layouts in the *Layout Examples* ..... 24
- Updated paragraph about WEBENCH tools to match the latest version issued by Texas Instruments in *Custom Design With WEBENCH® Tools* ..... 26

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**Changes from Revision A (December 2020) to Revision B (July 2024)** — **Page**

- データシートに TPSM82811 および TPSM82812 を追加 ..... 1
- データシートに VCA パッケージ オプションを追加 ..... 1
- Updated the *ESD Ratings* table to show CDM testing was per JS-002 ..... 4

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## 12 Mechanical, Packaging, and Orderable Information

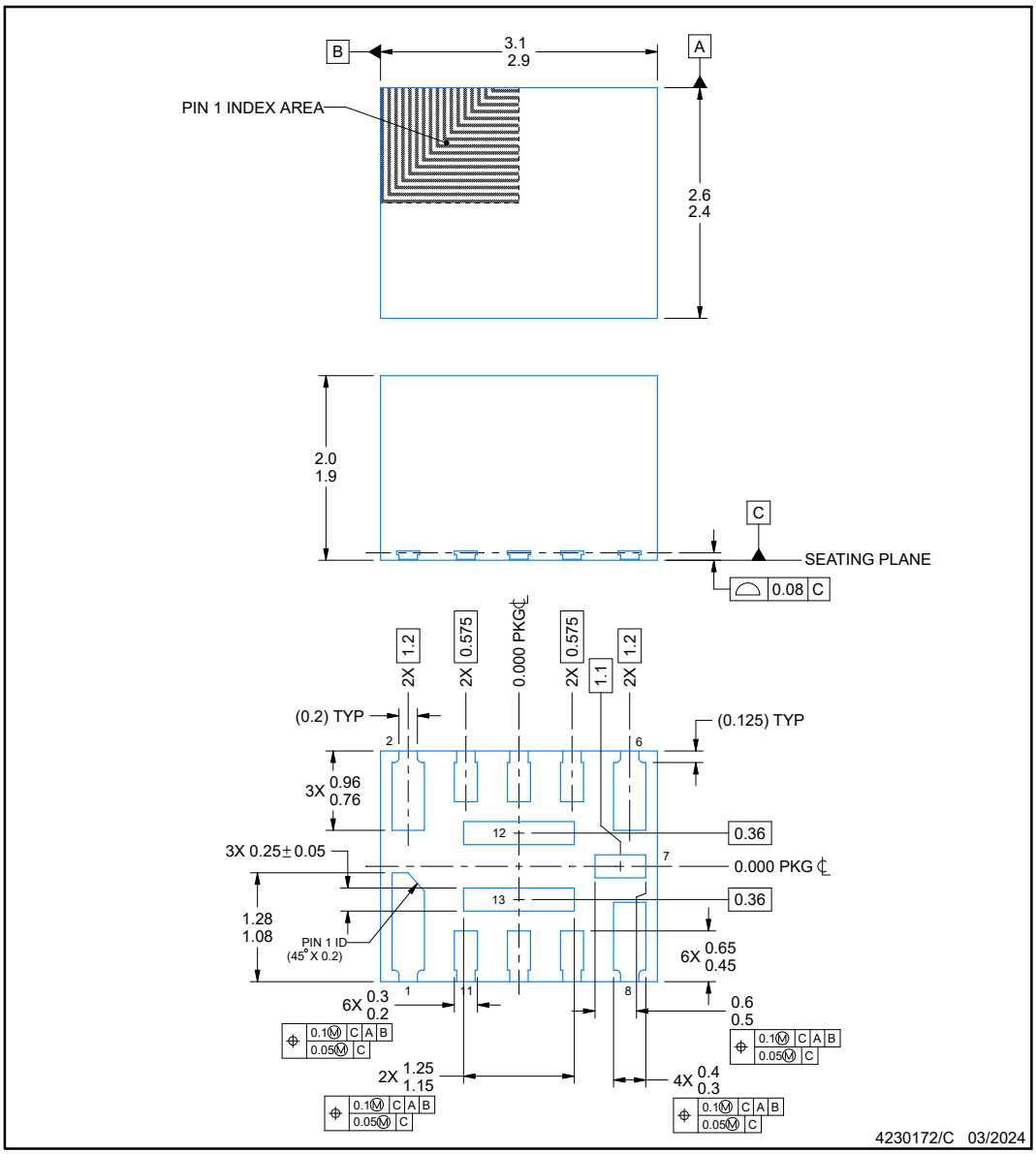
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OUTLINE

## VCA0013A

## QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

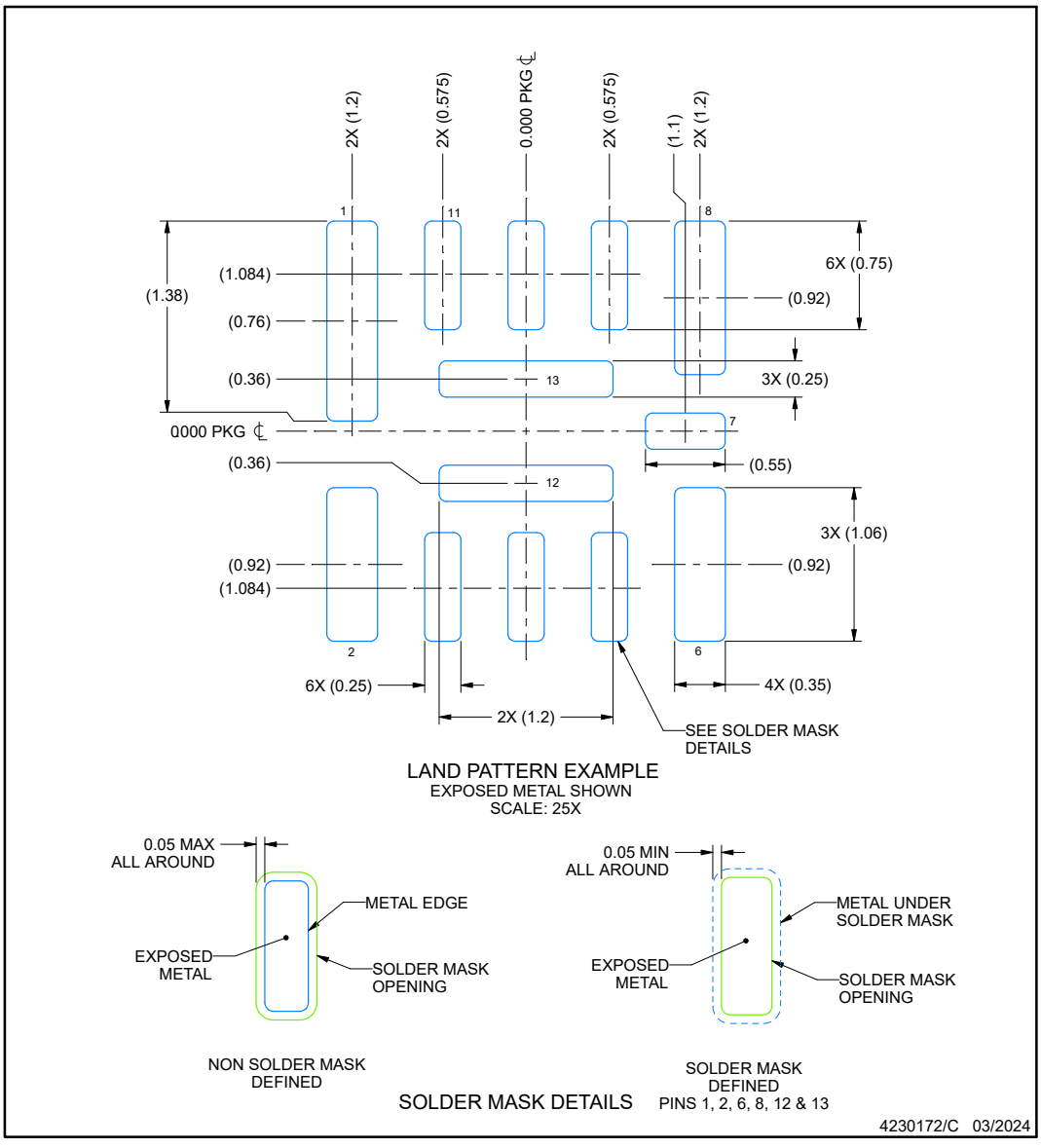
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

## VCA0013A

### QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



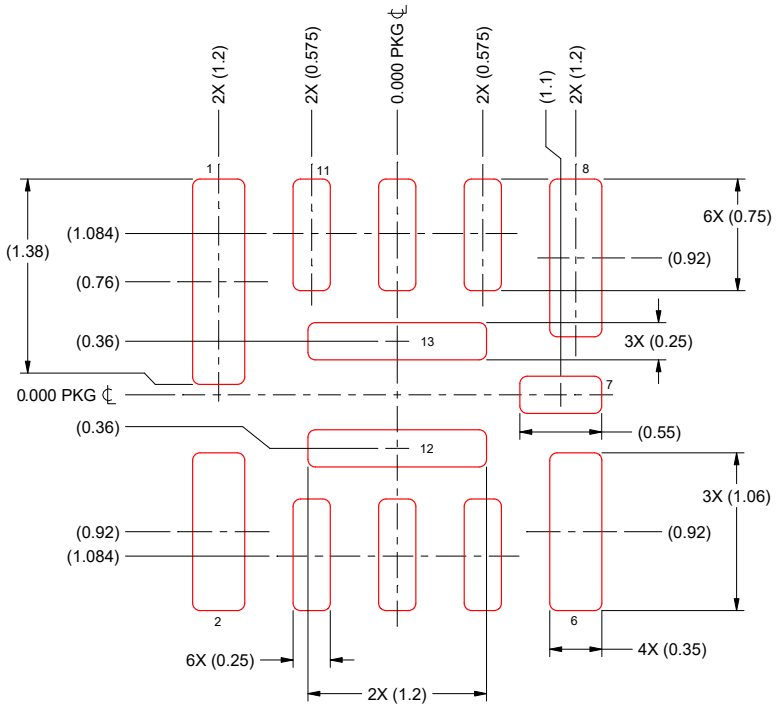

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271)

## EXAMPLE STENCIL DESIGN

**VCA0013A** — **QFN-FCMOD - 2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

4230172/C 03/2024

NOTES: (continued)

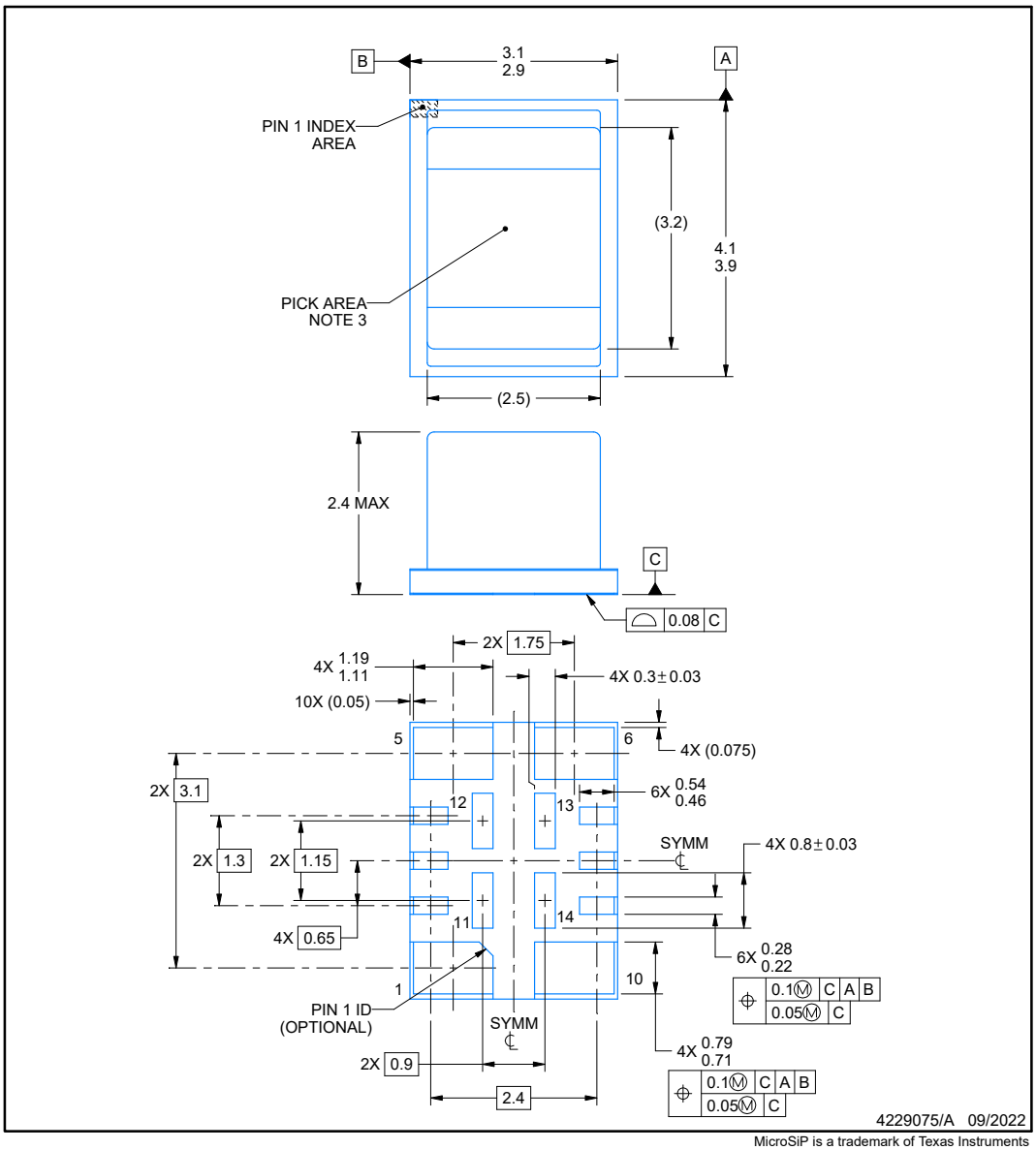
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# PACKAGE OUTLINE

## SIL0014B-C01

### uSIP™ - 2.4 mm max height

MICRO SYSTEM IN PACKAGE




MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

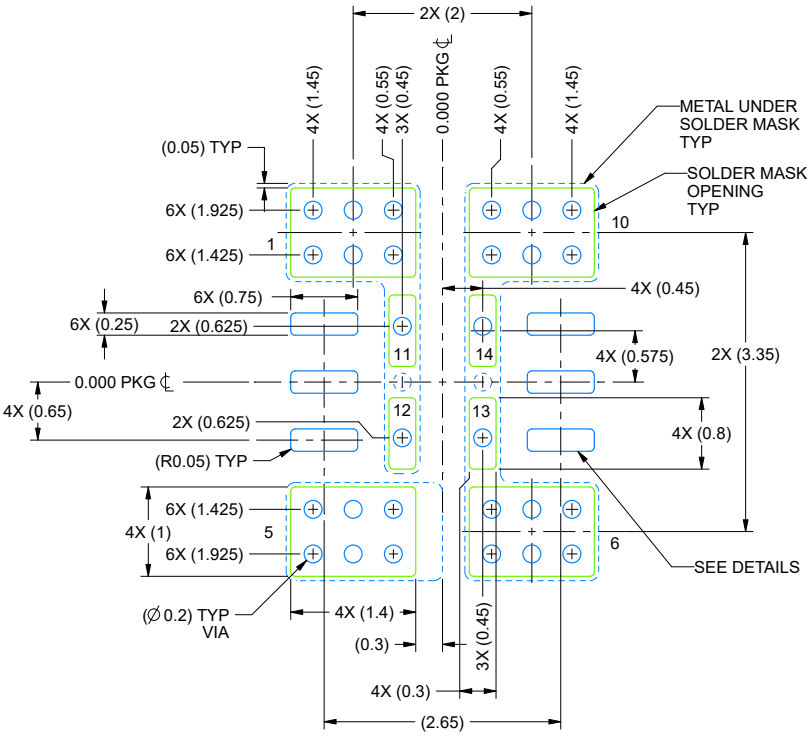
TEXAS INSTRUMENTS
www.ti.com

# EXAMPLE BOARD LAYOUT

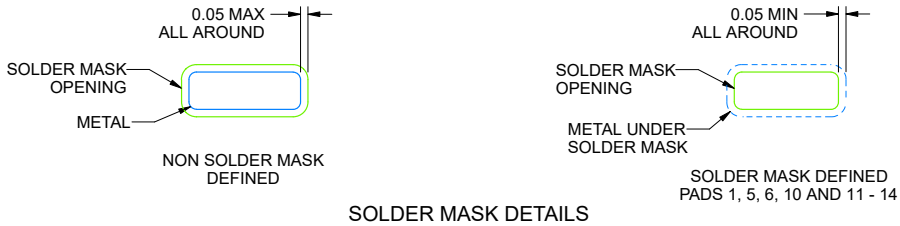
## SIL0014B-C01

**uSIP™ - 2.4 mm max height**

MICRO SYSTEM IN PACKAGE




LAND PATTERN EXAMPLE
SCALE:15X




SOLDER MASK DETAILS
NOT TO SCALE

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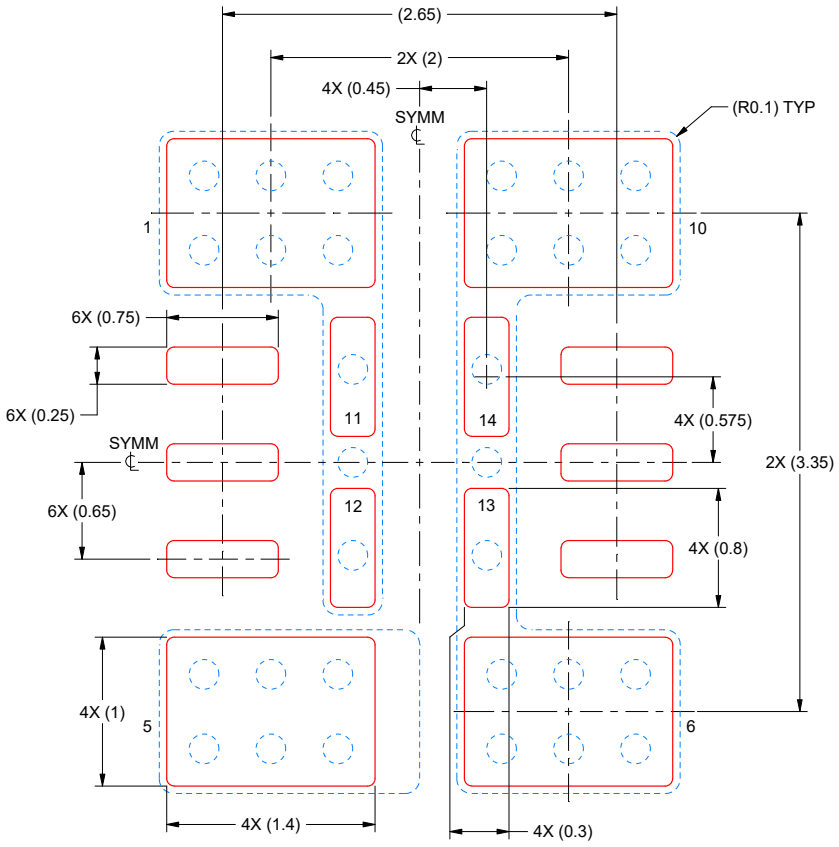
NOTES: (continued)

5. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**SIL0014B-C01** — **uSIP™ - 2.4 mm max height**

MICRO SYSTEM IN PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPSM82810SILR | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | Yes | NIAU | Level-2-260C-1 YEAR | -40 to 125 | FG |
| TPSM82810SILR.A | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | Yes | NIAU | Level-2-260C-1 YEAR | -40 to 125 | FG |
| TPSM82810SILR.B | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| TPSM82810SSILR | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | Yes | NIAU | Level-2-260C-1 YEAR | -40 to 125 | GC |
| TPSM82810SSILR.A | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | Yes | NIAU | Level-2-260C-1 YEAR | -40 to 125 | GC |
| TPSM82810SSILR.B | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| TPSM82813PVCAR | Active | Production | QFN-FCMOD (VCA) \| 13 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 3HAI |
| TPSM82813PVCAR.A | Active | Production | QFN-FCMOD (VCA) \| 13 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 3HAI |
| TPSM82813SILR | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | Yes | NIAU | Level-2-260C-1 YEAR | -40 to 125 | GD |
| TPSM82813SILR.A | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | Yes | NIAU | Level-2-260C-1 YEAR | -40 to 125 | GD |
| TPSM82813SILR.B | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| TPSM82813SSILR | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | Yes | NIAU | Level-2-260C-1 YEAR | -40 to 125 | HF |
| TPSM82813SSILR.A | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | Yes | NIAU | Level-2-260C-1 YEAR | -40 to 125 | HF |
| TPSM82813SSILR.B | Active | Production | uSiP (SIL) \| 14 | 3000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| XPSM82813PVCAR.A | Active | Preproduction | QFN-FCMOD (VCA) \| 13 | 2500 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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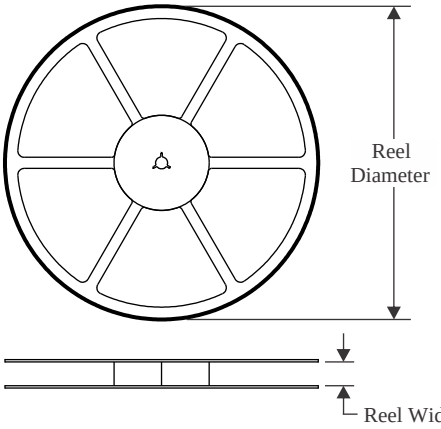
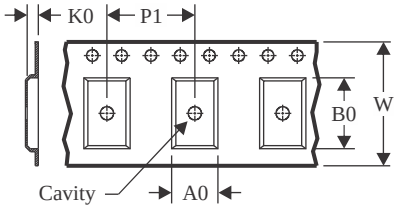
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

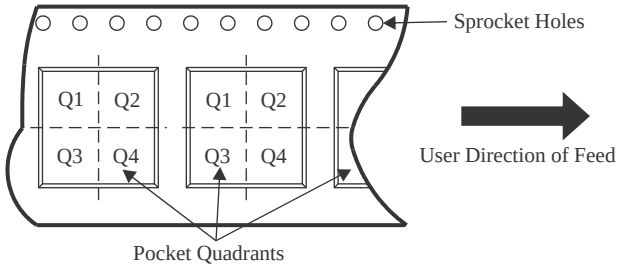



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

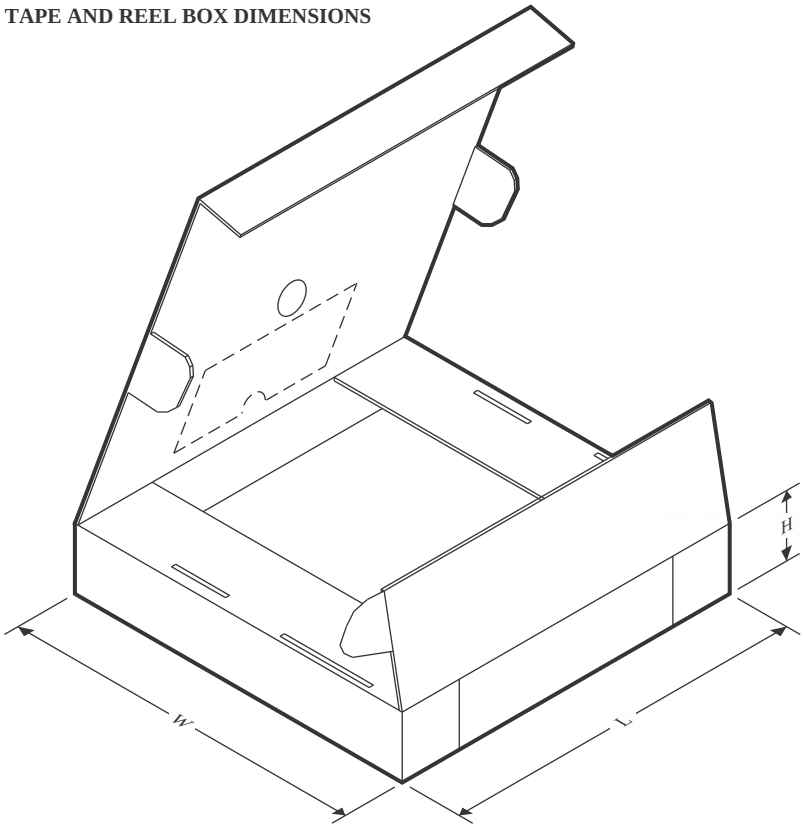
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPSM82810SILR | uSiP | SIL | 14 | 3000 | 178.0 | 13.2 | 3.3 | 4.3 | 2.6 | 8.0 | 12.0 | Q1 |
| TPSM82810SSILR | uSiP | SIL | 14 | 3000 | 178.0 | 13.2 | 3.3 | 4.3 | 2.6 | 8.0 | 12.0 | Q1 |
| TPSM82813PVCAR | QFN-FCMOD | VCA | 13 | 2500 | 330.0 | 12.4 | 3.3 | 2.8 | 2.2 | 8.0 | 12.0 | Q1 |
| TPSM82813SILR | uSiP | SIL | 14 | 3000 | 178.0 | 13.2 | 3.3 | 4.3 | 2.6 | 8.0 | 12.0 | Q1 |
| TPSM82813SSILR | uSiP | SIL | 14 | 3000 | 178.0 | 13.2 | 3.3 | 4.3 | 2.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPSM82810SILR | uSiP | SIL | 14 | 3000 | 383.0 | 353.0 | 58.0 |
| TPSM82810SSILR | uSiP | SIL | 14 | 3000 | 383.0 | 353.0 | 58.0 |
| TPSM82813PVCAR | QFN-FCMOD | VCA | 13 | 2500 | 367.0 | 367.0 | 35.0 |
| TPSM82813SILR | uSiP | SIL | 14 | 3000 | 383.0 | 353.0 | 58.0 |
| TPSM82813SSILR | uSiP | SIL | 14 | 3000 | 383.0 | 353.0 | 58.0 |

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最終更新日：2025 年 10 月