

TPSM82851x 2.7V~6V 入力、0.5A/1A/2A 降圧型電源モジュール、インダクタ内蔵

1 特長

- 入力電圧範囲: 2.7V~6V
- 出力電圧範囲: 0.6V~5.5V
- 0.5A、1A、2A のデバイス・ファミリ
- 静止電流 20 μ A (標準値)
- 帰還電圧精度: $\pm 1\%$ (PWM 動作)
- 2.25MHz のスイッチング周波数 (PWM 動作)
- 1.8MHz~4MHz の外部同期機能
- 強制 PWM または PFM/PWM 動作を選択可能
- 最大 10ms の可変ソフト スタートまたはトラッキング
- 高精度の ENABLE 入力が可能
 - ユーザー定義の低電圧誤動作防止機能
 - 正確なシーケンシング
- 100% デューティ・サイクル・モード
- アクティブ出力放電
- ウィンドウ・コンパレータを使用したパワー・グッド出力
- 40°C~125°C の動作温度範囲
- 2.7mm \times 3.0mm の QFN パッケージ、0.5mm ピッチ

2 アプリケーション

- ファクトリ・オートメーションおよび制御
- 信号測定、信号源生成、計測機器
- メディカル・モニタと診断
- ワイヤレス・インフラ
- 堅牢化された通信: センサ、画像処理、レーダー

3 概要

TPSM82851x はピン互換で 0.5A、1A、2A の高効率で使いやすい、インダクタ内蔵の同期整流降圧型 DC/DC パワー モジュールのファミリです。これらのデバイスは固定周波数のピーク電流モード制御トポロジに基づいており、高い電力密度と使いやすさが要件である、電気通信、テストと測定、医療用アプリケーションに使用できます。抵抗値の低いスイッチにより、高い周囲温度でも最大 2A の連続出力電流を供給できます。スイッチング周波数は内部で 2.25MHz に固定されており、1.8MHz から 4MHz までの範囲の外部クロックに同期することもできます。PFM/PWM モードでは、TPSM82851x は負荷が軽いとき自動的にパワーセーブ モードへ移行するため、負荷範囲全体にわたって高い効率が維持されます。TPSM82851x は PWM モードで 1% の帰還電圧精度を実現するため、出力電圧精度の高い電源の設計に役立ちます。SS/TR ピンを使用して、スタートアップ時間を設定したり、出力電圧が外部ソースに追従するよう設定したりできます。この特長によって、各種の電源レールの外部シーケンシングが可能で、スタートアップ時の突入電流が制限されます。

製品情報

部品番号 (2)	出力電流	パッケージ (1)	本体サイズ (公称)
TPSM828510	0.5A	RDY (QFN, 9)	2.7mm \times 3.0mm \times 2.0mm
TPSM828511	1A		
TPSM828512	2A		

- (1) 詳細については、[セクション 12](#) を参照してください。
 (2) [製品比較表](#) を参照してください。

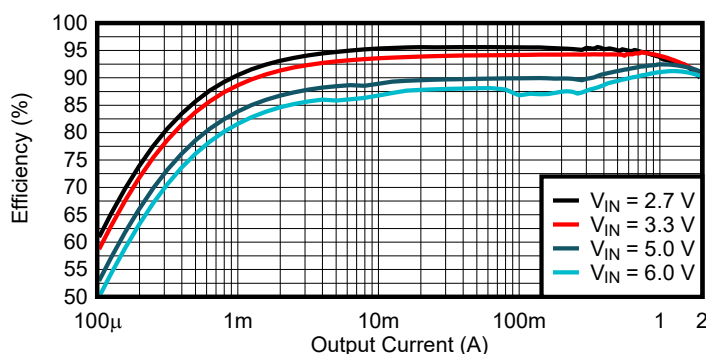
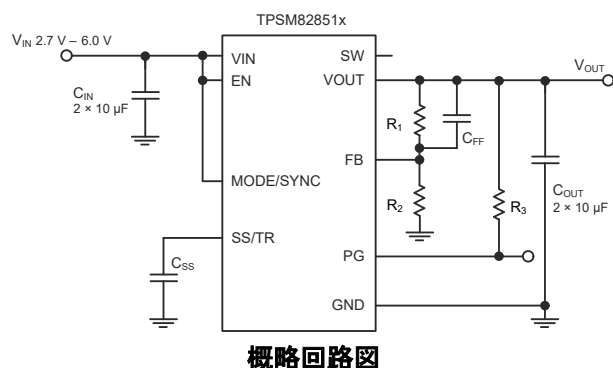


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4 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	OUTPUT VOLTAGE	TYPICAL INPUT CAPACITOR	TYPICAL OUTPUT CAPACITOR
TPSM828510RDY	0.5 A	Adjustable	$2 \times 4.7 \mu\text{F}$	$2 \times 10 \mu\text{F}$
TPSM828511RDY	1 A			
TPSM828512RDY	2 A			

5 Pin Configuration and Functions

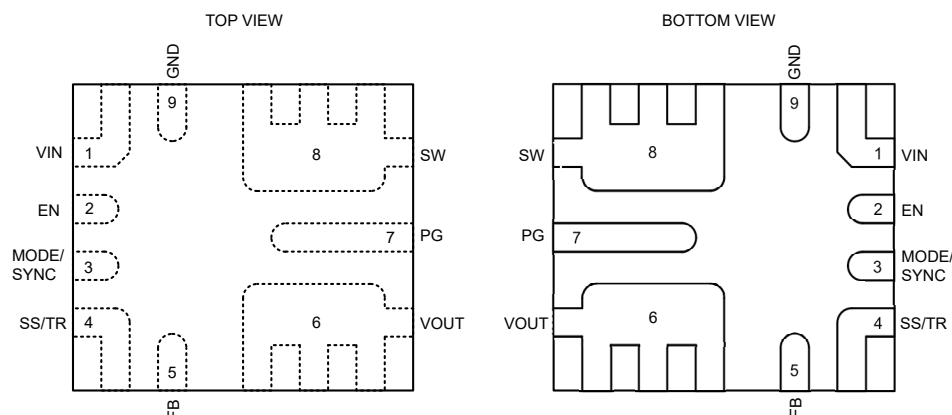


図 5-1. 9-Pin RDY QFN Package

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Power supply input. Connect the input capacitor as close as possible between the VIN and GND pins.
GND	9	PWR	Ground pin
SW	8	O	This pin is the switch pin of the converter. This pin is connected to the internal power MOSFET and the inductor. Avoid connecting this pin to larger traces as this can increase EMI. This pin can stay unconnected or be soldered to a small pad for thermal improvement.
PG	7	O	Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used. A pullup resistor can be connected to any voltage not larger than VIN.
VOUT	6	PWR	Output voltage pin. This pin is internally connected to the integrated inductor.
FB	5	I	Voltage feedback input. Connect the output voltage resistor divider to this pin.
SS/TR	4	I	Soft-start, tracking pin. A capacitor connected from this pin to GND defines the output voltage rise time. The pin can also be used as an input for tracking and sequencing - see Voltage Tracking .
MODE/SYNC	3	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The MODE/SYNC pin can also be used to synchronize the device to an external frequency. See Synchronizing to an External Clock .
EN	2	I	This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.

(1) I = input, O = output, N/A = not applicable

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Pin voltage ⁽²⁾	VIN	−0.3	6.5	V
	SW (DC)	−0.3	V _{IN} + 0.3	V
	SW (AC, less than 10ns) ⁽³⁾	−3	10	V
	SS/TR, PG	−0.3	V _{IN} + 0.3	V
	EN, MODE/SYNC, FB	−0.3	6.5	V
T _{stg}	Storage temperature	−65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the network ground terminal
- (3) While switching

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±750	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage range	2.7		6	V
V _{OUT}	Output voltage range	0.6		5.5	V
C _{OUT}	Effective output capacitance ⁽¹⁾	8	10	200	μF
C _{IN}	Effective input capacitance ⁽¹⁾	5	10		μF
I _{SINK_PG}	Sink current at PG pin	0		2	mA
T _J	Junction temperature	−40		125	°C

- (1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer's DC bias curves for the effective capacitance vs DC voltage applied.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPSM82851x	TPSM82851x	UNIT
		RDY (JEDEC) ⁽²⁾	RDY (EVM)	
		9 PINS	9 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	62.7	46.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	65.5	n/a	°C/W
R _{θJB}	Junction-to-board thermal resistance	18.5	n/a	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.4	1.0	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	18.3	20.8	°C/W

6.4 Thermal Information (続き)

THERMAL METRIC ⁽¹⁾		TPSM82851x	TPSM82851x	UNIT
		RDY (JEDEC) ⁽²⁾	RDY (EVM)	
		9 PINS	9 PINS	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) JEDEC standard PCB with 4 layers, no thermal vias

6.5 Electrical Characteristics

Over operating junction temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$) and $V_{IN} = 2.7\text{ V}$ to 6 V . Typical values at $V_{IN} = 5\text{ V}$ and $T_J = 25^{\circ}\text{C}$. (unless otherwise noted)

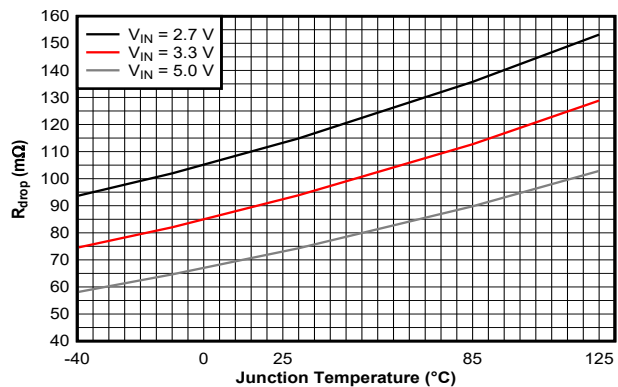
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I _Q	Quiescent current	EN = V _{IN} , no load, device not switching, MODE = GND, V _{OUT} = 0.6 V		20	32	μA
I _{SD}	Shutdown current	EN = GND, typical value at T _J = 25°C, maximum value at T _J = 125°C		1.5	18	μA
V _{UVLO}	Undervoltage lock out threshold	V _{IN} rising	2.45	2.6	2.7	V
		V _{IN} falling	2.1	2.5	2.6	V
T _{JSD}	Thermal shutdown threshold	T _J rising		170		°C
	Thermal shutdown hysteresis	T _J falling		15		°C
CONTROL and INTERFACE						
V _{EN,IH}	Input threshold voltage at EN, rising edge		1.05	1.1	1.15	V
V _{EN,IL}	Input threshold voltage at EN, falling edge		0.96	1.0	1.05	V
V _{IH}	High-level input-threshold voltage at MODE/SYNC		1.1			V
I _{EN,LKG}	Input leakage current into EN	V _{IH} = V _{IN} or V _{IL} = GND			125	nA
V _{IL}	Low-level input-threshold voltage at MODE/SYNC				0.3	V
I _{LKG}	Input leakage current into MODE/SYNC				100	nA
t _{Delay}	Enable delay time	Time from EN high to device starts switching; V _{IN} applied already	85	150	470	μs
t _{Ramp}	Output voltage ramp time, C _{SS} = 4.7 nF	Time from device starts switching to power good; device not in current limit	0.8	1.3	1.8	ms
t _{Ramp}	Output voltage ramp time, SS/TR pin open	Time from device starts switching to power good; device not in current limit	90	150	210	μs
I _{SS/TR}	SS/TR source current		2	2.5	2.8	uA
	Tracking gain	V _{FB} / V _{SS/TR}		1		
	Tracking offset	V _{FB} when V _{SS/TR} = 0 V		±1		mV
f _{SYNC}	Frequency range on MODE/SYNC pin for synchronization		1.8		4	MHz
	Duty cycle of synchronization signal at MODE/SYNC		20		80	%
	Time to lock to external frequency			50		μs
V _{TH_PG}	UVP power good threshold voltage; DC level	rising (%V _{FB})	92	95	98	%
V _{TH_PG}	UVP power good threshold voltage; DC level	falling (%V _{FB})	87	90	93	%

6.5 Electrical Characteristics (続き)

Over operating junction temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$) and $V_{IN} = 2.7\text{ V}$ to 6 V . Typical values at $V_{IN} = 5\text{ V}$ and $T_J = 25^{\circ}\text{C}$. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH_PG}	OVP power good threshold voltage; DC level	rising ($\%V_{FB}$)	107	110	113	%
	OVP power good threshold voltage; DC level	falling ($\%V_{FB}$)	104	107	111	%
V_{PG_OL}	Low-level output voltage at PG	$I_{SINK_PG} = 2\text{ mA}$		0.07	0.3	V
I_{PG_LKG}	Input leakage current into PG	$V_{PG} = 5\text{ V}$			100	nA
t_{PG}	PG deglitch time	for a high level to low level transition on the power good output		40		μs
OUTPUT						
V_{FB}	Feedback voltage, adjustable version			0.6		V
I_{FB_LKG}	Input leakage current into FB, adjustable version	$V_{FB} = 0.6\text{ V}$		1	70	nA
V_{FB}	Feedback voltage accuracy	PWM, $V_{IN} \geq V_{OUT} + 1\text{ V}$	-1		1	%
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT} + 1\text{ V}$, $V_{OUT} \geq 1.0\text{ V}$, $C_{o,eff} \geq 10\text{ }\mu\text{F}$	-1		2	%
V_{FB}	Feedback voltage accuracy	PFM, $V_{IN} \geq V_{OUT} + 1\text{ V}$, $V_{OUT} < 1.0\text{ V}$, $C_{o,eff} \geq 15\text{ }\mu\text{F}$	-1		3	%
V_{FB}	Feedback voltage accuracy with voltage tracking	$V_{IN} \geq V_{OUT} + 1\text{ V}$, $V_{SS/TR} = 0.3\text{ V}$	-4		4	%
	Load regulation	PWM		0.05		%/A
	Line regulation	PWM, $I_{OUT} = 1\text{ A}$, $V_{IN} \geq V_{OUT} + 1\text{ V}$		0.02		%/V
R_{DIS}	Output discharge resistance				100	Ω
f_{SW}	PWM Switching frequency		2.025	2.25	2.475	MHz
$t_{on,min}$	Minimum on-time of high-side FET	$V_{IN} = 3.3\text{ V}$, $T_J = -40^{\circ}\text{C}$ to 125°C		35	52	ns
$t_{on,min}$	Minimum on-time of low-side FET			10		ns
R_{DP}	Dropout resistance	$V_{IN} \geq 5\text{ V}$		85	120	m Ω
I_{LIMH}	High-side FET switch current limit	DC value, for TPSM828512; $V_{IN} = 3\text{ V}$ to 6 V	2.85	3.4	3.9	A
I_{LIMH}	High-side FET switch current limit	DC value, for TPSM828511; $V_{IN} = 3\text{ V}$ to 6 V	2.1	2.6	3.0	A
I_{LIMH}	High-side FET switch current limit	DC value, for TPSM828510; $V_{IN} = 3\text{ V}$ to 6 V	1.6	2.1	2.5	A
I_{LIMNEG}	Low-side FET negative current limit	DC value		-1.8		A

6.6 Typical Characteristics



6-1. Dropout Resistance

7 Parameter Measurement Information

7.1 Schematic

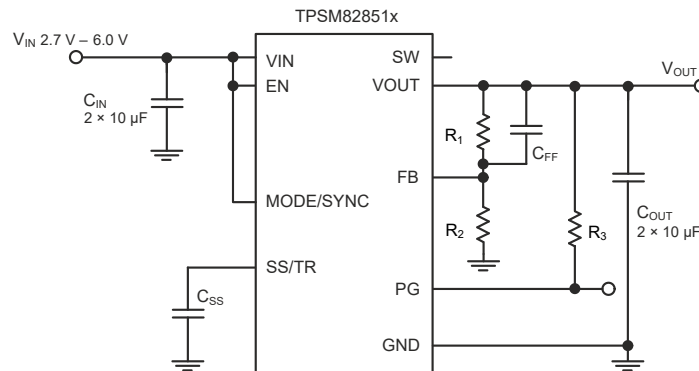


図 7-1. Measurement Setup for TPSM82851x

表 7-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER ⁽¹⁾
IC	TPSM828510 / TPSM828511 / TPSM828512	Texas Instruments
C _{IN}	2 × 10 μF / 6.3 V / GRM188D70J106MA73	Murata
C _{OUT}	2 × 10 μF / 6.3 V / GRM188D70J106MA73	Murata
C _{SS}	4.7 nF (equal to 1-ms start-up ramp); GCM188R72A472KA37	Any
C _{FF}	10 pF	Any
R ₁	Depending on V _{OUT}	Any
R ₂	Depending on V _{OUT}	Any
R ₃	100 kΩ	Any

(1) See the [Third-party Products Disclaimer](#).

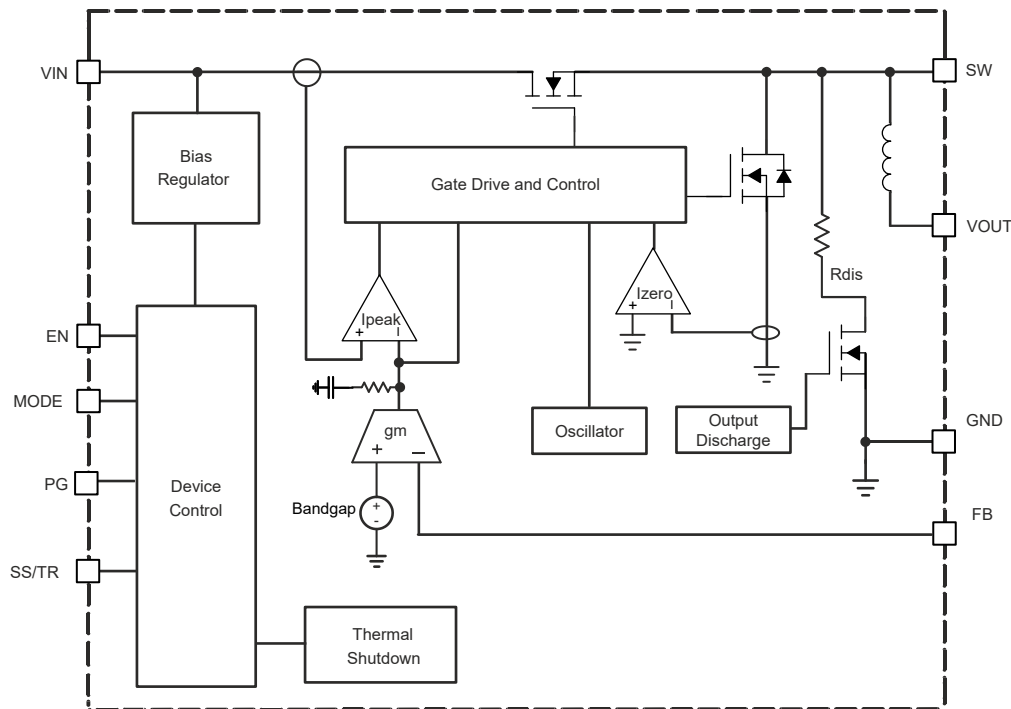
8 Detailed Description

8.1 Overview

The TPSM82851x synchronous, switch mode, DC/DC converter power modules are based on a fixed-frequency peak current-mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with the TPSM82851x. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors.

The devices support fixed-frequency forced PWM operation with the MODE/SYNC pin tied to a logic high level. When the MODE/SYNC pin is set to a logic low level, the device operates in power save mode (PFM) at low-output currents and automatically transitions to fixed-frequency PWM mode at higher output currents. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output currents. The device can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz applied to the MODE/SYNC pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Precise Enable (EN)

The voltage applied at the enable pin of the TPSM82851x is compared to a fixed threshold of 1.1 V for a rising voltage. This comparison allows you to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPSM82851x starts operation when the rising threshold is exceeded. For proper operation, terminate and do not leave the enable (EN) pin floating. Pulling the enable pin low forces the device into shutdown, with a shutdown current of typically 1 μ A. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire

internal control circuitry is switched off. See the [Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold analog design journal](#) for more details.

8.3.2 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin forces PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. When an external clock is applied, the device operates in PWM mode. As with the switching frequency selection, the specification for the minimum on-time has to be observed when applying the external clock signal. The synchronization to the external clock is done on the falling edge of the applied clock to the rising edge of the internal SW pin. The MODE/SYNC pin can be changed during operation.

8.3.3 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the MOSFETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage goes below the falling threshold.

8.3.4 Power-Good Output (PG)

Power good is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. Power good is driven by a window comparator. PG is held low when the device is

- disabled,
- in undervoltage lockout,
- in thermal shutdown,
- or in soft start.

When the output voltage is in regulation hence, within the window defined in the electrical characteristics, the PG output is high impedance. V_{IN} must remain present for the PG pin to stay low. If the power-good output is not used, TI recommends to tie to GND or leave open. The PG indicator features a de-glitch, as specified in the electrical characteristics, for the transition from "high impedance" to "low" of the output.

表 8-1. Power-Good Pin Logic

EN	DEVICE STATUS	PG LOGIC STATUS
X	$V_{IN} < 2\text{ V}$	Undefined
Low	$V_{IN} \geq 2\text{ V}$	Low
High	$2\text{ V} \leq V_{IN} < V_{UVLO}$ OR in thermal shutdown OR V_{OUT} not in regulation OR device in soft start	Low
High	V_{OUT} in regulation	High impedance

8.3.5 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During PFM, the thermal shutdown is not active.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPSM82851x has two operating modes: Forced PWM mode and PFM/PWM mode.

With the MODE/SYNC pin set to high, the TPSM82851x operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is 2.25 MHz or defined by an external clock signal applied to the MODE/SYNC pin. With an external clock applied to MODE/SYNC, the TPSM82851x follow the frequency applied to the pin. In general, the frequency range in forced PWM mode is 1.8 MHz to 4 MHz. However, the frequency must be in a range the TPSM82851x can operate at, taking the minimum on-time into account.

8.4.2 Power Save Mode Operation (PFM/PWM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 0.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. In power save mode, the switching frequency decreases with the load current maintaining high efficiency.

8.4.3 100% Duty-Cycle Operation

The duty cycle of a buck converter operated in PWM mode is given as $D = V_{OUT} / V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage and the off-time gets smaller. When the minimum off-time of typically 10 ns is reached, the TPSM82851x skips switching cycles while approaching 100% mode. In 100% mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the target. This feature is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT(min)} \times R_{DP} \quad (1)$$

where

- R_{DP} is the resistance from V_{IN} to V_{OUT} , which includes the high-side MOSFET on-resistance and DC resistance of the inductor.
- $V_{OUT(min)}$ is the minimum output voltage the load can accept.

8.4.4 Current Limit and Short-Circuit Protection

The TPSM82851x is protected against overload and short-circuit events. If the inductor current exceeds the current limit I_{LIMH} , the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. Due to internal propagation delays, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \quad (2)$$

where

- I_{LIMH} is the static current limit, as specified in the electrical characteristics
- L is the effective inductance of the internal inductor (typical 0.47 μ H)
- V_L is the voltage across the inductor ($V_{IN} - V_{OUT}$)
- t_{PD} is the internal propagation delay of typically 50 ns

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \times 50ns \quad (3)$$

8.4.5 Output Discharge

The purpose of the discharge function is to make sure a defined down-ramp of the output voltage when the device is disabled and keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after the TPSM82851x has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 2 V. Output discharge is not activated during a current limit event.

8.4.6 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This control avoids excessive inrush current and makes sure a controlled output voltage rise time. This control also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200 μ s, then the internal reference and hence V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin.

The SS/TR pin must not be connected to the SS/TR pin of other devices. TI recommends to keep C_{SS} at less than or equal to 47 nF. Larger capacitance can not fully discharge to zero during start-up. In this case the device starts the output voltage ramp at a value above zero Volt, leading to a short time period of increased device inrush current.

Leaving the SS/TR pin not connected provides the fastest start-up ramp with 160 μ s typically. A capacitor connected from SS/TR to GND is charged with 2.5 μ A by an internal current source during soft start. After the voltage on SS/TR exceeds 0.6 V the internal reference voltage of 0.6 V takes over control. The capacitance required to set a certain ramp-time (t_{ramp}) therefore is:

$$C_{SS}[nF] = \frac{2.5\mu A \times t_{ramp}[ms]}{0.6V} \quad (4)$$

If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin to GND to make sure a proper low level. Returning from those states causes a new start-up sequence.

A voltage of less than the internal reference voltage applied at SS/TR can be used as an external voltage reference. The following examples are potential applications for this feature:

- Track an external reference controller voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current in combination with the output capacitor value.
- Track another rail by connecting a voltage divider to the other rail and feed the junction point to SS/TR of this device as shown in [Figure 9-28](#) and in [Figure 9-29](#).
- Voltage sequencing and synchronization of multiple supply rails. Connect for example the open drain PG outputs of other converters to SS/TR of this converter to hold off output voltage generation until the other rails are ready and stable.
- Modulate the output voltage. The voltage level on the SS/TR pin can be changed dynamically during operation at any time after the device started switching. This can be used for example to implement dynamic core voltage scaling for MCUs/CPU/SoCs.

Note: Apply external voltages above 0.6 V at SS/TR. This voltage is then ignored by the device and the internal reference voltage is used instead. The internal current source can pull the SS/TR pin with a pullup current of typical 2.5 μ A above the 0.6-V level up to a level of approximately 1.5 V below V_{IN} . This must be considered for the maximum voltage capability of the soft-start (SS) capacitor and for weak external voltage sources.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TPSM82851x are synchronous, step-down, converter power modules. The required power inductor is integrated in a shielded version inside the TPSM82851x. The TPSM828510, TPSM828511, and TPSM828512 are pin-to-pin and BOM-to-BOM compatible, differing only in their rated output current.

9.2 Typical Application

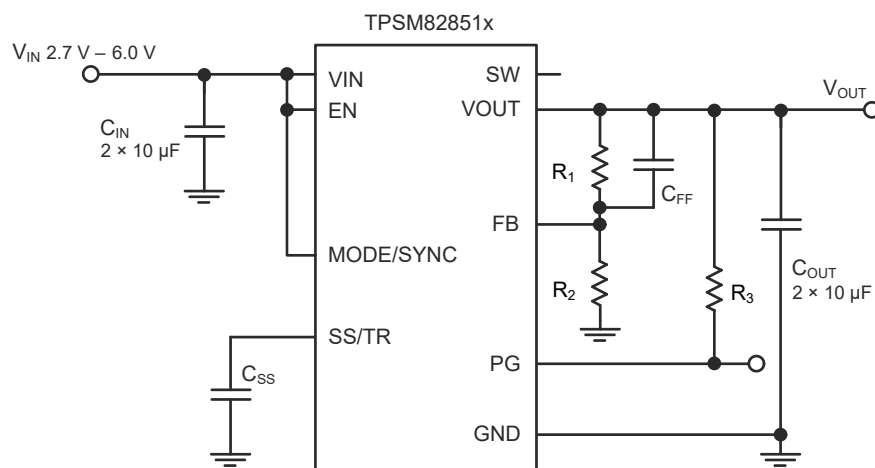


図 9-1. Typical Application Schematic

9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Programming the Output Voltage

The output voltage of the TPSM82851x is adjustable. Choose resistors R1 and R2 to set the output voltage within a range of 0.6 V to 5.5 V according to 式 5. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the [Design Considerations for a Resistive Feedback Divider in a DC/DC Converter analog design journal](#).

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (5)$$

With $V_{FB} = 0.6 \text{ V}$:

表 9-1. Setting the Output Voltage

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	C_{FF}	EXACT OUTPUT VOLTAGE
0.8 V	16.9 kΩ	51 kΩ	10 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	10 pF	1.0 V
1.1 V	39.2 kΩ	47 kΩ	10 pF	1.101 V

表 9-1. Setting the Output Voltage (続き)

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	C_{FF}	EXACT OUTPUT VOLTAGE
1.2 V	68 k Ω	68 k Ω	10 pF	1.2 V
1.5 V	76.8 k Ω	51 k Ω	10 pF	1.5 V
1.8 V	80.6 k Ω	40.2 k Ω	10 pF	1.803 V
2.5 V	47.5 k Ω	15 k Ω	10 pF	2.5 V
3.3 V	88.7 k Ω	19.6 k Ω	10 pF	3.315 V

9.2.2.2 Feedforward Capacitor

TI recommends a feedforward capacitor (C_{FF}) in parallel with R_1 to improve the transient response. Regardless of the FB resistor values, the C_{FF} value must always be 10 pF.

9.2.2.3 Input Capacitor

For most applications, 10- μ F nominal is sufficient and recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a low-ESR multilayer ceramic capacitor (MLCC) for best filtering and must be placed between VIN and GND as close as possible to those pins.

9.2.2.4 Output Capacitor

The architecture of the TPSM82851x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and TI recommends them. To keep low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode.

9.2.2.5 Application Curves

$T_A = 25^\circ\text{C}$, $V_{IN} = 5\text{ V}$, $V_{OUT} = 1.8\text{ V}$, 1.8 MHz, PWM mode, BOM = 表 7-1 unless otherwise noted.

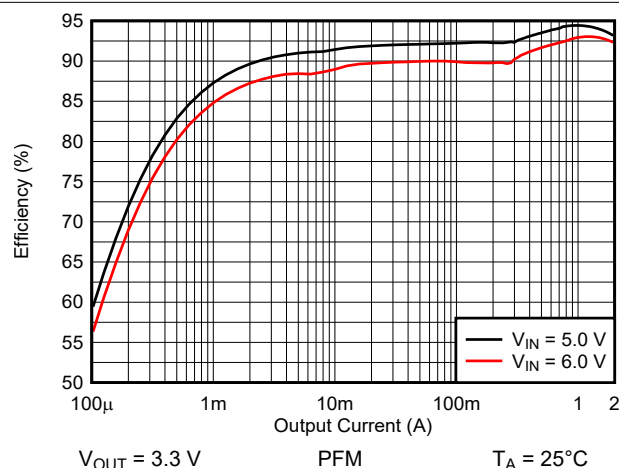


図 9-2. Efficiency versus Output Current

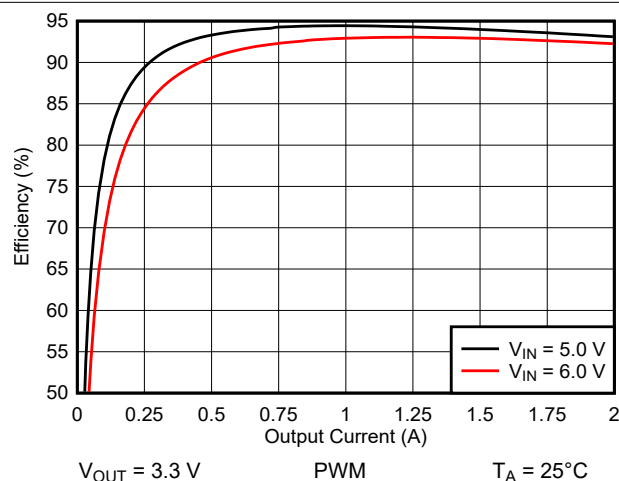


図 9-3. Efficiency versus Output Current

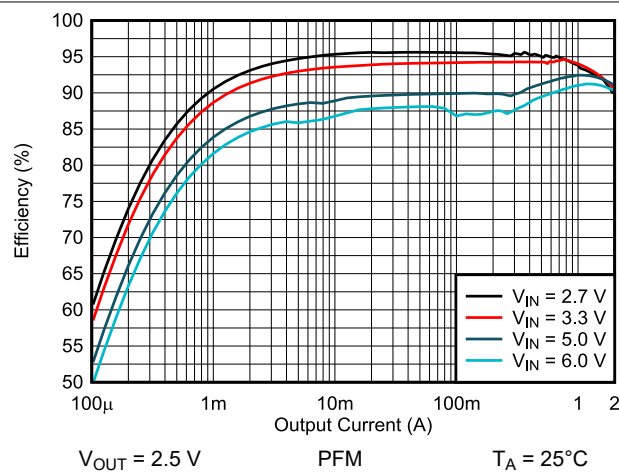


図 9-4. Efficiency versus Output Current

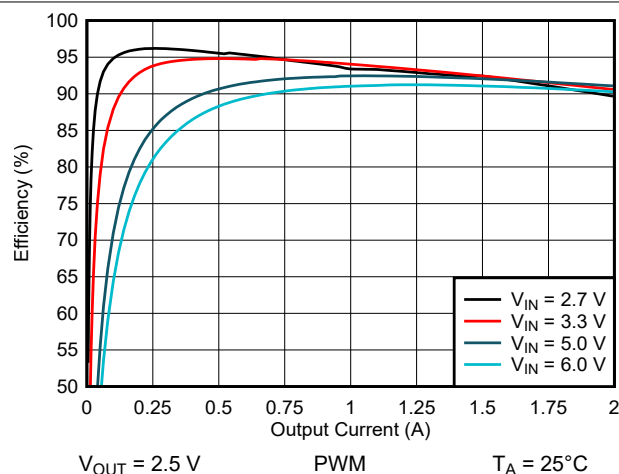


図 9-5. Efficiency versus Output Current

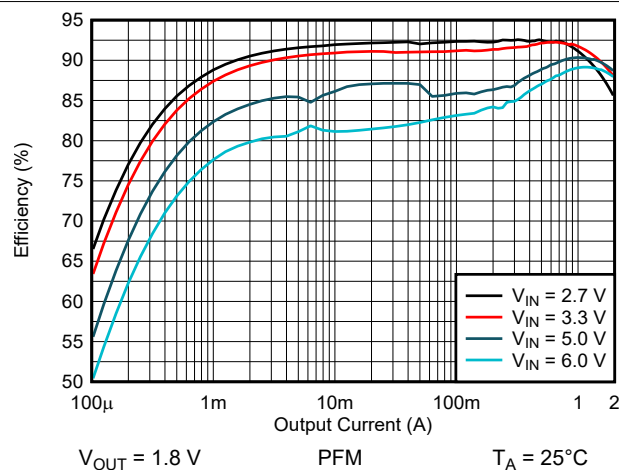


図 9-6. Efficiency versus Output Current

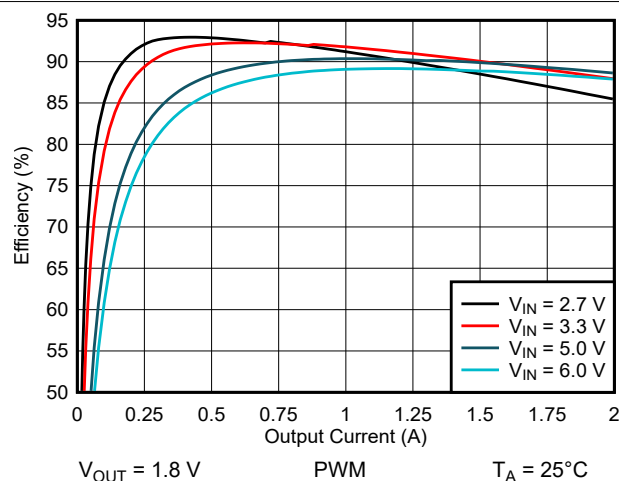
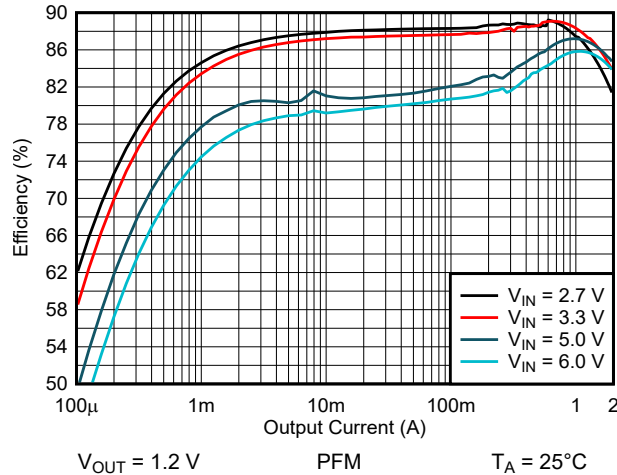
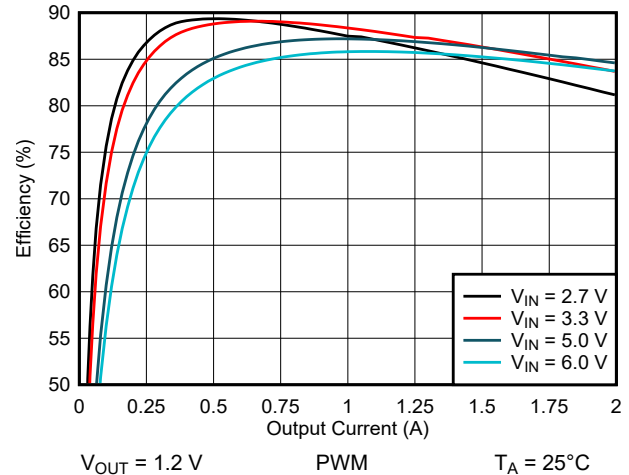


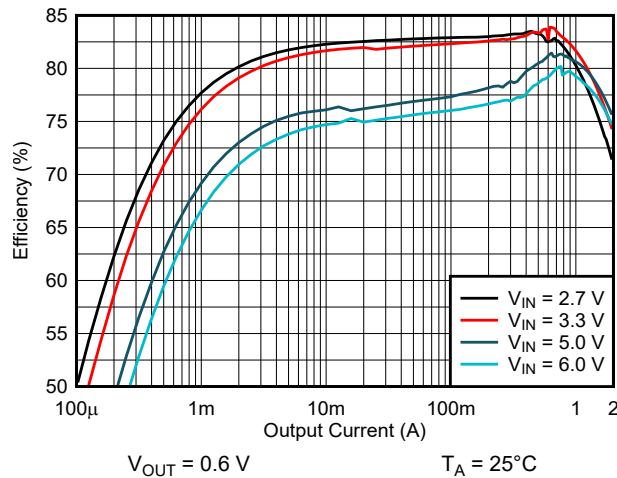
図 9-7. Efficiency versus Output Current



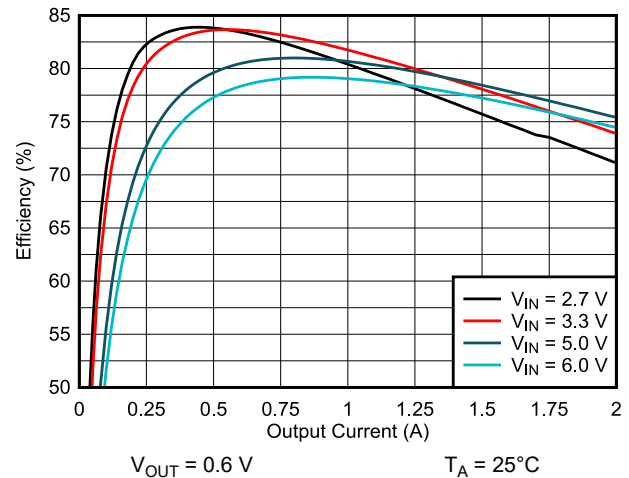
9-8. Efficiency versus Output Current



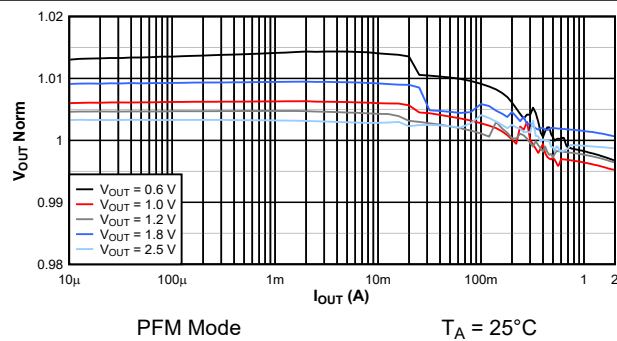
9-9. Efficiency versus Output Current



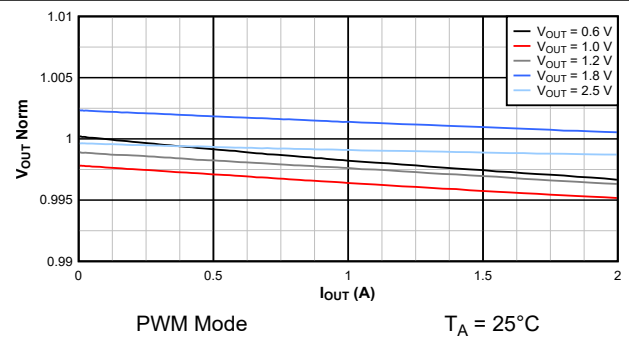
9-10. Efficiency versus Output Current



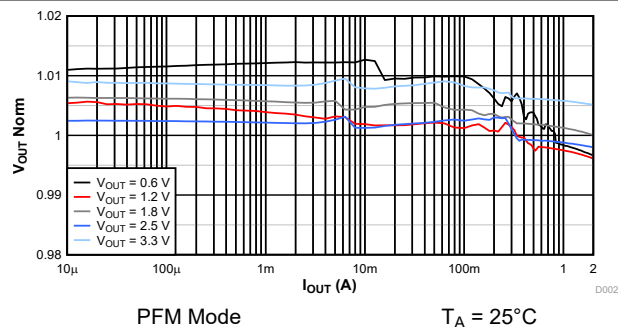
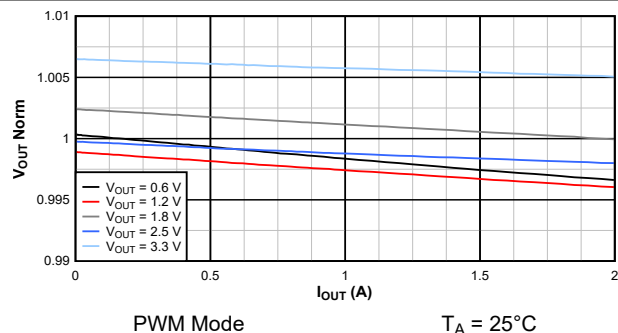
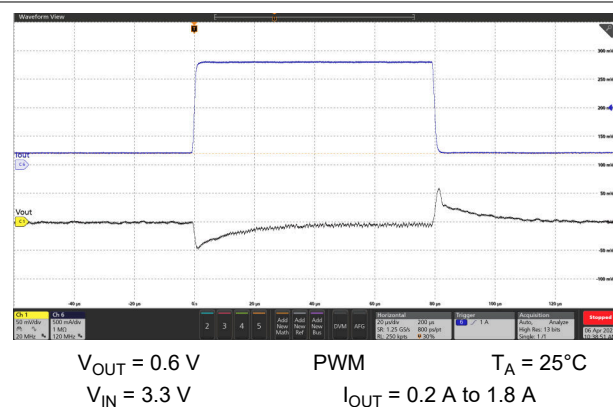
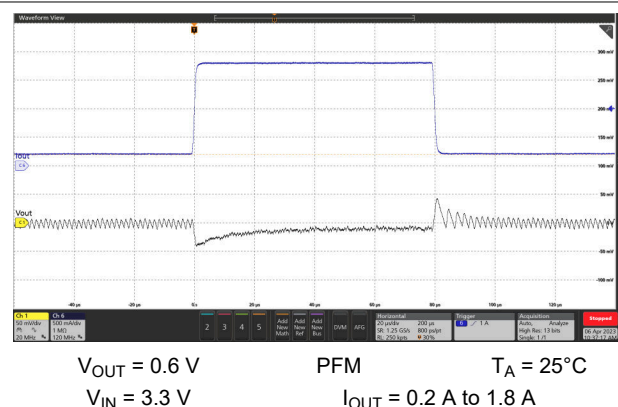
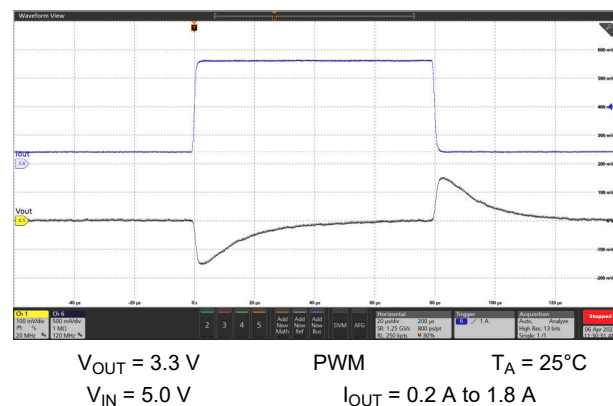
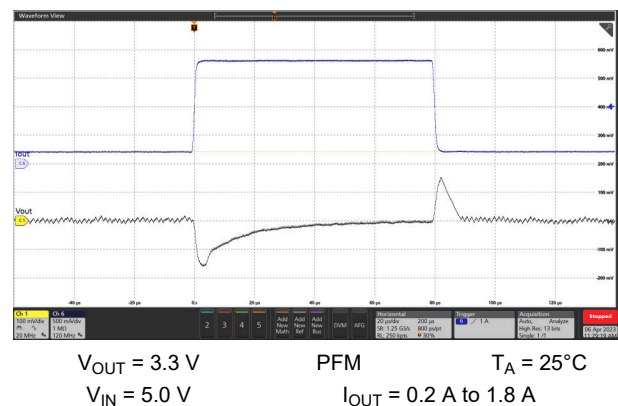
9-11. Efficiency versus Output Current

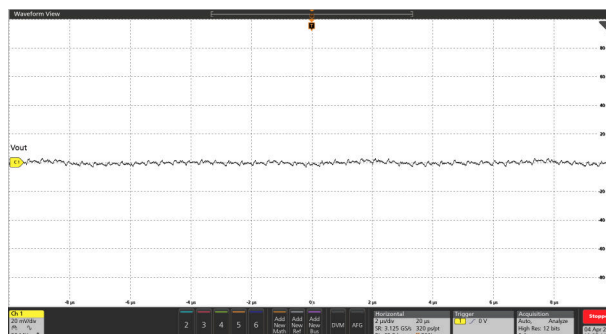


9-12. Load Regulation $V_{IN} = 3.3\text{ V}$



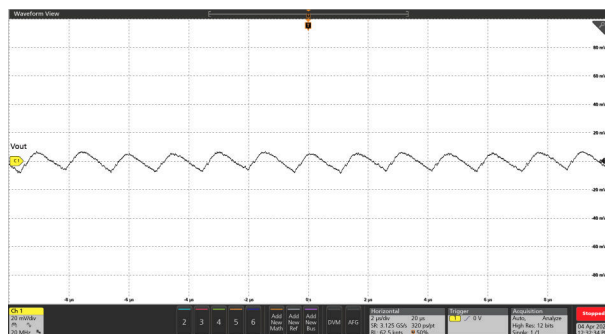
9-13. Load Regulation $V_{IN} = 3.3\text{ V}$


 **9-14. Load Regulation $V_{IN} = 5\text{ V}$**

 **9-15. Load Regulation $V_{IN} = 5\text{ V}$**

 **9-16. Load Transient Response**

 **9-17. Load Transient Response**

 **9-18. Load Transient Response**

 **9-19. Load Transient Response**



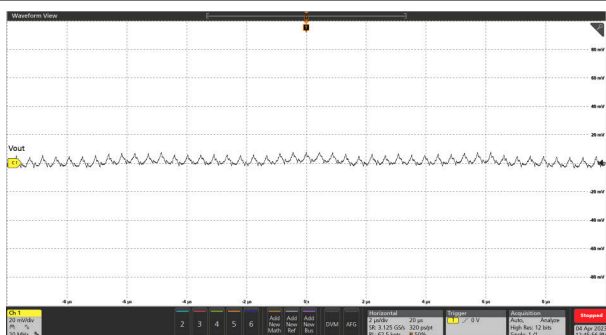
$V_{OUT} = 0.6 \text{ V}$ PWM $T_A = 25^\circ \text{C}$
 $I_{OUT} = 0.2 \text{ A}$ $V_{IN} = 3.3 \text{ V}$ BW = 20 MHz

9-20. Output and Input Voltage Ripple



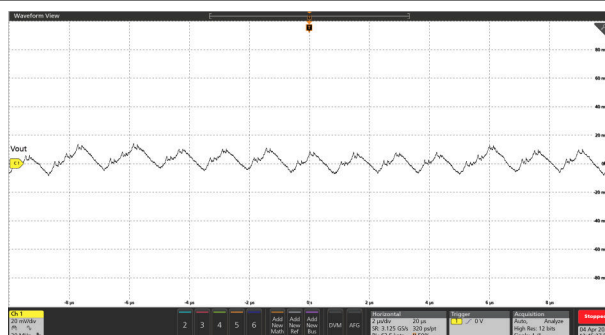
$V_{OUT} = 0.6 \text{ V}$ PFM $T_A = 25^\circ \text{C}$
 $I_{OUT} = 0.2 \text{ A}$ $V_{IN} = 3.3 \text{ V}$ BW = 20 MHz

9-21. Output and Input Voltage Ripple



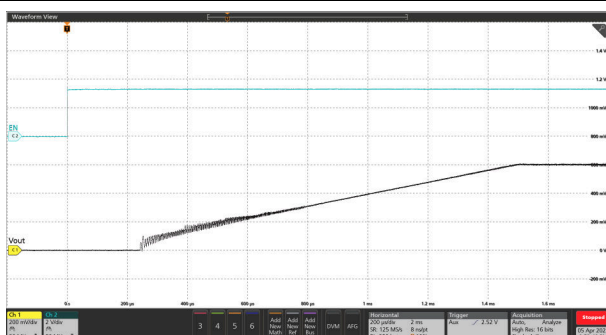
$V_{OUT} = 3.3 \text{ V}$ PWM $T_A = 25^\circ \text{C}$
 $I_{OUT} = 0.2 \text{ A}$ $V_{IN} = 5.0 \text{ V}$ BW = 20 MHz

9-22. Output and Input Voltage Ripple



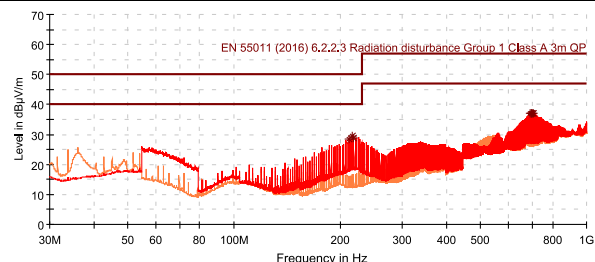
$V_{OUT} = 3.3 \text{ V}$ PFM $T_A = 25^\circ \text{C}$
 $I_{OUT} = 0.2 \text{ A}$ $V_{IN} = 5.0 \text{ V}$ BW = 20 MHz

9-23. Output and Input Voltage Ripple



$V_{OUT} = 0.6 \text{ V}$ PWM/PFM $T_A = 25^\circ \text{C}$
 $I_{OUT} = 2 \text{ A}$ $V_{IN} = 3.3 \text{ V}$ $C_{SS} = 4.7 \text{ nF}$

9-24. Start-Up Timing

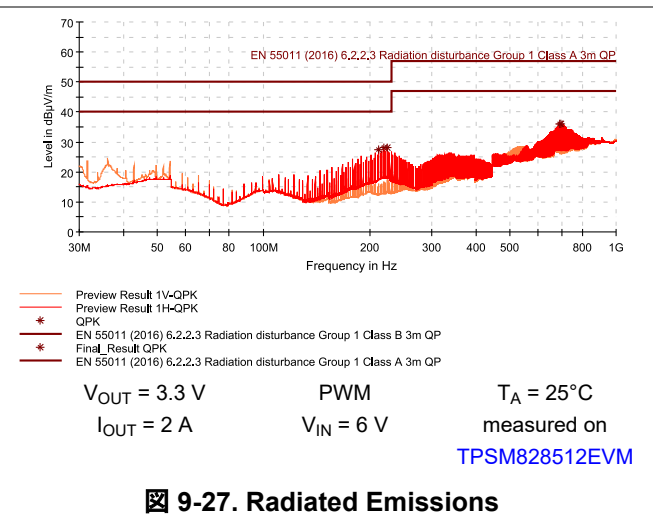
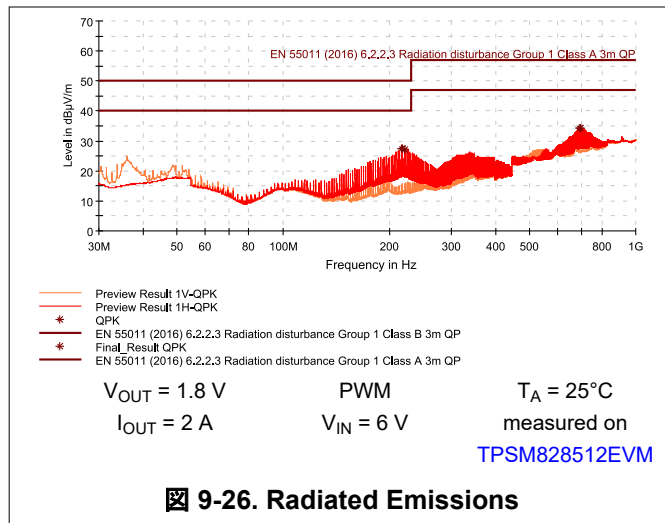


Preview Result 1V-QPK
Preview Result 1H-QPK
* QPK
* EN 55011 (2016) 6.2.2.3 Radiation disturbance Group 1 Class B 3m QP
* Final Result QPK
* EN 55011 (2016) 6.2.2.3 Radiation disturbance Group 1 Class A 3m QP

$V_{OUT} = 1.2 \text{ V}$ PWM $T_A = 25^\circ \text{C}$
 $I_{OUT} = 2 \text{ A}$ $V_{IN} = 6 \text{ V}$ measured on

TPSM828512EVM

9-25. Radiated Emissions



9.3 System Examples

9.3.1 Voltage Tracking

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 図 9-28. From 0 V to 0.6 V, the internal reference voltage to the internal error amplifier follows the SS/TR pin voltage. When the SS/TR pin voltage is above 0.6 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.6 V. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in 図 9-29.

Set the R2 value properly to achieve accurate voltage tracking by taking the 2.5-μA charging current into account. 1 kΩ or smaller is a sufficient value for R2. For decreasing SS/TR pin voltage, the device does not sink current from the output when the device is in PFM mode. The resulting decrease of the output voltage can be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is $V_{IN}+0.3\text{ V}$.

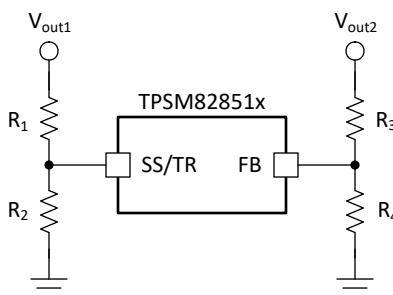


図 9-28. Schematic for Output Voltage Tracking

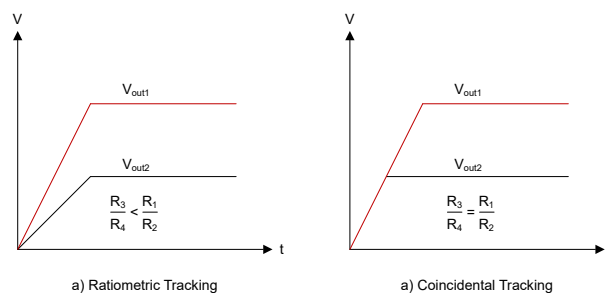


図 9-29. Output Voltage Tracking

9.5 Layout

9.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM82851x demands careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the [Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal](#) for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- Place the input capacitor as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and GND pins avoiding vias.
- Place the output capacitor ground close to the VOUT and GND pins and route directly avoiding vias.
- Place the FB resistors, R1 and R2, and the feedforward capacitor C_{FF} close to the FB pin and place C_{SS} close to the SS/TR pin to minimize noise pickup.
- The recommended layout is implemented on the EVM and shown in [TPSM82851xEVM Evaluation Module EVM user's guide](#) and in [Layout Example](#).
- See the recommended land pattern for the TPSM82851x at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD), when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

9.5.2 Layout Example

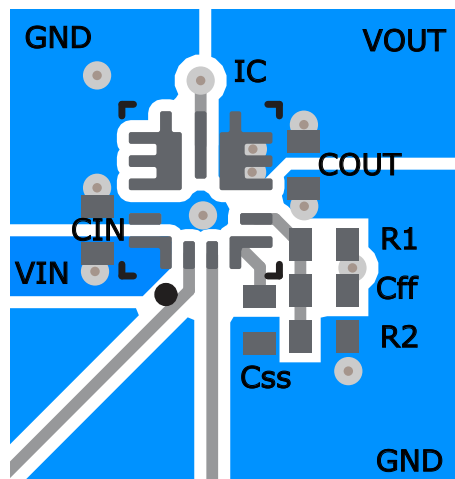


図 9-33. Example Layout

9.5.2.1 Thermal Consideration

The TPSM82851x module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM82851x, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the power dissipation thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs](#) and [Semiconductor and IC Package Thermal Metrics](#).

The thermal values in [Thermal Information](#) used the recommended land pattern, shown at the end of this data sheet, including the 18 vias as shown. The TPSM82851x was simulated on a PCB defined by JEDEC 51-7. The 9 vias on the GND pins were connected to copper on other PCB layers, while the remaining 9 vias were not connected to other layers.

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TPSM82810EVM-089 Evaluation Module EVM user's guide](#)
- Texas Instruments, [TPSM82851xEVM Evaluation Module EVM user's guide](#)
- Texas Instruments, [Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal](#)
- Texas Instruments, [Design Considerations for a Resistive Feedback Divider in a DC/DC Converter analog design journal](#)
- Texas Instruments, [Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold analog design journal](#)
- Texas Instruments, [Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs application note](#)

10.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

10.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
November 2023	*	Initial release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM828510RDYR	Active	Production	QFN-FCMOD (RDY) 9	3000 LARGE T&R	Yes	Call TI	Call TI	-40 to 125	88510
TPSM828510RDYR.A	Active	Production	QFN-FCMOD (RDY) 9	3000 LARGE T&R	Yes	Call TI	Call TI	-40 to 125	88510
TPSM828511RDYR	Active	Production	QFN-FCMOD (RDY) 9	3000 LARGE T&R	Yes	Call TI	Call TI	-40 to 125	88511
TPSM828511RDYR.A	Active	Production	QFN-FCMOD (RDY) 9	3000 LARGE T&R	Yes	Call TI	Call TI	-40 to 125	88511
TPSM828512RDYR	Active	Production	QFN-FCMOD (RDY) 9	3000 LARGE T&R	Yes	Call TI	Call TI	-40 to 125	88512
TPSM828512RDYR.A	Active	Production	QFN-FCMOD (RDY) 9	3000 LARGE T&R	Yes	Call TI	Call TI	-40 to 125	88512

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

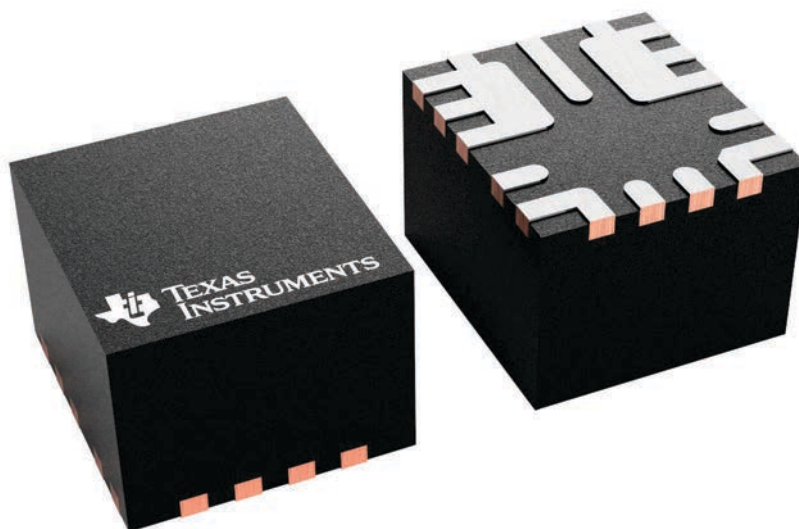
RDY 9

QFN-FCMOD - 2.05 mm max height

2 x 2.7, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

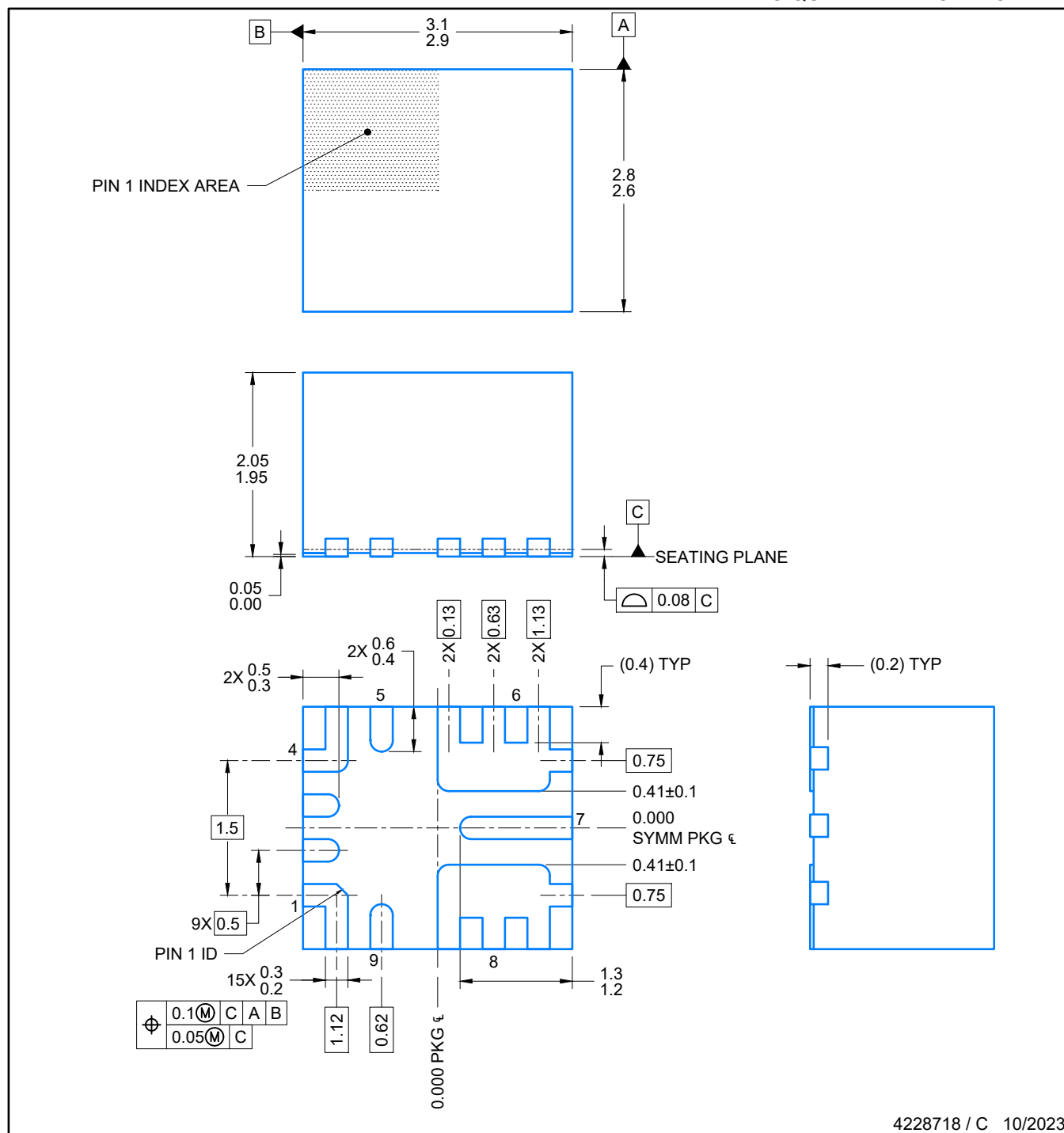
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

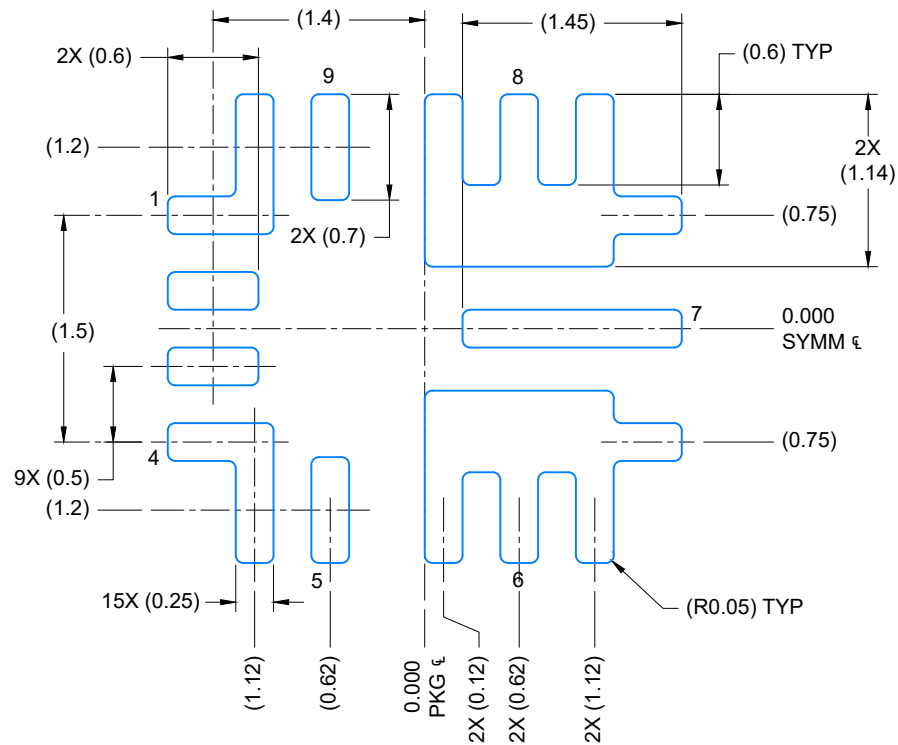
QFN - FCMOD - 2.05 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



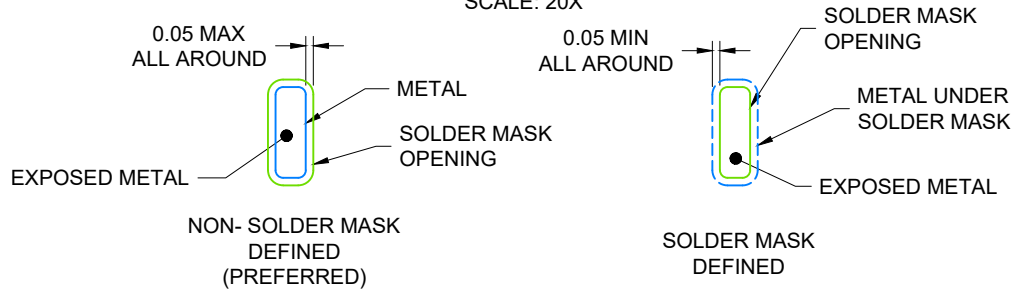
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN
SCALE: 20X

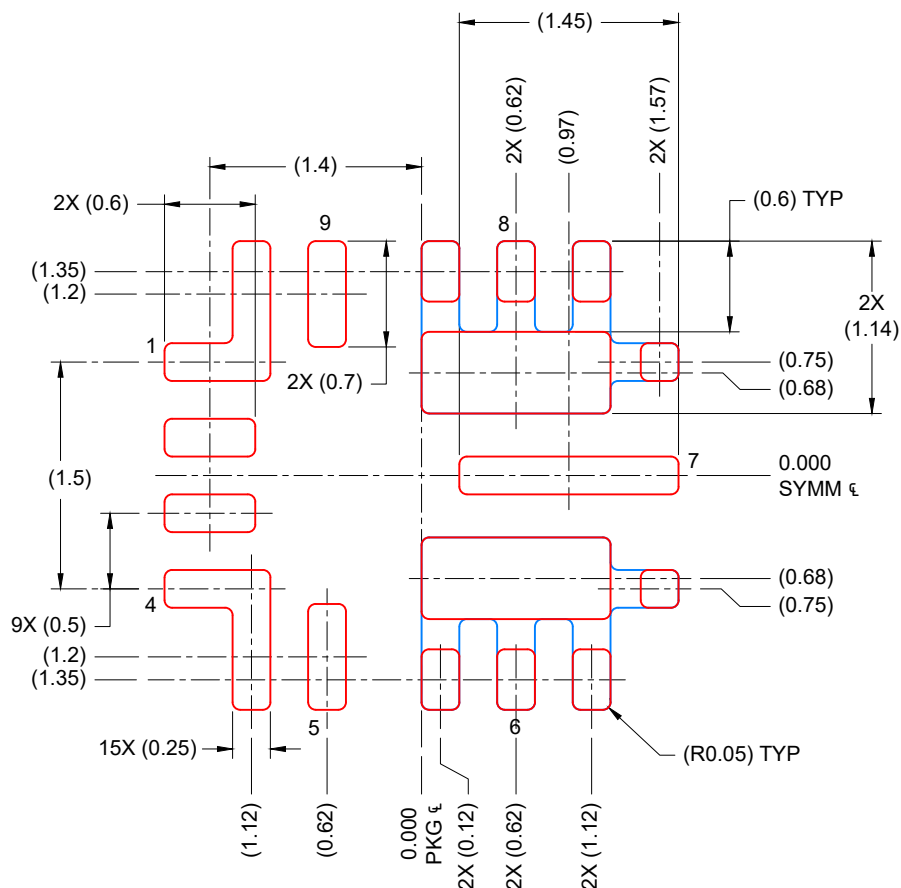


SOLDER MASK DETAILS

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 8 = 84%
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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