参考資料

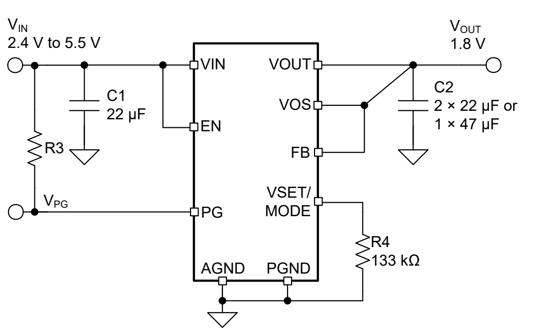
TPSM8286xA 2.4V～5.5V 入力、4A/6A 降圧パワー モジュール、インダクタ内蔵、薄型オーバーモールド QFN および MagPack™ パッケージ

1 特長

- 最大 96% の効率
- 優れた放熱対策
- 出力電圧精度:1%
- DCS-Control トポロジにより、高速過渡応答を実現
- 低 EMI 要件向けの設計
  - MagPack テクノロジーはインダクタと IC をシールド
  - ボンド ワイヤ パッケージなし
  - 最適化されたピン配置によるレイアウトの簡素化
- 入力電圧範囲:2.4V～5.5V
- 同じデバイスの型番で次を提供:
  - 可変出力電圧範囲:0.6V～V_{IN}
  - 13 の固定出力電圧オプションを内蔵
  - 強制 PWM またはパワー セーブ モード
- ウィンドウ コンパレータを使用したパワー グッド出力
- 2.4MHz のスイッチング周波数
- 動作時の静止電流 4μA
- 出力電圧放電
- 100% デューティ サイクル モード
- –40℃～125℃の動作温度範囲
- 0.5mm ピッチの QFN パッケージ:
  - RDJ、RDM:3.5mm × 4.0mm
  - RCF (MagPack):2.3mm × 3.0mm
- 小型設計サイズ:
  - RDJ、RDM:35mm^2 の設計サイズ
  - RCF (MagPack):28mm^2 の設計サイズ
- I^{2}C インターフェイスでも供給可能:TPSM82866C

2 アプリケーション

- FPGA、CPU、ASIC のコア電源
- 光モジュール
- 産業用輸送
- ファクトリ オートメーション / 制御
- 航空宇宙および防衛



代表的なアプリケーションの回路図 - 固定出力電圧オプション

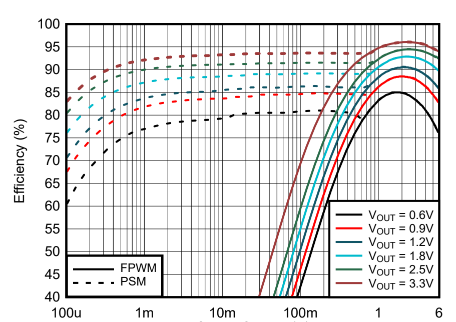
3 概要

TPSM8286xA デバイス ファミリは、小さいソリューション サイズと高い効率を実現できるように設計された 4A および 6A 降圧コンバータ パワー モジュールで構成されています。このパワー モジュールには同期整流降圧コンバータとインダクタが組み込まれているため、設計の簡素化、外付け部品の低減、PCB 面積の削減が可能です。薄く小型のソリューションなので、標準的な表面実装機による自動組み立てに適しています。DCS-Control アーキテクチャと優れた負荷過渡性能を活用して、小さな出力コンデンサでも、厳密な出力電圧精度を実現しています。中負荷から重負荷では PWM モードで動作し、軽負荷時には自動的に省電力モードへ移行するため、負荷電流の全範囲にわたって高効率が維持されます。このデバイスは、強制的に PWM モードで動作させて、出力電圧リップルを最小化することもできます。EN および PG ピンはシーケンシング構成をサポートするため、柔軟なシステム設計が可能です。内蔵のソフト スタートにより、入力電源からの突入電流が減少します。RDJ パッケージは、高さ 1.4mm の薄型設計に対応しています。

製品情報

部品番号(3)	出力電流	パッケージ(1)	本体サイズ (公称)
TPSM82864A	4A	RDJ または RDM (B0QFN、23)	3.50mm × 4.00mm
TPSM82866A	6A		
TPSM82864A(2)	4A	RCF (QFN-FCMOD、15)	2.30mm × 3.00mm
TPSM82866A	6A		

(1) 詳細については、セクション 11 を参照してください。
(2) プレビュー情報 (量産データではありません)。
(3) デバイスのオプションの表を参照してください。



TPSM82866AA0HRDMR – 効率と出力電流との関係、V_{IN} = 5.0V

Table of Contents

4 Device Options

<table>
<tr><th>ORDERABLE PART NUMBER(1)</th><th>OUTPUT CURRENT</th><th>OPERATING FREQUENCY</th><th>NOMINAL INDUCTANCE</th><th>BODY SIZE</th><th>DEVICE HEIGHT</th></tr>
<tr><td>TPSM82864AA0SRDJR</td><td>4 A</td><td rowspan="6">2.4 MHz</td><td rowspan="4">220 nH</td><td rowspan="4">3.5 mm × 4.0 mm</td><td rowspan="2">1.4 mm</td></tr>
<tr><td>TPSM82866AA0SRDJR</td><td>6 A</td></tr>
<tr><td>TPSM82864AA0HRDMR</td><td>4 A</td><td rowspan="2">1.8 mm</td></tr>
<tr><td>TPSM82866AA0HRDMR</td><td>6 A</td></tr>
<tr><td>TPSM82864AA0PRCFR(2)</td><td>4 A</td><td rowspan="4">200 nH</td><td rowspan="4">2.3 mm × 3.0 mm</td><td rowspan="4">1.95 mm</td></tr>
<tr><td>TPSM82866AA0PRCFR</td><td>6 A</td></tr>
<tr><td>TPSM82864BA0PRCFR(2)</td><td>4 A</td><td rowspan="2">1.2 MHz</td></tr>
<tr><td>TPSM82866BA0PRCFR(2)</td><td>6 A</td></tr>
</table>

(1) For more information, see セクション 11.
(2) Preview information (not Production Data).

5 Pin Configuration and Functions

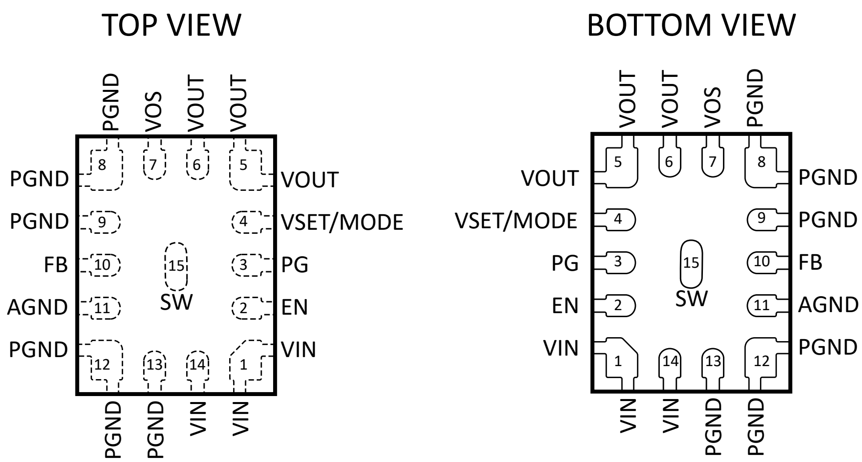


図 5-1. TPSM82864A, TPSM82866A - RCF (15 Pin) QFN-FCMOD

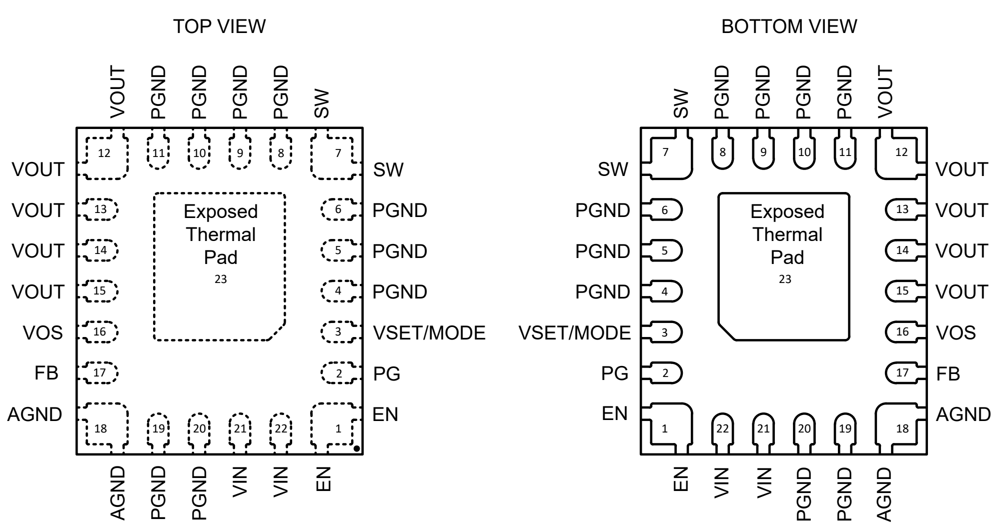


図 5-2. TPSM82864A, TPSM82866A - RDJ (23 Pin) and RDM (23 Pin) B0QFN

表 5-1. Pin Functions

PIN			TYPE[(1)]	DESCRIPTION
NAME	RDJ and RDM	RCF		
AGND	18	11	P	Analog ground pin. Must be connected to a common GND plane.
EN	1	2	I	Device enable pin. To enable the device, this pin must be pulled high. Pulling this pin low disables the device. Do not leave floating.
FB	17	10	I	Voltage feedback input. Connect the output voltage resistor divider to this pin. When using a fixed output voltage, connect directly to VOUT.
PG	2	3	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating. This pin is pulled to GND when the device is in shutdown.
PGND	4, 5, 6, 8, 9, 10, 11, 19, 20	8, 9, 12, 13	P	Power ground pin. Must be connected to common GND plane.
SW	7	15	O	Switch pin of the power stage. This pin can be left floating.
VIN	21, 22	1, 14	P	Power supply input voltage pin
VOS	16	7	I	Output voltage sense pin. This pin must be directly connected to the output capacitor.
VOUT	12, 13, 14, 15	5, 6	P	Output voltage pin
VSET/ MODE	3	4	I	Connecting a resistor to GND selects one of the fixed output voltages. Tying the pin high or low selects an adjustable output voltage. After the device has started up, the pin operates as a MODE input. Applying a high level selects forced PWM mode operation and a low level selects power save mode operation.
Exposed Thermal Pad	23	-	P	Internally connected to PGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability. Must be connected to common GND plane.

(1) I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
Voltage[(2)]	VIN, EN, VOS, FB, PG, VSET/MODE	–0.3	6	V
	SW (DC), VOUT	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10ns)[(3)]	–2.5	10	
I_{SINK_PG}	Sink current at PG		2	mA
T_J	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage range	2.4		5.5	V
V_{OUT}	Output voltage range	0.6		V_{IN}	V
t_{F_VIN}	Falling transition time at VIN [(1)]			10	mV/µs
I_{OUT}	Output current, TPSM82864A			4	A
	Output current, TPSM82866A			6	
R_{VSET}	Nominal resistance range for external voltage selection resistor (E96 resistor series)	10		249	kΩ
	External voltage selection resistor tolerance			1%	
	External voltage selection resistor temperature coefficient			±200	ppm/°C
T_J	Junction temperature	–40		125	°C

(1) The falling slew rate of V_{IN} must be limited if V_{IN} goes below V_{UVLO} (see Power Supply Recommendations).

6.4 Thermal Information

THERMAL METRIC[1]		TPSM8286xA						UNIT
		RDM (23 PINS)		RDJ (23 PINS)		RCF (15 PINS)		
		JEDEC 51-5	EVM	JEDEC 51-5	EVM	JEDEC 51-7	EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.2	25.9	43.3	25.4	66.4	29.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.5	n/a[2]	34.3	n/a[2]	31.8	n/a[2]	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	21.1	n/a[2]	22.2	n/a[2]	n/a[3]	n/a[2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.9	n/a[2]	10.8	n/a[2]	19.5	n/a[2]	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.8	3.7	3.6	2.4	(-2.2)[4]	(-4.2)[4]	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.8	12.7	10.7	10.9	18.8	15.5	°C/W

(1) For more information about thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Not applicable to an EVM.
(3) Only applicable for packages with exposed thermal pad.
(4) The junction temperature is lower than the inductor temperature leading to a temperature increase towards the top of the package

6.5 Electrical Characteristics

T_J = –40°C to 125°C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{Q_VIN}	Quiescent current into VIN pin	EN = High, no load, device not switching		4	10	µA
I_{Q_VOS}	Quiescent current into VOS pin	EN = High, no load, device not switching, V_{VOS} = 1.8 V		8		µA
I_{SD}	Shutdown current	EN = Low, T_J = −40℃ to 85℃		0.24	1	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.2	2.3	2.4	V
		V_{IN} falling	2.1	2.2	2.3	V
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE						
V_{IH}	High-level input threshold voltage at EN and VSET/MODE		1.0			V
V_{IL}	Low-level input threshold voltage at EN and VSET/MODE				0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	0.1	µA
START-UP, POWER GOOD						
t_{Delay}	Enable delay time	Time from EN high to device starts switching with a 249-kΩ resistor connected between VSET/ MODE and GND	420	650	1100	µs
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good	0.8	1	1.5	ms
$V_{PG(low)}$	Power-good lower threshold	V_{FB} referenced to $V_{FB(nominal)}$	85	91	96	%
$V_{PG(high)}$	Power-good upper threshold	V_{FB} referenced to $V_{FB(nominal)}$	103	111	120	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA			0.4	V
$I_{PG,LKG}$	Input leakage current into PG pin	V_{PG} = 5.0 V		0.01	0.1	µA
$t_{PG,DLY}$	Power good delay	Rising and falling edges		34		µs
OUTPUT						
V_{OUT}	Output voltage accuracy	Fixed voltage operation, FPWM, no load, T_J = 0°C to 85°C	–1		1	%
		Fixed voltage operation, FPWM, no load	–2		2	%
V_{FB}	Feedback voltage	Adjustable voltage operation	594	600	606	mV
$I_{FB,LKG}$	Input leakage into FB pin	Adjustable voltage operation, V_{FB} = 0.6 V		0.01	0.4	µA
R_{DIS}	Output discharge resistor at VOS pin			3.5		Ω
	Load regulation	V_{OUT} = 1.2 V, FPWM		0.04		%/A
POWER SWITCH						
R_{DP}	Dropout resistance	TPSM8286xAA0SRDJ 100% mode. V_{IN} = 3.3 V, T_J = 25°C		28	35	mΩ
		TPSM8286xAA0PRCF 100% mode. V_{IN} = 3.3 V, T_J = 25°C		26		mΩ
		TPSM8286xAA0HRDM 100% mode. V_{IN} = 3.3 V, T_J = 25°C		26		mΩ
I_{LIM}	High-side FET forward current limit	TPSM82864A	5	5.5	6	A
		TPSM82866A	7	7.9	9	A
	Low-side FET forward current limit	TPSM82864A		4.5		A
		TPSM82866A		6.5		A
	Low-side FET negative current limit			–3		A

T_J = –40°C to 125°C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	PWM switching frequency	TPSM82866Ax, I_{OUT} = 1 A, V_{OUT} = 1.2 V		2.4		MHz

6.6 Typical Characteristics

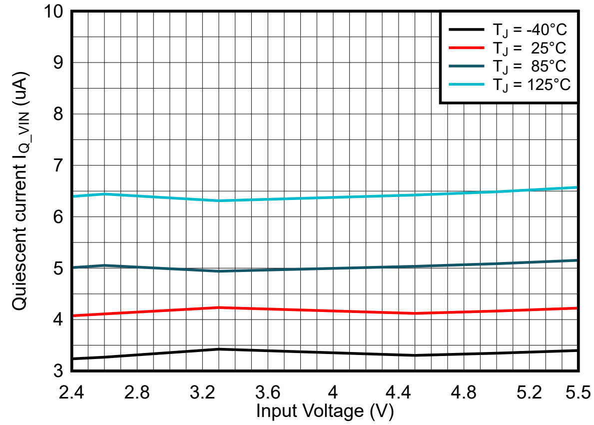


図 6-1. Quiescent Current into V_{IN} I_{Q_VIN}

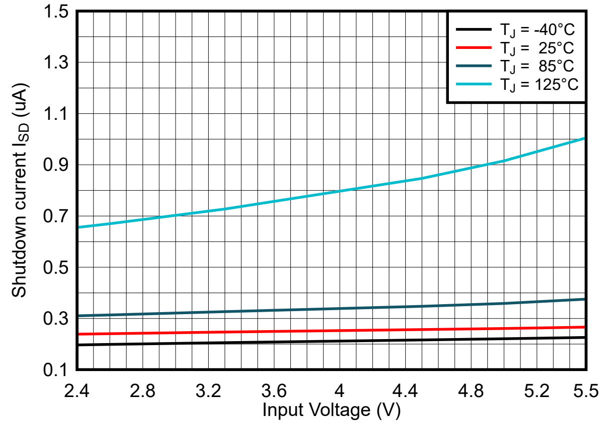


図 6-2. Shutdown Current I_{SD}

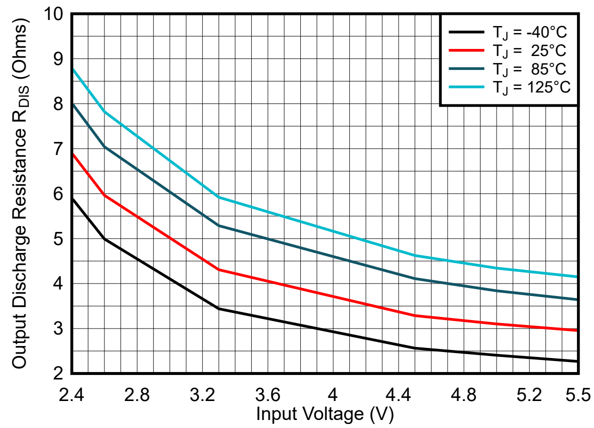
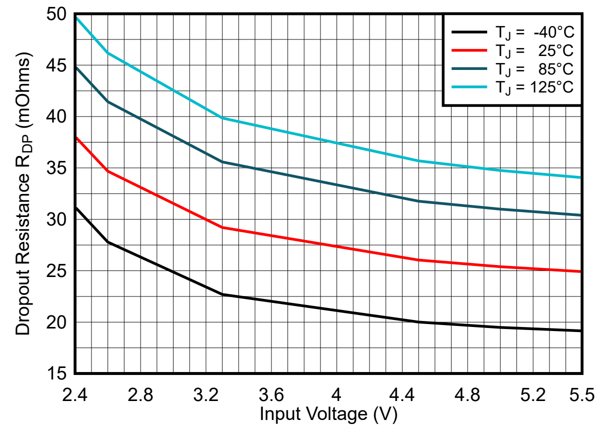
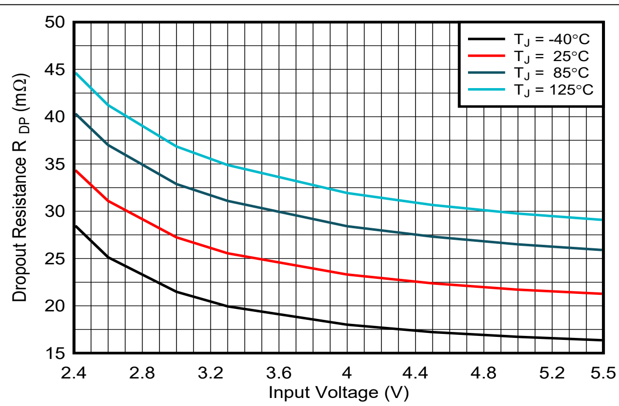


図 6-3. Output Discharge Resistance R_{DIS}



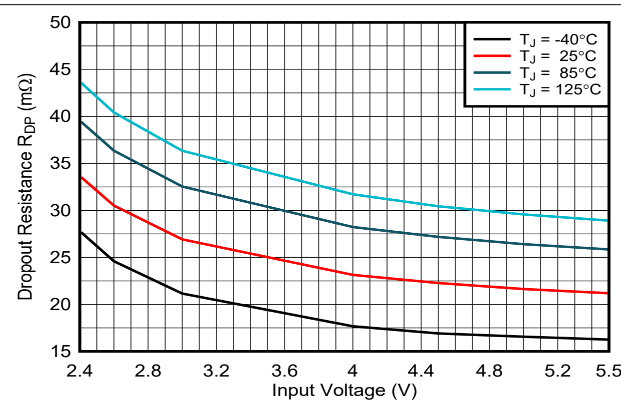
TPSM8286xAA0SRDJ

図 6-4. Dropout Resistance R_{DP}



TPSM8286xAA0HRDM

図 6-5. Dropout Resistance R_{DP}



TPSM8286xAA0PRCF

図 6-6. Dropout Resistance R_{DP}

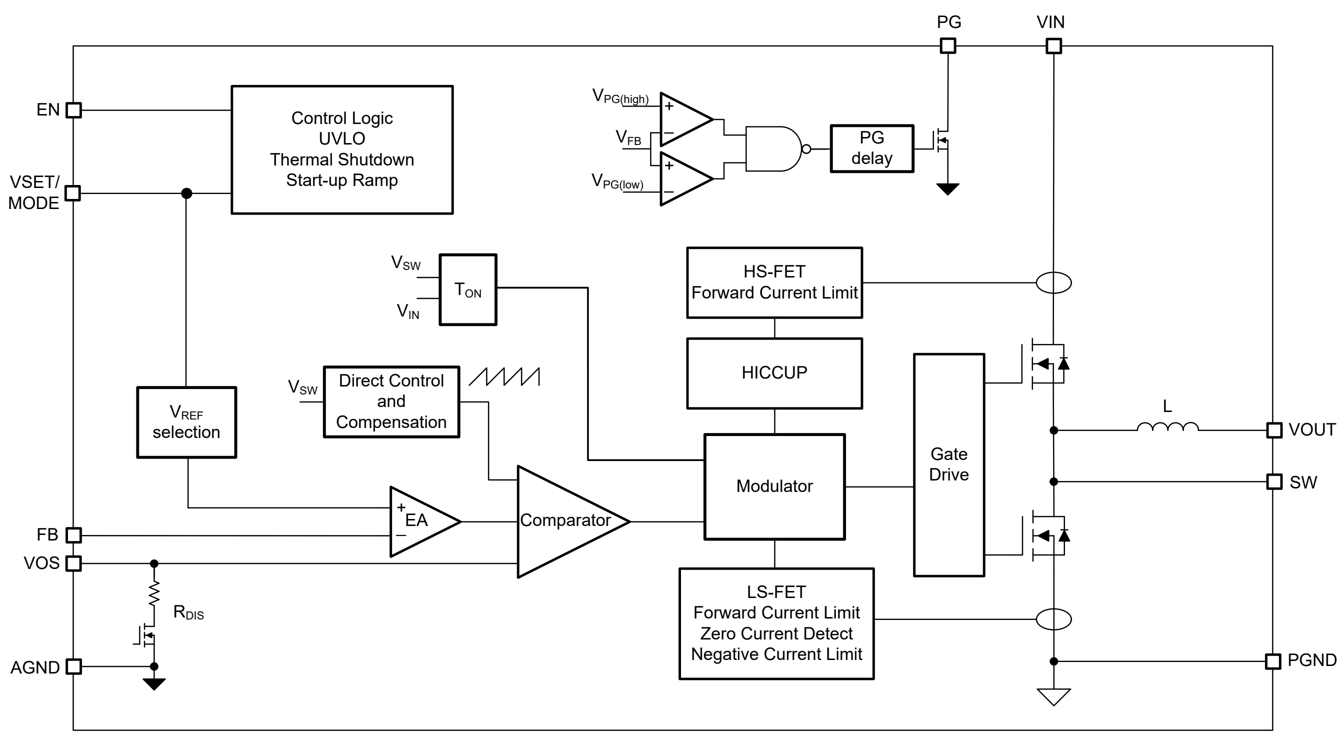
7 Detailed Description

7.1 Overview

The TPSM8286xA synchronous step-down converter power module is based on DCS-Control (Direct Control with Seamless transition into power save mode). This topology is an advanced regulation topology that combines the advantages of hysteretic, voltage, and current mode control. The DCS-Control topology operates in PWM (pulse width modulation) mode for medium-to-heavy load conditions and in PSM (power save mode) at light load currents. In PWM, the converter operates with the nominal switching frequency of 2.4 MHz, having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the quiescent current of the IC to achieve high efficiency over the entire load current range. DCS-Control supports both operation modes using a single building block and, therefore, has a seamless transition from PWM to PSM without effects on the output voltage. The TPSM8286xA offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

The TPSM8286xxxxP versions in the RCF package use MagPack technology to deliver the highest-performance power module design. Leveraging our proprietary integrated-magnetics MagPack packaging technology, these power modules deliver industry-leading power density, high efficiency and good thermal performance, ease of use, and reduced EMI emissions.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

As the load current decreases, the device seamlessly enters power save mode (PSM) operation. In PSM, the converter operates with a reduced switching frequency and a minimum quiescent current to maintain high efficiency. Power save mode is based on a fixed on-time architecture, as shown in 式 1. The inductance used in the RCF package using MagPack technology is 200 nH typical where the inductance used in the RDJ and RDM packages is 220 nH typical.

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \tag{1}$$

For very small output voltages, an absolute minimum on time of approximately 50ns is kept to limit switching losses. The operating frequency is thereby reduced from the nominal value, which keeps efficiency high. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}{}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \tag{2}$$

The load current at which PSM is entered is at one half of the ripple current of the inductor and can be estimated as:

$$I_{Load(PSM - entry)} = \frac{V_{IN} \times t_{ON}}{2} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L} \tag{3}$$

In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitance.

7.3.2 Forced PWM Mode

After the device has powered up and ramped up VOUT, the VSET/MODE pin acts as a digital input. With a high level on the VSET/MODE pin, the device enters forced PWM (FPWM) mode and operates with a constant switching frequency over the entire load range, even at very light loads. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications but lowers efficiency at light loads.

7.3.3 Optimized Transient Performance from PWM to PSM Operation

For most converters, the load transient response in PWM mode is improved compared to PSM, because the converter reacts faster on the load step and actively sinks energy on the load release. As an additional feature, the TPSM8286xA automatically stays in PWM mode for 128 cycles after a heavy load release to bring the output voltage back to the regulation level faster. After these 128 cycles of PWM mode, it automatically returns to PSM (if VSET/MODE is low). See 図 7-1. Without this optimization, the output voltage overshoot is higher.

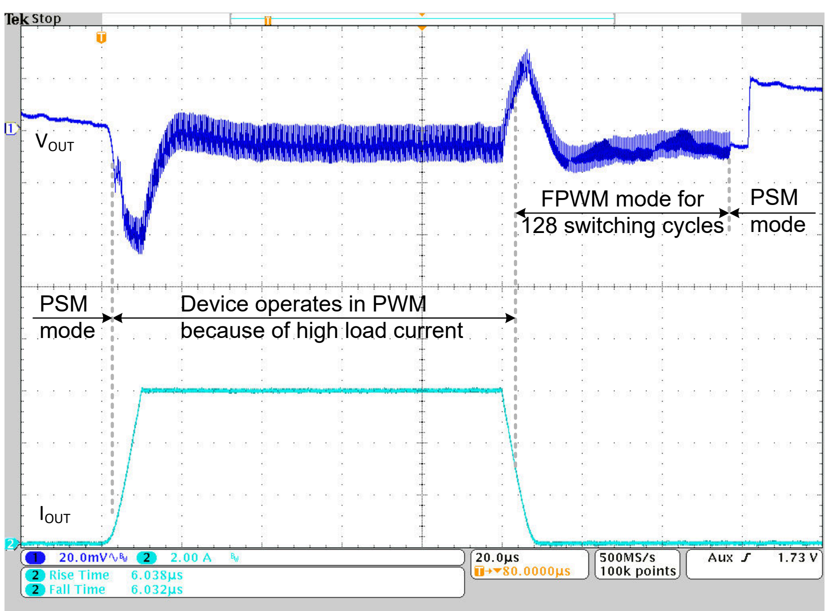


図 7-1. Optimized Transient Performance from PWM to PSM

7.3.4 Low Dropout Operation (100% Duty Cycle)

The device offers a low dropout operation by entering 100% duty cycle mode if the input voltage comes close to the target output voltage. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN\ (min)} = V_{OUT\ (min)} + I_{OUT\ (max)} \times R_{DP} \quad (4)$$

where

- $V_{OUT\ (min)}$ = Minimum output voltage the load can accept
- $I_{OUT\ (max)}$ = Maximum output current
- R_{DP} = Resistance from VIN to VOUT (high-side $R_{DS(on)}$ + R_{DC} of the inductor)

7.3.5 Soft Start

After enabling the device, there is a 650-µs enable delay (t_{Delay}) before the device starts switching. The t_{Delay} time varies with the VSET/MODE resistor used and is longest with a resistance of 249 kΩ or higher. After the enable delay, an internal soft-start circuit ramps up the output voltage in 1 ms (t_{Ramp}). This action avoids excessive inrush current and creates a smooth output voltage ramp up. This action also prevents excessive voltage drops of batteries that have a high internal impedance. 図 7-2 shows the start-up sequence.

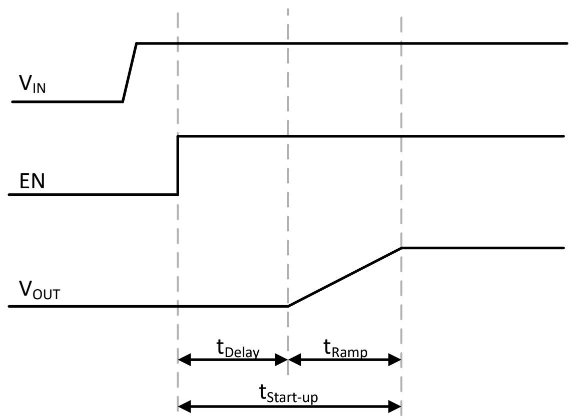


図 7-2. Start-Up Sequence

The device is able to start into a prebiased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.6 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current can occur with a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, cycle by cycle, the high-side MOSFET is turned off and the low-side MOSFET is turned on until the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 256 times, the device stops switching. The device then automatically re-starts with soft start after a typical delay time of 16 ms has passed. The device repeats this mode until the high load condition disappears. This HICCUP short-circuit protection reduces the current consumed from the input supply because the device only draws input current approximately 10% of the time during an overload condition. 図 8-37 shows the hiccup short-circuit protection.

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in forced PWM mode.

7.3.7 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, undervoltage lockout (UVLO) disables the device when the input voltage is lower than V_{UVLO}. When the input voltage recovers, the device automatically returns to operation with soft start.

7.3.8 Thermal Shutdown

When the junction temperature exceeds T_{JSD}, the device goes into thermal shutdown, stops switching, and activates the output voltage discharge. When the device temperature falls below the threshold by the hysteresis, the device returns to normal operation automatically with soft start.

7.4 Device Functional Modes

7.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal switch smoothly discharges the output through the VOS pin in shutdown mode. Do not leave the EN pin floating.

The typical enable threshold value of the EN pin is 0.66 V for rising input signals and the typical shutdown threshold is 0.52 V for falling input signals.

7.4.2 Output Discharge

The purpose of the output discharge function is to make sure of a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge is active when the EN pin is pulled low, when the input voltage is below the UVLO threshold or during thermal shutdown. The discharge is active down to an input voltage of 1.6 V (typical).

7.4.3 Power Good (PG)

The device has an open-drain power-good pin, which is specified to sink up to 2 mA. The power-good output requires a pullup resistor connected to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used. 表 7-1 shows the typical PG pin logic.

表 7-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable	$0.9 \times V_{OUT\_NOM} \le V_{VOUT} \le 1.1 \times V_{OUT\_NOM}$	√	
	$V_{VOUT} < 0.9 \times V_{OUT\_NOM}$ or $V_{VOUT} > 1.1 \times V_{OUT\_NOM}$		√
Shutdown	EN = low		√
Thermal shutdown	$T_J > T_{JSD}$		√
UVLO	$1.8\text{ V} < V_{IN} < V_{UVLO}$		√
Power supply removal	$V_{IN} < 1.8\text{ V}$	undefined	

The PG pin has a 34-µs delay time on the falling edge and a 34-µs delay before PG goes high. See 図 7-3.

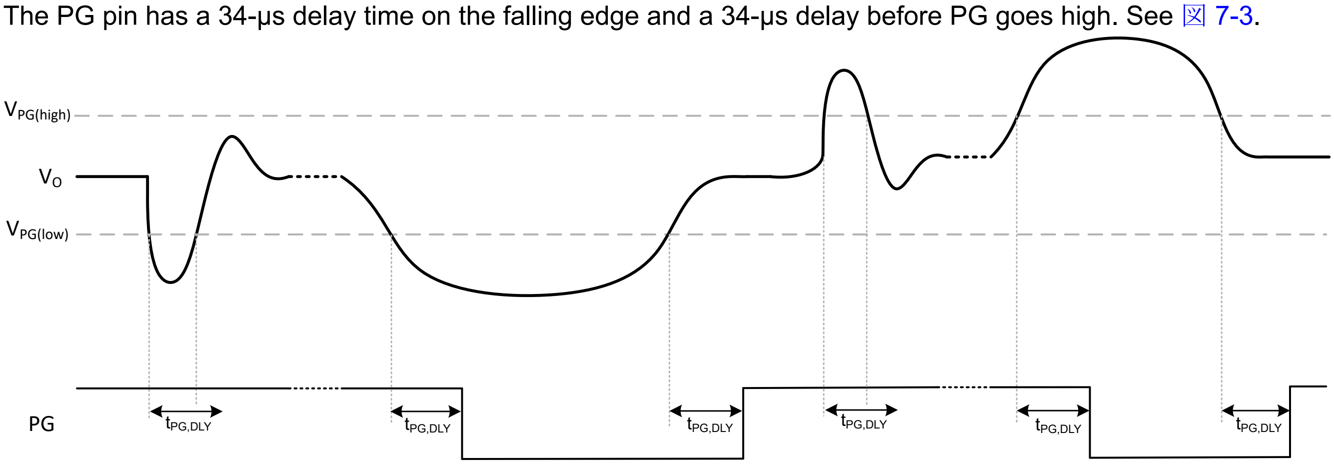


図 7-3. Power-Good Transient and Delay Behavior

7.4.4 Output Voltage and Mode Selection (VSET/MODE)

The TPSM8286xA family devices are configurable as either an adjustable output voltage or a fixed output voltage, depending on the needs of each individual application. This feature simplifies the logistics during mass production, as one part number offers several fixed output voltage options as well as an adjustable output voltage option. During the enable delay (t_{Delay}), the device configuration is set by an external resistor connected to the VSET/MODE pin through an internal R2D (resistor to digital) converter. This configures the V_{REF} input to the error amplifier (EA) to be either the V_{FB} voltage (0.6-V typical) or the selected output voltage. 表 7-2 shows the options.

表 7-2. Output Voltage Selection Table

RESISTOR AT VSET/MODE PIN (E96 SERIES, ±1% ACCURACY, 200 ppm/°C OR BETTER)	FIXED OR ADJUSTABLE OUTPUT VOLTAGE
249 k or logic high	Adjustable (through a resistive divider on the FB pin)
205 k	3.30 V
162 k	2.50 V
133 k	1.80 V
105 k	1.50 V
68.1 k	1.35 V
56.2 k	1.20 V
44.2 k	1.10 V
36.5 k	1.05 V
28.7 k	1.00 V
23.7 k	0.95 V
18.7 k	0.90 V
15.4 k	0.85 V
12.1 k	0.80 V
10 k or logic low	Adjustable (through a resistive divider on the FB pin)

The R2D converter has an internal current source, which applies current through the external resistor, and an internal ADC, which reads back the resulting voltage level. Depending on the detected resistance, the output voltage is set. After this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Make sure that the additional leakage current path is less than 20 nA and the capacitance is not greater than 30 pF from this pin to GND during R2D conversion, otherwise a false V_{OUT} value is set. For more details, refer to the *Benefits of a Resistor-to-Digital Converter in Ultra-Low Power Supplies White Paper*. When the device is set to a fixed output voltage, the FB pin must be connected to the output directly. See 図 7-4.

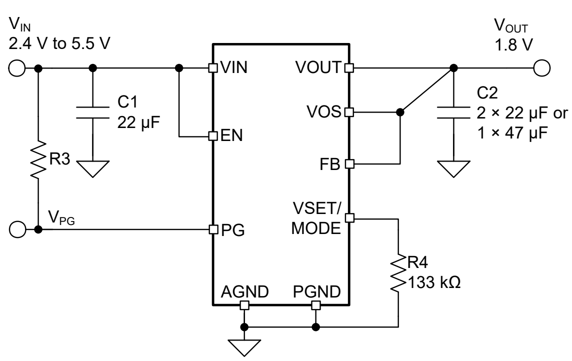


図 7-4. Fixed Output Voltage Application Circuit

After the start-up period ($t_{Start\text{-}up}$), a different operation mode can be selected. When VSET/MODE is set to high, the device is in forced PWM mode. Otherwise, the VSET/MODE resistor pulls the pin low and the device operates in power save mode.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TPSM8286xA is a synchronous step-down converter power module family. The following section discusses the selection of the external components to complete the power supply design. The required power inductor is integrated inside the TPSM8286xA. The integrated shielded inductor has a value of 220 nH with a ±20% tolerance for the RDJ and RDM packages. The RCF MagPack package not only has a 200 nH shielded inductor but also shields the IC for a better EMI performance. The TPSM82864A and TPSM82866A in the RDJ and RDM packages are pin-to-pin and BOM-to-BOM compatible. The TPSM8286xAA0HRDMR devices give a higher efficiency than the TPSM8286xAA0SRDJR devices due to the increased height. For a given package height (RDM or RDJ), the 4A and 6A version give the same efficiency and performance and are different only in the rated output current. The RCF package, using MagPack technology, is less than half the size of the other package versions (RDM and RDJ), thus shrinking the total design size by about 20%, while maintaining the same high efficiency as the other packages.

8.2 Typical Application

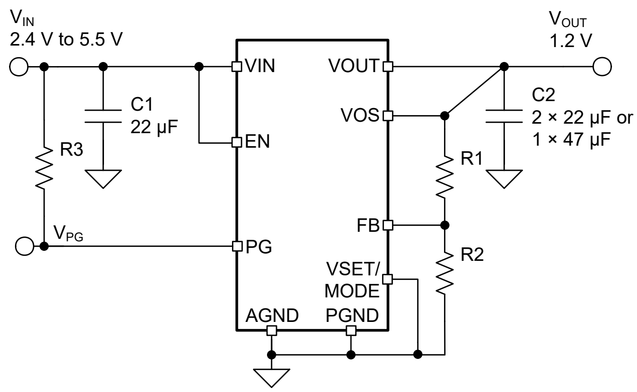


図 8-1. Typical Application

8.2.1 Design Requirements

For this design example, use 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4 V to 5.5 V
Output voltage	1.2 V
Maximum output current	6 A

表 8-2 lists the components used for the example.

表 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1	22 µF, Ceramic capacitor, 6.3 V, X7R, size 0805, GRM21BZ70J226ME44	Murata
C2	47 µF, Ceramic capacitor, 6.3 V, X6S, size 0805, JMK212BC6476MG-T or GRM21BC80J476ME01L	Taiyo Yuden or Murata
R1	Depending on the output voltage, Chip resistor, 1/16 W, 1%	Std
R2	100 kΩ, Chip resistor, 1/16 W, 1%	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%	Std

(1) See the *Third-party Products* disclaimer.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting The Output Voltage

With the VSET/MODE pin set high or low, an adjustable output voltage is set by an external resistor divider according to 式 5:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \tag{5}$$

To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity but lower light-load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter Technical Brief*.

When a fixed output voltage is selected, connect the FB pin directly to the output. R1 and R2 are not needed, as V_{OUT} is set through a resistor on the VSET/MODE pin. Select the recommended resistor value from the list in 表 7-2.

8.2.2.2 Input and Output Capacitor Selection

For the best output and input voltage filtering, low-ESR ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. The input capacitor must be placed between VIN and PGND as close as possible to those pins. For most applications, 22 µF is sufficient, though a larger value reduces input current ripple. The input capacitor plays an important role in the EMI performance of the system as explained in the *Simplify Low EMI Design With Power Modules White Paper*.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. The capacitor value can range from 2 × 22 µF up to 150 µF. The recommended typical output capacitors are 2 × 22 µF or 1 × 47 µF with an X5R or better dielectric. Values over 150 µF can degrade the loop stability of the converter.

Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating. Make sure that the effective input capacitance is at least 10 µF and the effective output capacitance is at least 22 µF.

8.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 1.2 V, T_A = 25°C, BOM = 表 8-2, unless otherwise noted. Solid lines show the FPWM mode and dashed lines show PSM.

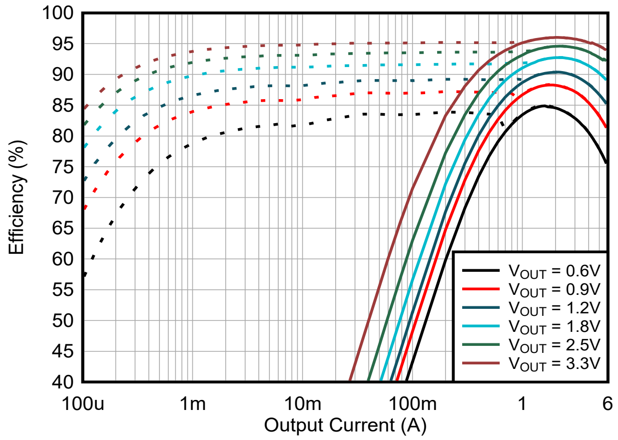


図 8-2. Efficiency V_{IN} = 5.0 V and T_A = 25°C

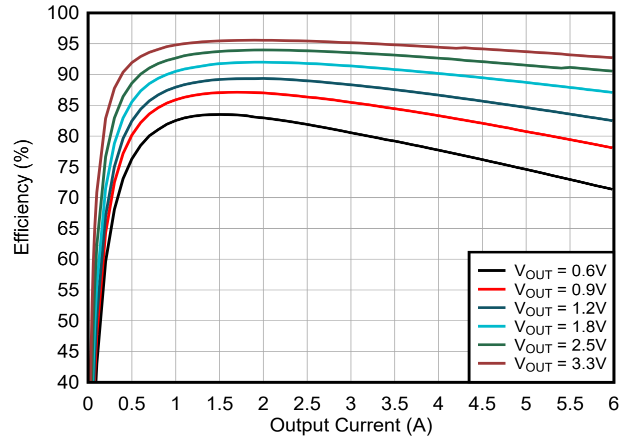


図 8-3. Efficiency V_{IN} = 5.0 V and T_A = 85°C

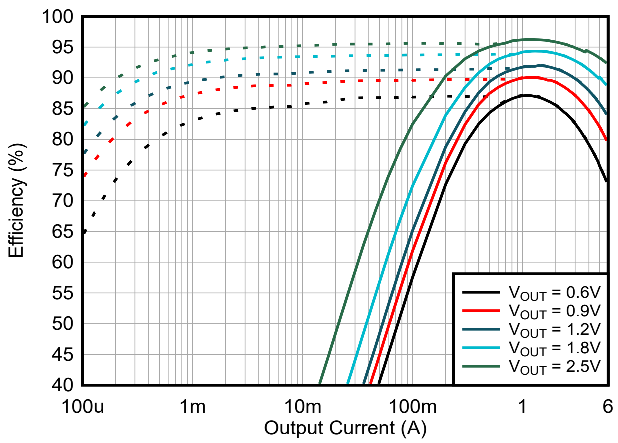


図 8-4. Efficiency V_{IN} = 3.3 V and T_A = 25°C

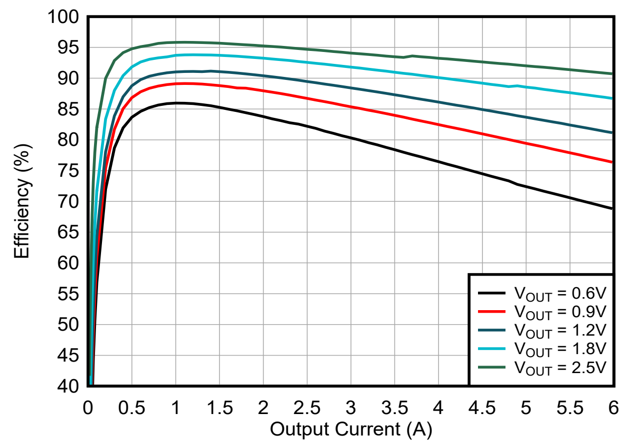
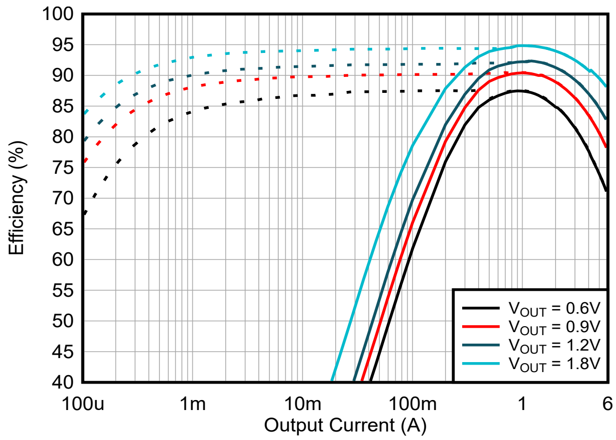
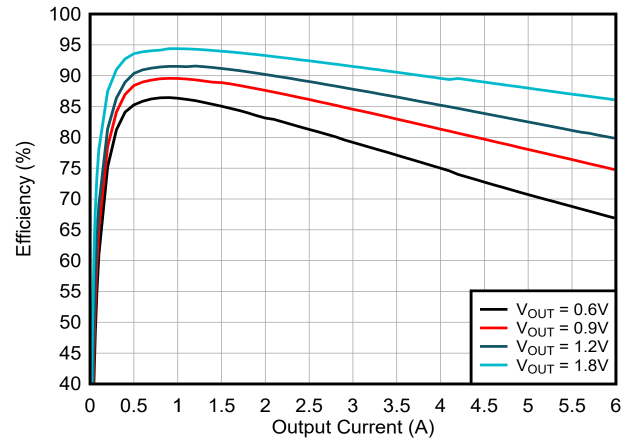


図 8-5. Efficiency V_{IN} = 3.3 V and T_A = 85°C



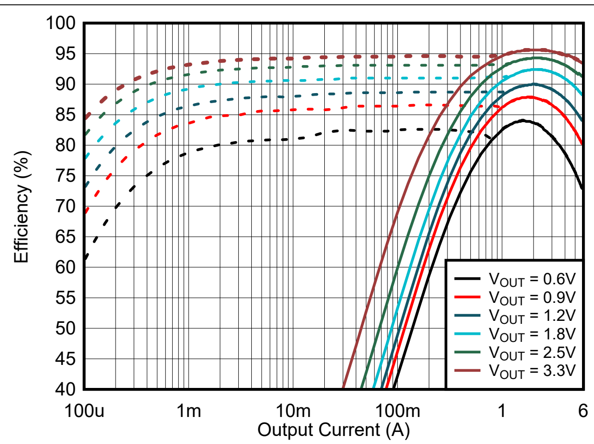
TPSM8286xAA0PRCF PSM and FPWM

図 8-6. Efficiency V_{IN} = 2.8 V and T_A = 25°C



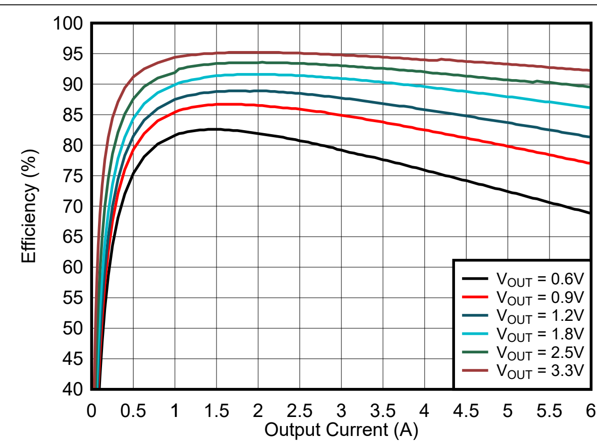
TPSM8286xAA0PRCF FPWM

図 8-7. Efficiency V_{IN} = 2.8 V and T_A = 85°C



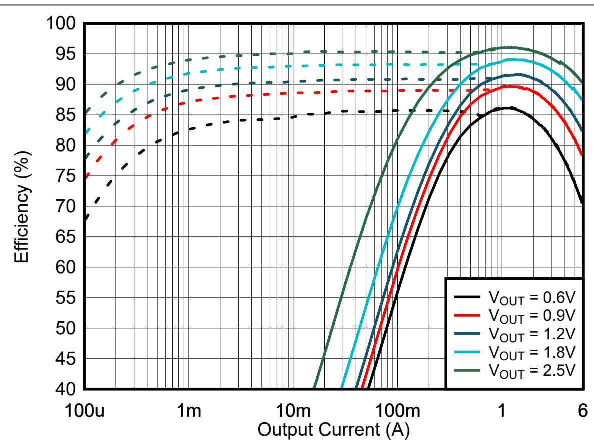
TPSM8286xAA0SRDJ PSM and FPWM

図 8-8. Efficiency V_{IN} = 5.0 V and T_A = 25°C



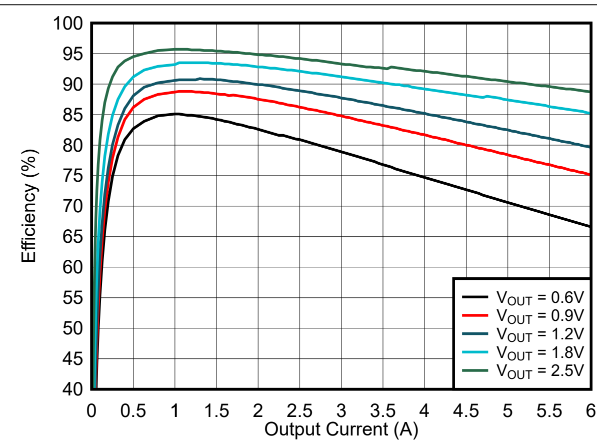
TPSM8286xAA0SRDJ FPWM

図 8-9. Efficiency V_{IN} = 5.0 V and T_A = 85°C



TPSM8286xAA0SRDJ PSM and FPWM

図 8-10. Efficiency V_{IN} = 3.3 V and T_A = 25°C



TPSM8286xAA0SRDJ FPWM

図 8-11. Efficiency V_{IN} = 3.3 V and T_A = 85°C

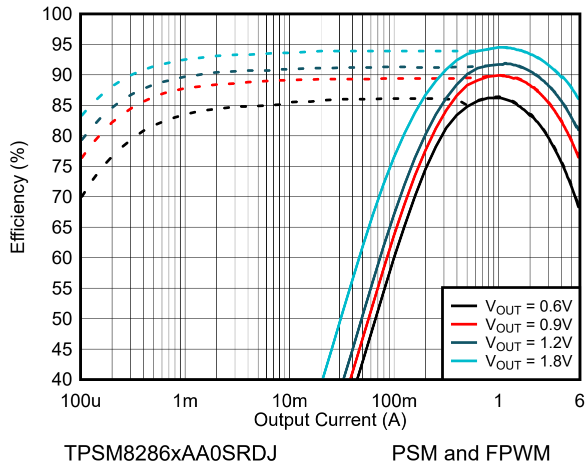


図 8-12. Efficiency V_{IN} = 2.8 V and T_A = 25°C

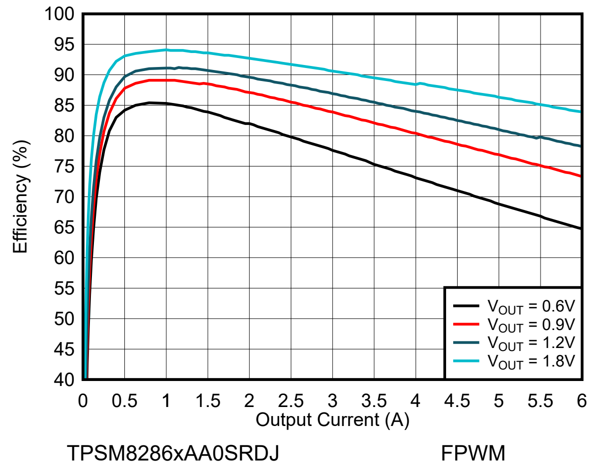


図 8-13. Efficiency V_{IN} = 2.8 V and T_A = 85°C

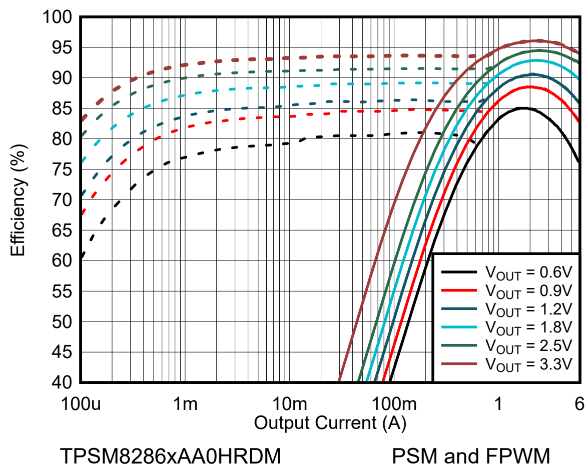


図 8-14. Efficiency V_{IN} = 5.0 V and T_A = 25°C

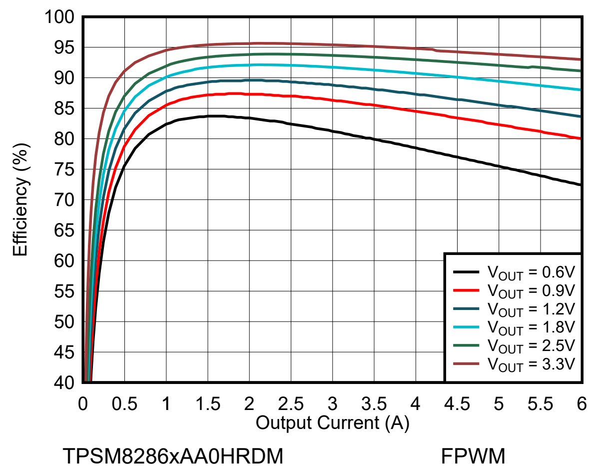


図 8-15. Efficiency V_{IN} = 5.0 V and T_A = 85°C

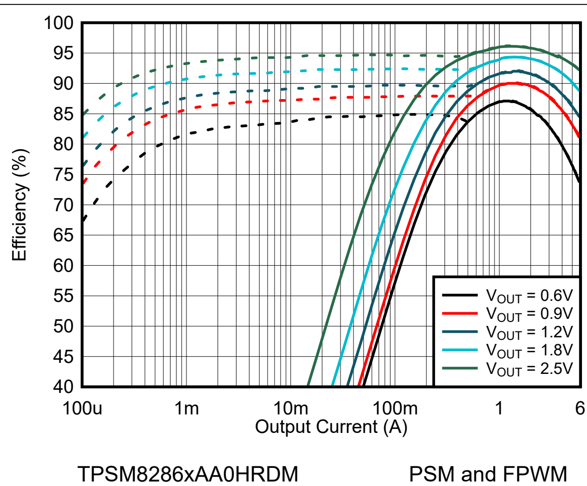


図 8-16. Efficiency V_{IN} = 3.3 V and T_A = 25°C

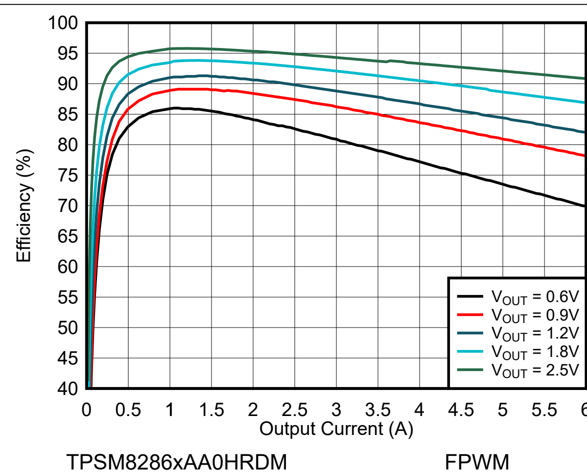


図 8-17. Efficiency V_{IN} = 3.3 V and T_A = 85°C

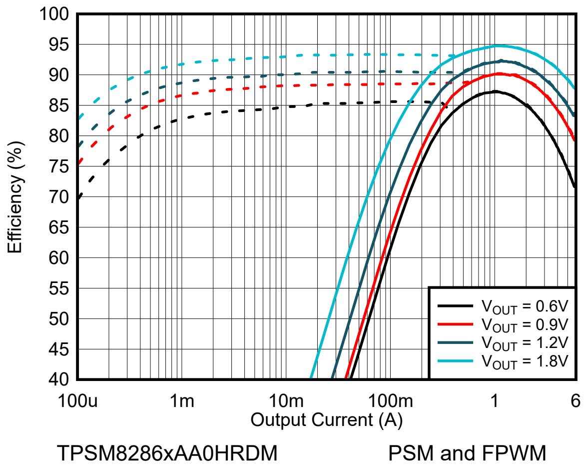


図 8-18. Efficiency V_{IN} = 2.8 V and T_A = 25°C

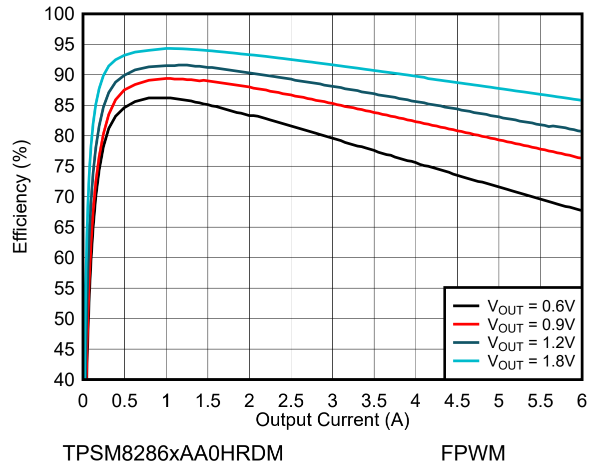


図 8-19. Efficiency V_{IN} = 2.8 V and T_A = 85°C

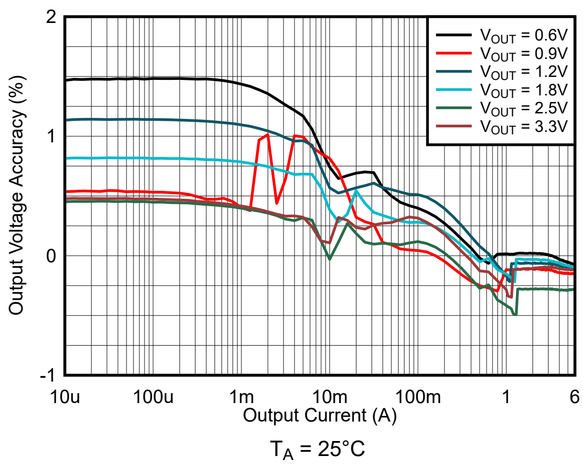


図 8-20. Load Regulation V_{IN} = 5.0 V and PSM

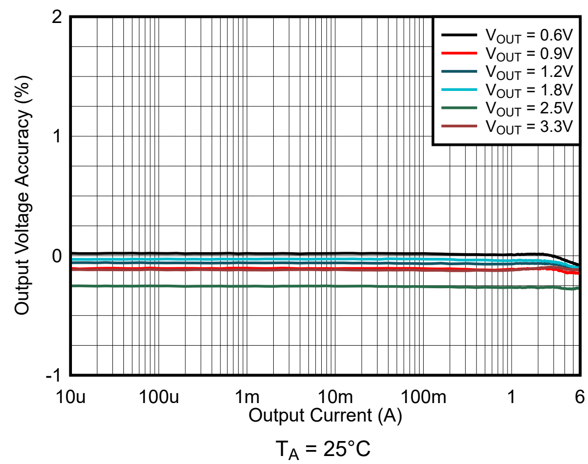


図 8-21. Load Regulation V_{IN} = 5.0 V and FPWM

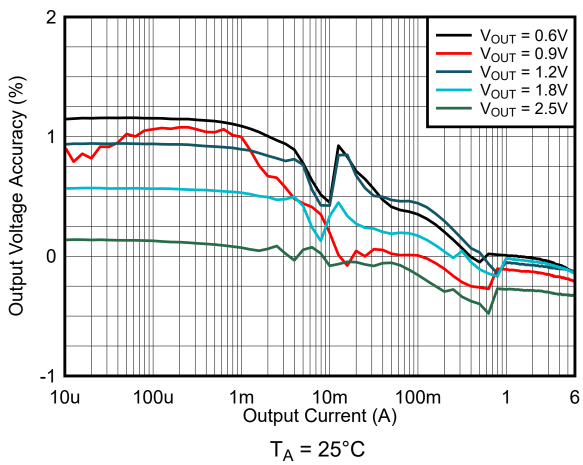


図 8-22. Load Regulation V_{IN} = 3.3 V and PSM

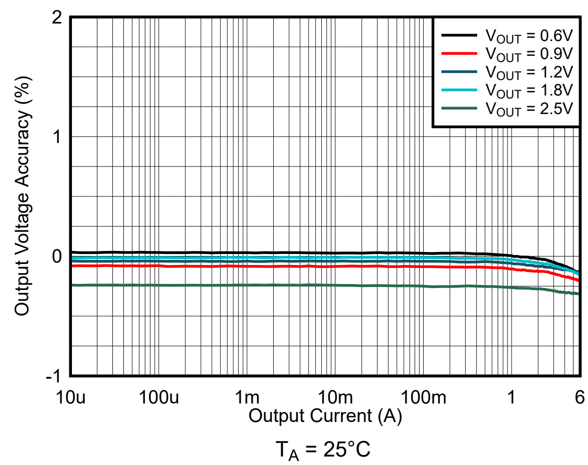
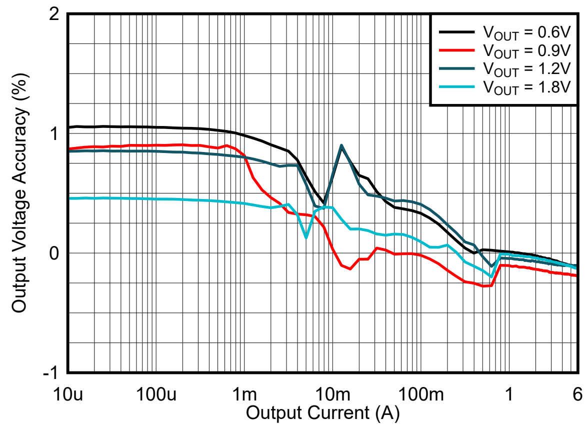
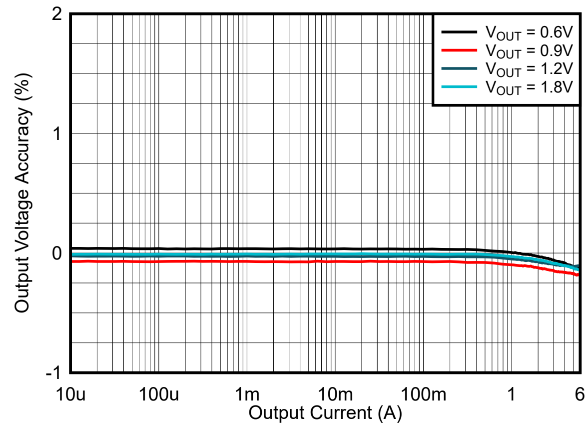


図 8-23. Load Regulation V_{IN} = 3.3 V and FPWM



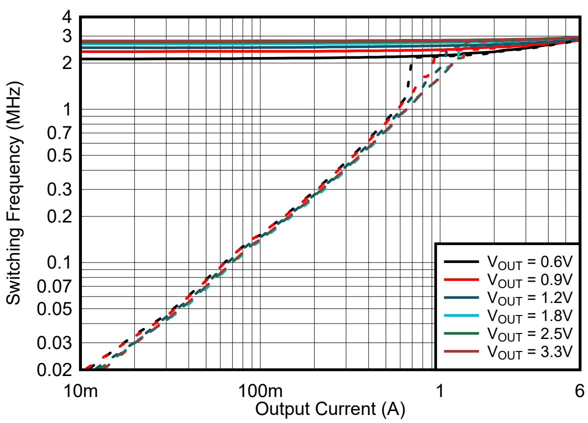
T_A = 25°C

図 8-24. Load Regulation V_{IN} = 2.8 V and PSM



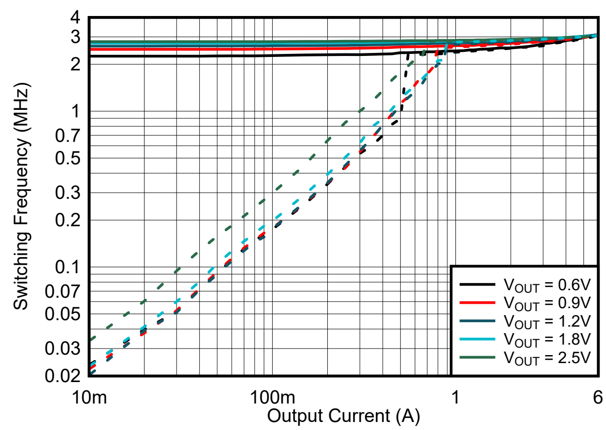
T_A = 25°C

図 8-25. Load Regulation V_{IN} = 2.8 V and FPWM



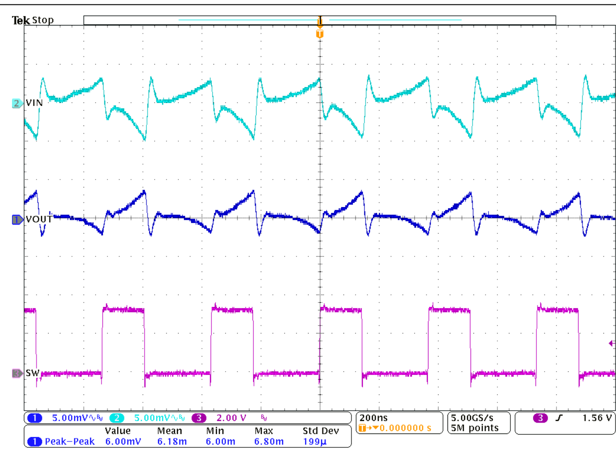
PSM and FPWM T_A = 25°C

図 8-26. Switching Frequency V_{IN} = 5.0 V



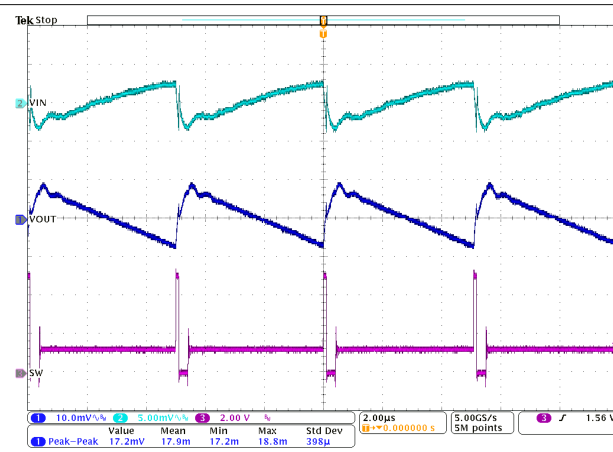
PSM and FPWM T_A = 25°C

図 8-27. Switching Frequency V_{IN} = 3.3 V



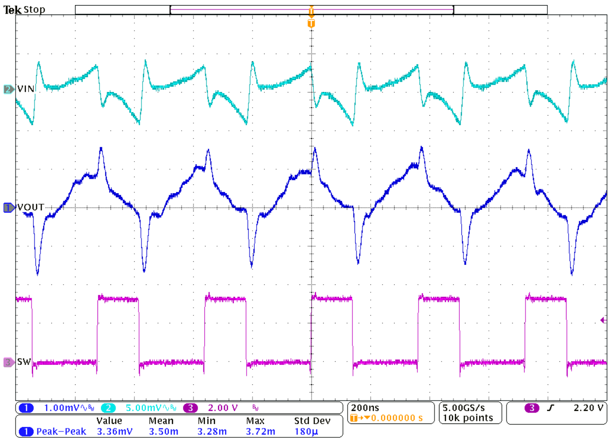
V_{IN} = 3.3 V V_{OUT} = 1.2 V C_{OUT} = 1 × 47uF

図 8-28. FPWM Operation I_{OUT} = 3 A



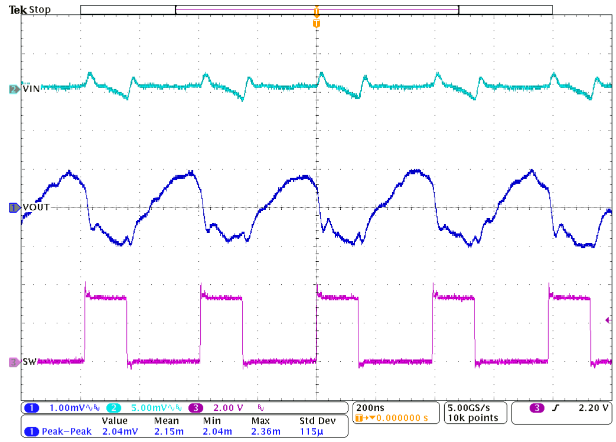
V_{IN} = 5.0 V V_{OUT} = 1.2 V C_{OUT} = 1 × 47 uF

図 8-29. PSM Operation I_{OUT} = 0.1 A



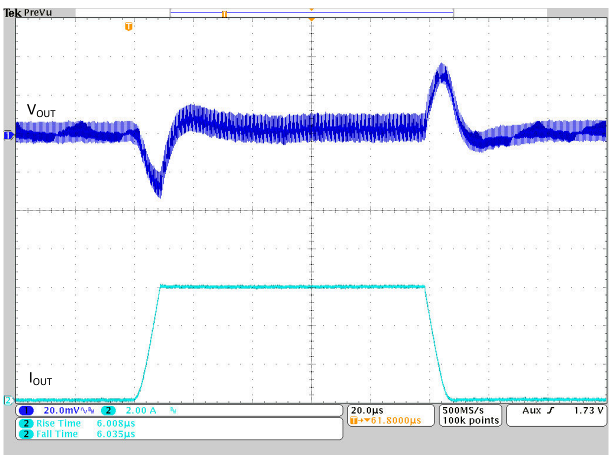
V_{IN} = 3.3 V V_{OUT} = 1.2 V C_{OUT} = 3 × 22uF

図 8-30. FPWM Operation I_{OUT} = 3 A



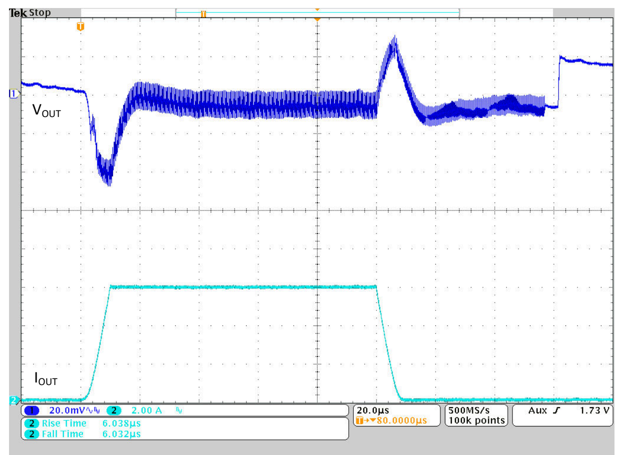
V_{IN} = 3.3 V V_{OUT} = 1.2 V C_{OUT} = 3 × 22uF

図 8-31. FPWM Operation I_{OUT} = 0.1 A



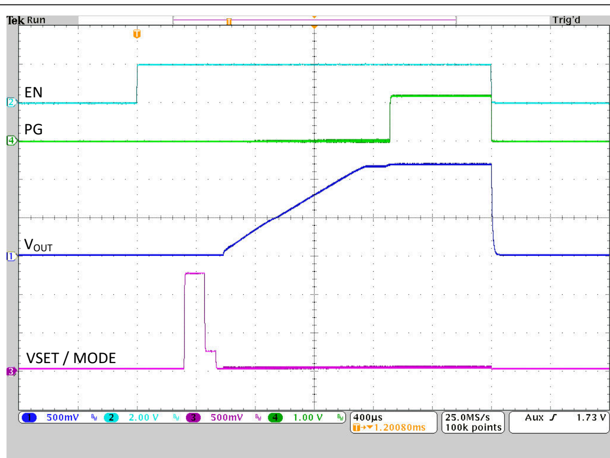
V_{IN} = 5.0 V V_{OUT} = 1.2 V C_{OUT} = 2 × 22uF

図 8-32. Load Transient FPWM I_{OUT} = 0 A → 6 A



V_{IN} = 5.0 V V_{OUT} = 1.2 V C_{OUT} = 2 × 22uF

図 8-33. Load Transient PSM I_{OUT} = 0 A → 6 A

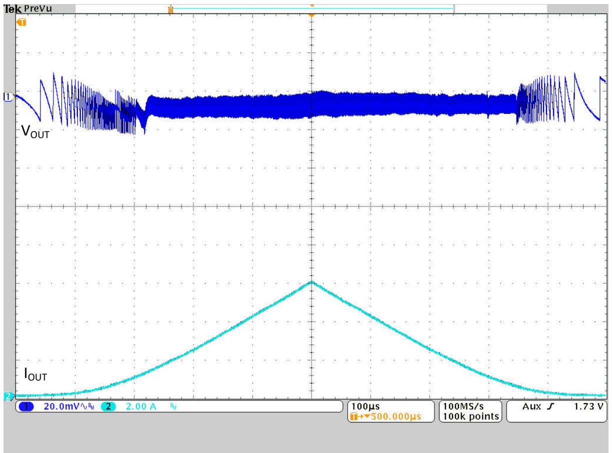


R_{VSET} = 56.2 kΩ I_{OUT} = 6.0 A

図 8-34. Start-Up into Full Load

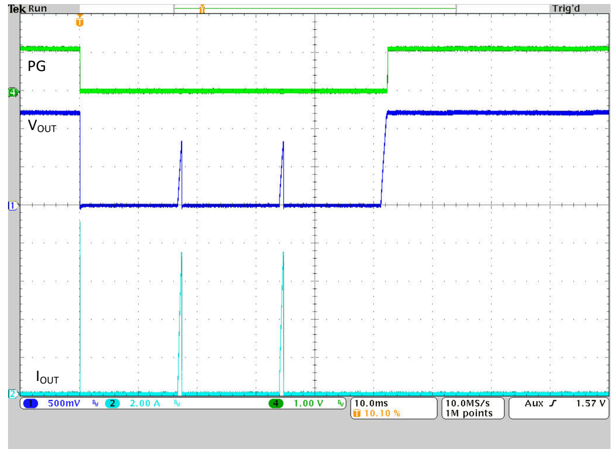
R_{VSET} = 56.2 kΩ I_{OUT} = 0 A

図 8-35. Start-Up with No Load



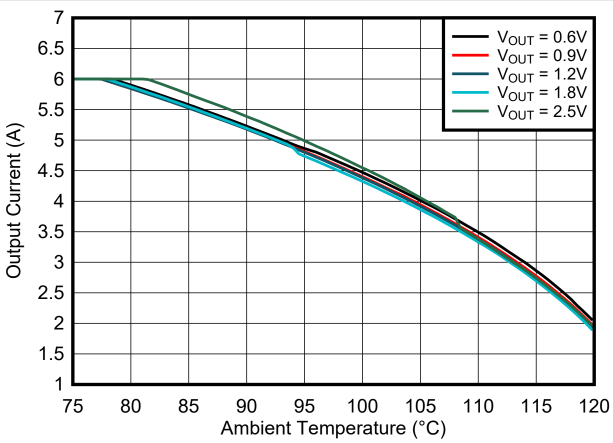
V_{IN} = 5.0 V V_{OUT} = 1.2 V C_{OUT} = 2 × 22uF

図 8-36. Load Sweep I_{OUT} = 20 mA → 6 A



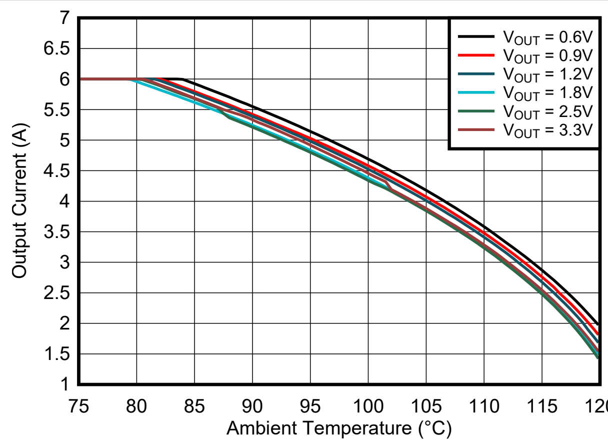
R_{LOAD} = 100 mΩ (during overload)

図 8-37. HICCUP Short-Circuit Protection



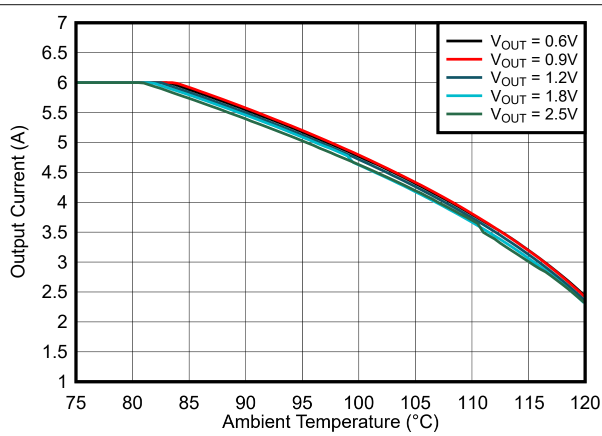
$R_{\theta JA}$ = 29.9°C/W T_{Jmax} = 125°C

図 8-38. Safe Operating Area V_{IN} = 3.3-V TPSM82866AA0PRCFR



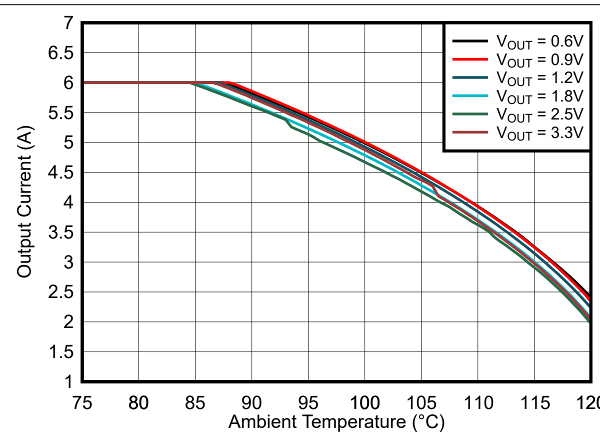
$R_{\theta JA}$ = 29.9°C/W T_{Jmax} = 125°C

図 8-39. Safe Operating Area V_{IN} = 5.0-V TPSM82866AA0PRCFR



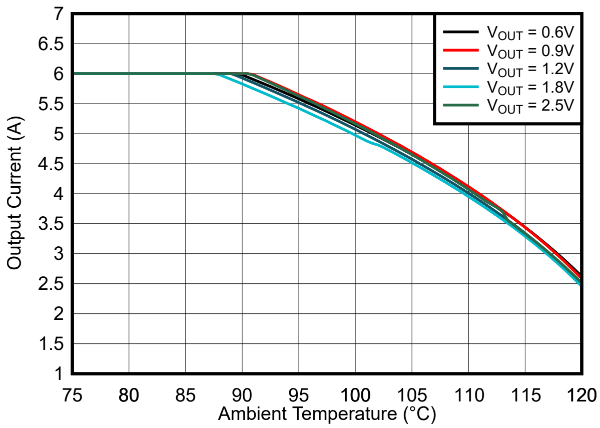
$R_{\theta JA}$ = 25.4°C/W T_{Jmax} = 125°C

図 8-40. Safe Operating Area V_{IN} = 3.3-V TPSM82866AA0SRDJR



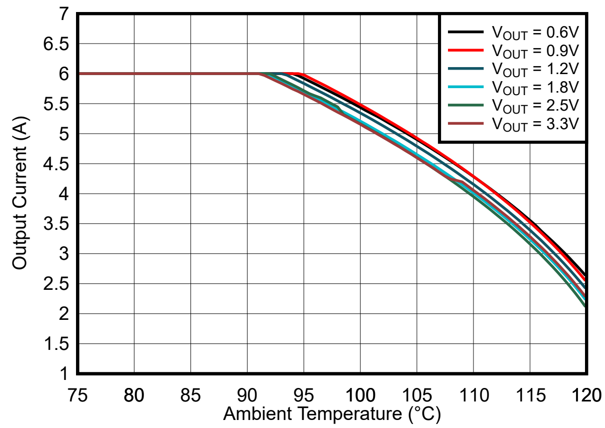
$R_{\theta JA}$ = 25.4°C/W T_{Jmax} = 125°C

図 8-41. Safe Operating Area V_{IN} = 5.0-V TPSM82866AA0SRDJR



$R_{\theta JA}$ = 25.9°C/W T_{Jmax} = 125°C

図 8-42. Safe Operating Area V_{IN} = 3.3-V TPSM82866AA0HRDMR



$R_{\theta JA}$ = 25.9°C/W T_{Jmax} = 125°C

図 8-43. Safe Operating Area V_{IN} = 5.0-V TPSM82866AA0HRDMR

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. The average input current of the TPSM8286xA is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \tag{6}$$

Make sure that the input power supply has a sufficient current rating for the application. The power supply must avoid a fast ramp down. The falling ramp speed must be slower than 10 mV/µs if the input voltage drops below V_{UVLO}.

8.4 Layout

8.4.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8286xA demands careful attention to make sure of best performance. A poor layout can lead to issues like the following:

- Bad line and load regulation
- Instability
- Increased EMI radiation
- Noise sensitivity

Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter Technical Brief* for a detailed discussion of general best practices. The following are specific recommendations for the TPSM8286xA:

- Place the input capacitor as close as possible to the VIN and PGND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and PGND pins avoiding vias.
- Place the output capacitor close to the VOUT and PGND pins and route directly avoiding vias.
- Place the FB resistors R1 and R2 close to the FB and AGND pins and place R4 close to the VSET/MODE pin to minimize noise pickup.
- The sense traces connected to the VOS pin is a signal trace. Take special care to avoid noise being induced. Keep the trace away from SW.
- To improve thermal performance, use GND vias under the exposed thermal pad. Directly connect the AGND and PGND pins to the exposed thermal pad with copper on the top PCB layer.

- Refer to 図 8-44 and 図 8-45 for an example of component placement, routing, and thermal design.
- The recommended land pattern for the TPSM8286xA is shown at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD) when some pins (such as VIN, VOUT, and PGND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

8.4.2 Layout Examples

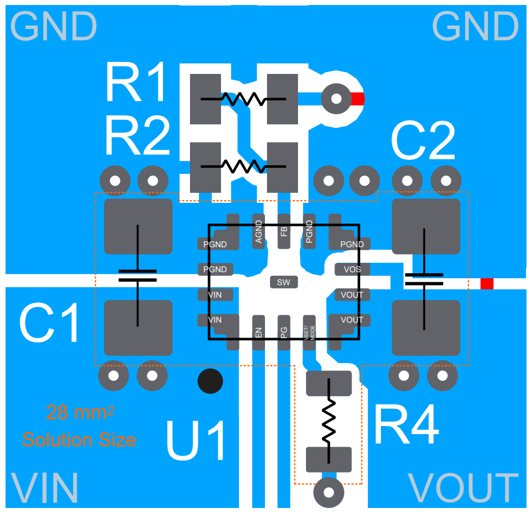


図 8-44. Layout Example RCF package

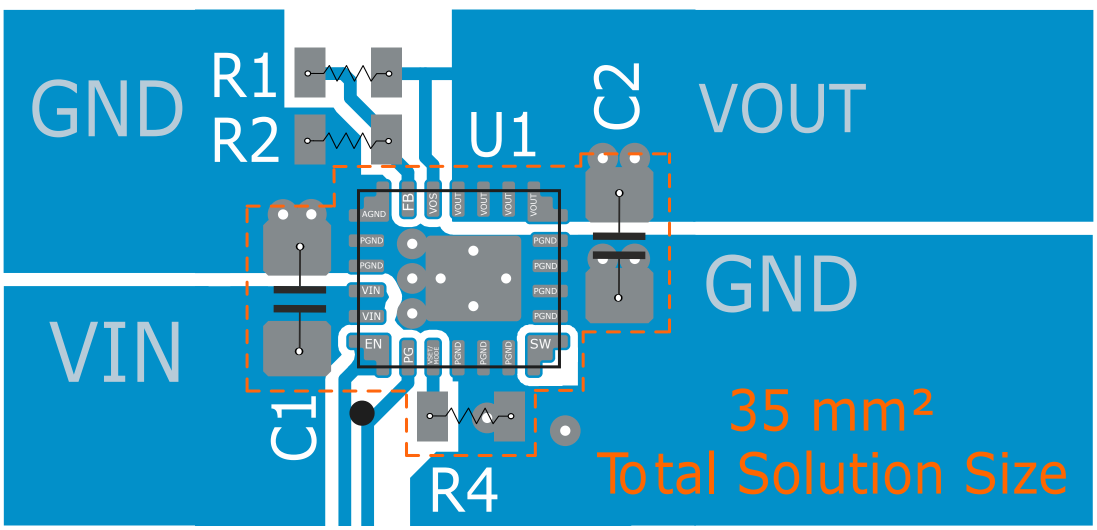


図 8-45. Layout Example RDJ and RDM package

8.4.2.1 Thermal Considerations

The TPSM8286xA power module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM8286xA, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the thermal resistance. Using this method to compute the maximum device temperature, the Safe Operating Area (SOA) graphs demonstrate the required derating in maximum output current at high ambient temperatures. For more details on how to use the thermal parameters in real applications, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report* and *Semiconductor and IC Package Thermal Metrics Application Report*.

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs Application Report*
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics Application Report*
- Texas Instruments, *Benefits of a Resistor-to-Digital Converter in Ultra-Low Power Supplies White Paper*
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter Technical Brief*
- Texas Instruments, *Simplify Low EMI Design With Power Modules White Paper*

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.5 Trademarks

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9.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (June 2024) to Revision D (November 2024) **Page**

- Changed TPSM82866AA0PRCFR from Advance Information to Production Data... 3

Changes from Revision B (November 2022) to Revision C (June 2024) **Page**

- Added TPSM82864AA0PRCFR (preview), TPSM82864BA0PRCFR (preview), TPSM82866AA0PRCFR (advance information), and TPSM82866BA0PRCFR (preview) to the data sheet.. 3

11 Mechanical, Packaging, and Orderable Information

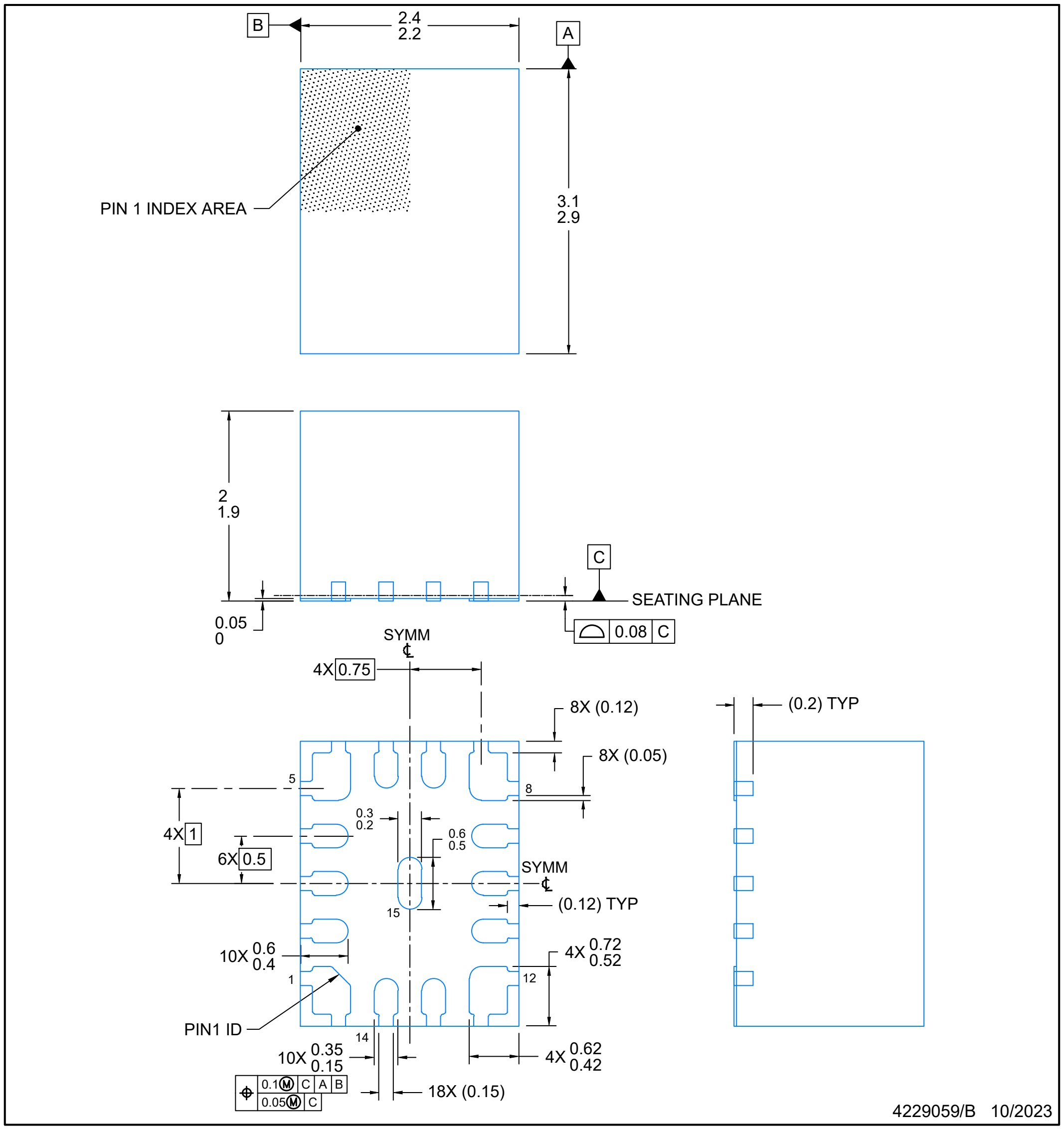
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RCF0015A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



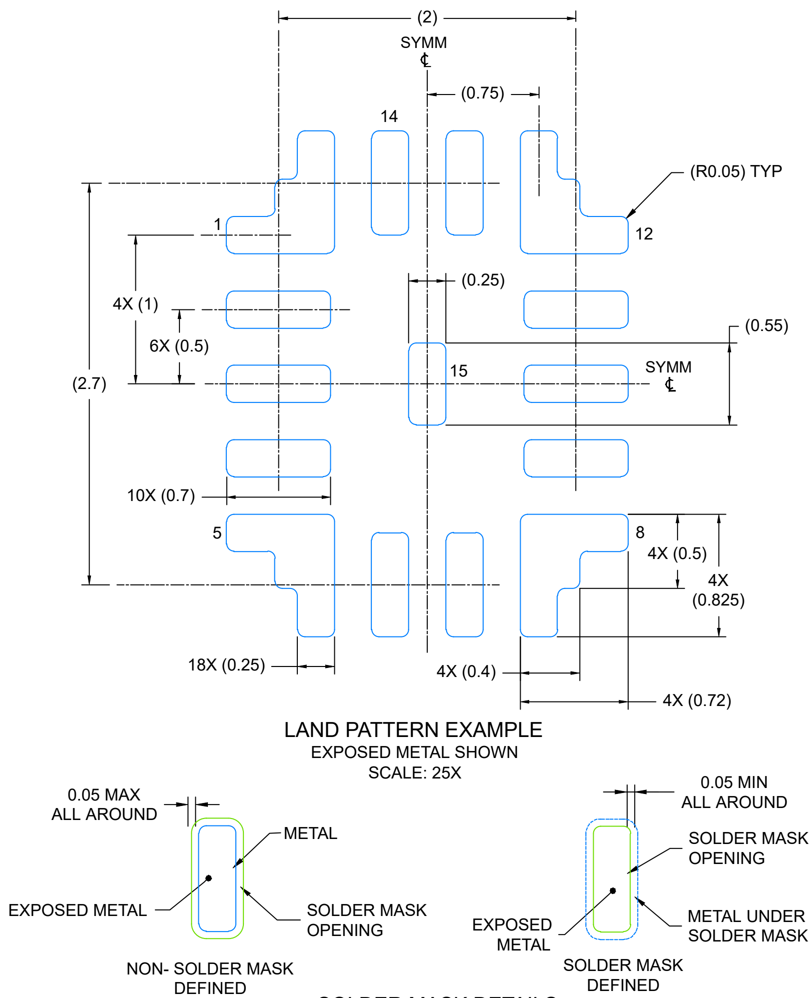
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RCF0015A **QFN-FCMOD - 2 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

SOLDER MASK DETAILS

4229059/B 10/2023

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

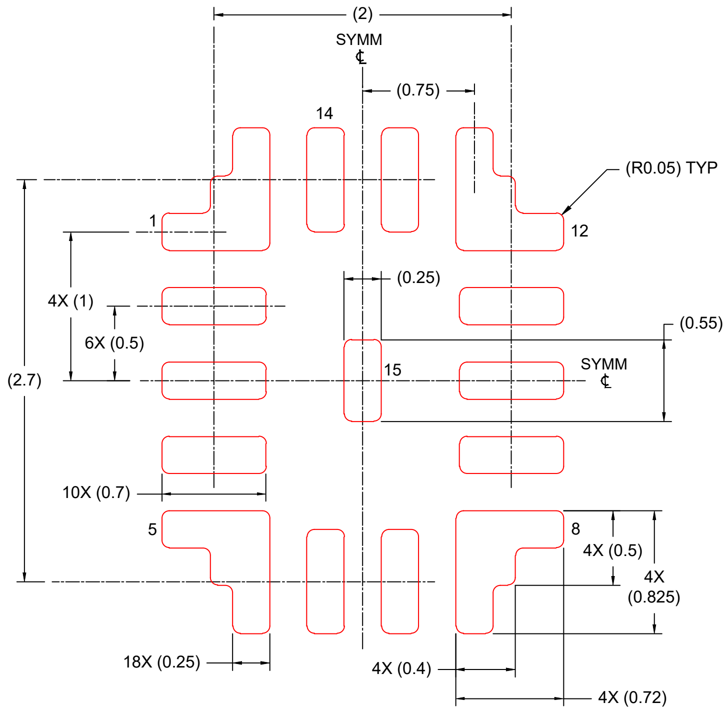
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE STENCIL DESIGN

RCF0015A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

4229059/B 10/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
M8864AA0SRDJRG4	Active	Production	B0QFN (RDJ) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM864AA0S
M8864AA0SRDJRG4.A	Active	Production	B0QFN (RDJ) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM864AA0S
M8866AA0HRDMRG4	Active	Production	B0QFN (RDM) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM866AA0H
M8866AA0HRDMRG4.A	Active	Production	B0QFN (RDM) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM866AA0H
M8866AA0SRDJRG4	Active	Production	B0QFN (RDJ) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM866AA0S
M8866AA0SRDJRG4.A	Active	Production	B0QFN (RDJ) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM866AA0S
TPSM82864AA0HRDMR	Active	Production	B0QFN (RDM) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM864AA0H
TPSM82864AA0HRDMR.A	Active	Production	B0QFN (RDM) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM864AA0H
TPSM82864AA0SRDJR	Active	Production	B0QFN (RDJ) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM864AA0S
TPSM82864AA0SRDJR.A	Active	Production	B0QFN (RDJ) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM864AA0S
TPSM82866AA0HRDMR	Active	Production	B0QFN (RDM) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM866AA0H
TPSM82866AA0HRDMR.A	Active	Production	B0QFN (RDM) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM866AA0H
TPSM82866AA0PRCFR	Active	Production	QFN-FCMOD (RCF) | 15	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	T8866A
TPSM82866AA0PRCFR.A	Active	Production	QFN-FCMOD (RCF) | 15	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	T8866A
TPSM82866AA0PRCFR.B	Active	Production	QFN-FCMOD (RCF) | 15	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPSM82866AA0SRDJR	Active	Production	B0QFN (RDJ) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM866AA0S
TPSM82866AA0SRDJR.A	Active	Production	B0QFN (RDJ) | 23	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TM866AA0S
XPSM82866AA0PRCFR	Active	Preproduction	QFN-FCMOD (RCF) | 15	2500 | LARGE T&R	-			-40 to 125	
XPSM82866AA0PRCFR.A	Active	Preproduction	QFN-FCMOD (RCF) | 15	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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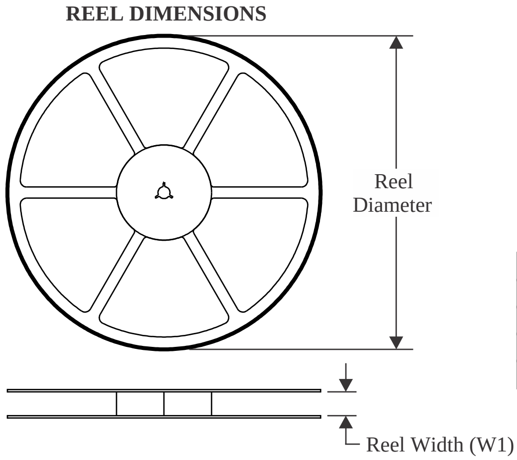
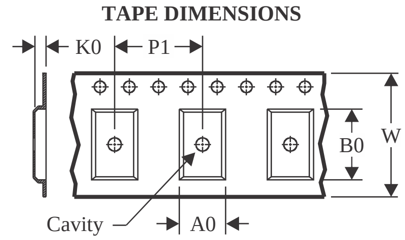
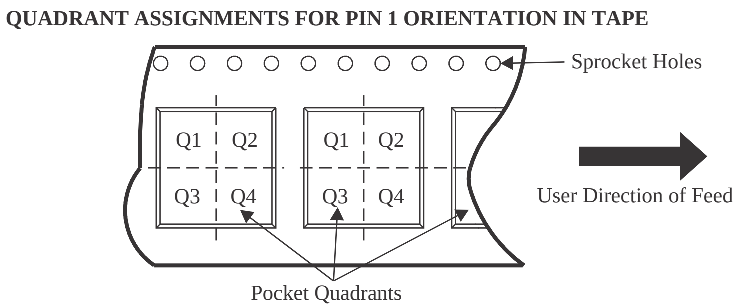
TAPE AND REEL INFORMATION





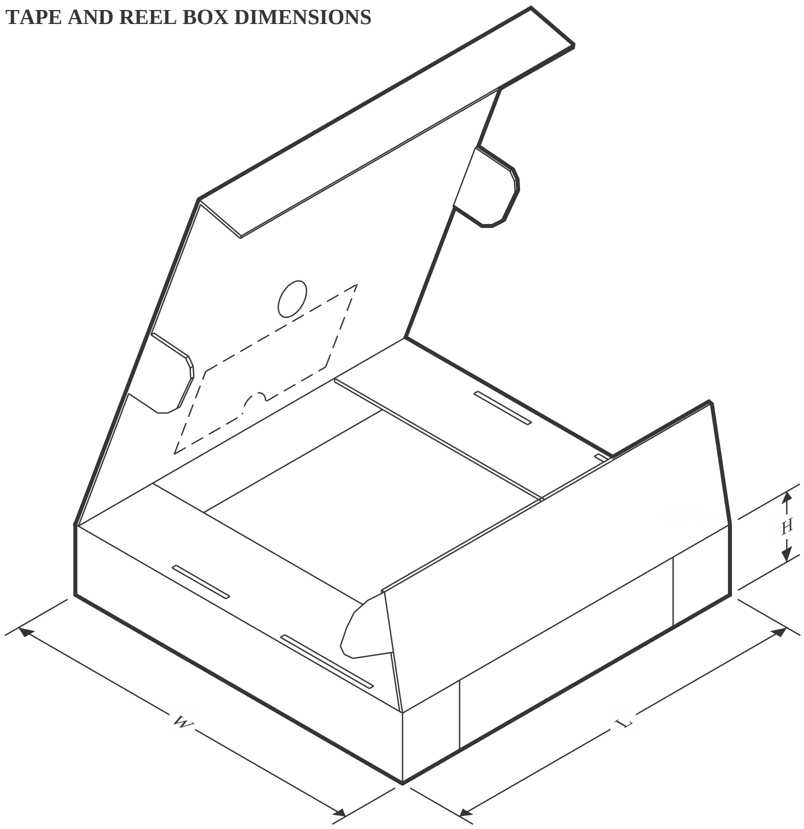
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

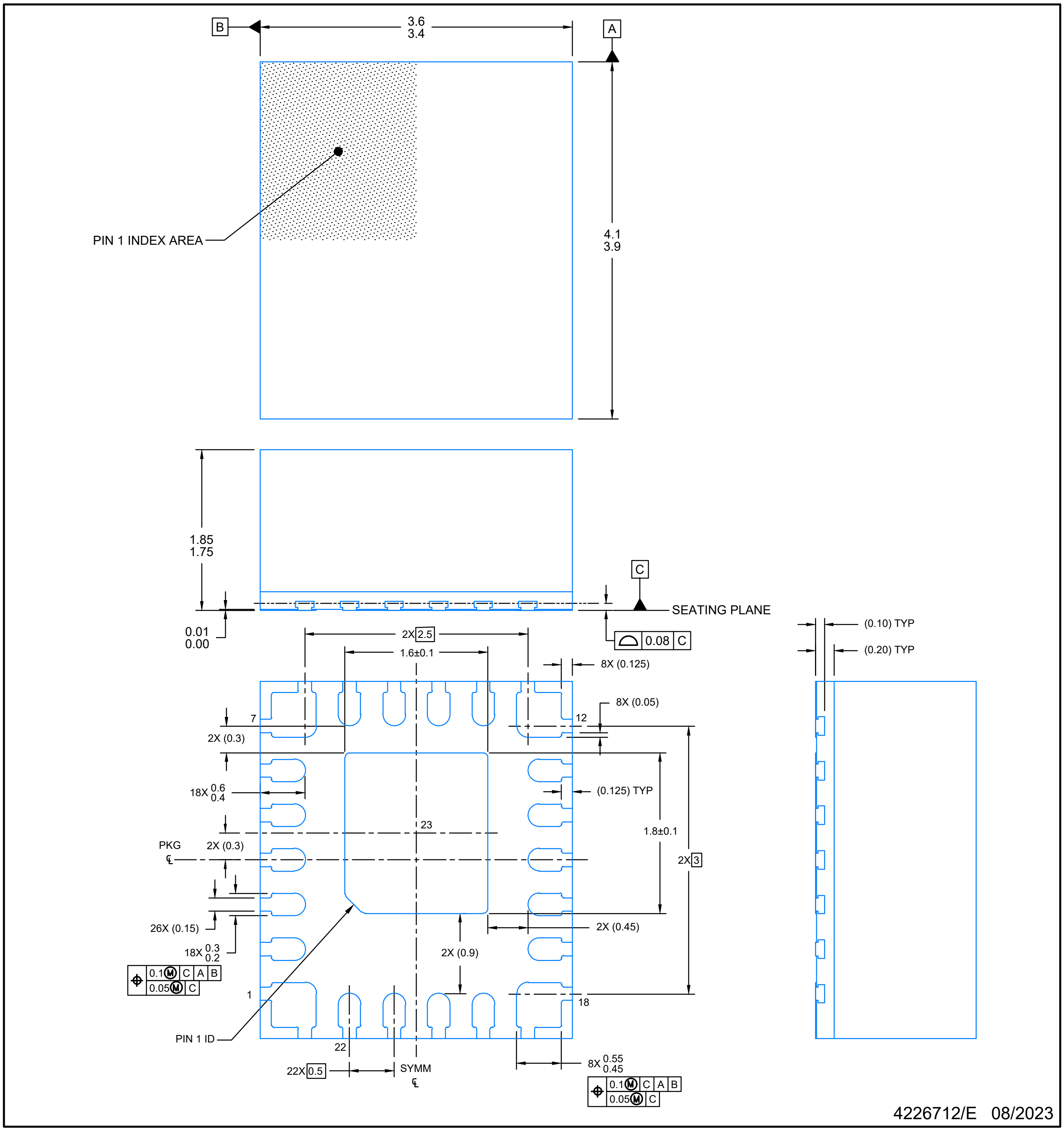
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
M8864AA0SRDJRG4	B0QFN	RDJ	23	3000	330.0	17.6	3.8	4.3	2.0	8.0	12.0	Q1
M8866AA0HRDMRG4	B0QFN	RDM	23	3000	330.0	17.6	3.8	4.3	2.0	8.0	12.0	Q1
M8866AA0SRDJRG4	B0QFN	RDJ	23	3000	330.0	17.6	3.8	4.3	2.0	8.0	12.0	Q1
TPSM82864AA0HRDMR	B0QFN	RDM	23	3000	330.0	17.6	3.8	4.3	2.0	8.0	12.0	Q1
TPSM82864AA0SRDJR	B0QFN	RDJ	23	3000	330.0	17.6	3.8	4.3	2.0	8.0	12.0	Q1
TPSM82866AA0HRDMR	B0QFN	RDM	23	3000	330.0	17.6	3.8	4.3	2.0	8.0	12.0	Q1
TPSM82866AA0PRCFR	QFN-FCMOD	RCF	15	2500	330.0	12.4	2.6	3.3	2.2	8.0	12.0	Q1
TPSM82866AA0SRDJR	B0QFN	RDJ	23	3000	330.0	17.6	3.8	4.3	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



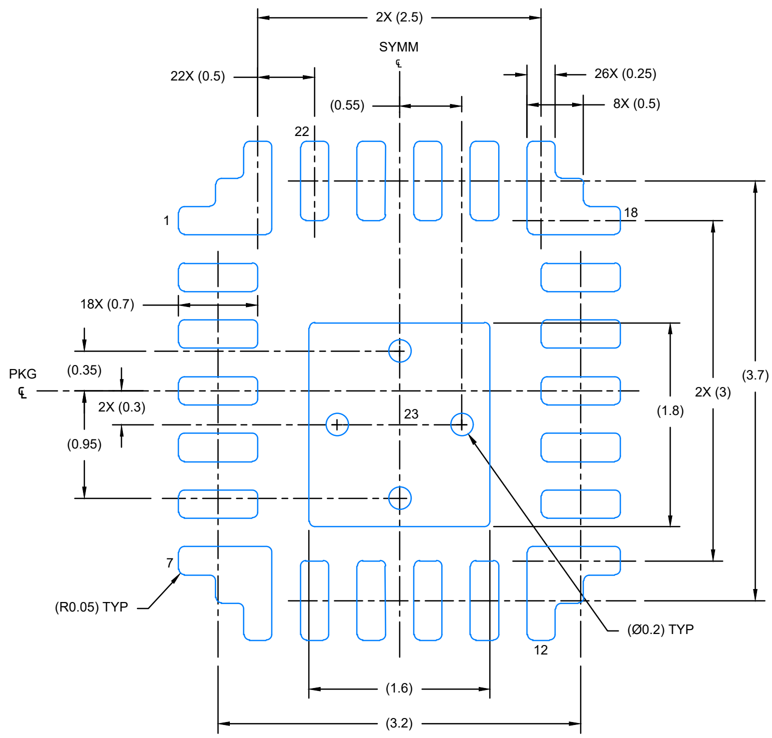
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
M8864AA0SRDJRG4	B0QFN	RDJ	23	3000	336.0	336.0	48.0
M8866AA0HRDMRG4	B0QFN	RDM	23	3000	336.0	336.0	48.0
M8866AA0SRDJRG4	B0QFN	RDJ	23	3000	336.0	336.0	48.0
TPSM82864AA0HRDMR	B0QFN	RDM	23	3000	336.0	336.0	48.0
TPSM82864AA0SRDJR	B0QFN	RDJ	23	3000	336.0	336.0	48.0
TPSM82866AA0HRDMR	B0QFN	RDM	23	3000	336.0	336.0	48.0
TPSM82866AA0PRCFR	QFN-FCMOD	RCF	15	2500	367.0	367.0	35.0
TPSM82866AA0SRDJR	B0QFN	RDJ	23	3000	336.0	336.0	48.0

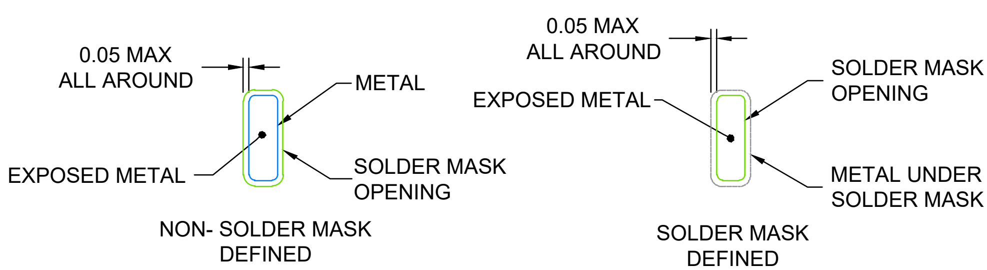


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

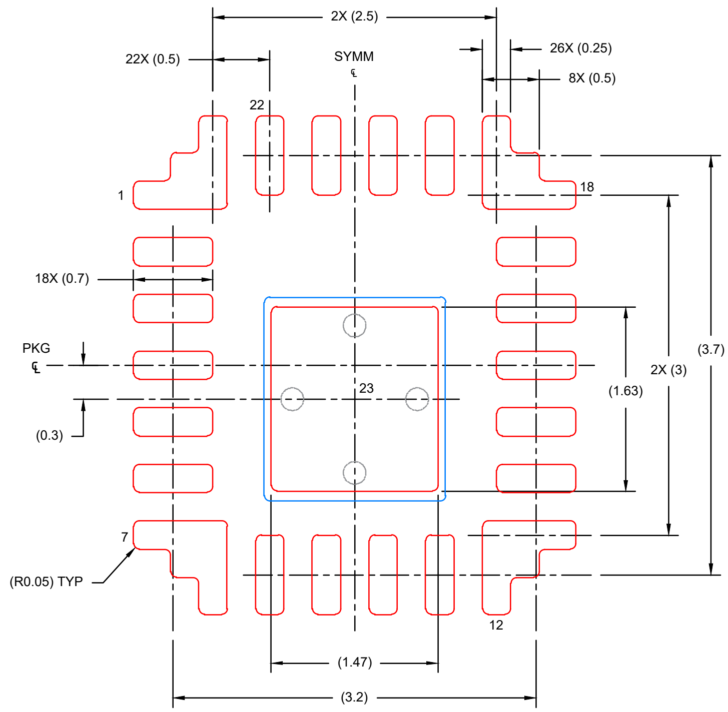


SOLDER MASK DETAILS

4226712/E 08/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

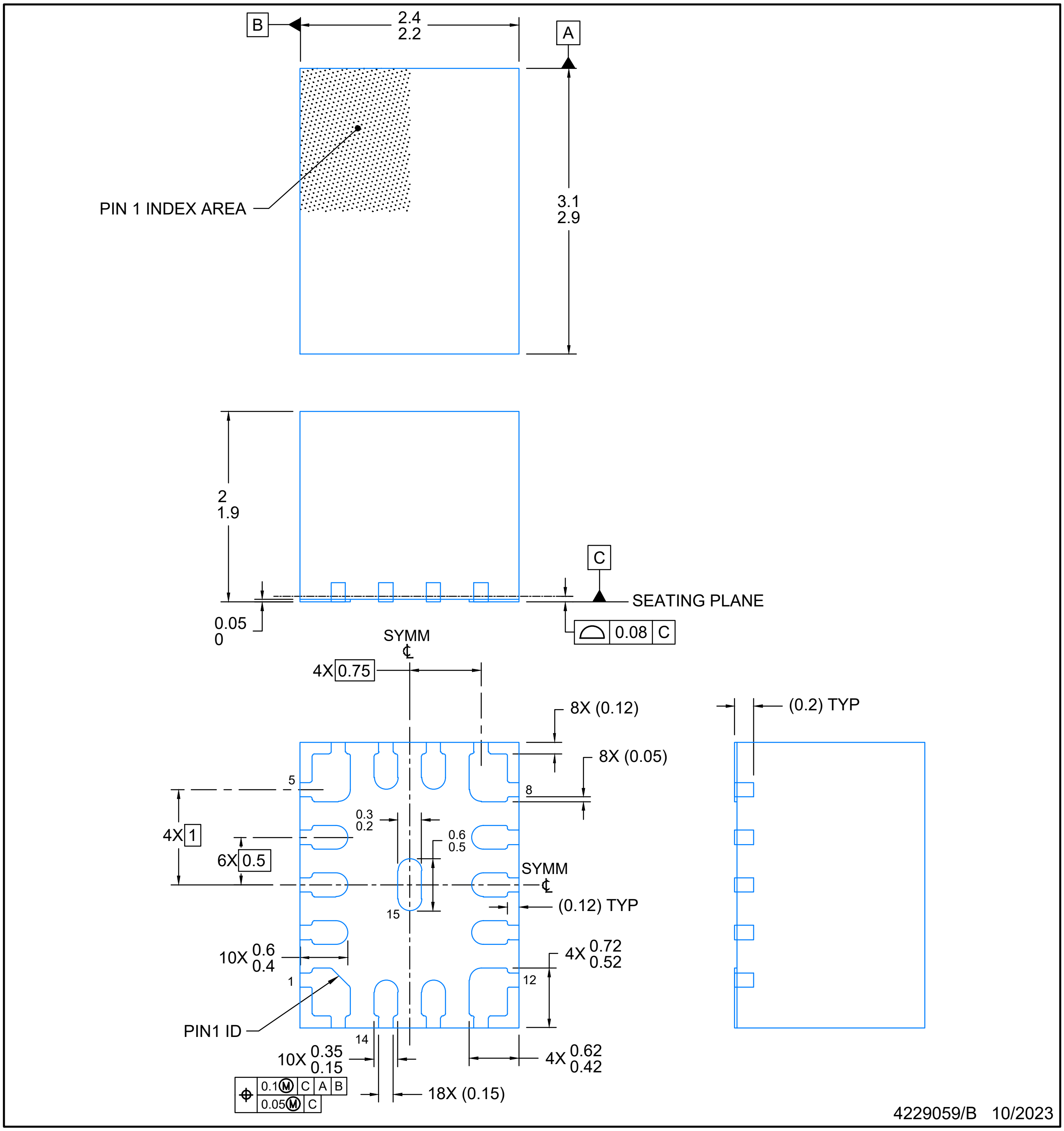
EXPOSED PAD:
83% PRINTED SOLDER COVERAGE BY AREA

SCALE: 15X

4226712/E 08/2023

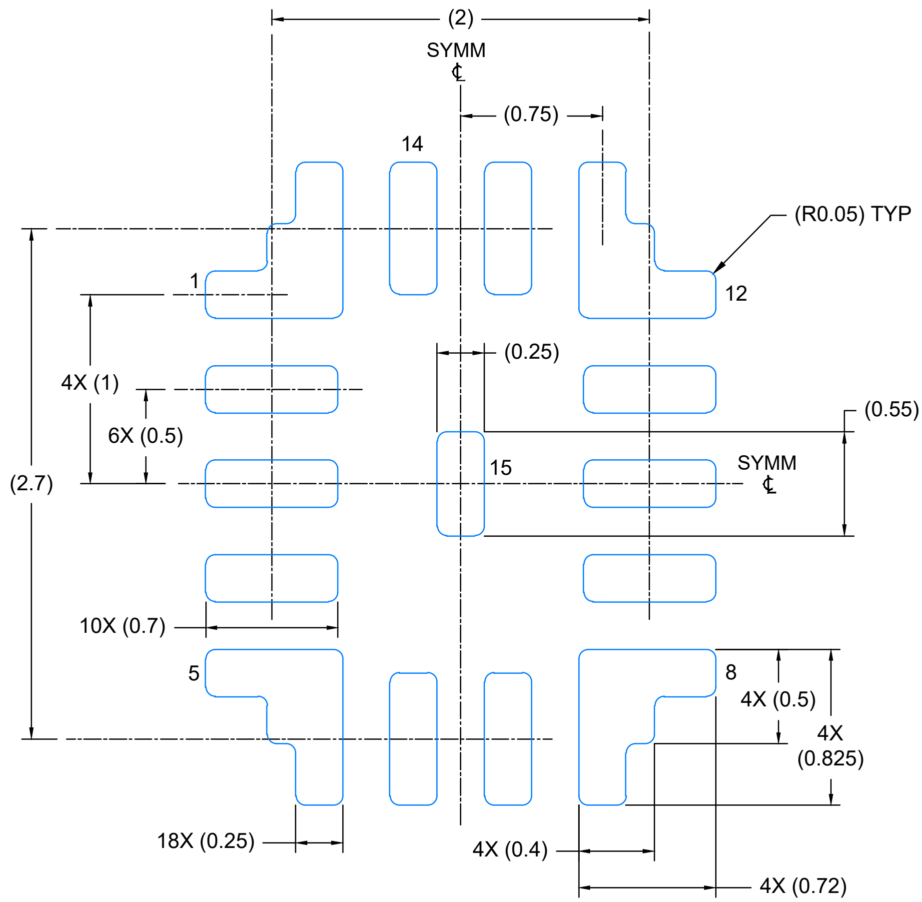
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

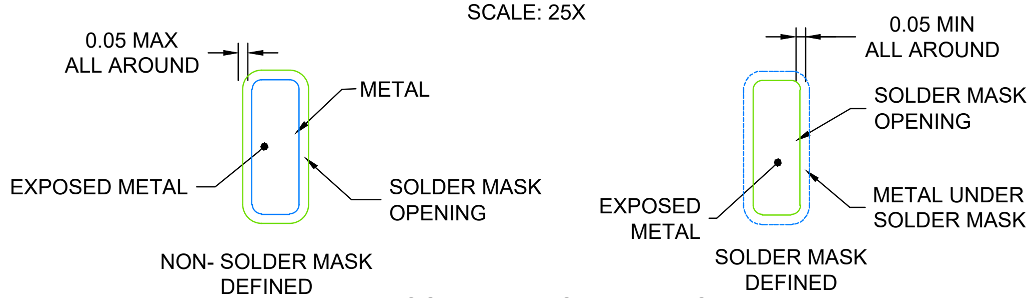


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

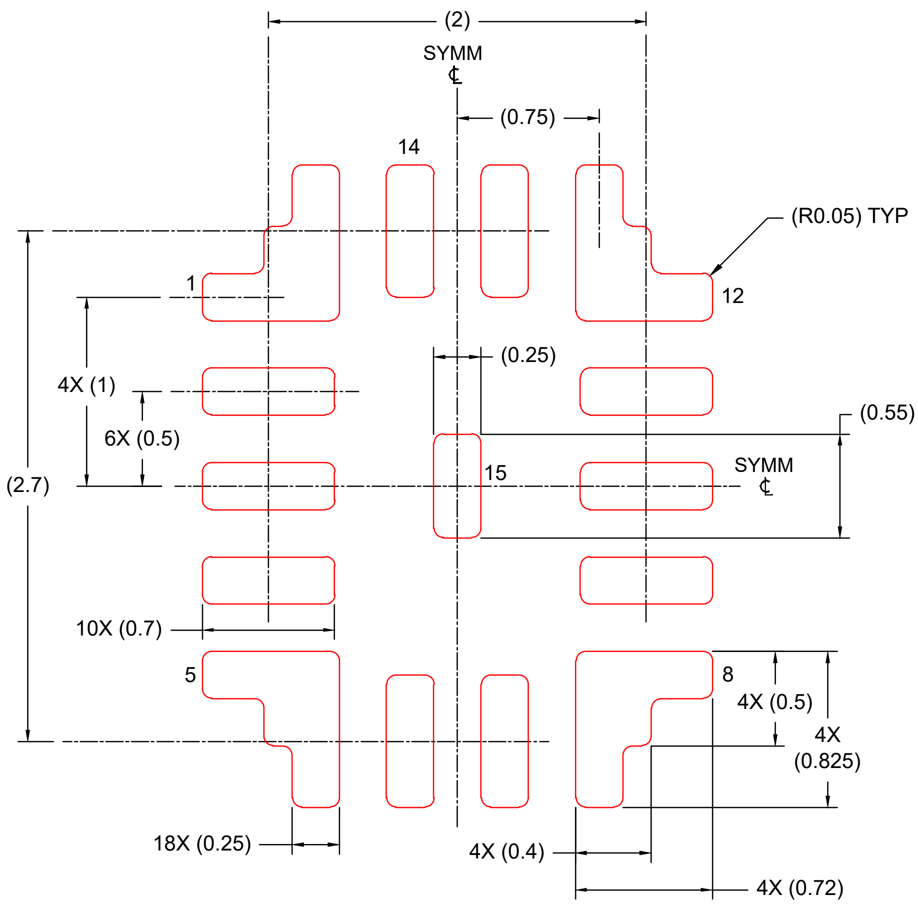


SOLDER MASK DETAILS

4229059/B 10/2023

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

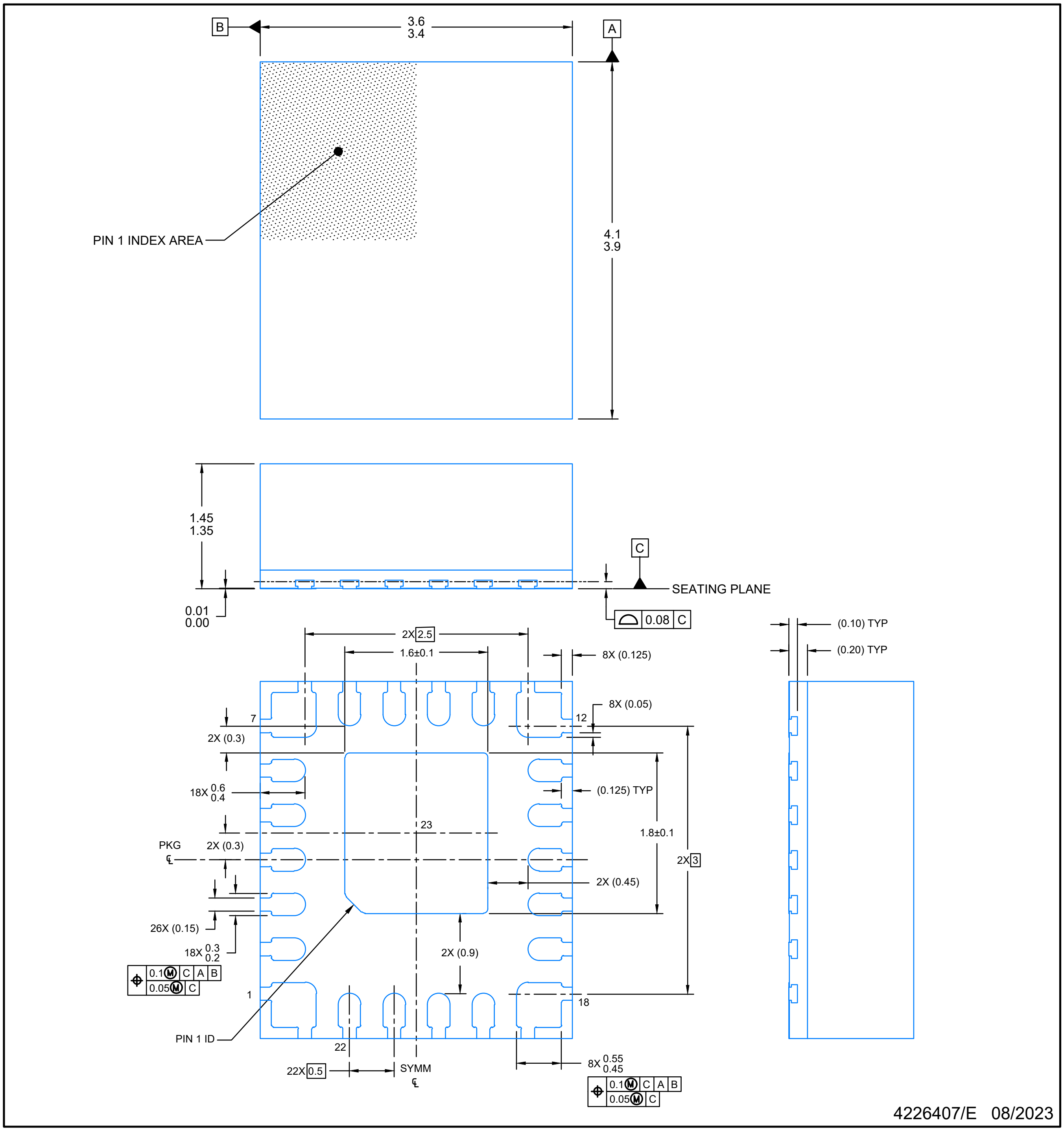


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

4229059/B 10/2023

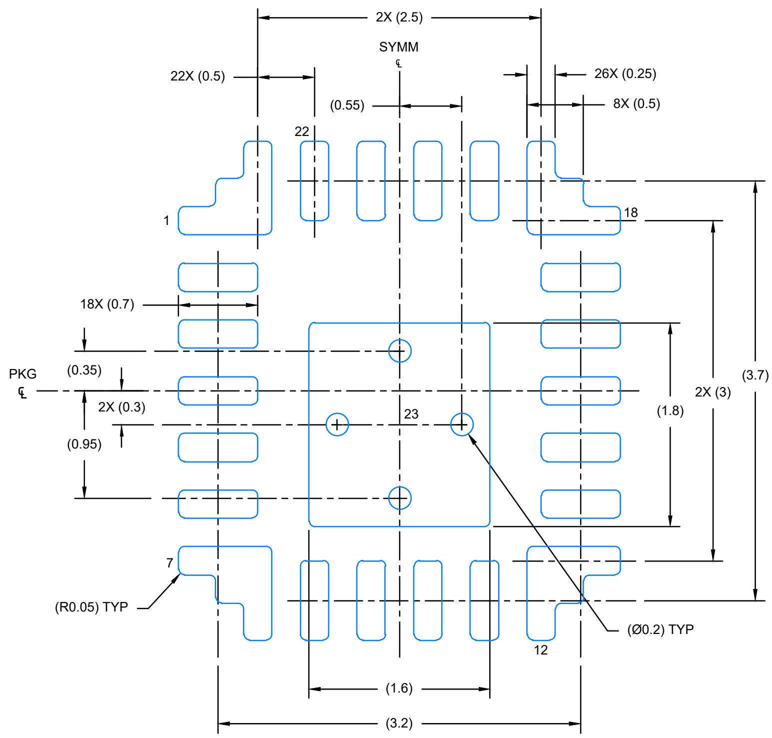
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

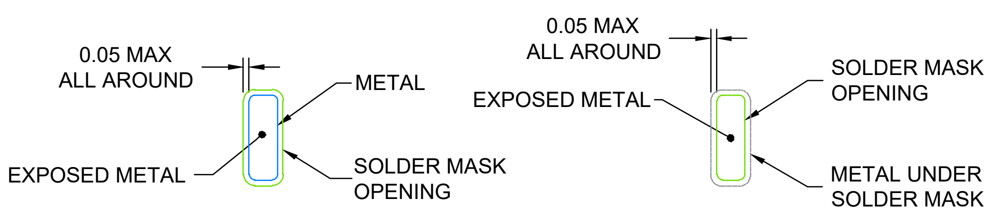


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON- SOLDER MASK DEFINED

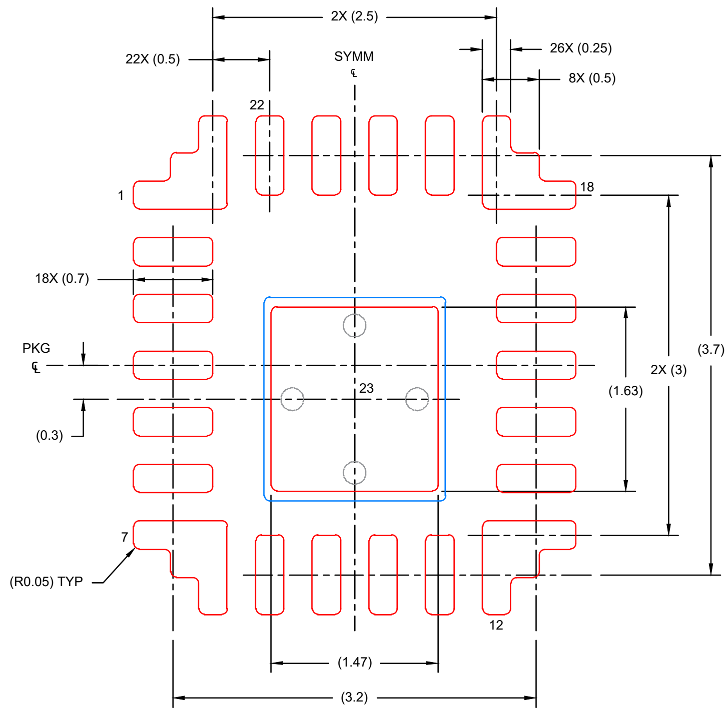
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4226407/E 08/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD:
83% PRINTED SOLDER COVERAGE BY AREA

SCALE: 15X

4226407/E 08/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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