TEXAS INSTRUMENTS
TPSM86637, TPSM86638
JAJSTV6 – MAY 2024

TPSM8663x 4.5V～28V 入力、6A 同期整流降圧パワー モジュール

1 特長

- 入力電圧範囲:4.5V～28V
- 出力電圧範囲:0.6V ～ 13V
- 6A の連続出力電流に対応できる能力
- MOSFET、インダクタ、基本的なパッシブ部品を内蔵
- 25℃で 0.6V ±1% の基準電圧
- D-CAP3™ 制御モードによる高速過渡応答
- TPSM86838 は、出力リップルが小さい疑似固定周波数向け FCCM 搭載
- TPSM86837 は、軽負荷時の高効率を実現する Eco-mode 搭載
- SS コンデンサによる可変ソフト スタート時間
- 出力放電機能を内蔵
- 800kHz と 1200kHz のスイッチング周波数を選択可能
- パワー グッド インジケータにより出力電圧を監視
- 最高 98% デューティの動作をサポート
- ラッチなしの UV、OV、OT、UVLO 保護
- 動作時接合部温度:-40℃～+150℃
- 19 ピン、5.0mm × 5.5mm の QFN HotRod™ パッケージ

2 アプリケーション

- 産業用アプリケーション:医療用アプリケーション、ファクトリ オートメーションおよび制御 (IPC、ロボット)、試験および測定機器、プロ オーディオ ビデオ
- 12V、19V、24V パワー バス アプリケーション向けのスペースに制約のある POL

3 概要

TPSM8663x は、高効率で高電圧入力に対応した、使いやすい同期整流降圧パワー モジュールです。このデバイスが搭載しているのは、複数のパワー MOSFET、1 個のシールド付きインダクタ、いくつかの基本的な受動部品であり、設計サイズの最小化に役立ちます。

動作入力電圧範囲が 4.5V～28V と広いため、このデバイスは 12V、19V、24V の電源バス レールで電力供給するシステムの優れた選択肢です。TPSM8663x は、0.6V～13V の出力電圧で、最大 6A の連続出力電流をサポートします。

TPSM8663x は DCAP3 制御モードを使用して高速な過渡応答と優れたラインおよび負荷レギュレーションを実現し、かつ外部補償を必要としません。MLCC などの等価直列抵抗 (ESR) の低い出力コンデンサにも対応しています。

TPSM86638 は、軽負荷時に強制連続導通モード (FCCM) で動作し、あらゆる負荷条件において出力リップルを低減します。TPSM86637 は Eco-mode で動作し、軽負荷時に高い効率を実現します。

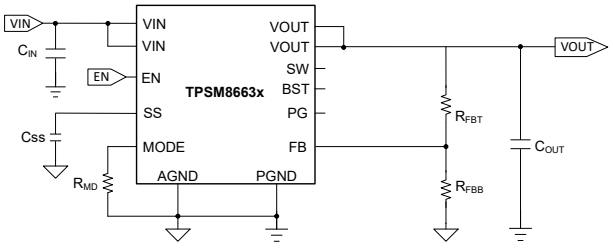
TPSM8663x は完全なラッチなしの OV (過電圧)、UV (低電圧)、OC (過電流)、OT (過熱)、UVLO (低電圧誤動作防止) 保護機能に加え、パワー グッド インジケータ、出力放電機能も搭載しています。

TPSM8663x は、19 ピンの 5.0mm × 5.5mm HotRod QFN パッケージで供給され、-40℃～150℃の接合部温度で動作が規定されています。

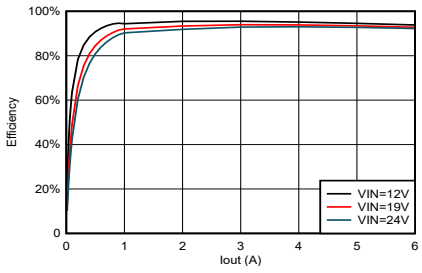
製品情報

部品番号	モード	パッケージとパッケージ サイズ (1) (2)
TPSM86638	FCCM	RCG (B3QFN、19)、5.0mm × 5.5mm
TPSM86637	ECO	

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



TPSM86638 効率、Vout = 5V、Fsw = 800kHz

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4 Pin Configuration and Functions

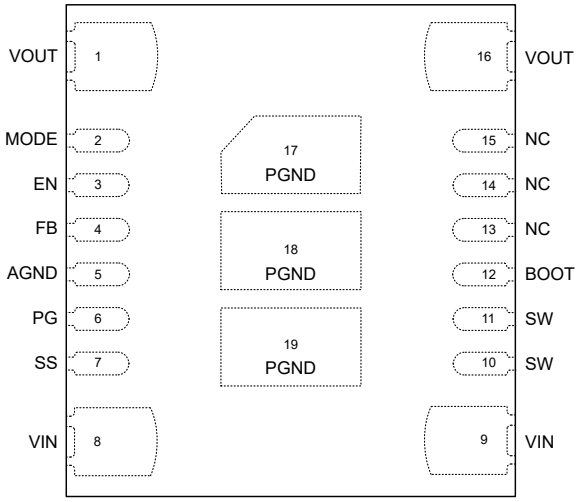


図 4-1. 19-Pin B3QFN RCG Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VOUT	1, 16	O	Output voltage. These pins are connected to the internal buck inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
MODE	2	I	Switching frequency selection pin. Connect this pin to a resistor to AGND for different switching frequency options shown in 表 6-1.
EN	3	I	Enable input control. Driving EN high or leaving this pin floating enables the module. A resistor divider can be used to imply an UVLO function.
FB	4	I	Feedback input. Connect the midpoint of the feedback resistor divider to this pin. Connect the upper resistor (RFBT) of the feedback divider to VOUT at the desired point of regulation. Connect the lower resistor (RFBB) of the feedback divider to AGND. Do not leave open or connect to ground.
AGND	5	G	Ground of internal analog circuitry. Connect AGND to PGND plane at a single point.
PG	6	O	Open-drain power-good monitor output that asserts low if the output voltage is out of PG threshold due to overvoltage, undervoltage, thermal shutdown, EN shutdown, or during soft start.
SS	7	I	Soft-start time selection pin. Connecting an external capacitor to AGND to set the soft-start time. A minimum 22nF ceramic capacitor must be connected at this pin, which sets the minimum soft-start time to approximately 2.2ms. Do not float.
VIN	8, 9	P	Input supply voltage. A 100nF input capacitor is internally connected from this pin to PGND within the module. Externally, connect input capacitors between these pins and PGND in close proximity to the device.
SW	10, 11	O	Switching node. *Do not place any external component on this pin or connect to any signal.* The amount of copper placed on this pin must be kept to a minimum to prevent issues with noise and EMI.
BOOT	12	I/O	Bootstrap pin for the internal high-side gate driver. A 100nF bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage. *Do not place any external component on this pin or connect to any signal.*
NC	13, 14, 15	—	No connection. Tie to GND for better thermal performance.
PGND	17, 18, 19	G	Power ground. This pin is the return current path for the power stage of the device. Connect these pads to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins.

(1) I = input, O = output, G = ground, P = power

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	32	V
	BOOT	–0.3	SW + 6	V
	BOOT-SW	–0.3	6	V
	EN, FB, MODE	–0.3	6	V
	PGND, AGND	–0.3	0.3	V
Output voltage	SW	–2	32	V
	SW (< 10ns transient)	–5	35	V
	PG	–0.3	6	V
Mechanical vibration	MIL-STD-883D, Method 2007.2, 20Hz to 2kHz		20	G
Mechanical shock	MIL-STD-883D, Method 2002.3, 1ms, 1/2 sine, mounted		500	G
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	4.5		28	V
	BOOT	–0.1		SW + 5.5	V
	BOOT-SW	–0.1		5.5	V
	EN, FB, MODE	–0.1		5.5	V
	PGND, AGND	–0.1		0.1	V
Output voltage	SW	–1		28	V
	PG	–0.1		5.5	V
Operating junction temperature, T_J		–40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPSM8663x RCG (B3QFN) 19 PINS	UNIT
Eff $R_{\theta JA}$	Effective Junction-to-ambient thermal resistance (TPSM86638 EVM)	24	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC)	36	°C/W
Ψ_{JT}	Junction-to-top characterization parameter[2]	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter[3]	12	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The junction-to-top board characterization parameter, Ψ_{JT}, estimates the junction temperature, T_J , of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \Psi_{JT} \times P_{DIS} + T_T$; where P_{DIS} is the power dissipated in the device and T_T is the temperature of the top of the device.
(3) The junction-to-top board characterization parameter, Ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \Psi_{JB} \times P_{DIS} + T_B$; where P_{DIS} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

5.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the parametric or functional specifications of the device for the life of the product containing it. Typical values correspond to T_J = 25°C, V_{IN} = 24V. Minimum and maximum limits are based on T_J = –40°C to +150°C, V_{IN} = 4.5V to 28V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Quiescent current, operating [1]	T_J = 25°C, V_{EN} = 5V, V_{FB} = 0.7V (TPSM86638)		350		µA
		T_J = 25°C, V_{EN} = 5V, V_{FB} = 0.65V (TPSM86637)		45		µA
I_{SD}	Shutdown supply current	T_J = 25°C, V_{EN} = 0V		3		µA
UVLO						
UVLO	V_{IN} undervoltage lockout	Wake up V_{IN} voltage	4.0	4.2	4.4	V
		Shutdown V_{IN} voltage	3.5	3.65	3.8	V
		Hysteresis V_{IN} voltage		550		mV
ENABLE(EN PIN)						
I_{EN_INPUT}	Input current	V_{EN} = 1.1V		1		µA
I_{EN_HYS}	Hysteresis current	V_{EN} = 1.3V		3		µA
V_{EN_ON}	Enable threshold	EN rising		1.18	1.26	V
V_{EN_OFF}		EN falling	1	1.07		V
FEEDBACK VOLTAGE						
V_{FB}	Feedback voltage	V_{OUT} = 5V, continuous mode operation, T_J = 25°C	0.594	0.6	0.606	V
		V_{OUT} = 5V, continuous mode operation, T_J = –40°C to 150°C	0.591	0.6	0.609	V
CURRENT LIMIT						
I_{LS_OCL}	Low-side MOSFET valley current limit		6	7.2	8.5	A

5.5 Electrical Characteristics (続き)

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the parametric or functional specifications of the device for the life of the product containing it. Typical values correspond to T_J = 25°C, V_{IN} = 24V. Minimum and maximum limits are based on T_J = –40°C to +150°C, V_{IN} = 4.5V to 28V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{HS_OCL}	High-side MOSFET peak current limit		12.75	15	17.25	A
I_{NOC}	Reverse current limit for FCCM		3			A
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	V_{IN} = 24V, V_{OUT} = 5V, continuous mode operation, Mode setting to 800kHz		800		kHz
$t_{ON(MIN)}$	Minimum on time[2]			50		ns
$t_{OFF(MIN)}$	Minimum off time[2]	T_J = 25°C		150		ns
SOFT START						
I_{SS}	Soft-start charging current			6		uA
POWER GOOD						
V_{PGTH}	PG lower threshold - falling	% of V_{FB}		85%		
	PG lower threshold - rising	% of V_{FB}		90%		
	PG upper threshold - falling	% of V_{FB}		110%		
	PG upper threshold - rising	% of V_{FB}		115%		
t_{PG_DLY}	PG delay	PG from low-to-high		64		us
		PG from high-to-low		32		us
V_{OVP}	Output OVP threshold	OVP detect(L->H)		125%		
t_{OVP_DEG}	OVP Prop deglitch	T_J = 25°C		32		us
V_{UVP}	Output UVP threshold	Hiccup detect(H->L)		65%		
t_{UVP_WAIT}	UV protection hiccup wait time			256		us
t_{UVP_HICCUP}	UV protection hiccup time before recovery			10.5		*t_{SS}
THERMAL SHUTDOWN						
Thermal shutdown threshold[3]		Temperature rising	150	165		°C
		Hysteresis		30		°C
SW DISCHARGE RESISTANCE						
V_{OUT} discharge resistance		V_{EN} = 0, V_{SW} = 0.5V, T_J = 25°C		200		Ω

(1) Not representative of the total input current of the system when in regulation. Specified by design and characterization test.
(2) Not production tested. Specified by design.
(3) Not production tested. Specified by design and engineering sample correlation.

5.6 Typical Characteristics

V_{IN} = 12V (unless otherwise noted)

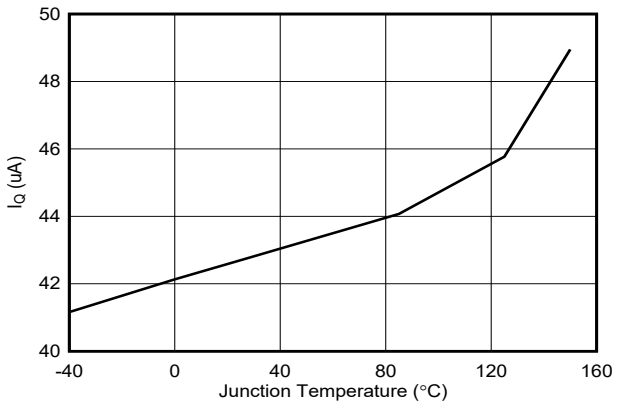


図 5-1. TPSM86637 Quiescent Current vs Temperature

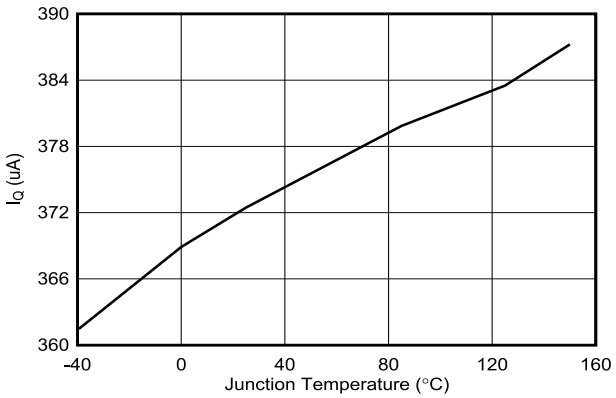


図 5-2. TPSM86638 Quiescent Current vs Temperature

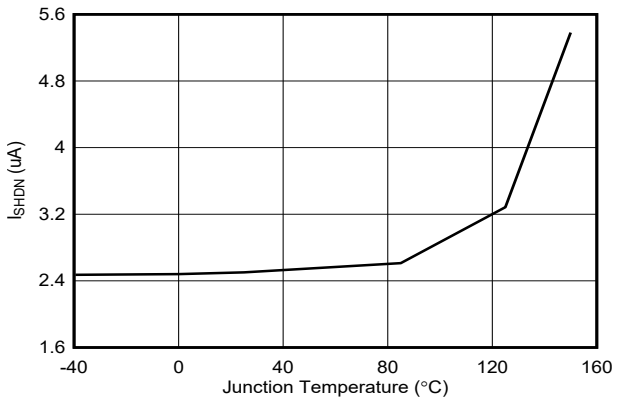


図 5-3. Shutdown Current vs Temperature

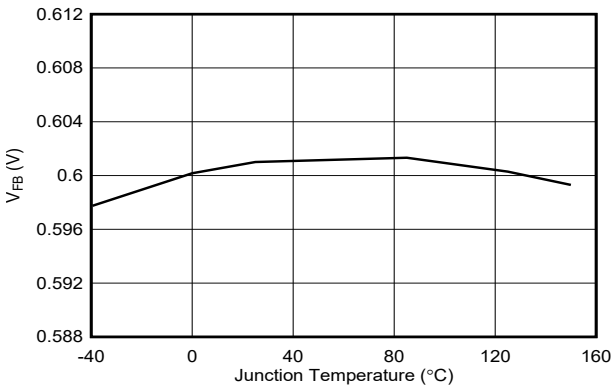


図 5-4. Feedback Voltage vs Temperature

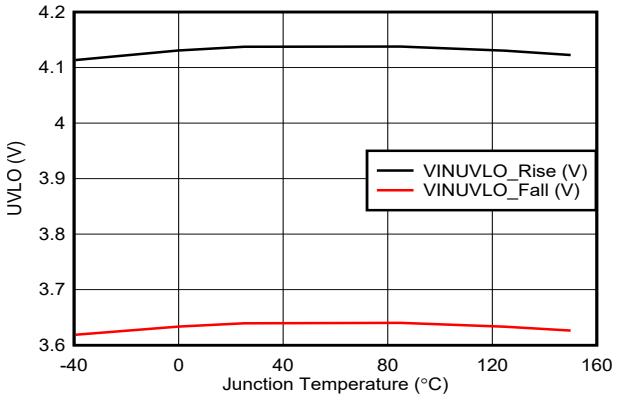


図 5-5. VIN UVLO Threshold vs Temperature

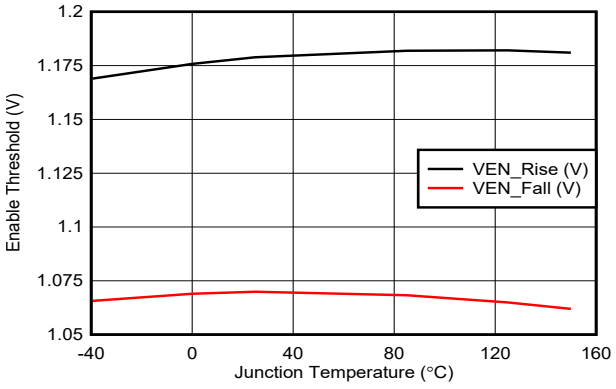


図 5-6. EN Threshold vs Temperature

5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

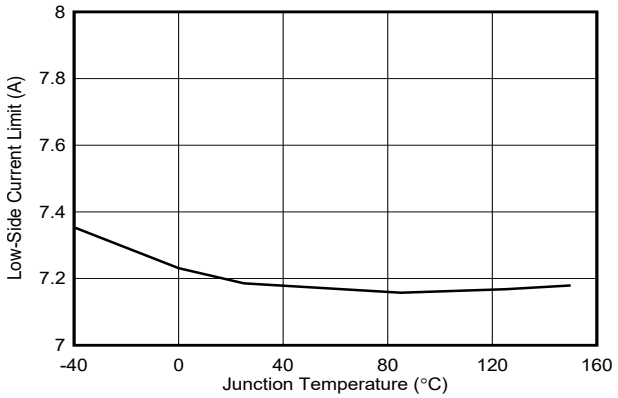


図 5-7. Low-Side Valley Current Limit vs Temperature

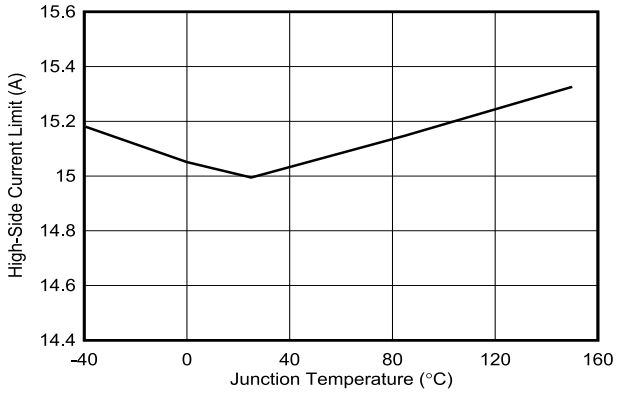


図 5-8. High-Side Peak Current Limit vs Temperature

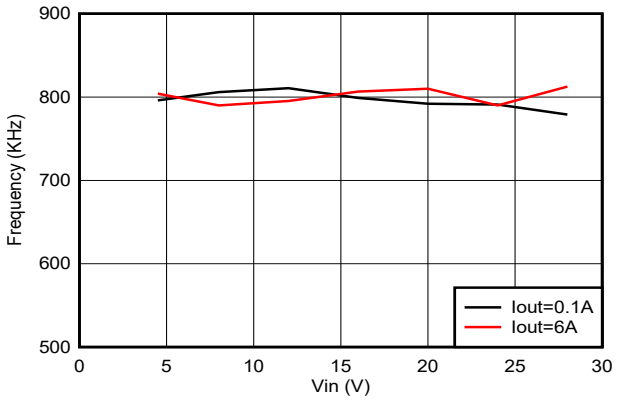


図 5-9. TPSM86638 Switching Frequency vs Input Voltage, Fsw = 800kHz, Vo = 1.8V

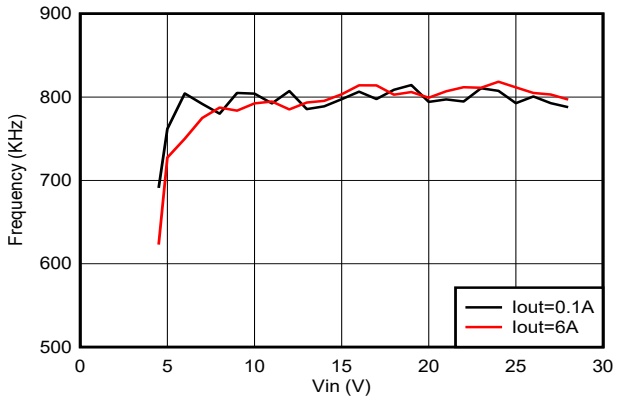


図 5-10. TPSM86638 Switching Frequency vs Input Voltage, Fsw = 800kHz, Vo = 3.3V

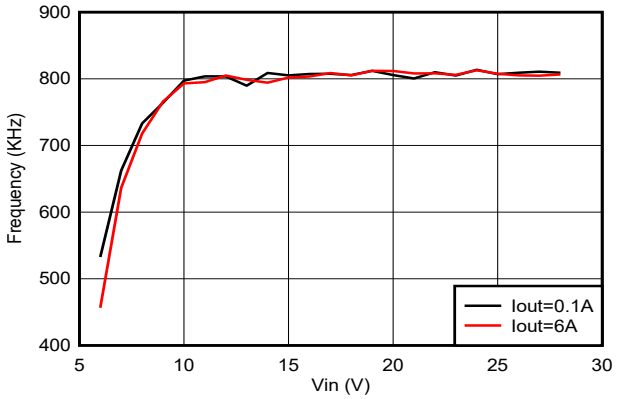


図 5-11. TPSM86638 Switching Frequency vs Input Voltage, Fsw = 800kHz, Vo = 5V

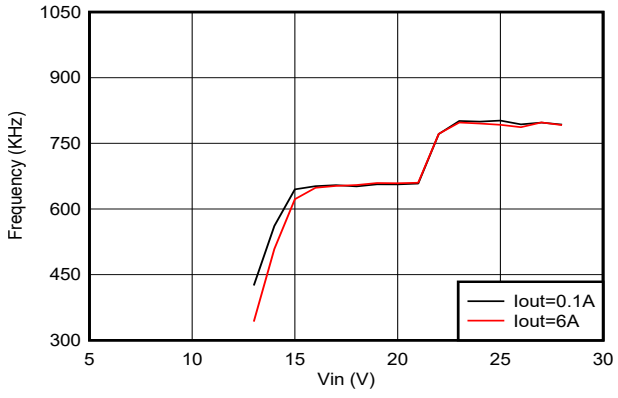


図 5-12. TPSM86638 Switching Frequency vs Input Voltage, Fsw = 800kHz, Vo = 12V

5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

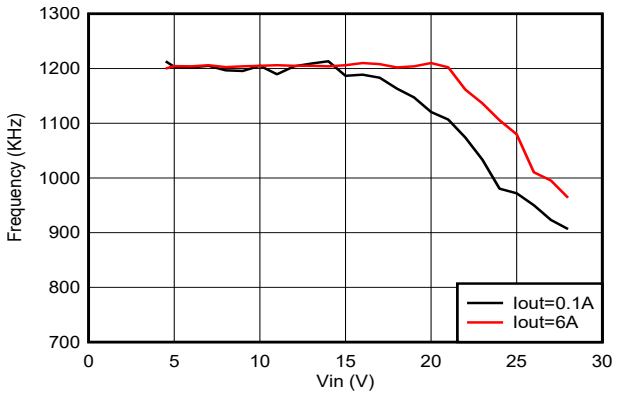


図 5-13. TPSM86638 Switching Frequency vs Input Voltage, Fsw = 1200kHz, Vo = 1.8V

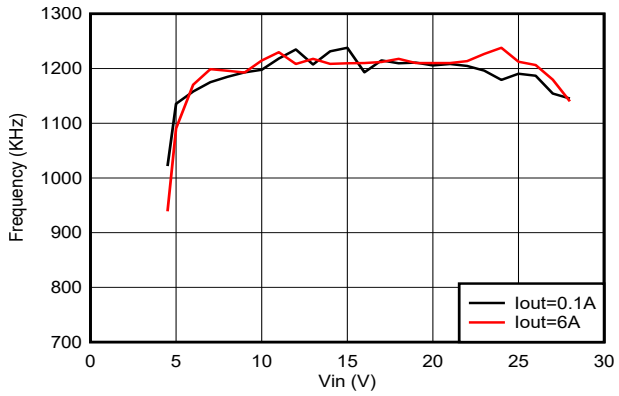


図 5-14. TPSM86638 Switching Frequency vs Input Voltage, Fsw = 1200kHz, Vo = 3.3V

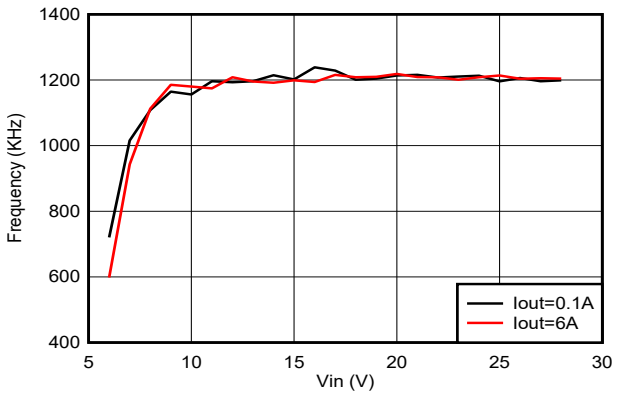


図 5-15. TPSM86638 Switching Frequency vs Input Voltage, Fsw = 1200kHz, Vo = 5V

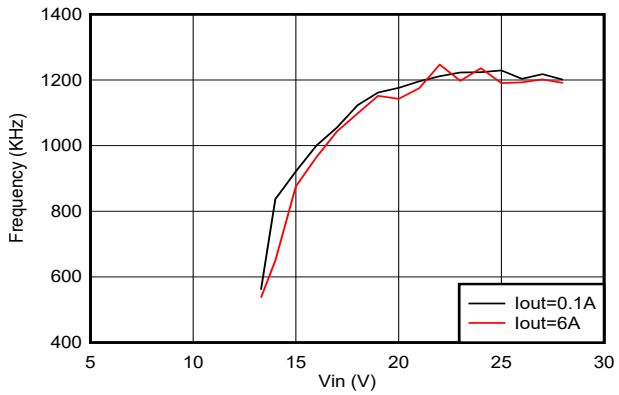


図 5-16. TPSM86638 Switching Frequency vs Input Voltage, Fsw = 1200kHz, Vo = 12V

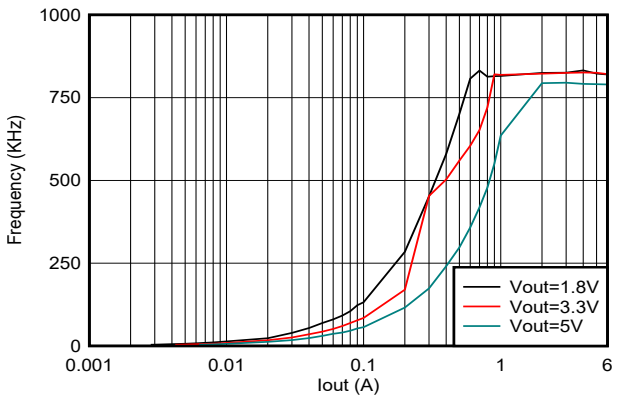


図 5-17. TPSM86637 Switching Frequency vs Output Current, Fsw = 800kHz, Vin = 24V

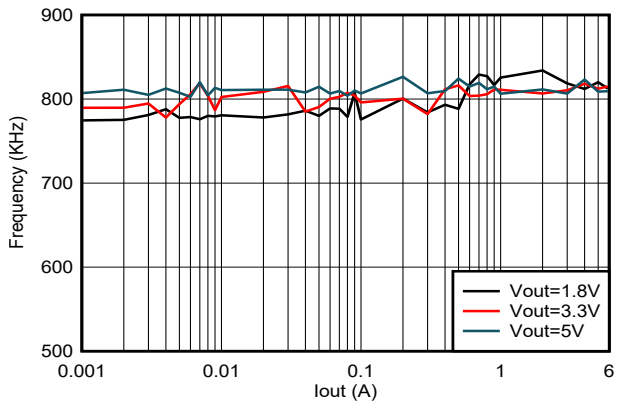


図 5-18. TPSM86638 Switching Frequency vs Output Current, Fsw = 800kHz, Vin = 24V

5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

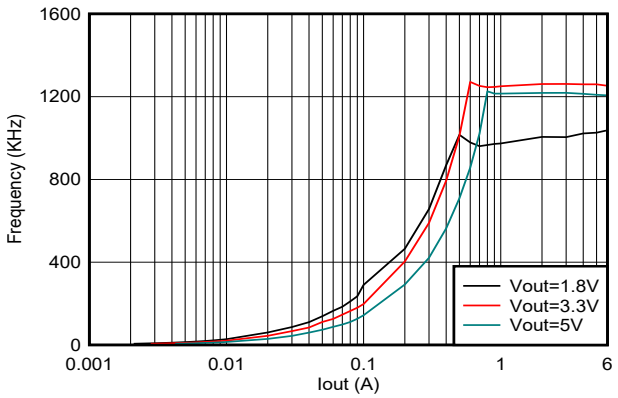


図 5-19. TPSM86637 Switching Frequency vs Output Current, Fsw = 1200kHz, Vin = 24V

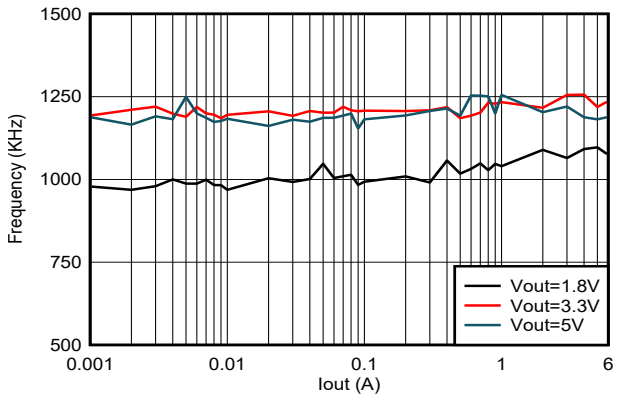


図 5-20. TPSM86638 Switching Frequency vs Output Current, Fsw = 1200kHz, Vin = 24V

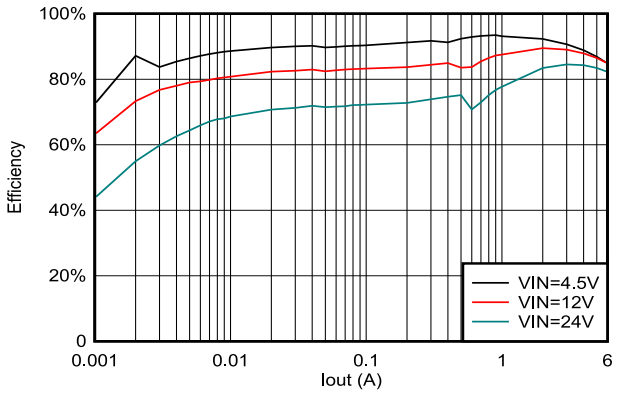


図 5-21. TPSM86637 Efficiency, VOUT = 1.8V, Fsw = 800kHz

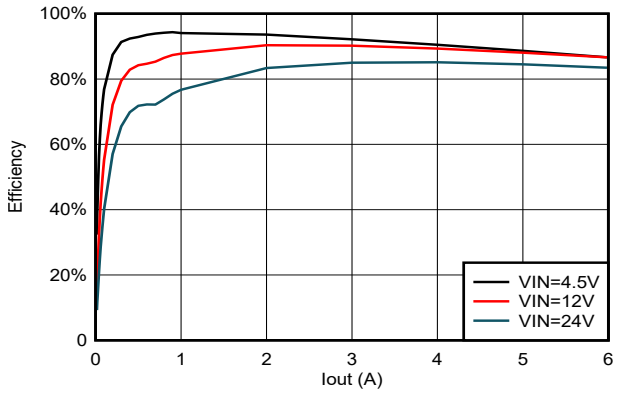


図 5-22. TPSM86638 Efficiency, VOUT = 1.8V, Fsw = 800kHz

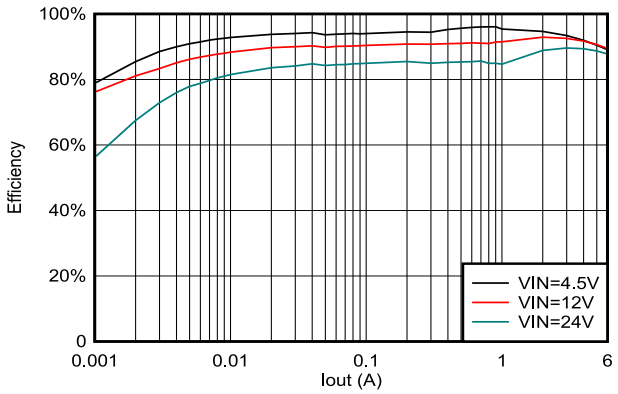


図 5-23. TPSM86637 Efficiency, VOUT = 3.3V, Fsw = 800kHz

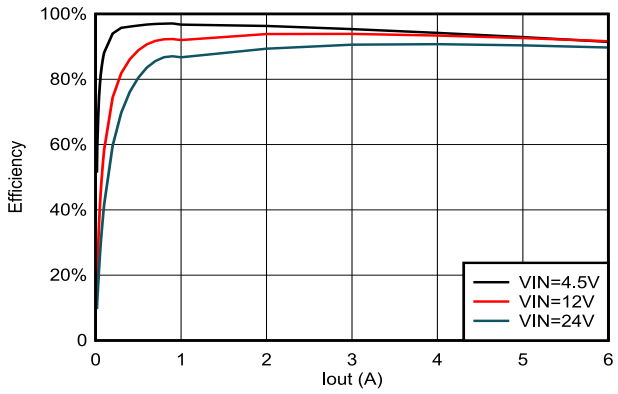


図 5-24. TPSM86638 Efficiency, VOUT = 3.3V, Fsw = 800kHz

5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

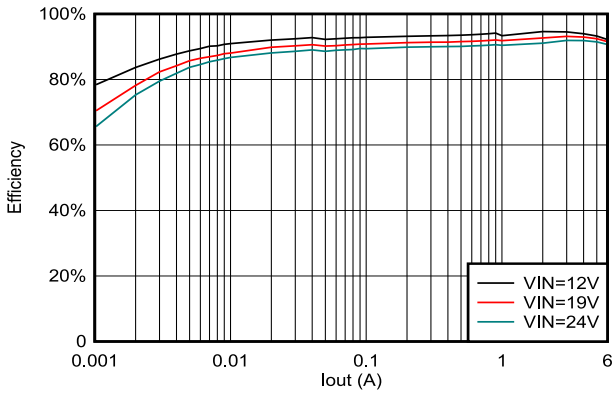


図 5-25. TPSM86637 Efficiency, VOUT = 5V, Fsw = 800kHz

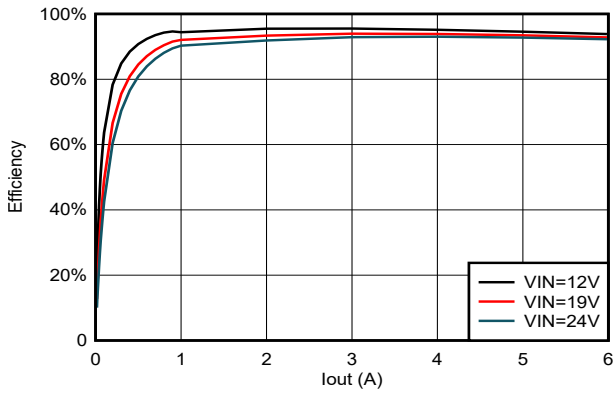


図 5-26. TPSM86638 Efficiency, VOUT = 5V, Fsw = 800kHz

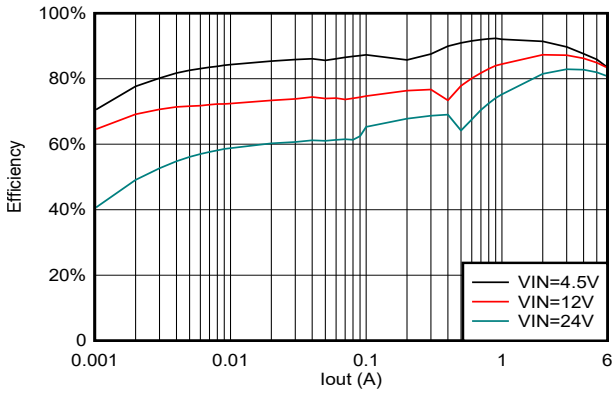


図 5-27. TPSM86637 Efficiency, VOUT = 1.8V, Fsw = 1200kHz

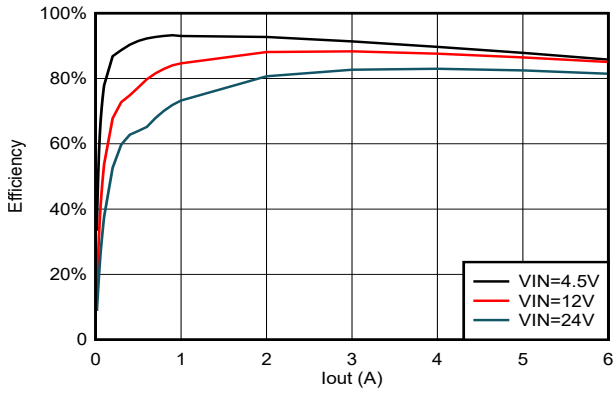


図 5-28. TPSM86638 Efficiency, VOUT = 1.8V, Fsw = 1200kHz

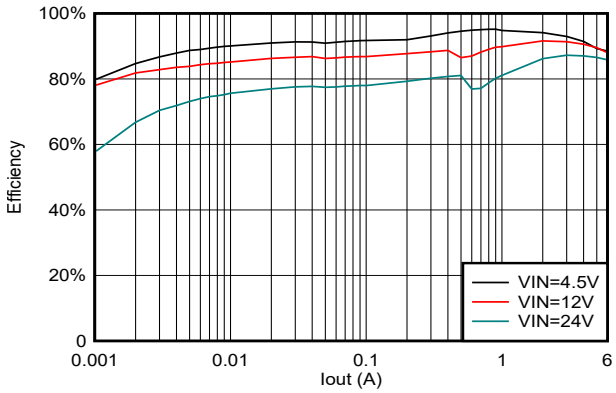


図 5-29. TPSM86637 Efficiency, VOUT = 3.3V, Fsw = 1200kHz

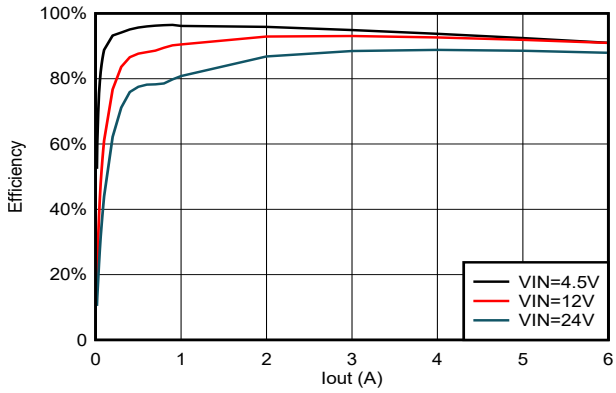


図 5-30. TPSM86638 Efficiency, VOUT = 3.3V, Fsw = 1200kHz

5.6 Typical Characteristics (continued)

V_{IN} = 12V (unless otherwise noted)

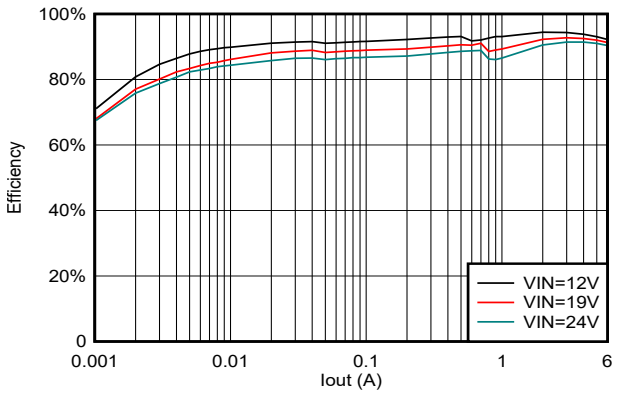


図 5-31. TPSM86637 Efficiency, VOUT = 5V, Fsw = 1200kHz

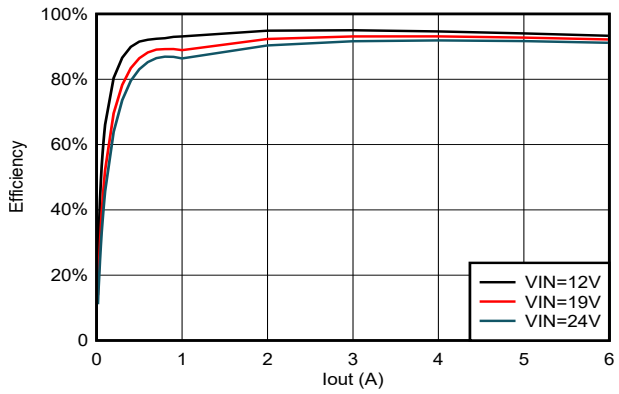


図 5-32. TPSM86638 Efficiency, VOUT = 5V, Fsw = 1200kHz

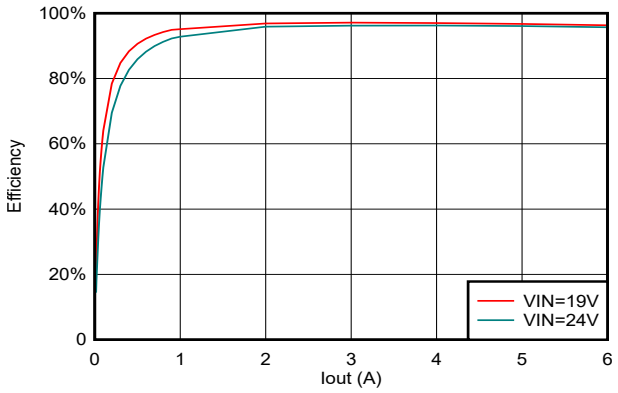


図 5-33. TPSM86638 Efficiency, VOUT = 12V, Fsw = 800kHz

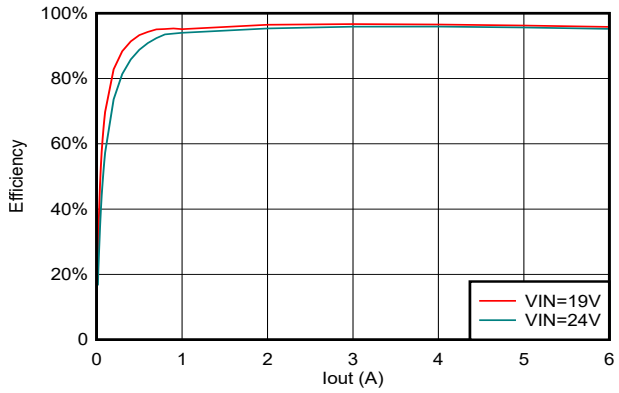


図 5-34. TPSM86638 Efficiency, VOUT = 12V, Fsw = 1200kHz

6 Detailed Description

6.1 Overview

The TPSM8663x is an easy-to-use, synchronous buck DC/DC power module designed for a wide variety of applications where reliability, small design size, and low EMI signature are of paramount importance. With integrated power MOSFETs, a shielded buck inductor, and basic passives, the TPSM8663x is a 6A synchronous buck module operating from 4.5V to 28V input voltage (V_{IN}), and the output voltage ranges from 0.6V to 13V. The proprietary D-CAP3 control mode enables low external component count, ease of design, optimization of the power design for power, size, and efficiency. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. TPSM86637 operates in Eco-mode to attain high efficiency at light load. TPSM86638 operates in FCCM mode which has the quasi-fixed switching frequency at both light and heavy load. The TPSM8663x is able to adapt both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The TPSM8663x incorporates specific features to improve EMI performance in noise-sensitive applications:

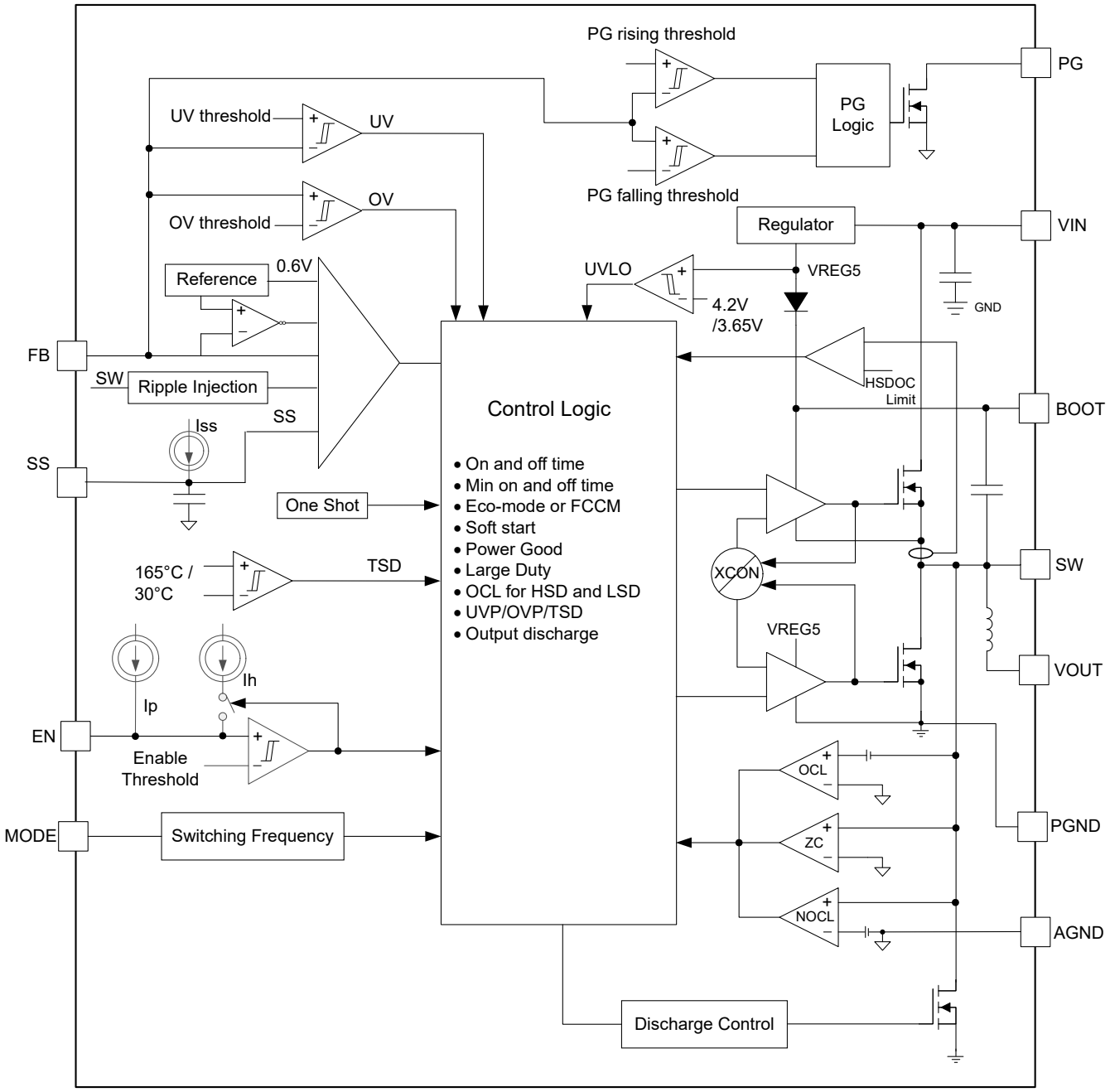
- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI.
- Parallel input and output paths with symmetrical capacitor layouts minimize parasitic inductance, switch voltage ringing, and radiated field coupling
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching.

The TPSM8663x module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing programmable non-latched input undervoltage lockout (UVLO)
- Non-latched overvoltage protections
- Hiccup-mode overcurrent protection with cycle-by-cycle valley current limits
- Thermal shutdown with automatic recovery.

Leveraging a pin arrangement designed for simple layout that requires only a few external components, the TPSM8663x is specified to maximum junction temperatures of 150°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPSM8663x is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for quasi-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The D-CAP3 control mode is stable even with virtually no ripple at the output. The TPSM8663x also includes an error amplifier that makes the output voltage very accurate. No external current sense network or loop compensation is required for D-CAP3 control mode.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the module input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence called adaptive on-time control. When the feedback voltage falls below the reference voltage, the one-shot timer is reset and the high-side MOSFET is turned on again. An internal ripple generation circuit is added to the reference voltage for emulating the output ripple, and this action enables the use of very low-ESR output capacitors, such as multi-layered ceramic caps (MLCC).

6.3.2 Mode Selection

TPSM8663x has a MODE pin to configure the switching frequency, as shown in 表 6-1. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options list in 表 6-1.The voltage on the MODE pin can be set by connecting a resistor to AGND. A guideline for the MODE resistor in 1% resistors in shown in 表 6-1. The MODE pin setting can be reset only by a VIN or EN power cycling.

図 6-1 shows the typical start-up sequence of the device after the enable signal triggers the EN turn-on threshold. After the voltage of internal VCC crosses the UVLO rising threshold, the MODE setting is read. After this process, the MODE is latched and does not change until VIN or EN toggles to restart-up this device. Then after a delay, the internal soft-start function begins to ramp up and Vout ramps up smoothly. When Vout is up to the reference voltage, PGOOD turns to high after a delay.

表 6-1. MODE Pin Settings for TPSM86638

MODE Pin	Switching Frequency
R = 102kohm	800kHz
R = 249kohm	1200kHz

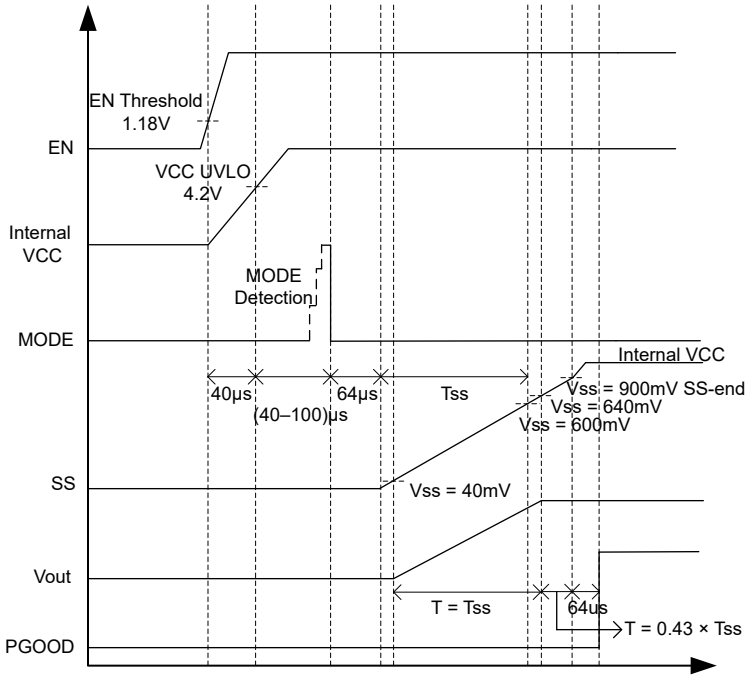


図 6-1. Power-Up Sequence

6.3.2.1 FCCM Control and Eco-mode Control

TPSM86638 operates in forced continuous conduction mode (FCCM) in light load conditions and allows the inductor current to become negative. In FCCM, the switching frequency is maintained at a quasi-fixed level over the entire load range, which is designed for applications requiring tight control of the switching frequency and

output voltage ripple at the cost of lower efficiency under light load compared with that under Eco-mode. This mode also can help to avoid switching frequency dropping into audible range that can introduce some audible "noise".

TPM86637 is set to Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as in the continuous conduction mode so that longer time is needed to discharge the output capacitor with smaller load current to the level of the reference voltage. This process makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation IOUT(LL) current can be calculated by 式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times Fsw} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

6.3.3 Soft Start and Prebiased Soft Start

The TPSM8663x has an adjustable soft-start time that can be set by connecting a capacitor between SS and AGND. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. 式 2 calculates the soft-start time (T_{SS}) :

$$T_{ss} = \frac{C_{ss} \times V_{REF}}{I_{SS}} \quad (2)$$

If the external capacitor (C_{SS}) has pre-stored voltage at start-up, the device initially discharges the external capacitor voltage to lower voltage then charge again to prevent inrush start-up.

If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme makes sure that the converters ramp up smoothly into regulation point.

6.3.4 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the standby operation.

The EN pin has an internal pullup current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, open-drain or open-collector output logic can be used to interface with the pin.

The TPSM8663x implements internal undervoltage lockout (UVLO) circuitry on the V_{IN} pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold has a hysteresis of 550mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in 図 6-2. When using the external UVLO function, TI recommends setting the hysteresis at a value greater than 500mV.

The EN pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because the pullup current increases by I_h when the EN pin crosses the enable threshold. Use 式 3 and 式 4 to calculate the values of R1 and R2 for a specified UVLO threshold. After R1, R2 are settled down, the V_{EN} voltage can be calculated by 式 5, which must be lower than 5.5V with maximum V_{IN}.

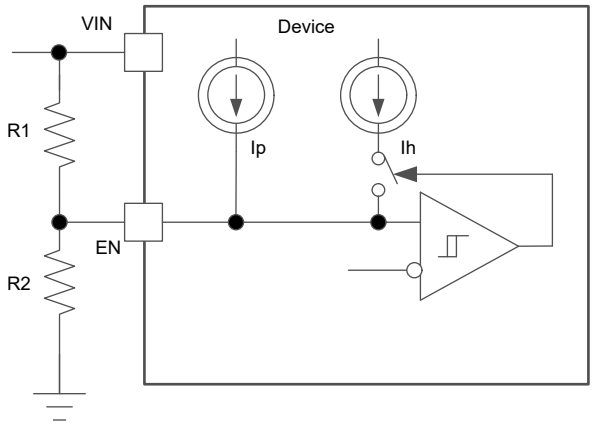


図 6-2. Adjustable VIN Undervoltage Lockout

$$R_1 = \frac{V_{START} \times \frac{V_{ENfalling}}{V_{ENrising}} - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \quad (3)$$

$$R_2 = \frac{R_1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R_1 \times \left(I_p + I_h\right)} \quad (4)$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 \times R_2 \times \left(I_p + I_h\right)}{R_1 + R_2} \quad (5)$$

Where

- I_p = 1µA
- I_h = 3µA
- $V_{ENfalling}$ = 1.07V
- $V_{ENrising}$ = 1.18V

6.3.5 Output Overcurrent Limit and Undervoltage Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle low-side MOSFET valley current detection and high-side MOSFET peak current detection. The switching current is monitored by measuring the MOSFET drain to source voltage. This voltage is proportional to the switching current. To improve accuracy, the voltage sensing is temperature compensated.

There are some important considerations for this type of overcurrent limit. When the load current is higher than the I_{LS_LIMIT} added by one half of the peak-to-peak inductor ripple current, or higher than I_{HS_LIMIT} subtracted by one half of the peak-to-peak inductor ripple current, the OCP is triggered and the current is being limited, output voltage tends to drop because the load demand is higher than what the module can support. When the output voltage falls below 65% of the target voltage, the UVP comparator detects this fall and shuts down the device after a deglitch wait time of 256 us and then re-start after the hiccup time of 10.5 cycles of soft-start time. When the overcurrent condition is removed, the output recovers.

6.3.6 Overvoltage Protection

When the output voltage becomes higher than 125% of the target voltage, the OVP is triggered. The output is discharged after a deglitch time of 32us and both the high-side MOSFET driver and the low-side MOSFET driver turn off. When the overvoltage condition is removed, the output voltage recovers.

6.3.7 UVLO Protection

Undervoltage Lockout protection(UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut down. This protection is non-latched.

6.3.8 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 165°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and the discharge path is turned on. When T_J decreases below the hysteresis amount, the module resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 30°C is implemented on the thermal shutdown temperature.

6.3.9 Output Voltage Discharge

The TPSM8663x has a built-in discharge function by using an integrated MOSFET with 200Ω $R_{DS(on)}$, which is connected to the output terminal SW. The discharge is slow due to the lower current capability of the MOSFET. The discharge path turns on when the device is turned off due to UV, OV, OT, and EN shutdown conditions.

6.3.10 Power Good

The TPSM8663x has a built-in power-good (PG) function to indicate whether the output voltage has reached an appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage below 13V). TI recommends a pullup resistor of 100 kΩ to pull the pin up to 5V voltage. The pin can sink 10mA of current and maintain the specified logic low level. After the FB pin voltage is between 90% and 110% of the internal reference voltage (V_{REF}) and after a deglitch time of 64µs, the PG turns to high impedance status. The PG pin is pulled low after a deglitch time of 32µs when FB pin voltage is lower than 85% of the internal reference voltage or greater than 115% of the internal reference voltage, or in events of thermal shutdown, EN shutdown, UVLO conditions. V_{IN} must remain present for the PG pin to stay Low. The PG pin logic are shown in 表 6-2.

表 6-2. Power-Good Pin Logic Table

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN = High)	V_{FB} does not trigger V_{PGTH}	√	
	V_{FB} triggers V_{PGTH}		√
Shutdown (EN = Low)			√
UVLO	$2V < V_{IN} < V_{UVLO}$		√
Thermal shutdown	$T_J > T_{SD}$		√
Power supply removal	$V_{IN} < 2V$	√	

6.3.11 Large Duty Operation

The TPSM8663x can support large duty operations by smoothly dropping down the switching frequency. The switching frequency is allowed to smoothly drop to make T_{ON} extended to implement the large duty operation and also improve the performance of the load transient performance. The TPSM86638 can support up to 98% duty cycle operation.

6.4 Device Functional Modes

6.4.1 Standby Operation

The TPSM8663x can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 3µA (typical) when in standby condition.

6.4.2 Light Load Operation

TPSM86637 operates in Eco-mode, which maintains high efficiency at light loading. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point

where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as the on-time was in continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes longer. This fact makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

TPSM86638 operates in forced CCM (FCCM) mode. The switching frequency is maintained at an almost constant level over the entire load range which is designed for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The schematic of 図 7-1 shows a typical application for TPSM8663x. This design converts an input voltage range of 4.5V to 28V down to 1.8V with a maximum output current of 6A.

7.2 Typical Application

The application schematic in 図 7-1 shows the TPSM8663x 4.5V to 28V Input, 1.8V output module design meeting the requirements for 6A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

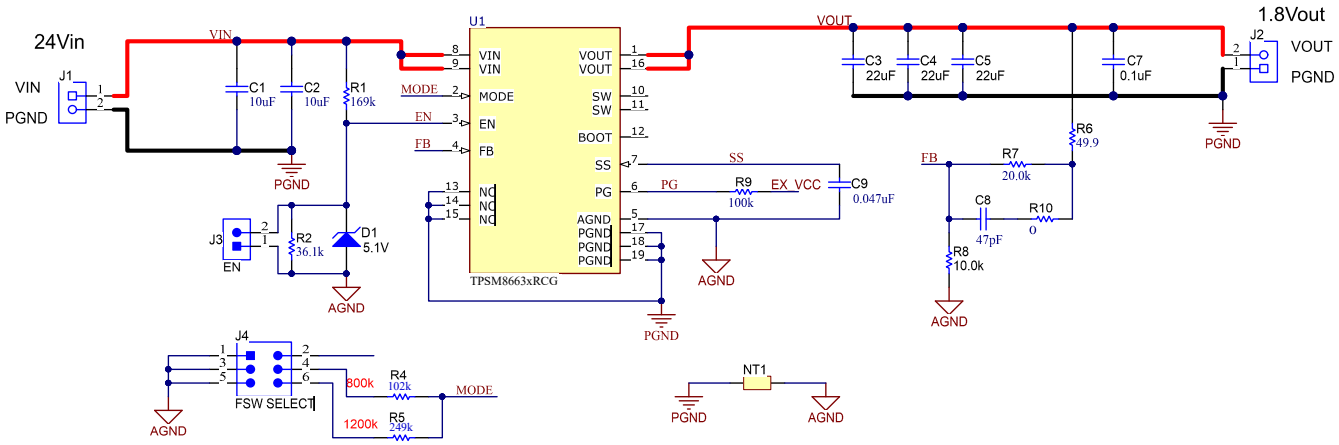


図 7-1. TPSM8663x 1.8V, 6A Reference Design

7.2.1 Design Requirements

表 7-1 shows the design parameters for this application.

表 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	24V nominal, 4.5V to 28V
Output voltage	1.8V
Transient response, 6A load step	ΔV_{OUT} = ±5%
Output ripple voltage	20mV
Output current rating	6A
Operating frequency	800kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the V_{FB} pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 式 6 to calculate V_{OUT}. R_6 is optional and can be used to measure the control loop frequency response.

To improve efficiency at very light loads consider using larger value resistors. If the resistance is too high, the device is more susceptible to noise and voltage errors from the V_{FB} input current are more noticeable. Please note that TI does not recommend dynamically adjusting output voltage.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R7}{R8}\right) \quad (6)$$

7.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (7)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. D-CAP3 control mode introduces a high frequency zero that reduces the gain roll off to –20dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 7 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, use the values recommended in 表 7-2.

表 7-2. Recommended Component Values

Switching Frequency (kHz)	Output Voltage (V)(1)	R7 (kΩ)(2)	R8 (kΩ)	C_{OUT} (µF)(3)		C8 (pF)(4)
				Typical	Maximum	
800	1.05	7.5	10	22uF × 3	22uF × 10	
	1.8	20	10	22uF × 3	22uF × 10	30-100 (47 typical)
	3.3	45.3	10	22uF × 3	22uF × 10	30-100 (47 typical)
	5	73.2	10	22uF × 2	22uF × 10	30-100 (47 typical)
	12	190	10	22uF × 4	22uF × 10	30-100 (47 typical)
1200	1.05	7.5	10	22uF × 3	22uF × 10	
	1.8	20	10	22uF × 3	22uF × 10	30-100 (47 typical)
	3.3	45.3	10	22uF × 3	22uF × 10	30-100 (47 typical)
	5	73.2	10	22uF × 2	22uF × 10	100-200 (150 typical)
	12	190	10	22uF × 4	22uF × 10	30-100 (47 typical)

(1) Please use the recommended C_{OUT} of the higher and closest output rail for unlisted output rails.
(2) R7 = 0Ω for V_{OUT} = 0.6V.

(3) COUT in this data sheet is using Murata GRM32ER71E226KE15L 25VDC capacitor. TI recommends to use the same effective output capacitance. The effective capacitance is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of effective capacitance is provided. Refer to the information of DC bias and temperature characteristics from manufacturers of ceramic capacitors. Higher than Cout_max capacitance is allowed by careful tuning the feedforward compensation.

(4) R10 and C8 can be used to improve the load transient response or improve the loop-phase margin. The *Optimizing Transient Response of Internally Compensated DCDC Converters with Feed-forward Capacitor* application report is helpful when experimenting with a feed-forward capacitor.

The capacitor value and ESR determines the amount of output voltage ripple. The TPSM86638 is intended for use with ceramic or other low ESR capacitors. Use 式 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times Fsw} \quad (8)$$

For this design, three MuRata GRM32ER71E226KE15L 25VDC 22µF output capacitors are used so that the effective capacitance is 68µF at DC biased voltage of 1.8V.

7.2.2.3 Input Capacitor Selection

The TPSM8663x requires input decoupling capacitors, and a bulk capacitor is needed depending on the application. TI recommends at least two 10µF ceramic capacitors for the decoupling capacitor. The capacitor voltage rating must be greater than the maximum input voltage. Use 式 9 to calculate the input voltage ripple.

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times 0.25}{C_{IN} \times Fsw} \quad (9)$$

The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. Use 式 10 to calculate the input ripple current:

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}} \times \frac{V_{IN(MIN)} - V_{OUT}}{V_{IN(MIN)}}} \quad (10)$$

7.2.3 Application Curves

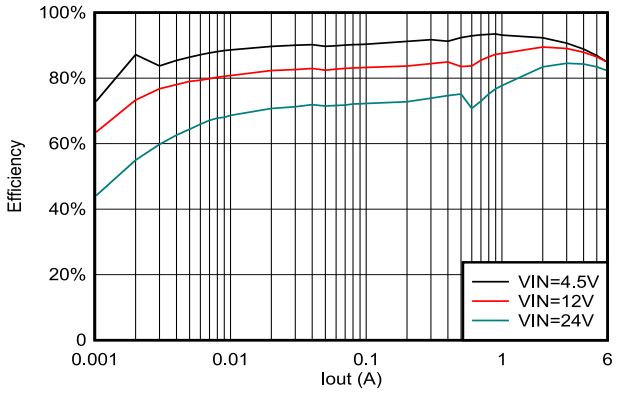


図 7-2. TPSM86637 Efficiency

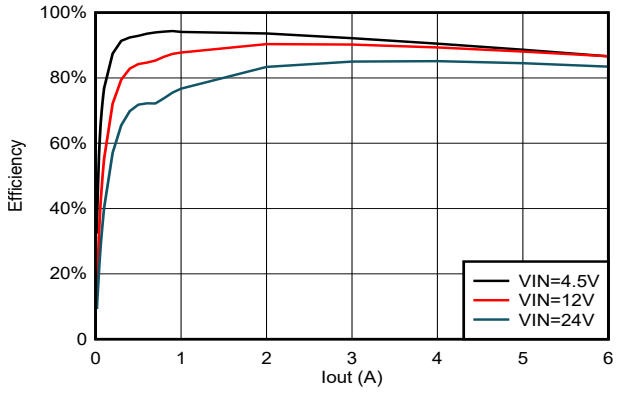


図 7-3. TPSM86638 Efficiency

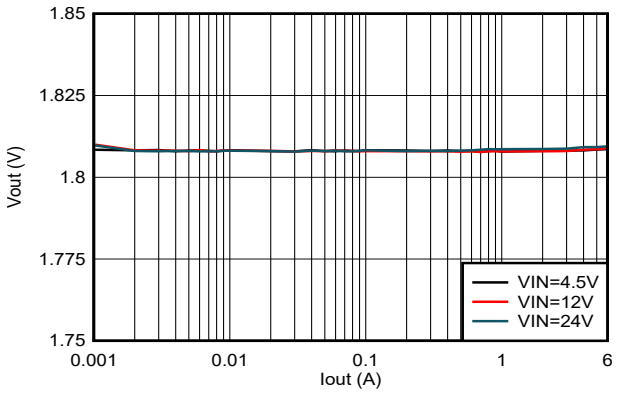


図 7-4. TPSM86638 Load Regulation

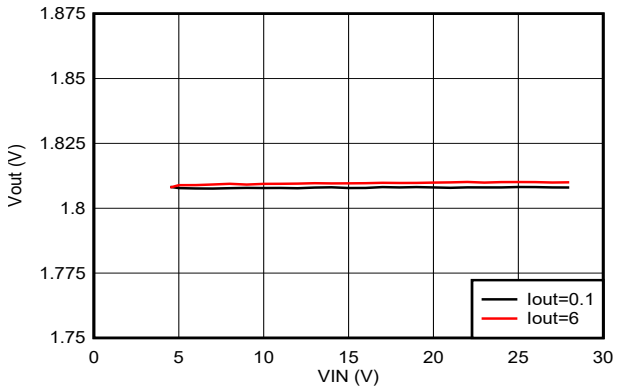


図 7-5. TPSM86638 Line Regulation

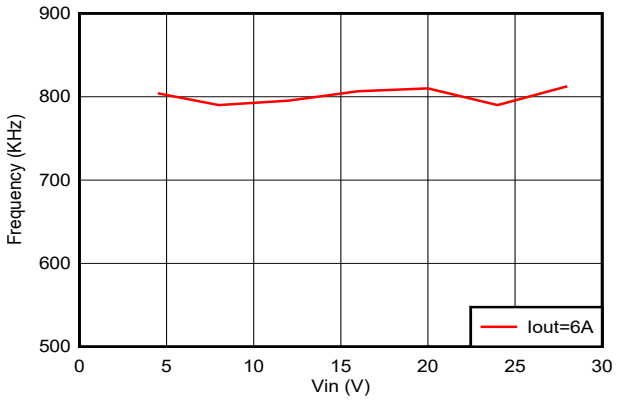


図 7-6. Switching Frequency vs Input Voltage

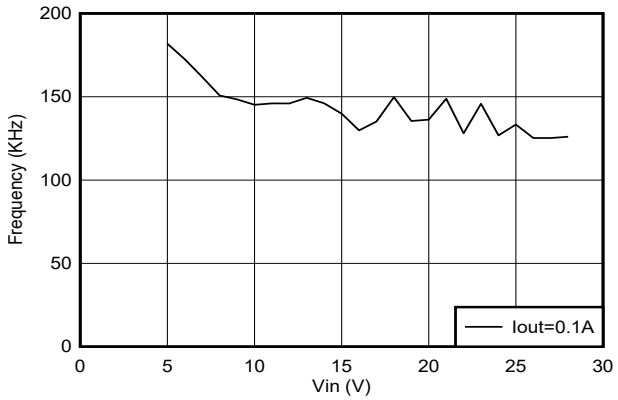


図 7-7. TPSM86637 Switching Frequency vs Input Voltage

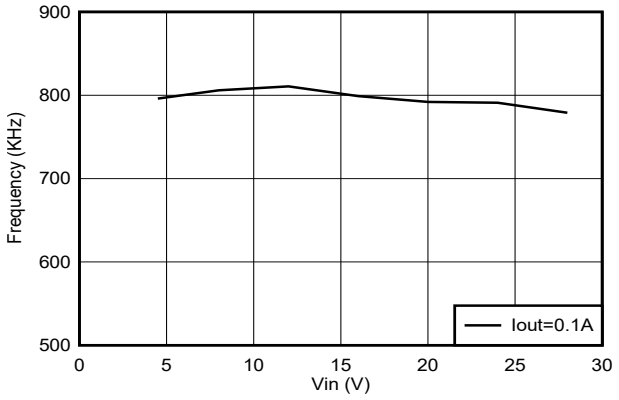


図 7-8. TPSM86638 Switching Frequency vs Input Voltage

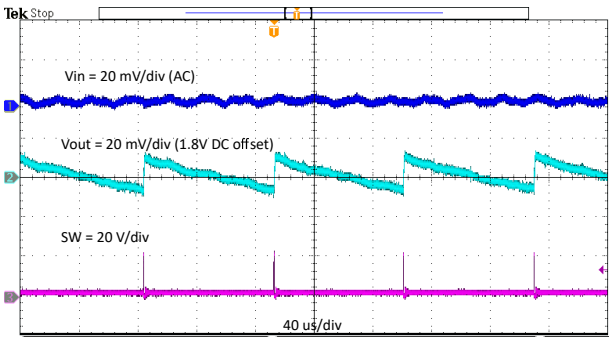


図 7-9. TPSM86637 Steady State Waveform, I_{OUT} = 0.01A

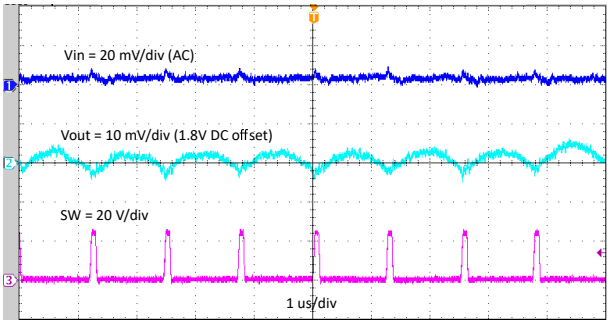


図 7-10. TPSM86638 Steady State Waveform, I_{OUT} = 0.01A

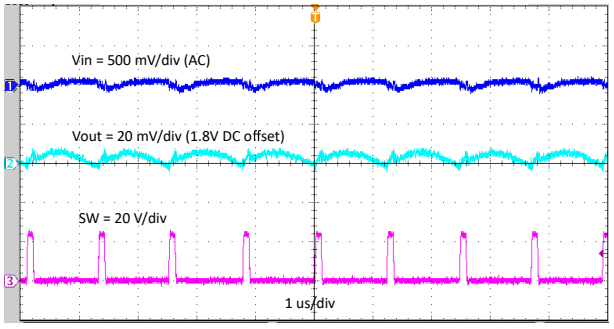


図 7-11. Steady State Waveform, I_{OUT} = 6A

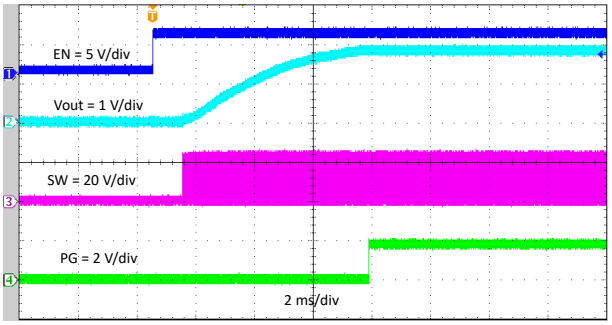


図 7-12. Enable Relative to EN

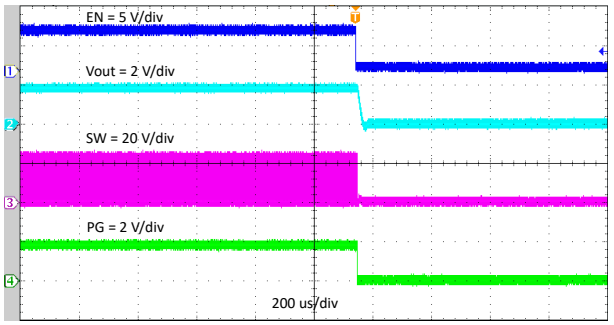


図 7-13. Disable Relative to EN

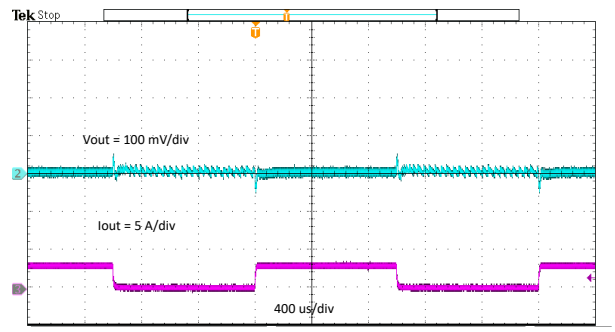


図 7-14. TPSM86637 Transient Response 0A to 3A

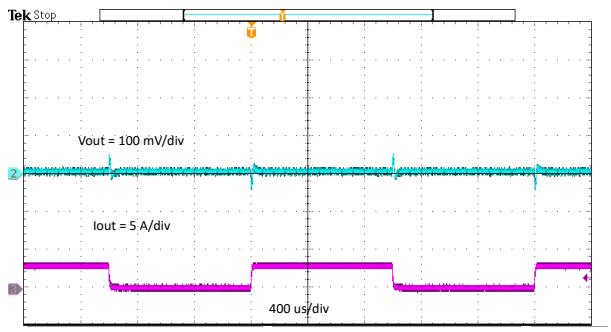


図 7-15. TPSM86638 Transient Response 0A to 3A

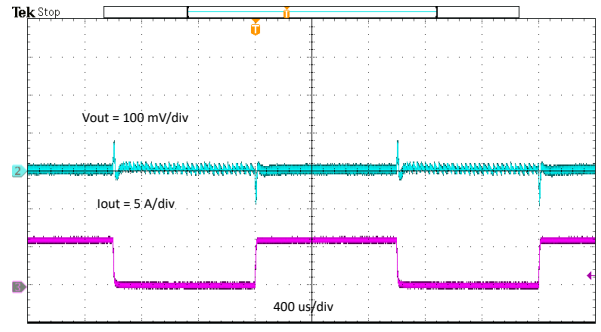


図 7-16. TPSM86637 Transient Response 0A to 6A

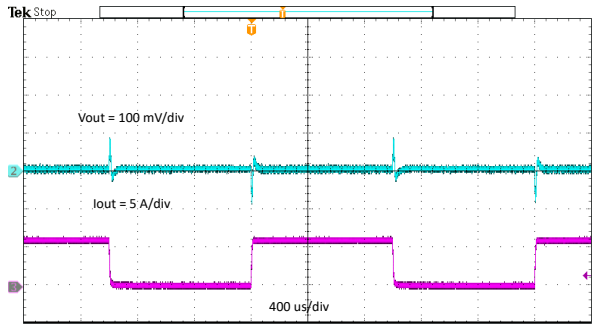


図 7-17. TPSM86638 Transient Response 0A to 6A

7.3 Power Supply Recommendations

The TPSM8663x is designed to operate from input supply voltage in the range of 4.5V to 28V. Buck modules require the input voltage to be higher than the output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPSM8663x circuit, TI recommends some additional input bulk capacitance.

7.3.1 Application Thermal Considerations

The power module integrates the main power dissipating elements, the power switches and magnetics, all into one package, which enables smaller design size and simplifies the development. Therefore, in addition to the IC losses, the heat generated from the inductor direct current resistance (DCR) and core losses add to the total power dissipated in the package. Under the same operating conditions as the discrete counterparts (which have an external inductor), the module has the challenge of dissipating more heat through a smaller surface area. There is a constraint on the maximum output current that modules can deliver at higher operating ambient temperatures due to limitations in maximum temperature ratings for both the inductor and IC.

The temperature rise of module can be calculated by using efficiency and EVM effective $R_{\theta JA}$. 式 11 calculates the power loss from the data sheet efficiency curves:

$$Power\ Loss = \left(V_{OUT} \times I_{OUT}\right) \times \left(\frac{1}{\eta} - 1\right) \quad (11)$$

Where η is the application conditions efficiency.

7.4 Layout

7.4.1 Layout Guidelines

The following list summarizes the essential guidelines for PCB layout and component placement to optimize DC/DC module performance, including thermals and EMI signature.

1. Use a four-layer PCB with two-ounce copper thickness for good thermal performance and with maximum ground plane.
2. Place input capacitors as close as possible to the VIN pins. Note the dual and symmetrical arrangement of the input capacitors based on the VIN1 and VIN2 pins located on each side of the module package. The high-frequency currents are split in two and effectively flow in opposing directions such that the related magnetic fields contributions cancel each other, leading to improved EMI performance.
   - Use low-ESR 1206 or 1210 ceramic capacitors with X7R or X7S dielectric.
   - Make ground return paths for the input capacitors consist of localized top-side planes that connect to the PGND pads under the module.
   - Make VIN traces as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation. Even though the VIN pins are connected internally, use a wide polygon plane on a bottom PCB layer to connect these pins together and to the input supply.
3. Place output capacitors as close as possible to the VOUT pins. A similar dual and symmetrical arrangement of the output capacitors enables magnetic field cancellation and EMI mitigation.
   - Make ground return paths for the output capacitors consist of localized top-side planes that connect to the PGND pads under the module.
   - Make VOUT traces as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation. Even though the VOUT pins are connected internally, use a wide polygon plane on a bottom PCB layer to connect these pins together and to the load, thus reducing conduction loss and thermal stress.
4. Keep the FB trace as short as possible by placing the feedback resistors close to the FB pin. Reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. FB is the input to the voltage-loop error amplifier and represents a high-impedance node sensitive to noise. Route a trace from the upper feedback resistor to the required point of output voltage regulation. Place the voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
5. Provide enough PCB area for proper heatsinking. Use sufficient copper area to achieve a low thermal impedance commensurate with the maximum load current and ambient temperature conditions. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pads (PGND) of the package to the PCB ground plane. If the PCB has multiple copper layers, connect these thermal vias to inner-layer ground planes.

7.4.2 Layout Example

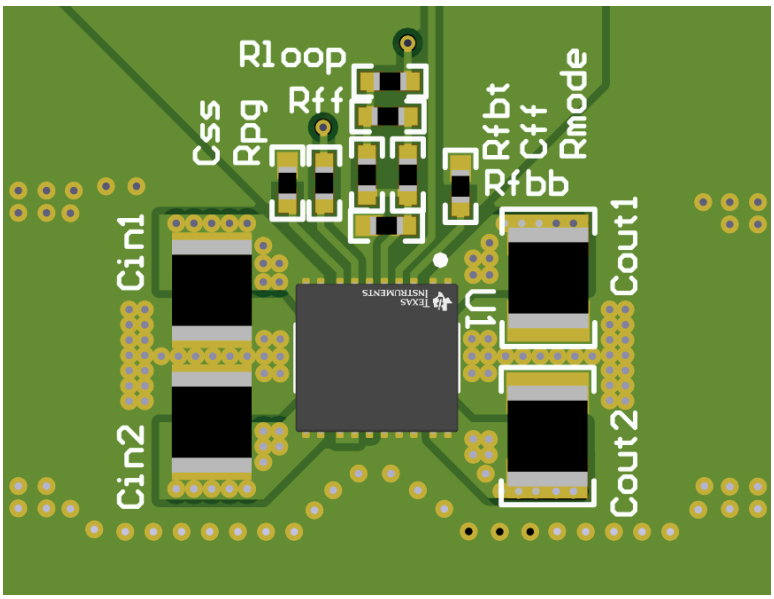


図 7-18. TPSM8663x Layout

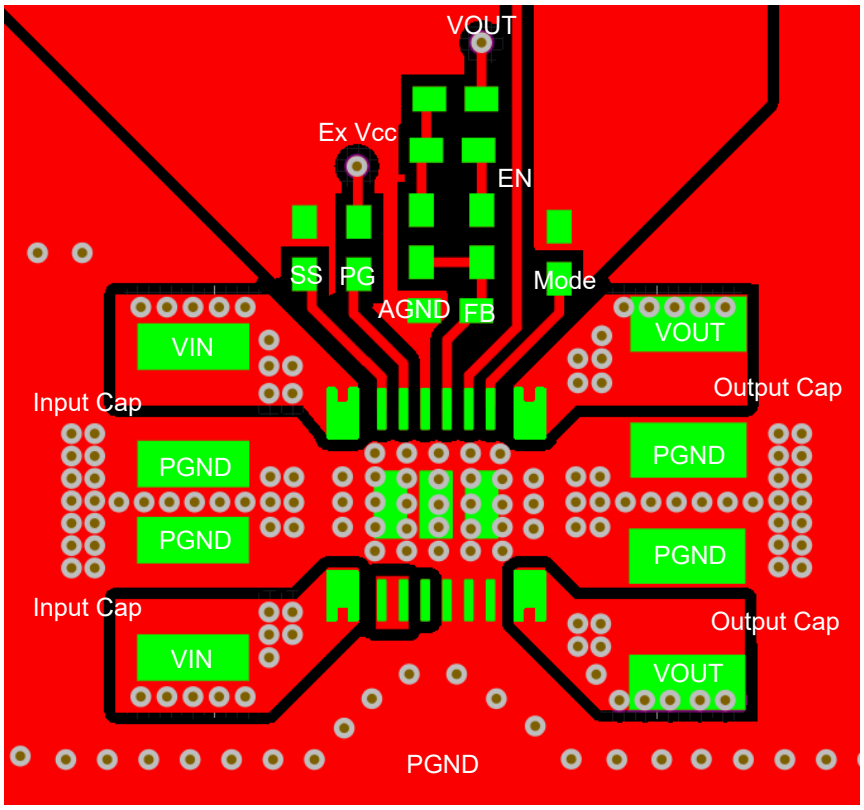


図 7-19. TPSM8663x Top Layer Design

8 Device and Documentation Support

8.1 Device Support

8.1.1 サード・パーティ製品に関する免責事項

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8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Optimizing Transient Response of Internally Compensated DCDC Converters with Feed-forward Capacitor* application report

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
May 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM86637RCGR	Active	Production	B3QFN (RCG) | 19	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 150	TPSM86637
TPSM86637RCGR.A	Active	Production	B3QFN (RCG) | 19	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 150	TPSM86637
TPSM86638RCGR	Active	Production	B3QFN (RCG) | 19	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 150	TPSM86638
TPSM86638RCGR.A	Active	Production	B3QFN (RCG) | 19	1000 | LARGE T&R	Yes	NIPDAU	Level-3-250C-168 HR	-40 to 150	TPSM86638

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

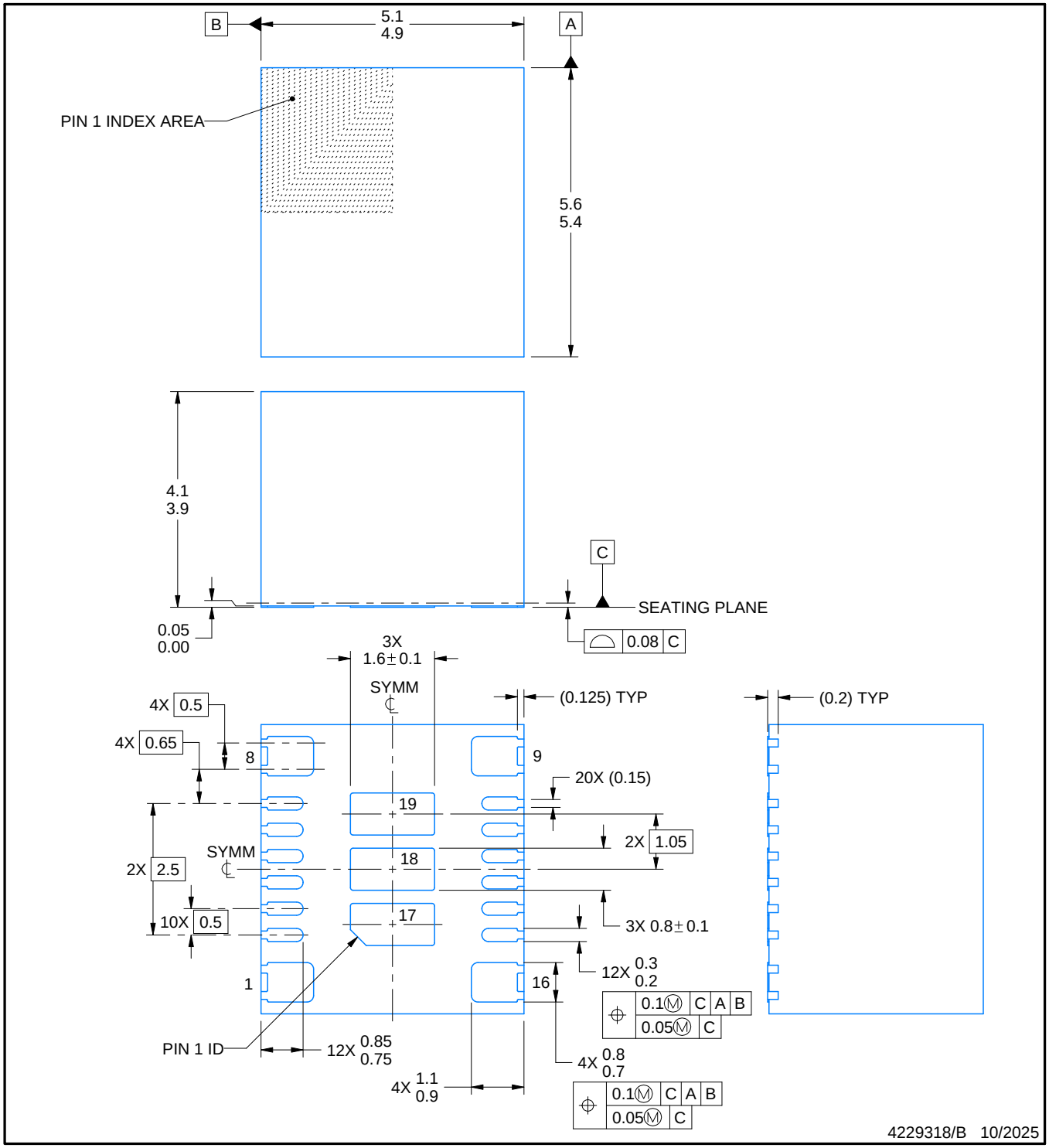
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RCG0019A

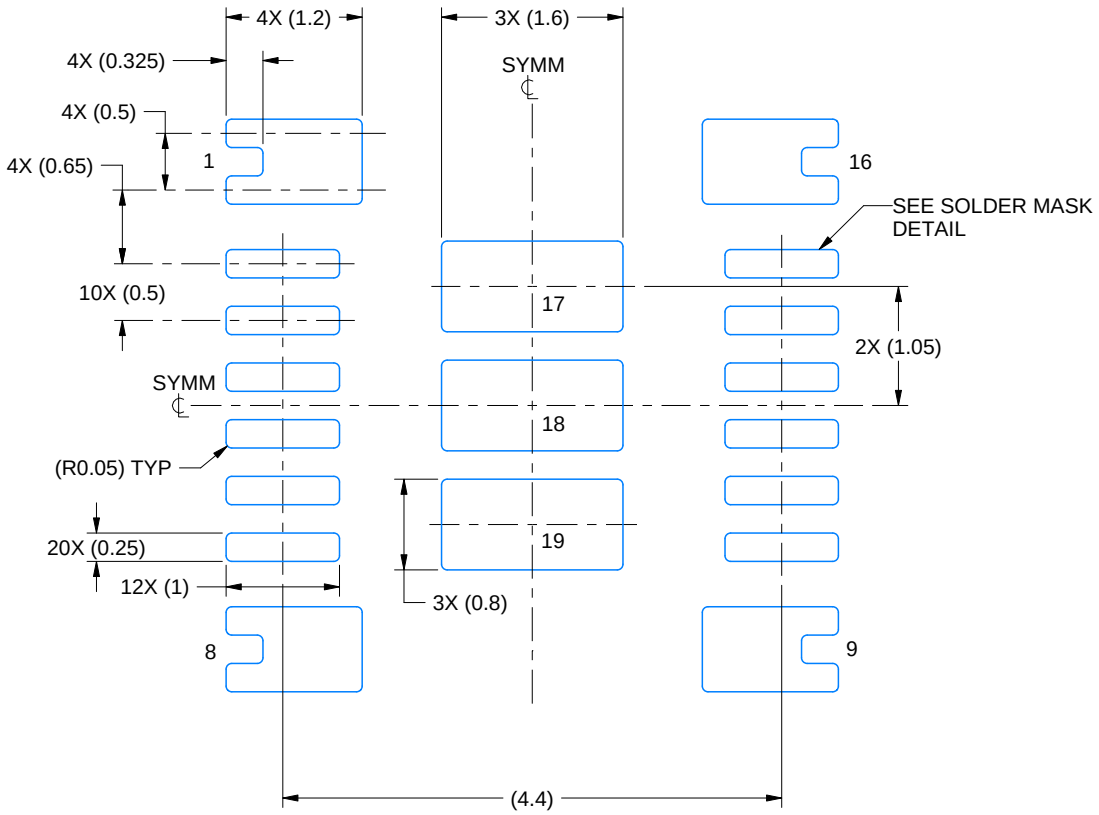
B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

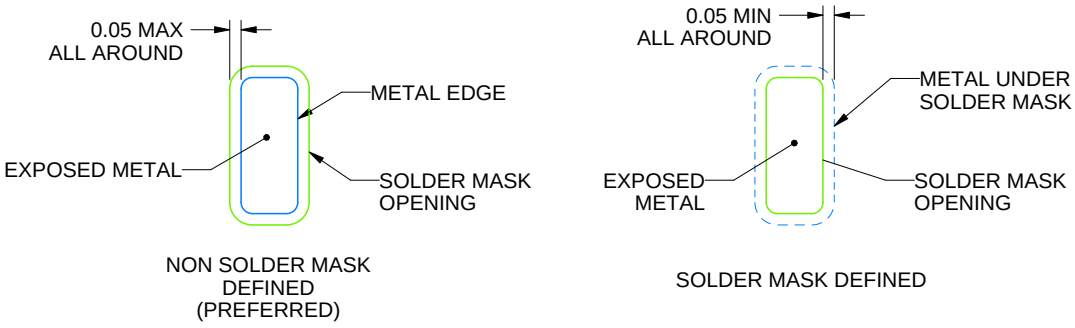


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS
NOT TO SCALE

4229318/B 10/2025

NOTES: (continued)

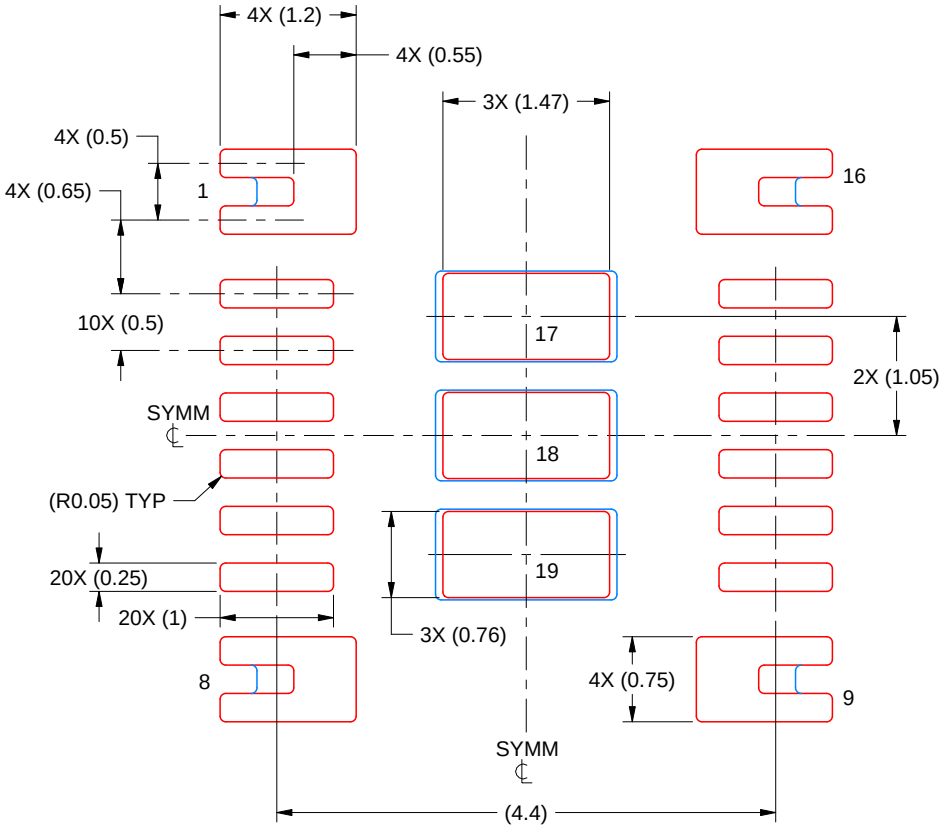
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RCG0019A

B3QFN - 4.1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1, 8, 9 & 16: 90%
PADS 17, 18 & 19: 82%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月