TRF1305B1 シングル チャネル、DC から 7GHz 超、3dB 帯域幅、RF 完全差動アンプ

1 特長

- 性能が最適化された 3 つのパワー ゲインのバリエーション:
  - 15dB (TRF1305A1)
  - 10dB (TRF1305B1)
  - 5dB (TRF1305C1)
- 固定ゲインは外付け抵抗で低減可能
- 幅広い大信号 RF 帯域幅:
  - TRF1305B1:7.2GHz (3dB)、6.4GHz (1dB)
- OP1dB (差動 100Ω 負荷):
  - 15.6dBm (2GHz)、12.9dBm (4GHz)
- OIP3:34.5dBm (2GHz)、25.5dBm (4GHz)
- ノイズ フィギュア:10.4dB (2GHz)、13.4dB (4GHz)
- スルーレート:25kV/µs
- 広い入力 (±1V) および出力 (±0.5V) の同相電圧範囲
- 柔軟な構成とモード:
  - シングルエンド入力、差動出力 (S2D)
  - 差動入力、差動出力 (D2D)
  - シングルエンド出力 (性能に制限あり)
  - AC 結合または DC 結合の入出力
  - 調整可能な出力同相電圧
  - 同相入力範囲拡張モード
- 5V、柔軟な単一または分割電源をサポート
- アクティブな消費電力:475 mW
- (パワーダウン モード時)

2 アプリケーション

- RF サンプリングまたは GSPS ADC ドライバ
- 試験および測定機器
- ワイヤレス通信テスト
- RF デジタイザ
- オシロスコープ (DSO)
- 高速デジタイザ
- スペクトル アナライザ
- ベクトル信号トランシーバ (VST)
- 質量分析システム
- 同相モード レベル シフト
- IQ ミキサ インターフェイス

3 概要

TRF1305B1 は、非常に高性能な閉ループの シングル チャネル RF アンプで、真の DC から 7GHz を超える動作帯域幅を持ちます。このデバイスは、ADC12DJ5200RF や ADC32RF5x などの高速で高性能な ADC を、DC 結合または AC 結合のインターフェイスで駆動する優れた性能を備えています。このアンプは、RF、ゼロ IF、複素 IF、および高速の時間領域アプリケーションでの使用に最適化されています。このデバイスは、固定ゲイン構成での性能に最適化されています。より低いゲインが必要な場合は、外付け抵抗を使用します。

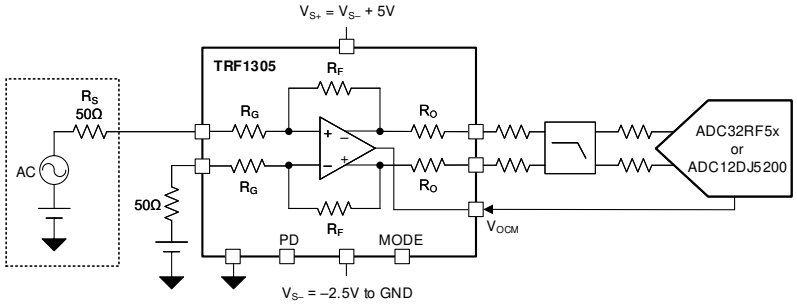
TRF1305B1 は、異なる出力同相電圧と入力同相電圧を設定できる VOCM ピンを備えています (たとえば、レベル シフトや、異なる DC 同相電圧を持つほとんどの IQ 降圧コンバータの ADC インターフェイス アプリケーション用)。また TRF1305B1 は、2 レールのフローティング分割または単一電源のオプションと、入力同相範囲を電源に近い範囲に拡張できる MODE ピンを備えています。

TRF1305B1 には、パワー ダウン機能があります。このデバイスは、テキサス・インスツルメンツ独自の高度な BiCMOS プロセスで製造されており、省スペースの 2mm × 2mm、12 ピンの WQFN-FCRLF パッケージで供給されます。

製品情報

部品番号 (1)	D2D パワー ゲイン	パッケージ (2)
TRF1305A1 (3)	15 dB	RPV (WQFN-FCRLF、12)
TRF1305B1	10 dB	
TRF1305C1 (3)	5 dB	

(1) セクション 4 を参照してください。
(2) 詳細については、セクション 11 を参照してください。
(3) プレビュー情報 (量産データではありません)。



S2D 構成で高速 ADC を駆動する TRF1305x1

Table of Contents

4 Device Comparison Table

DEVICE	GAIN	CHANNEL COUNT
TRF1305A1 (preview)	15dB	1
TRF1305B1	10dB	
TRF1305C1 (preview)	5dB	
TRF1305A2 (preview)	15dB	2
TRF1305B2	10dB	
TRF1305C2 (preview)	5dB	

5 Pin Configuration and Functions

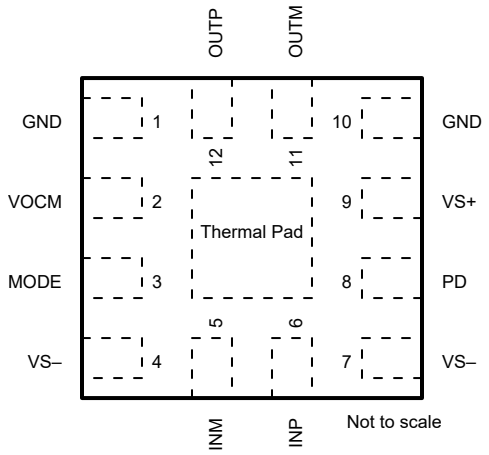


図 5-1. RPV Package, 12-Pin WQFN-FCRLF (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 10	Ground	Ground. Reference for RF signals and PD control signal. Connect to ground plane on the board. Internally shorted to the thermal pad.
INM	5	Input	Negative side of differential input signal
INP	6	Input	Positive side of differential input signal
MODE	3	Input	Mode selection pin. See also MODE Pin section.
OUTM	11	Output	Negative side of differential output signal
OUTP	12	Output	Positive side of differential output signal
PD	8	Input	Power-down signal, referenced to GND. Supports both 1.8V and 3.3V logic. Logic 0 or open = device enabled. Logic 1 = device powered down.
VOCM	2	Input	Output common-mode voltage input pin. Floating the pin sets the output common-mode voltage to $V_{S–}$ + 2.5V.
VS–	4, 7	Power	Negative supply voltage
VS+	9	Power	Positive supply voltage
Thermal Pad	Pad	Ground	Thermal pad. Connect to heat-dissipating ground plane on the board. Internally shorted to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{S–}$	Negative supply voltage, referenced to GND	–3	0.3	V
V_{S+}	Positive supply voltage	–0.3	$V_{S–}$ + 5.5	V
V_S	Total supply voltage, $V_S = V_{S+} – V_{S–}$	–0.3	5.5	V
P_{IN}	Input RF power(2)		20	dBm
V_{PD}	PD pin voltage, referenced to GND, $V_{S+} \geq 3.3V$	–0.3	3.6	V
	PD pin voltage, referenced to GND, $V_{S+} < 3.3V$	–0.3	V_{S+} + 0.3	
V_{OCM}	VOCM pin voltage	$V_{S–}$ + 1	$V_{S–}$ + 4	V
V_{MODE}	MODE pin voltage	$V_{S–}$ – 0.3	$V_{S–}$ + 3.3	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) When device supplies are present; otherwise, limit swing at the device pins to $V_{S–}$ ± 0.3V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{S–}$	Negative supply voltage	–2.5		0	V
V_S	Total supply voltage, $V_S = V_{S+} – V_{S–}$	4.75	5	5.25	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TRF1305x1 RPV (WQFN-FCRLF) 12 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	62.6	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	29.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	26.1	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	0.5	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	26.1	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	18.8	°C/W

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics - TRF1305B1

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output with differential source impedance (Z_S) = 100Ω, differential output load (Z_L) = 100Ω, external input resistor network (see 図 8-3), and inputs de-embedded up to R_{IN_SER} and outputs up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth (3dB)	P_{IN} = –20dBm at each input			7.3		GHz
	Small-signal bandwidth (1dB)	P_{IN} = –20dBm at each input			6.4		
LSBW	Large-signal bandwidth (3dB)	Differential P_{IN} = –3dBm			7.2		GHz
	Large-signal bandwidth (1dB)	Differential P_{IN} = –3dBm			6.4		
Sdd21	Power gain	f = 500MHz			9.8		dB
		f = 4GHz			10		
	Gain variation over temperature	f = 4GHz, T_A = –40℃ to +85℃			2		dB
Sdd11	Input return loss	f = 10MHz to 5GHz			–13		dB
Sdd12	Reverse isolation	f < 5GHz (device enabled)			–23		dB
G_{IMB}	Differential gain imbalance	f < 5GHz, S2D, P_{IN} = –20dBm with 50Ω Z_S			±0.2		dB
PH_{IMB}	Differential phase imbalance	f < 5GHz, S2D, P_{IN} = –20dBm with 50Ω Z_S			±2		°
OP1dB	Output 1dB compression point	f = 500MHz			15.5		dBm
		f = 1GHz			15.8		
		f = 2GHz			15.6		
		f = 3GHz			14.9		
		f = 4GHz			12.9		
		f = 5GHz			11		
HD2	Second-order harmonic distortion	V_O = $2V_{PP}$	f = 500MHz		–87		dBc
			f = 1GHz		–72		
			f = 2GHz		–60		
			f = 3GHz		–55		
			f = 4GHz		–53		
HD3	Third-order harmonic distortion	V_O = $2V_{PP}$	f = 500MHz		–70		dBc
			f = 1GHz		–63		
			f = 2GHz		–67.5		
			f = 3GHz		–50		
			f = 4GHz		–48		
OIP2	Output second-order intercept point	P_O = 1dBm per tone, 2MHz spacing	f = 500MHz		90		dBm
			f = 1GHz		73		
			f = 2GHz		61		
			f = 3GHz		56		
			f = 4GHz		55		
			f = 5GHz		58		
OIP3	Output third-order intercept point	P_O = 1dBm per tone, 2MHz spacing	f = 500MHz		43.5		dBm
			f = 1GHz		40		
			f = 2GHz		34.5		
			f = 3GHz		32.5		
			f = 4GHz		25.5		
			f = 5GHz		20		

6.5 Electrical Characteristics - TRF1305B1 (続き)

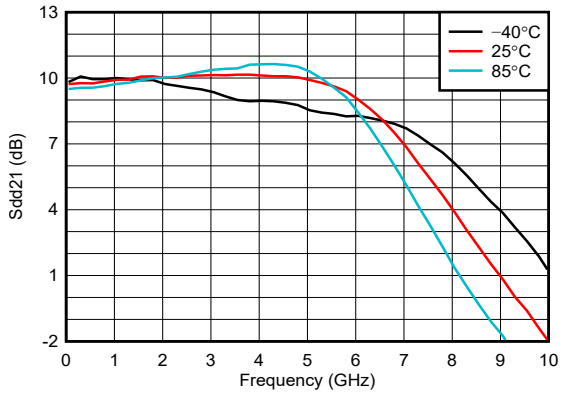
at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output with differential source impedance (Z_S) = 100Ω, differential output load (Z_L) = 100Ω, external input resistor network (see 図 8-3), and inputs de-embedded up to R_{IN_SER} and outputs up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise figure	f = 500MHz		8		dB
		f = 1GHz		8.6		
		f = 2GHz		10.4		
		f = 3GHz		11.6		
		f = 4GHz		13.4		
		f = 5GHz		13.2		
NSD	Output noise spectral density	f = 500MHz		–156.2		dBm/Hz
		f = 1GHz		–155.5		
		f = 2GHz		–153.6		
		f = 3GHz		–152.3		
		f = 4GHz		–150.5		
		f = 5GHz		–150.8		
DC PERFORMANCE						
V_{OD-MAX}	Max differential output voltage	f = 1GHz		4		V_{PP}
	Slew rate	2V V_O step, S2D configuration, V_{S+} = 2.5V, $V_{S–}$ = –2.5V		25		kV/µs
	Output differential offset voltage			±3		mV
	Overdrive recovery time	From 2 × overdrive of each SE output to each output voltage settling to < ±50mV		6		ns
COMMON-MODE						
V_{ICM}	Input common-mode voltage	Default range(1)	$V_{S–}$ + 1.5		$V_{S–}$ + 3.5	V
V_{OCM}	Output common-mode voltage		$V_{S–}$ + 2		$V_{S–}$ + 3	V
	Output common-mode offset voltage from V_{OCM} voltage			±10		mV
IMPEDANCE						
Z_{in-SE}	Single-ended input impedance	At INP pin with appropriate termination on INM pin		47		Ω
Z_{O-DIFF}	Differential output impedance	f = near dc		8		Ω
POWER SUPPLY						
I_{QA}	Active quiescent current			95		mA
I_{QPD}	Power-down quiescent current			13.5		mA
POWER DOWN						
V_{PD_Hi}	PD pin logic high	Referenced to GND, see セクション 6.1	1.35			V
V_{PD_Lo}	PD pin logic low	Referenced to GND, see セクション 6.1			0.3	V
I_{PD_Bias}	PD bias current (current on PD pin)	PD = high (1.8V logic)		10.5	15	µA
		PD = high (3.3V logic)		19	30	
t_{ON}	Turn-on time	From 50% V_{PD} transition to 90% RF out		25		ns
t_{OFF}	Turn-off time	From 50% V_{PD} transition to 10% RF out		20		ns

(1) V_{ICM} range can be extended closer to V_{S+} or $V_{S–}$ in D2D configuration. See also セクション 7.4.1.

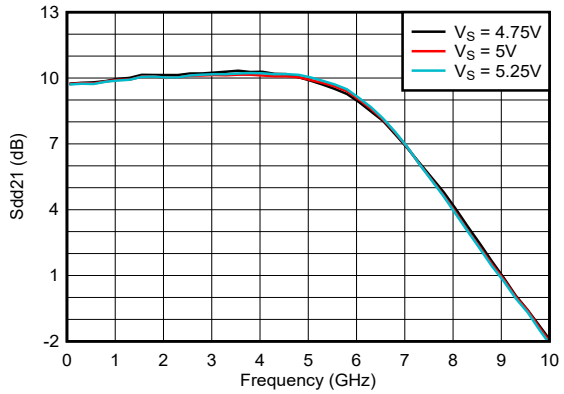
6.6 Typical Characteristics - TRF1305B1

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



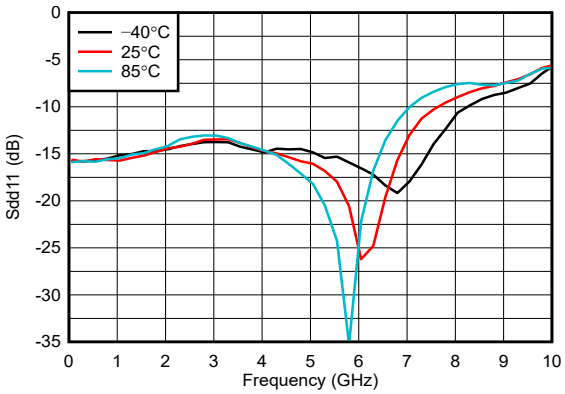
P_{IN} = –20dBm at each input pin with 50Ω source

図 6-1. Power Gain (Sdd21) Across Temperature



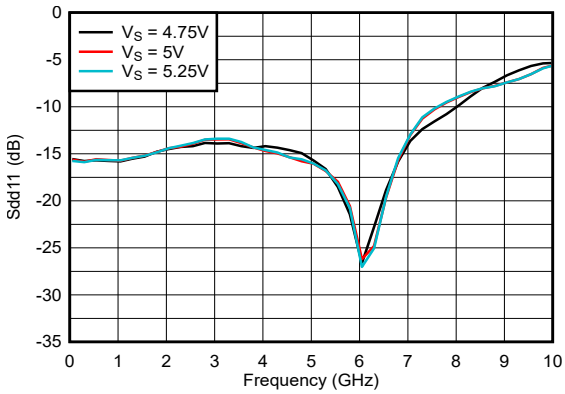
P_{IN} = –20dBm at each input pin with 50Ω source

図 6-2. Power Gain (Sdd21) Across Supply Voltage



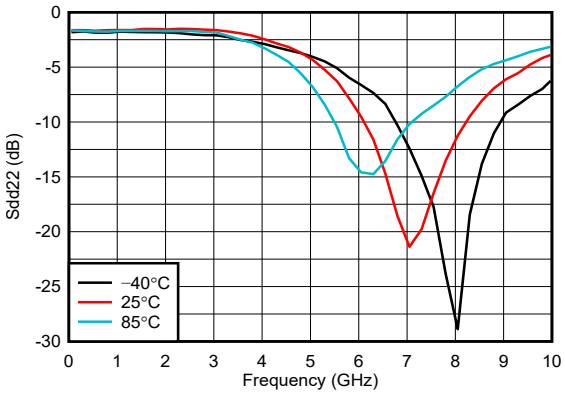
P_{IN} = –20dBm at each input pin with 50Ω source

図 6-3. Input Return Loss (Sdd11) Across Temperature



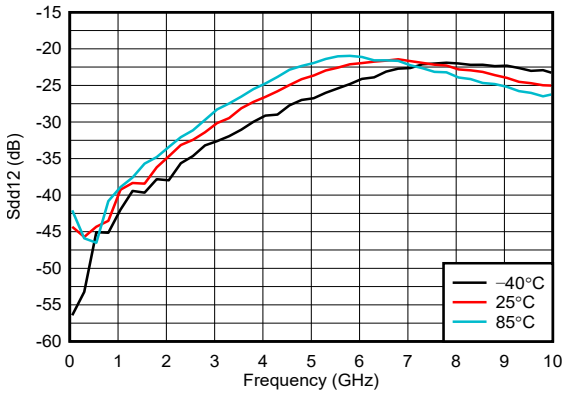
P_{IN} = –20dBm at each input pin with 50Ω source

図 6-4. Input Return Loss (Sdd11) Across Supply Voltage



P_{IN} = –20dBm at each input pin with 50Ω source

図 6-5. Output Return Loss (Sdd22) Across Temperature

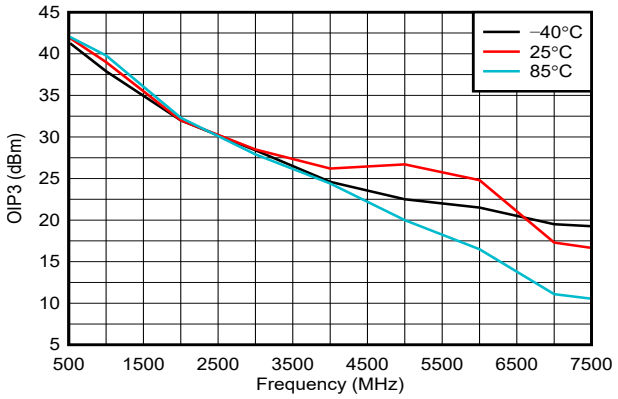


P_{IN} = –20dBm at each input pin with 50Ω source

図 6-6. Reverse Isolation (Sdd12) Across Temperature

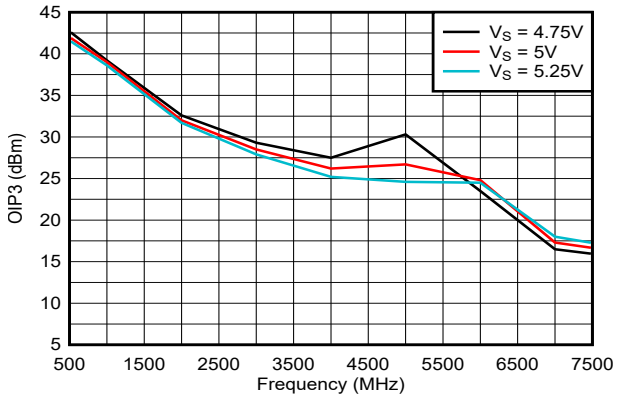
6.6 Typical Characteristics - TRF1305B1 (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



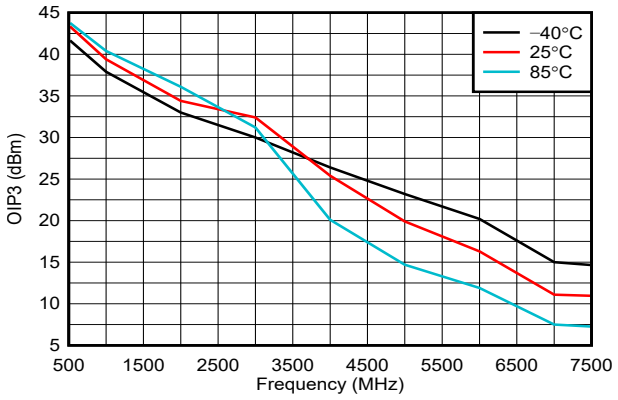
P_O = –5dBm/tone, 2MHz tone spacing

図 6-7. OIP3 Across Temperature



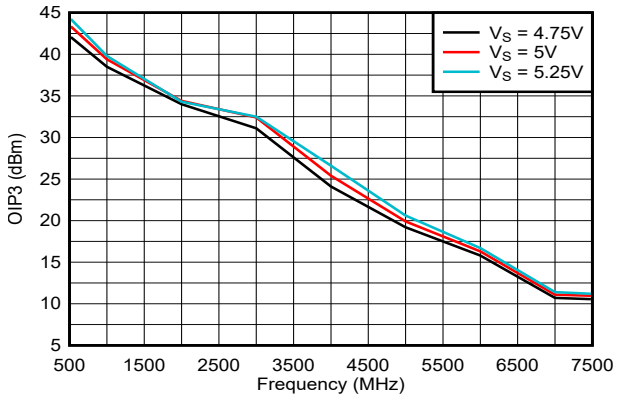
P_O = –5dBm/tone, 2MHz tone spacing

図 6-8. OIP3 Across Supply Voltage



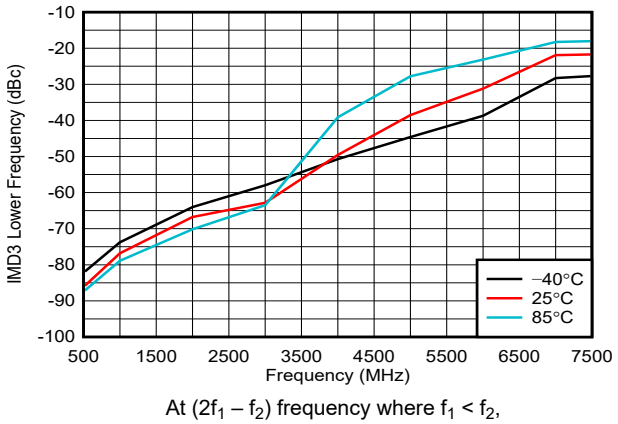
P_O = 1dBm/tone, 2MHz tone spacing

図 6-9. OIP3 Across Temperature



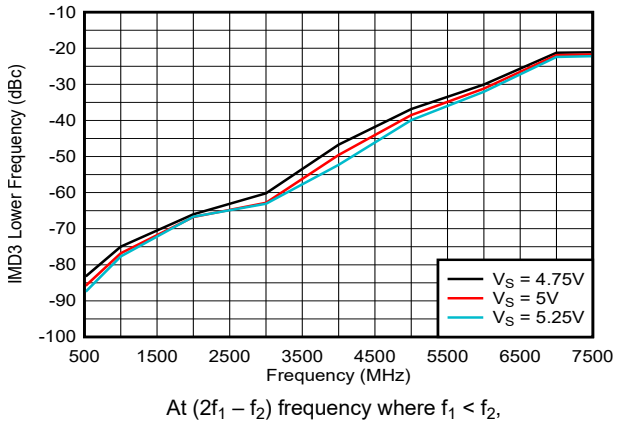
P_O = 1dBm/tone, 2MHz tone spacing

図 6-10. OIP3 Across Supply Voltage



At ($2f_1 – f_2$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

図 6-11. IMD3 Lower Across Temperature

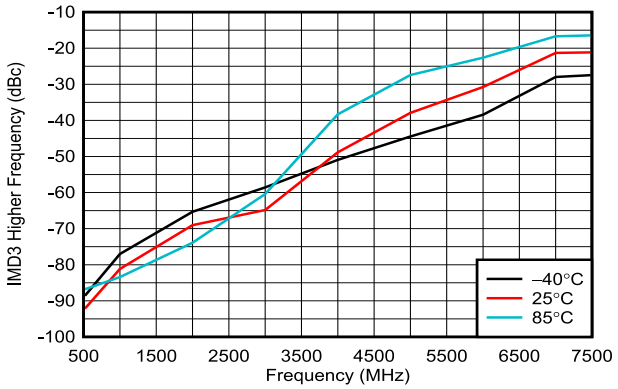


At ($2f_1 – f_2$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

図 6-12. IMD3 Lower Across Supply Voltage

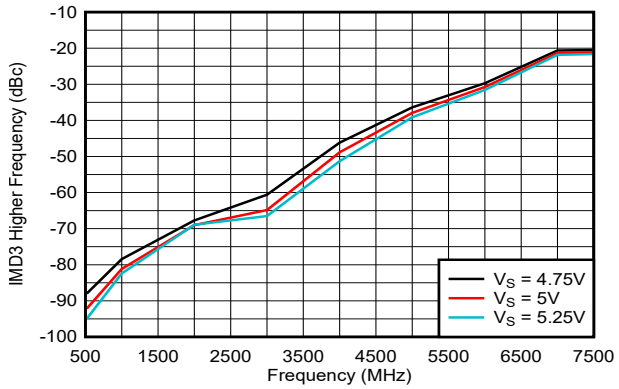
6.6 Typical Characteristics - TRF1305B1 (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



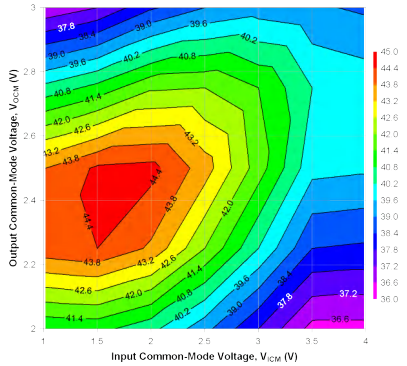
At ($2f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

図 6-13. IMD3 Higher Across Temperature



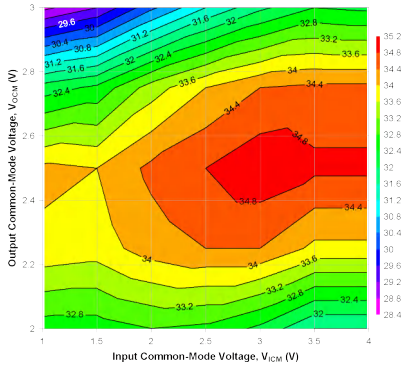
At ($2f_2 – f_1$) frequency where $f_1 < f_2$,
P_O = 1dBm/tone, 2MHz tone spacing

図 6-14. IMD3 Higher Across Supply Voltage



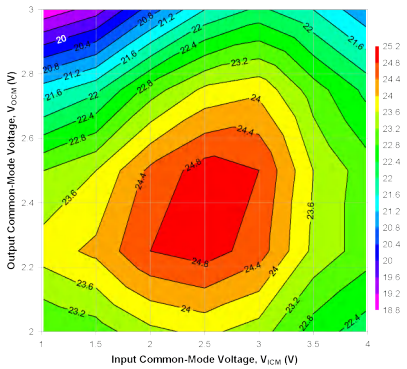
P_O = 1dBm/tone, 2MHz tone spacing,
dc-coupled inputs with V_{ICM} forced through bias tees

図 6-15. OIP3 Across V_{ICM} and V_{OCM} at 500MHz



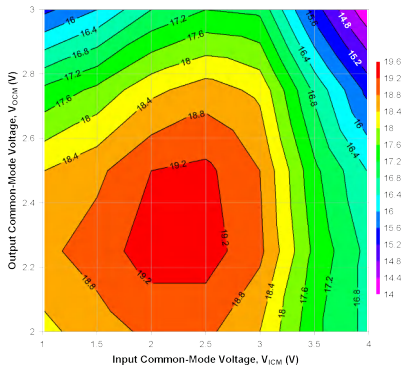
P_O = 1dBm/tone, 2MHz tone spacing,
dc-coupled inputs with V_{ICM} forced through bias tees

図 6-16. OIP3 Across V_{ICM} and V_{OCM} at 2GHz



P_O = 1dBm/tone, 2MHz tone spacing,
dc-coupled inputs with V_{ICM} forced through bias tees

図 6-17. OIP3 Across V_{ICM} and V_{OCM} at 4GHz

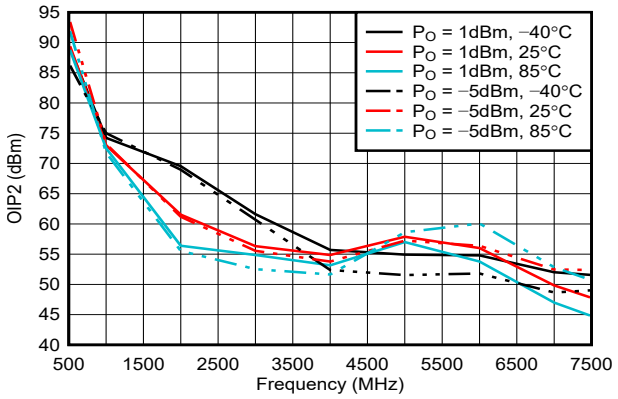


P_O = 1dBm/tone, 2MHz tone spacing,
dc-coupled inputs with V_{ICM} forced through bias tees

図 6-18. OIP3 Across V_{ICM} and V_{OCM} at 5GHz

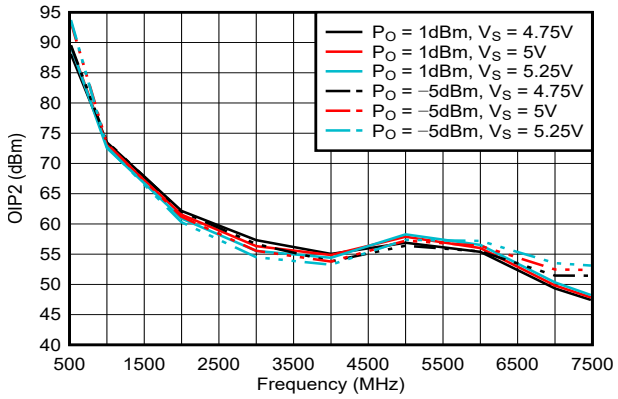
6.6 Typical Characteristics - TRF1305B1 (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



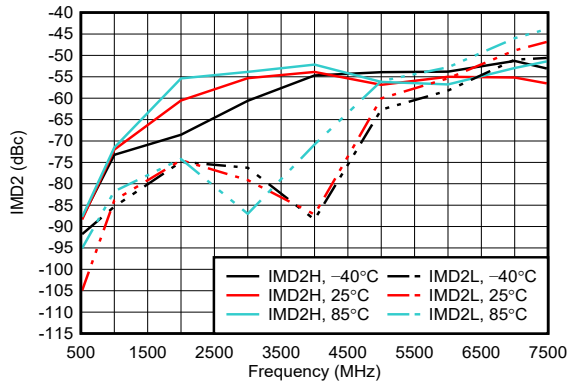
Per tone P_O as shown, 2MHz tone spacing

図 6-19. OIP2 Across Temperature



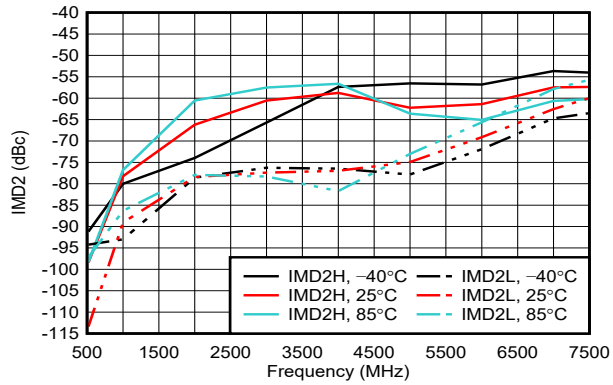
Per tone P_O as shown, 2MHz tone spacing

図 6-20. OIP2 Across Supply Voltage



P_O = 1dBm/tone, 2MHz tone spacing

図 6-21. IMD2 Across Temperature



P_O = –5dBm/tone, 2MHz tone spacing

図 6-22. IMD2 Across Temperature

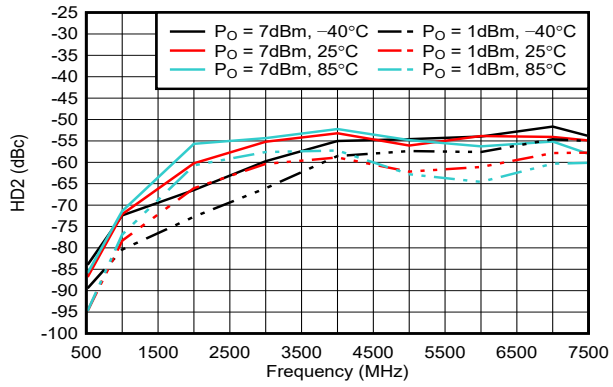


図 6-23. HD2 Across Output Power and Temperature

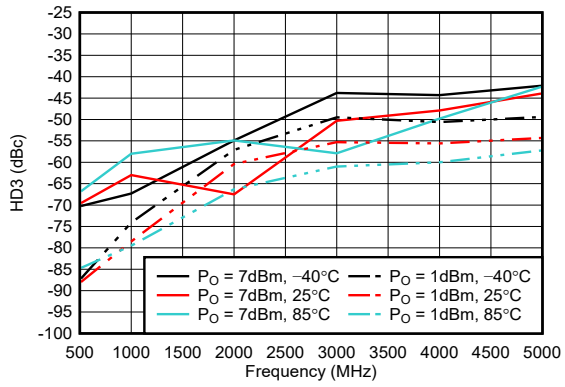


図 6-24. HD3 Across Output Power and Temperature

6.6 Typical Characteristics - TRF1305B1 (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

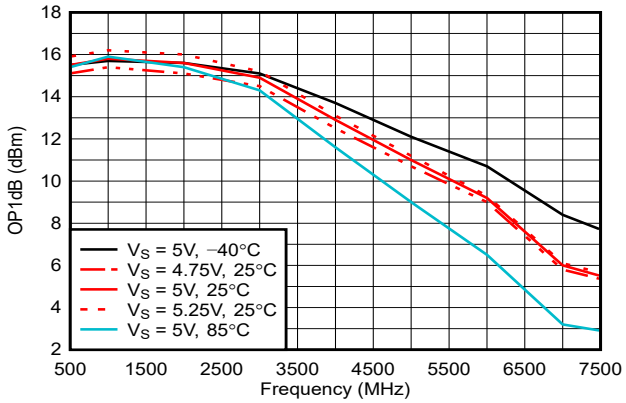


図 6-25. OP1dB Across Supply Voltage and Temperature

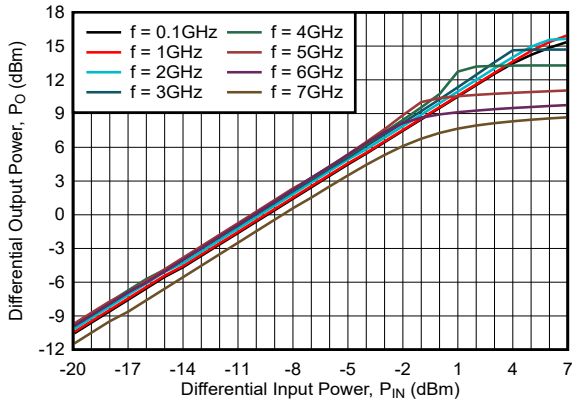


図 6-26. Differential Input vs Differential Output Power

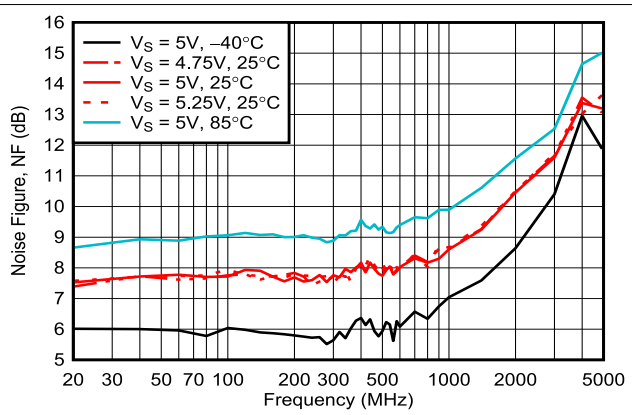


図 6-27. Noise Figure Across Temperature

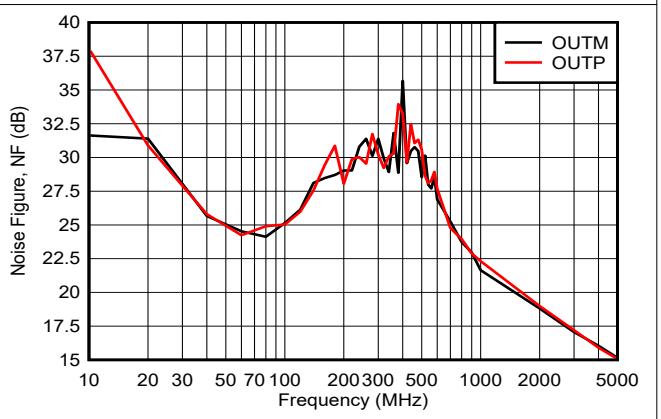
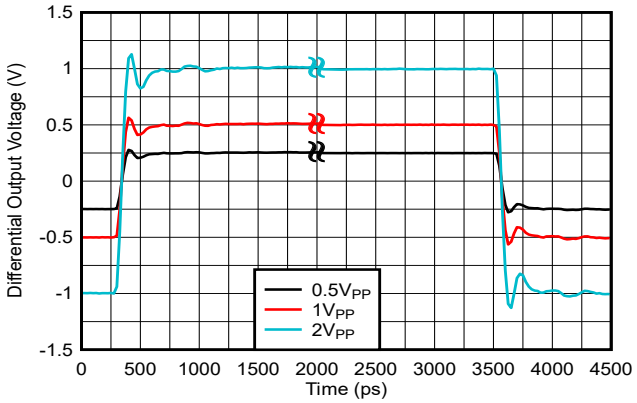


図 6-28. Noise Figure at Each Single-Ended Output

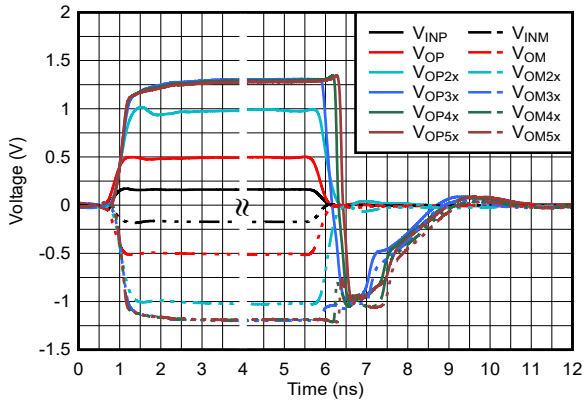
6.6 Typical Characteristics - TRF1305B1 (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



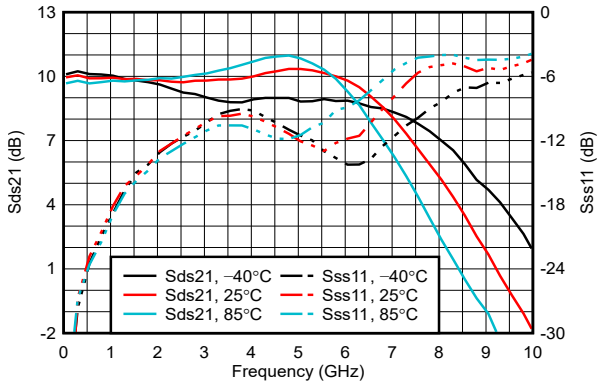
dc-coupled, V_{S+} = 2.5V, $V_{S–}$ = –2.5V

図 6-29. Step Response



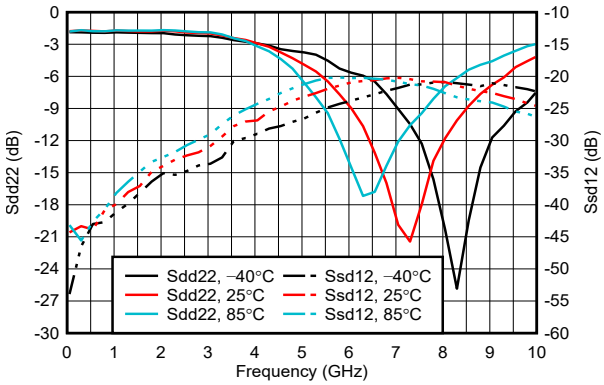
dc-coupled, V_{S+} = 2.5V, $V_{S–}$ = –2.5V, 2x to 5x output voltages are with an input voltage 2 to 5 times of V_{INP} and V_{INM} as shown, respectively

図 6-30. Overdrive Recovery Response



S2D, P_{IN} = –20dBm at each input pin with 50Ω source, de-embedded up to INP and OUTP/OUTM pins

図 6-31. S-Parameters Across Temperature in S2D Configuration

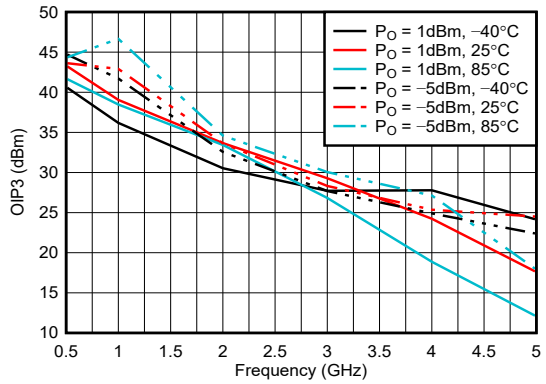


S2D, P_{IN} = –20dBm at each input pin with 50Ω source, de-embedded up to INP and OUTP/OUTM pins

図 6-32. S-Parameters Across Temperature in S2D Configuration

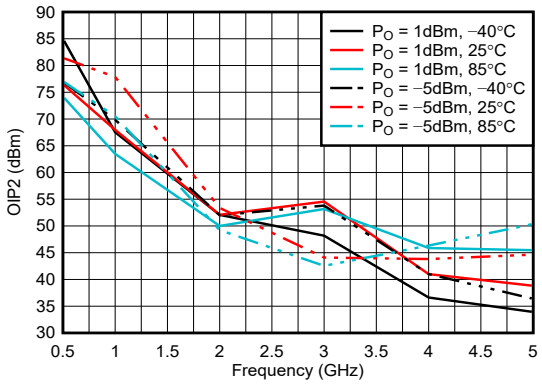
6.6 Typical Characteristics - TRF1305B1 (continued)

at T_A = 25℃, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



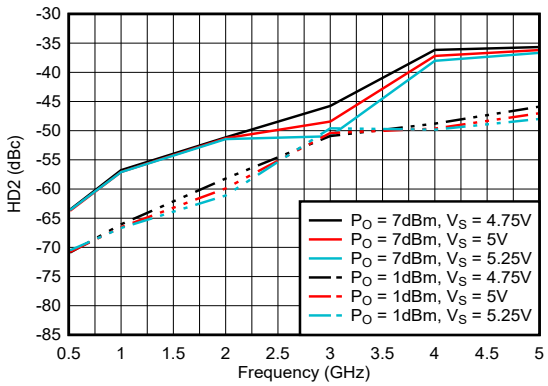
S2D, per tone P_O as shown, 2MHz tone spacing, de-embedded up to INP and OUTP/OUTM pins

図 6-33. OIP3 Across Temperature and Output Power



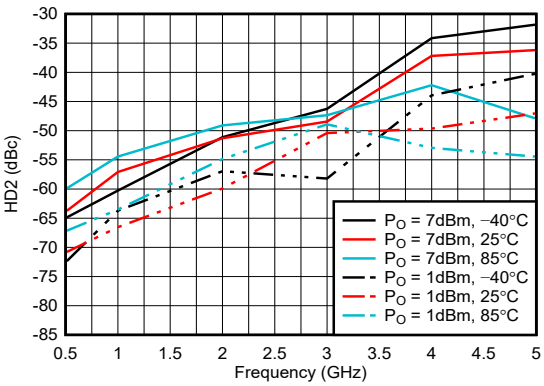
S2D, per tone P_O as shown, 2MHz tone spacing, de-embedded up to INP and OUTP/OUTM pins

図 6-34. OIP2 Across Temperature and Output Power



S2D configuration
de-embedded up to INP and OUTP/OUTM pins

図 6-35. HD2 Across Supply Voltage and Output Power

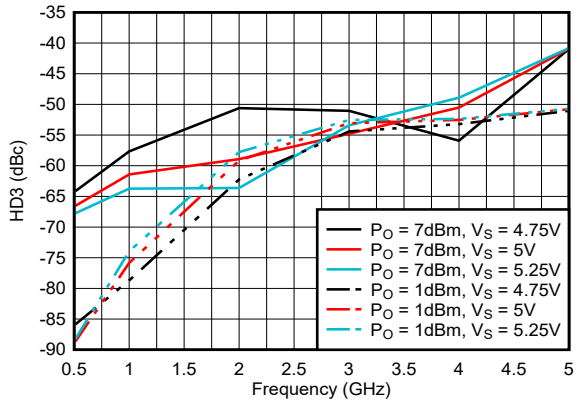


S2D configuration
de-embedded up to INP and OUTP/OUTM pins

図 6-36. HD2 Across Temperature and Output Power

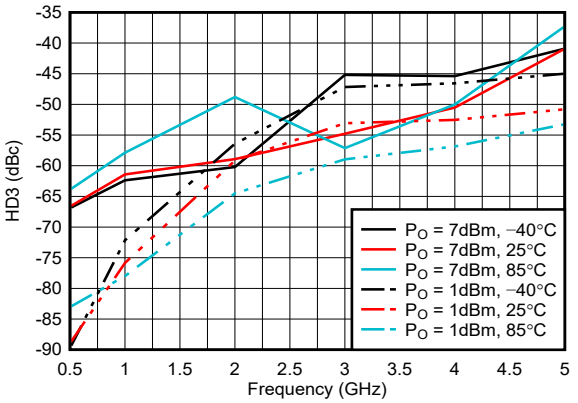
6.6 Typical Characteristics - TRF1305B1 (continued)

at T_A = 25°C, V_{S+} = 5V, V_{S-} = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



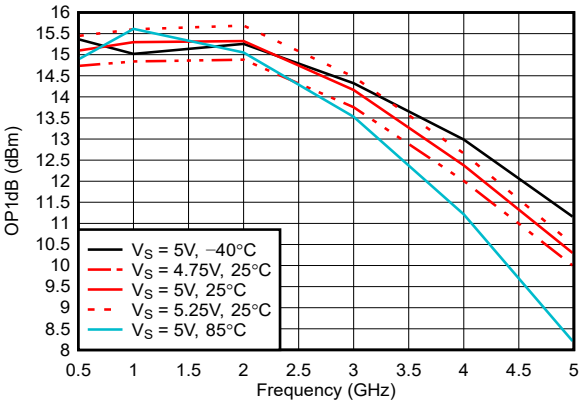
S2D configuration
de-embedded up to INP and OUTP/OUTM pins

図 6-37. HD3 Across Supply Voltage and Output Power



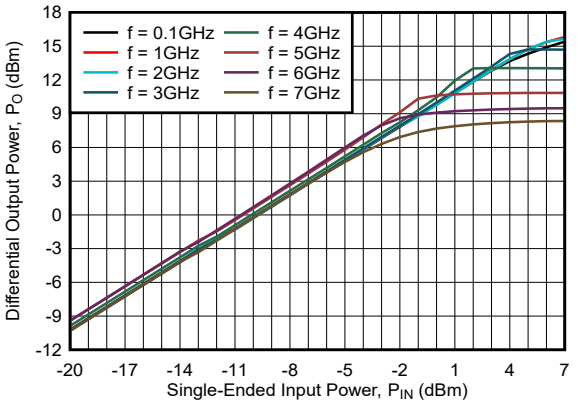
S2D configuration
de-embedded up to INP and OUTP/OUTM pins

図 6-38. HD3 Across Temperature and Output Power



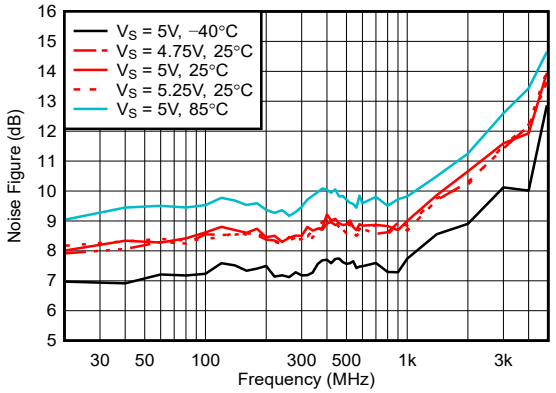
S2D, de-embedded up to INP and OUTP/OUTM pins

図 6-39. OP1dB Across Supply Voltage and Temperature



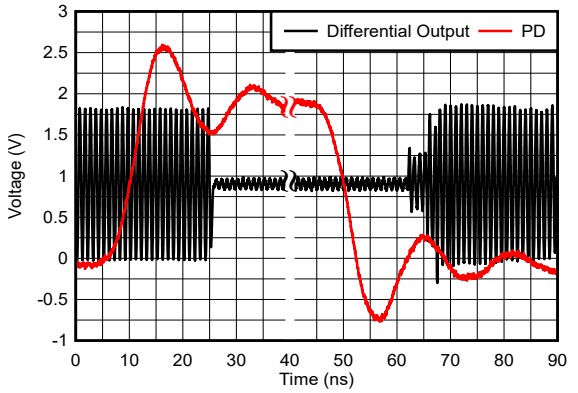
S2D, de-embedded up to INP and OUTP/OUTM pins

図 6-40. Single-Ended Input vs Differential Output Power



S2D, de-embedded up to INP and OUTP/OUTM pins

図 6-41. Noise Figure in S2D Configuration

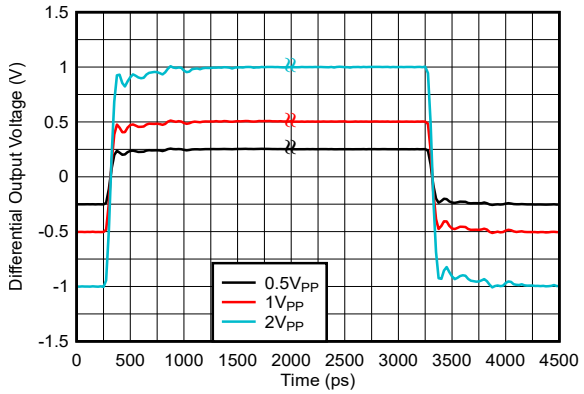


S2D, dc-coupled, V_{S+} = 2.5V, V_{S-} = –2.5V

図 6-42. Power Up and Power Down Timing

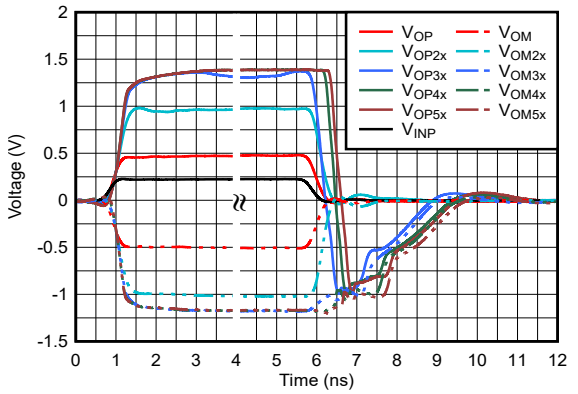
6.6 Typical Characteristics - TRF1305B1 (continued)

at T_A = 25℃, V_{S+} = 5V, $V_{S–}$ = 0V, floating VOCM, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with Z_S = 100Ω, Z_L = 100Ω, external input resistor network (see 図 8-3), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



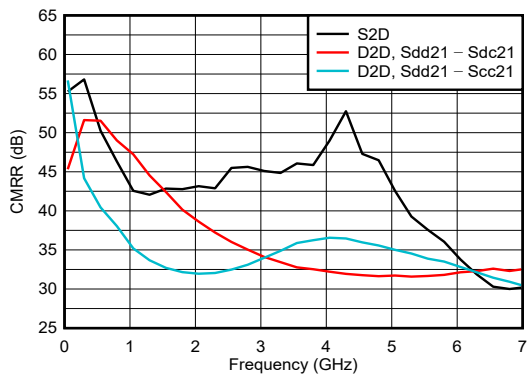
S2D, dc-coupled, V_{S+} = 2.5V, $V_{S–}$ = –2.5V

図 6-43. S2D Step Response



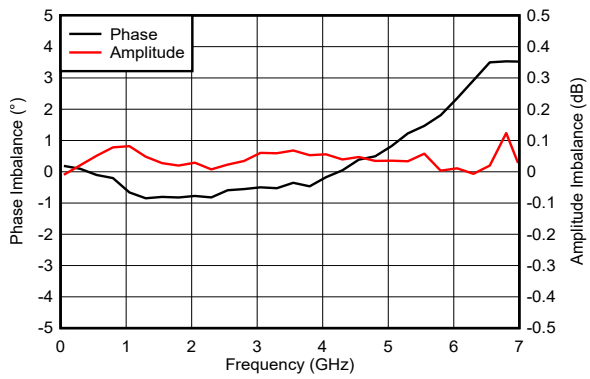
S2D, dc-coupled, V_{S+} = 2.5V, $V_{S–}$ = –2.5V,
2x to 5x output voltages are with an input voltage 2 to 5 times that of V_{INP} as shown, respectively

図 6-44. S2D Overdrive Recovery Response



P_{IN} = –20dBm at each driven input pin with 50Ω source,
c in Sdc21 and Scc21 is for common-mode

図 6-45. Common-Mode Rejection Ratio (CMRR)



S2D, P_{IN} = –20dBm at each input pin with 50Ω source

図 6-46. Amplitude and Phase Imbalance

7 Detailed Description

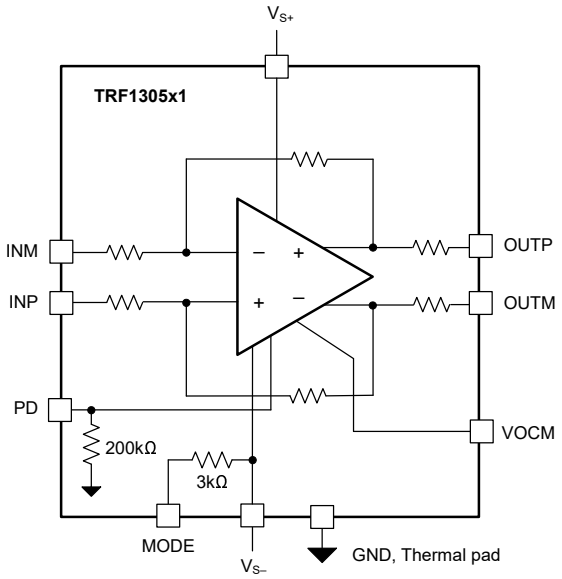
7.1 Overview

The TRF1305A1, TRF1305B1, and TRF1305C1 (TRF1305x1) devices are シングル チャネル, high-performance fully differential RF amplifiers optimized for very wideband signals from dc to > 7GHz. This device family is primarily designed to interface with high-speed and RF data converters that often require differential input (ADCs) and output (DACs) signaling. The TRF1305x1 can be dc or ac coupled, and configured as single-ended input and differential output (S2D) or differential input and differential output (D2D). The devices feature an output common-mode pin (VOCM) that allows the flexibility to set a desired common-mode output voltage. The amplifier allows the data converters to interface with a dc-coupled IQ demodulator or modulator if used in a direct conversion system. The TRF1305x1 family comes in three fixed power gain variants (15dB, 10dB, and 5dB), and has a closed-loop feedback-amplifier architecture.

The devices are powered using two-rail supplies with a typical differential voltage of 5V between the positive and negative supplies, and usable in split- or single-supply configurations. A power-down feature is also available that allows the amplifier to be powered down.

The output of the amplifiers is low impedance. Use appropriate external series termination or resistive pad to match to an arbitrary impedance.

7.2 Functional Block Diagram



7.3 Feature Description

The TRF1305x1 includes the following key features:

- Two-rail floating supply with supply-independent thermal pad
  - Connect the thermal pad to GND
  - RF signals and PD pin are referenced to GND
- Single-supply or split-supply operation
- Supports single-ended and differential input configurations
- Performance-optimized preset fixed-gain variants
- Output common-mode control
- MODE pin: V_{ICM} range extension closer to V_{S+} or V_{S-} modes
- Digital-logic-controllable power-down option

7.3.1 Fully Differential RF Amplifier

The TRF1305x1 is a voltage-feedback fully differential amplifier (FDA) with wide bandwidth. The amplifier is designed for a differential power gain of 15dB, 10dB, or 5dB depending on the device variant. This amplifier has excellent time-domain specifications with high slew rate, high input and output common-mode ranges, and fast transient settling time.

The output average voltage (common-mode) of the FDA device is controlled by a separate common-mode loop. The target output common-mode voltage is set by the VOCM input pin.

7.3.2 Output Common-Mode Control

図 7-1 shows a functional diagram of the output common-mode control. Internally, the VOCM pin potential is set by the LDO output voltage that is equal to $V_{S–}$ + 2.5V connected through a 2.5kΩ resistor.

Floating the VOCM pin is allowed. The output common-mode voltage at the output pins, OUTP and OUTM, defaults to the LDO output voltage of $V_{S–}$ + 2.5V when VOCM pin is floated. Floating the VOCM pin results in a V_{OCM} voltage equal to midsupply when V_S = 5V. If the VOCM pin is driven, then drive the pin from a low-impedance source. Limit the value of R_{OCM} to less than 25Ω for accurate reflection of the forced V_{OCM} voltage at the device outputs.

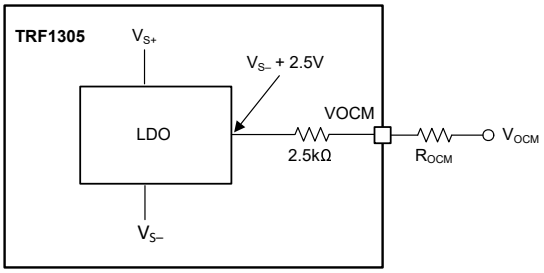


図 7-1. Output Common-Mode Control

7.3.3 Internal Resistor Configuration

図 7-2 shows the internal resistor configurations of TRF1305x1. 表 7-1 provides the values of these resistors for different gain variants.

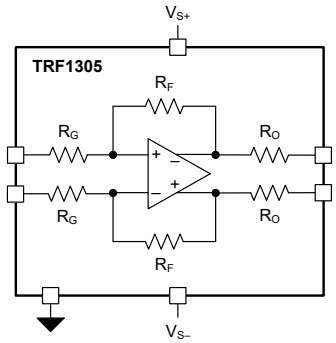


図 7-2. TRF1305x1 Internal Resistor Configuration

表 7-1. Resistor Values

DEVICE NAME	GAIN (dB)	R_G (Ω)	R_F (Ω)	R_O (Ω)
TRF1305A1	15	6.25	258	4
TRF1305B1	10	12.5	161	4
TRF1305C1	5	17	97	4

7.4 Device Functional Modes

7.4.1 MODE Pin

The TRF1305x1 have additional useful features that can be configured using the MODE pin. To select the device mode, either connect a ±2% maximum tolerance pullup resistor between the MODE pin and VS+, or force a voltage on the MODE pin. Internally, the MODE pin is referenced to $V_{S–}$ through a 3kΩ resistor (see セクション 7.2).

表 7-2 provides the value of the pullup resistor for each mode, the expected voltage, V_{MODE}, at the MODE pin when the pullup resistor is used or the necessary V_{MODE} voltage to set the device mode, and the mode configurations. The V_{MODE} voltage thresholds are approximately midway between the adjacent modes typical V_{MODE} voltage. If the mode functionality is used, use a decoupling capacitor on the MODE pin.

表 7-2. MODE Pin Configuration

MODE NUMBER	PULLUP RESISTOR TO VS+ (±2% MAXIMUM TOLERANCE)	MODE PIN VOLTAGE, V_{MODE} (V)	V_{ICM} RANGE EXTENSION(1)
0	OPEN	$V_{S–}$	Default V_{ICM} range
1	28.7kΩ	$V_{S–}$ + 0.5V	Low side, extends V_{ICM} range closer to $V_{S–}$
2	12.7kΩ	$V_{S–}$ + 1V	High side, extends V_{ICM} range closer to V_{S+}
N/A	Do not use pullup resistor < 10kΩ or do not set V_{MODE} > $V_{S–}$ + 1.15V		

(1) Only available in D2D configuration.

To switch the mode without turning the supplies off, use a switch or MUX connected between the pullup resistor options and VS+, or force a mode-appropriate V_{MODE} voltage. However, powering down the device using the power-down feature between mode changes is preferred. The low-side and high-side V_{ICM} range extension modes source and sink currents, respectively (see also セクション 7.4.1.1). Ensure that the external circuitry is ready to sink or source these currents before the device is put in the active mode from the powered-down state.

7.4.1.1 Input Common-Mode Extension

The TRF1305x1 supports a V_{ICM} voltage closer to either V_{S+} or $V_{S–}$ voltage than the default specified input common-mode range in the *Electrical Characteristics*, when configured in one of the V_{ICM} extension modes. The V_{ICM} extension mode can only be used in D2D configuration.

When configured in the low-side V_{ICM} extension mode, TRF1305B1 supports a 450mV lower input common-mode voltage than the default option. For example, the lower limit of V_{ICM} voltage range extends from a default value of $V_{S–}$ + 1.5V to $V_{S–}$ + 1.05V for the TRF1305B1 variant, and the higher limit also shifts lower from a default value of $V_{S–}$ + 3.5V to $V_{S–}$ + 3.05V. At the lowest V_{ICM} voltage, approximately 15mA current must be sunk by the external circuitry connected to the INP and INM pins.

When configured in the high-side V_{ICM} extension mode, TRF1305B1 supports a 450mV higher input common-mode voltage than the default option. For example, the higher limit of V_{ICM} voltage range extends from a default value of $V_{S–}$ + 3.5V to $V_{S–}$ + 3.95V for the TRF1305B1 variant, and the lower limit also shifts up from a default of $V_{S–}$ + 1.5V to $V_{S–}$ + 1.95V. At the highest V_{ICM} voltage, approximately 15mA current must be sourced by the external circuitry connected to the INP and INM pins.

Either resistors connected to supplies or external current sources can be used to sink or source the currents flowing out or into to the INP and INM pins during the low-side or high-side V_{ICM} extension modes, respectively.

7.4.2 Power-Down Mode

The TRF1305x1 have two bias modes, active and power-down, that are controlled by the voltage on the PD pin. The PD pin is referenced to GND through a 200kΩ resistor; see also セクション 7.2. If the V_{S+} ≥ 3.3V configuration is used, ensure that the PD voltage does not exceed the *Absolute Maximum Ratings* in case the high PD voltage is derived from V_{S+}.

Both 1.8V and 3.3V digital logic is supported for power-down control.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Input and Output Interface Considerations

8.1.1.1 Single-Ended Input

In the single-ended input configuration, one of the amplifier input pins is driven from a source while the other input is terminated with an external resistor. 図 8-1 shows an ac-coupled, single-ended input configuration driven from and matched to a 50Ω source. 図 8-1 shows how the non-driven INM pin is terminated with a 50Ω external resistor to match to a source with the same 50Ω impedance at the INP pin. The configuration shown in 図 8-1 works for all gain versions of TRF1305x1.

To configure the design in 図 8-1 for single-ended, dc-coupled input, replace the ac-coupling capacitors with shorts, and externally bias both INP and INM pins to a voltage close to the mid-supply or within the common-mode limits of the amplifier.

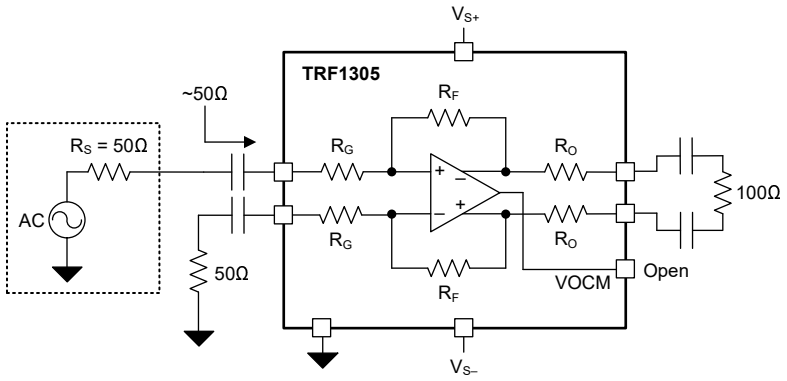


図 8-1. AC-Coupled, Single-Ended Input Matched to a 50Ω Source

8.1.1.2 Differential Input

図 8-2 shows how a simple network consisting of three resistors is used to match the differential input to a 100Ω differential source. Though the 1kΩ shunt resistor, R_{IN_SH}, does not have any impact at dc to low frequencies, the resistor is necessary to get the full wideband performance from TRF1305x1. 図 8-3 shows the configuration for ac-coupled differential input designs. The resistors values shown in 図 8-2 and 図 8-3 work for all gain versions of the TRF1305x1 for an 100Ω input match to a 100Ω differential source.

Use small foot-print resistors (0201 preferred), and RF quality for high-frequency matching.

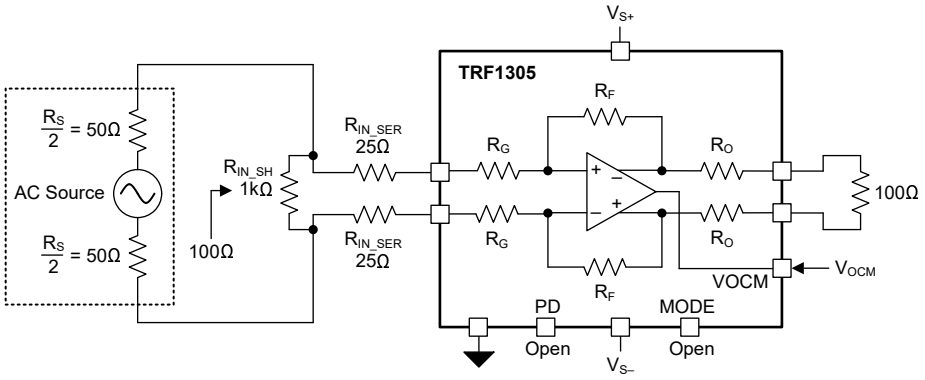


図 8-2. DC-Coupled Differential Input Matched to a 100Ω Differential Source

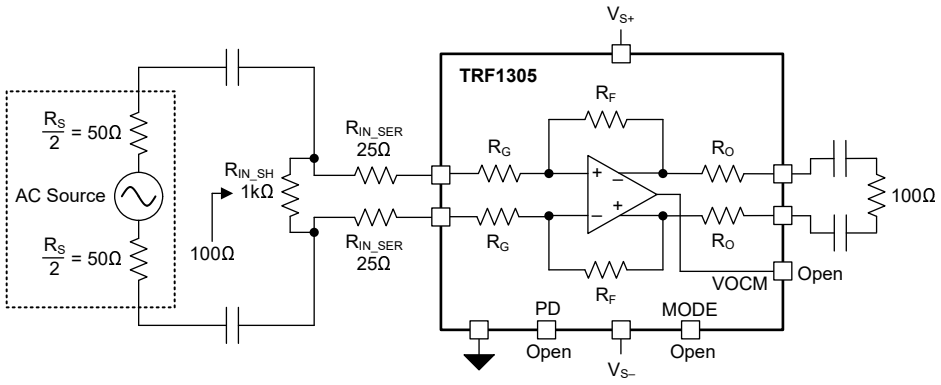


図 8-3. AC-Coupled Differential Input Matched to a 100Ω Differential Source

8.1.1.3 DC Coupling Considerations

The TRF1305x1 accepts a wide range of input dc common-mode (CM) voltages. Take into consideration the dc current loading of the source when the TRF1305x1 is dc-coupled at the input. 図 8-4 shows that when the input CM voltage, V_{ICM}, is different than the output CM voltage, V_{OCM}, a net dc current flow from or to the source occurs. 式 1 shows the relationship that the source or sink current, I_{CM}, has with the input and output CM voltages:

$$I_{CM} = \frac{(V_{OCM} - V_{ICM})}{(R_F + R_G)} \quad (1)$$

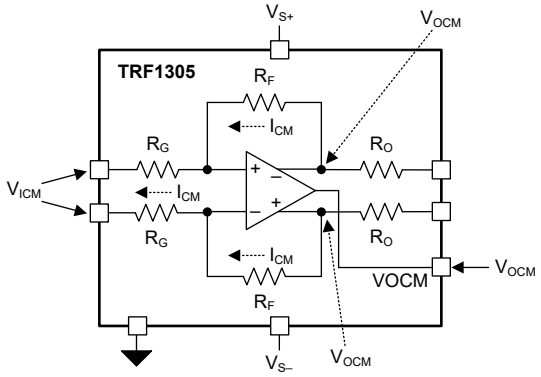


図 8-4. Net DC Current Flow When Input and Output Common-Mode Voltages are not Equal

8.1.2 Gain Adjustment With External Resistors in a Differential Input Configuration

The TRF1305x1 allow minor gain adjustments by configuring the input external resistive network that is part of the differential input configuration. 図 8-5 shows the external input network that comprises of a shunt resistor, R_{IN_SH}, and two series input resistors, R_{IN_SER}, connected to the input pins of the amplifier.

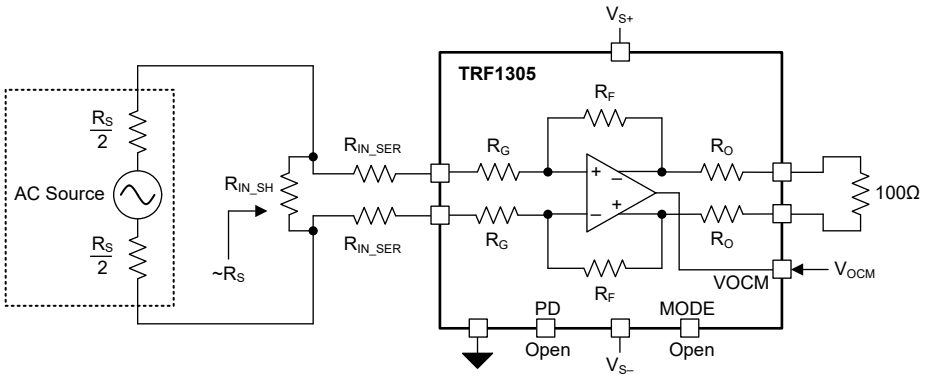


図 8-5. Gain Adjustment With External Resistor Network

表 8-1 provides resistor configurations for a 100Ω differential source impedance.

表 8-1. Resistor Table for R_S = 100Ω

TRF1305B1		
POWER GAIN (dB)	R_{IN_SH} (Ω)	R_{IN_SER} (Ω)
10	1000	25
9	408	30
8	267	35
7	204	41
6	169	47
5	146	54

Use external resistive attenuation network only for small gain adjustments because there is a dB-to-dB noise figure degradation with the resistive attenuators. Use an amplifier version that requires minimal attenuation for achieving the overall gain.

8.2 Typical Application

8.2.1 TRF1305x1 as ADC Driver in a Zero-IF Receiver

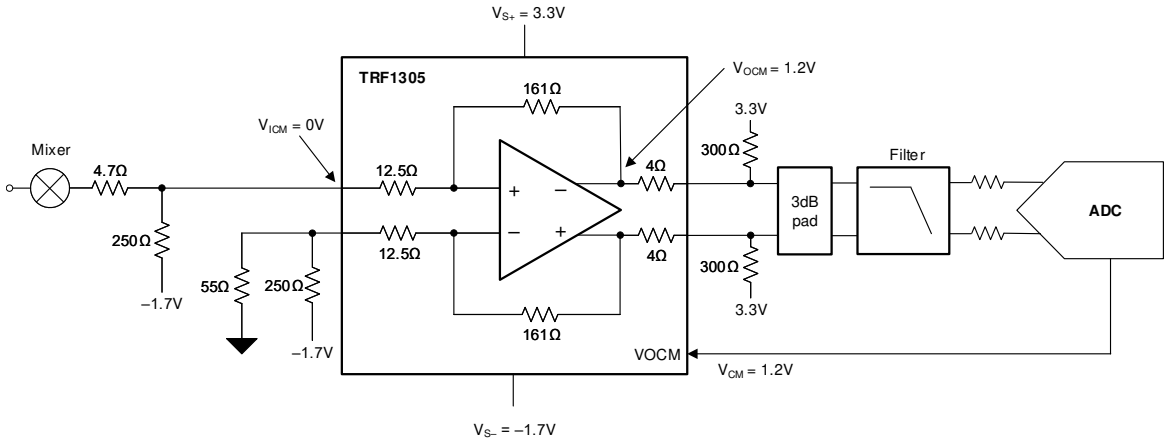


図 8-6. TRF1305x1 as ADC Driver in a Zero-IF Receiver

Consider a zero-IF (direct down conversion) application with an IQ demodulator interfaced to a pair of ADCs. In this case, the TRF1305x1 is used as an interface amplifier between the demodulator and the ADCs. The dc common-mode of the demodulator output and ADC input are different. The TRF1305x1 dc couples the demodulator to ADC without degrading the signal integrity of the signal chain.

8.2.1.1 Design Requirements

The primary design requirement for an IQ demodulator application is to interface a pair of passive mixers with an RF ADC. The mixers have a 0-V common-mode voltage. The ADC requires an input common-mode voltage of 1.2V with full-scale swing of 1.35V_{PP}. Choose the power supplies, and design the input/output network for the TRF1305x1 as the ADC driver amplifier, to perform the dc level shifting and amplification function.

8.2.1.2 Detailed Design Procedure

The first step is to choose the TRF1305x1 supplies. Ensure that the midsupply voltage, $V_{MIDSUPPLY}$, is between the ADC common-mode (CM) voltage and the mixer CM voltage. $V_{MIDSUPPLY}$ is typically positioned closer to the ADC CM because the output CM range of the amplifier is less than the input CM range. Ensure that the dc of the signal at the input and output of the amplifier are within the valid operating common-mode voltage range. Use the MODE pin for cases where an extended range of the input CM is required.

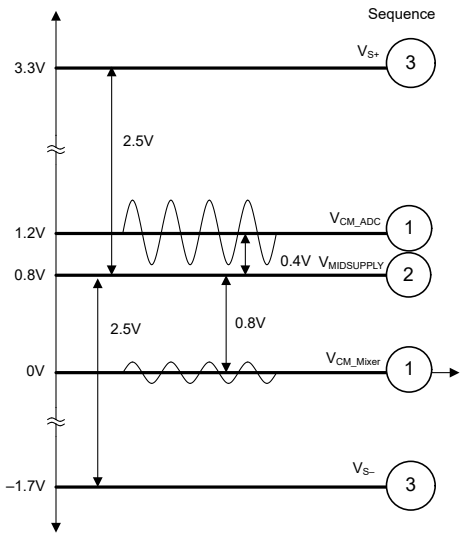


図 8-7. Choosing Supply Voltages With Given Common-Mode Voltages

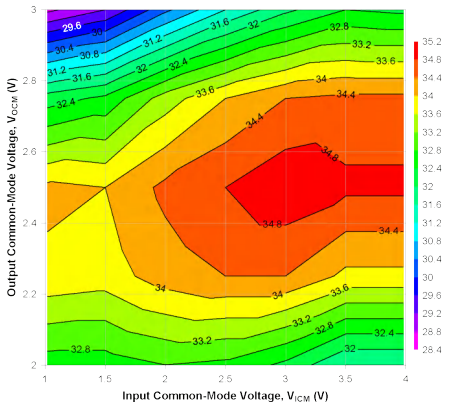
図 8-7 shows how $V_{MIDSUPPLY}$ is chosen to be 0.8V, so that the amplifier input has a CM offset from $V_{MIDSUPPLY}$ of 0.8V and output has a CM offset from $V_{MIDSUPPLY}$ of 0.4V (1.2V – 0.8V). The CM offsets are within the valid common-mode range of the amplifier, so the supplies of the TRF1305B1 are chosen to be V_{S+} = 3.3V (0.8V + 2.5V) and $V_{S–}$ = −1.7V (0.8V – 2.5V). Further optimization in the choice of supply is possible by selecting the input and output CM voltages for the best OIP3 performance. セクション 8.2.1.3 has contour graphs that show OIP3 across input and output common-mode voltages.

The output CM is greater than the input CM; therefore, a net 6.9-mA ((1.2V – 0V) / (161Ω + 12.5Ω)) dc current flows from the output to input through the internal feedback resistors. Depending on the choice of the passive mixer, this current can required to be sunk outside the mixer so that the bias conditions of the mixer are not disturbed. A 250Ω pulldown resistor connected to the INP pin to −1.7V supply is adequate. If the 6.9mA dc current is sourced entirely from the amplifier, then the output headroom can be affected. Therefore, source the current externally from the supply using a pair of pullup resistors connected to the amplifier outputs. 300Ω pullup resistors from OUTP and OUTM to 3.3V are adequate.

The I-channel mixer output has a 50Ω port and is connected to the amplifier INP pin through a small (4.7Ω) series resistor. The INM pin is terminated to ground through a 55Ω resistor and to −1.7V through a 250Ω resistor. This configuration allows the amplifier to have the same input impedance at each of the INP and INM input pins. The impedance of the mixer is close to 43Ω and provides better than a −20-dB return loss (theoretically). Be aware that there is some drop in the gain due to these resistor networks. The values of the resistors chosen in 図 8-6 are a good starting point; in practice, some adjustment is often needed to simultaneously meet the dc conditions and the RF performance.

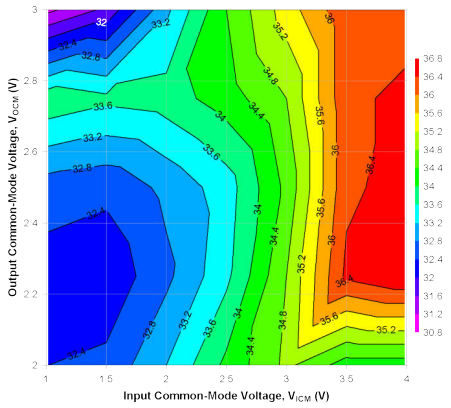
At the amplifier output, a 3dB pad with a 100Ω differential impedance is used to match to the antialiasing filter with a 100Ω differential input impedance. The filter output is connected to ADC with appropriate matching. 図 8-6 only shows the I-channel; the Q-channel has an identical configuration.

8.2.1.3 Application Curves



f = 2GHz, P_O/tone = 1dBm, 2MHz tone spacing

図 8-8. OIP3 Across Input and Output Common-Mode Voltage



f = 2GHz, P_O/tone = –5dBm, 2MHz tone spacing

図 8-9. OIP3 Across Input and Output Common-Mode Voltage

8.3 Power Supply Recommendations

8.3.1 Supply Voltages

For the TRF1305x1, the typical differential supply between VS+ and VS– is 5V. The VS+ and VS– supply pins can be floated with respect to ground within the specified range listed in the *Absolute Maximum Ratings* and *Recommended Operating Conditions*.

8.3.2 Single-Supply Operation

The VS– pin is connected to ground in the single-supply configuration. Single-supply operation is most convenient in ac-coupled configurations because the dc common-mode voltages of the source at the inputs and the driven circuit at the outputs are inherently decoupled.

8.3.3 Split-Supply Operation

In split-supply configuration, choose the V_{S+} and $V_{S–}$ voltages to be within the ranges specified in the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. The TRF1305x1 allows choosing negative voltages for the $V_{S–}$ supply, thereby allowing the flexibility to choose input and output common-mode voltages according to the input network and output network requirements.

8.3.4 Supply Decoupling

The VS+ and VS– supply pins are decoupled individually to ground using external capacitors. Place the decoupling capacitors close to the device supply pins.

8.4 Layout

8.4.1 Layout Guidelines

The TRF1305x1 devices are wideband closed-loop feedback amplifiers. When designing with wideband RF amplifiers that have high gain, take certain board layout precautions to maintain stability and optimized performance. Use a multilayer board to maintain signal integrity, power integrity, and thermal performance.

Route the RF input and output lines as grounded coplanar waveguide (GCPW) lines. Ground pins are the reference for the RF signals. Ensure that the second layer of the PCB has a continuous ground layer without any ground cutouts in the vicinity of the amplifier. To minimize phase imbalance, match the length of the output differential lines of both channels. Length matching the input traces is also important, especially if the input configuration is differential. Use small-footprint, passive components wherever possible.

For good heat dissipation, connect the device thermal pad to the board ground planes using thermal vias under the device. For improved heat dissipation, connect the device thermal pad to the top layer ground plane of the board.

8.4.1.1 Thermal Considerations

The TRF1305x1 are packaged in a WQFN-FCRLF package that has excellent thermal properties. Connect the thermal pads underneath the devices to the thermally dissipative ground plane on the board. For good thermal design, use thermal vias to connect the thermal pad plane on the top layer of the PCB to the ground planes in the inner layers.

8.4.2 Layout Example

図 8-10 shows an example layout for TRF1305x1 with a differential input configuration. Key areas are highlighted in the figure.

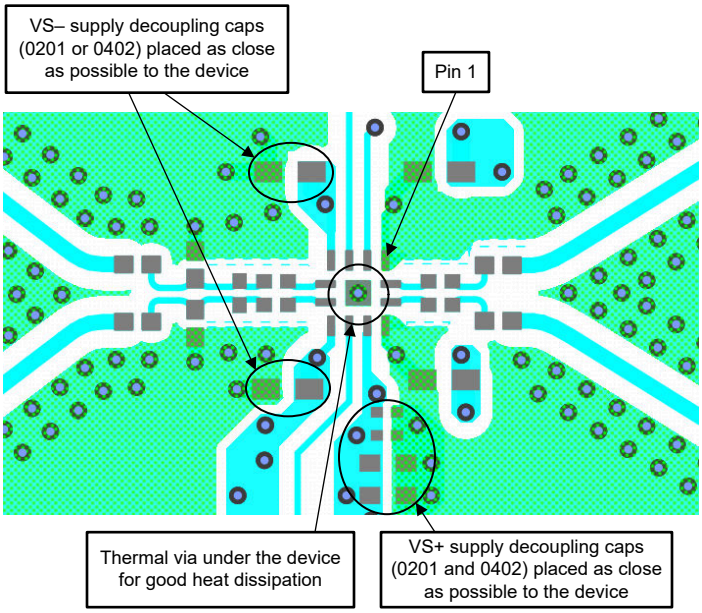


図 8-10. Layout Example: TRF1305x1 With Differential Input

The TRF1305x1 can be evaluated using EVM boards that can be ordered from the TRF1305B1 product folder. For more information about the evaluation board construction and test setup, see the *TRF1305x1 EVM User's Guide*.

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TRF1305x1-D2D EVM User's Guide*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2024) to Revision A (December 2024)	Page
• TRF1305B1 のステータスを「事前情報」から「量産データ」(アクティブ) に変更	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRF1305B1RPVR	Active	Production	WQFN-HR (RPV) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	135B
TRF1305B1RPVR.A	Active	Production	WQFN-HR (RPV) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	135B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

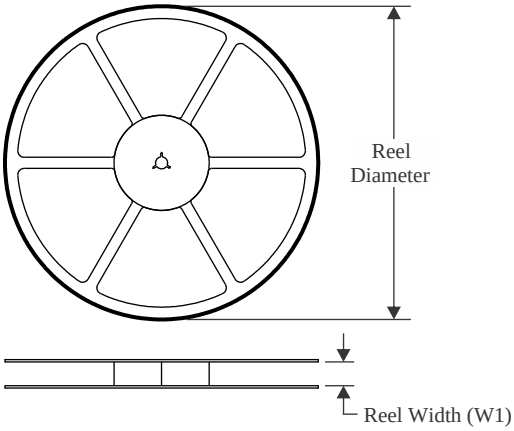
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

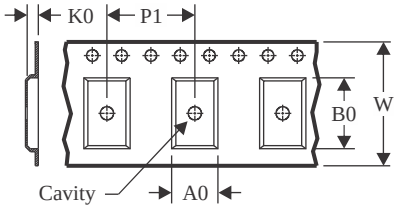
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

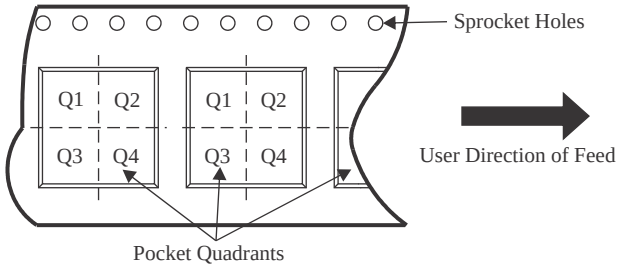


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

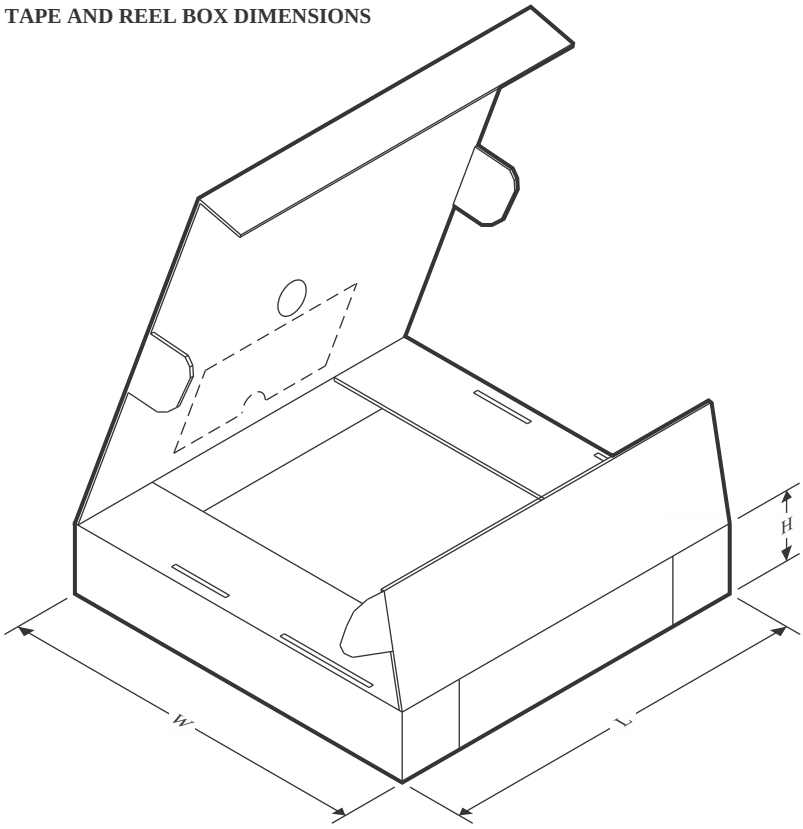
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1305B1RPVR	WQFN-HR	RPV	12	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

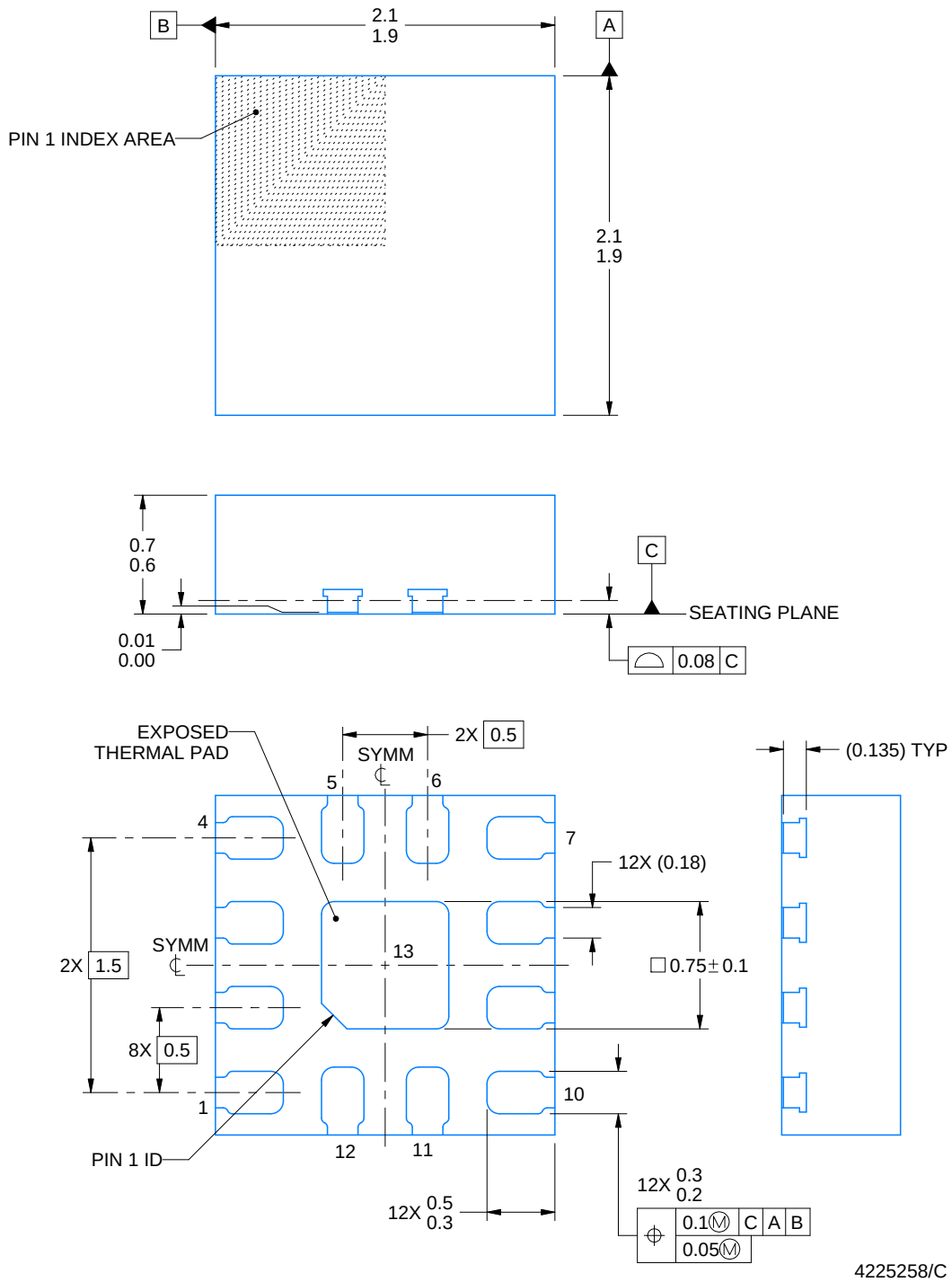
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1305B1RPVR	WQFN-HR	RPV	12	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPV0012A

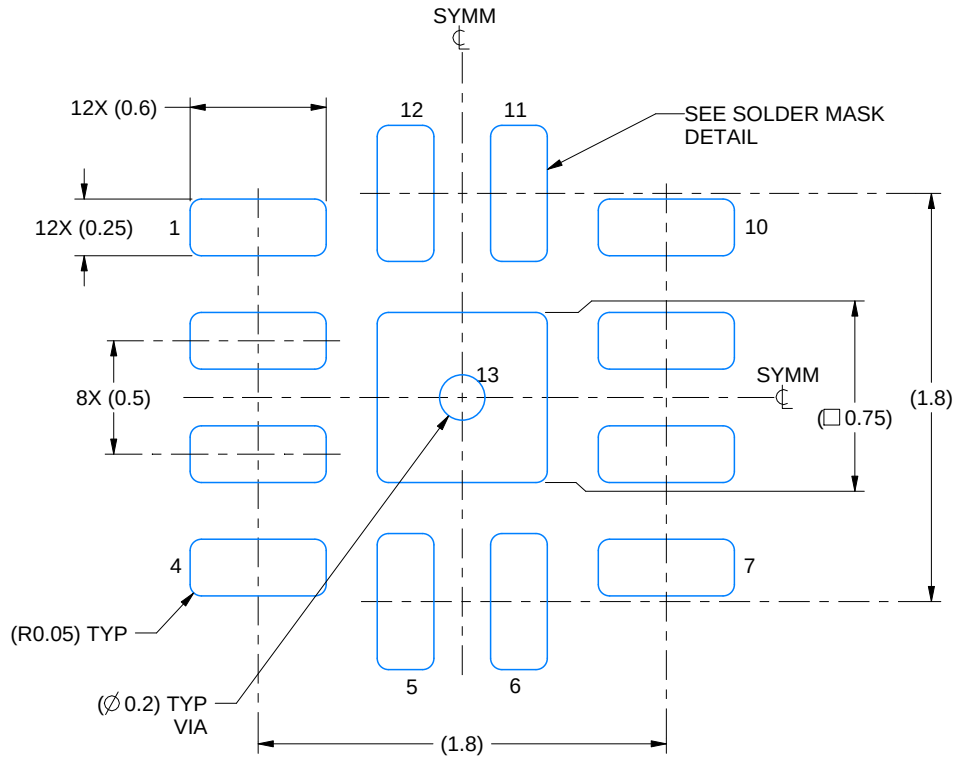
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

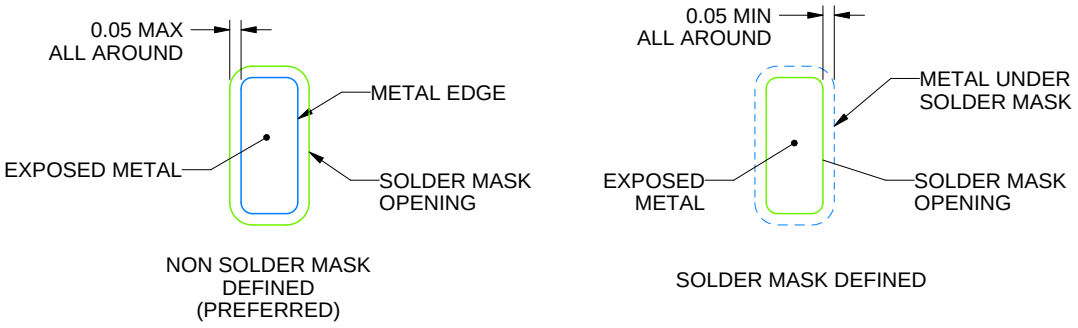


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

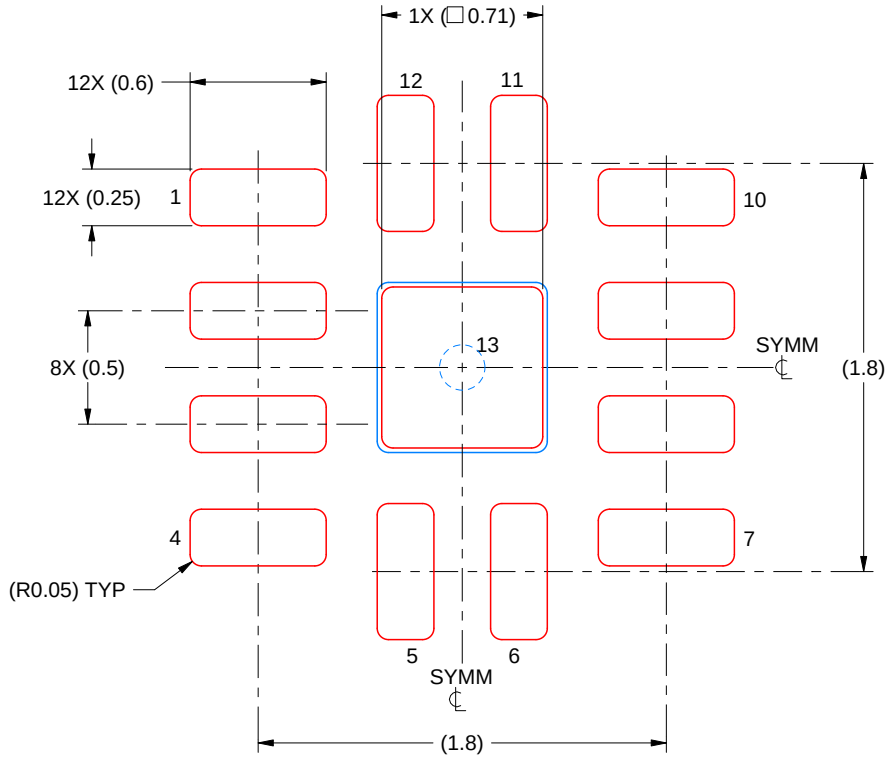


SOLDER MASK DETAILS

4225258/C 08/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225258/C 08/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月