TEXAS INSTRUMENTS

TRS232E
JAJST55D – JUNE 2007 – REVISED FEBRUARY 2024

TRS232E デュアル RS-232 ドライバ / レシーバ、IEC61000-4-2 保護機能搭載

1 特長

- TIA/RS-232-F および ITU 勧告 V.28 適合またはそれを上回る性能
- 1μF チャージ ポンプ コンデンサを使用して 5V 単一電源で動作
- 最大 250kbit/s で動作
- 2 つのドライバと 2 つのレシーバ
- ±30V の入力レベル
- 低い消費電流：8mA (代表値)
- RS-232 バス ピン用 ESD 保護機能
  - ±15kV 人体モデル (HBM)
  - ±8kV IEC 61000-4-2、接触放電
  - ±15kV IEC 61000-4-2、気中放電

2 アプリケーション

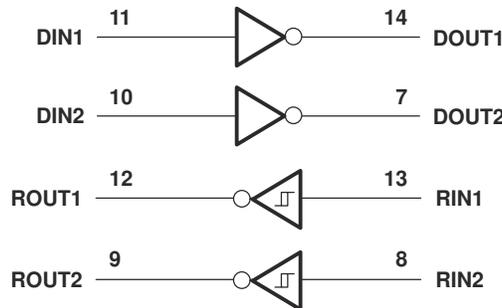- TIA/RS-232-F
- バッテリ駆動システム
- 端末
- モデム
- コンピュータ

3 概要

TRS232E は、5V 単一電源から TIA/RS-232-F の電圧レベルを供給する容量性電圧発生器を内蔵したデュアルドライバ / レシーバです。各レシーバは、TIA/RS-232-F の入力を 5V の TTL/CMOS レベルに変換します。このレシーバは、標準スレッショルドが 1.3V 、標準ヒステリシスが 0.5V で、±30V の入力を受け入れます。各ドライバは、TTL/CMOS 入力レベルを TIA/RS-232-F レベルに変換します。ドライバ、レシーバ、電圧発生器は、いずれもテキサス・インスツルメンツの LinASIC™ ライブラリのセルとして利用できます。

パッケージ情報

部品番号	パッケージ [1]	パッケージ サイズ [2]
TRS232E	SOIC (D、16)	9.9mm × 6mm
	SOIC (DW、16)	10.4mm × 10.3mm
	PDIP (N、16)	19.3mm × 9.4mm
	TSSOP (PW、16)	5mm × 6.4mm

(1) 詳細については、セクション 11 を参照してください。
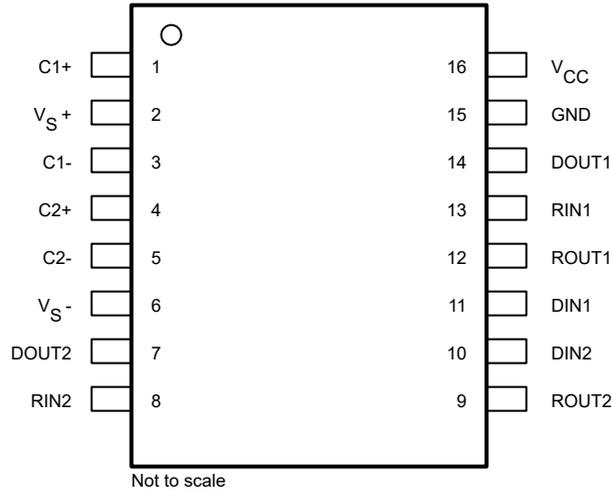(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

DIN1	11		14	DOUT1
DIN2	10		7	DOUT2
ROUT1	12		13	RIN1
ROUT2	9		8	RIN2

論理図 (正論理)

English Data Sheet: SLLS791

Table of Contents

Product Folder Links: *TRS232E*
English Data Sheet: SLLS791

4 Pin Configuration and Functions

図 4-1. D, DW, N, NS or PW Package
(Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
V_S+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
V_S-	6	O	Negative charge pump output for storage capacitor only
DOUT2	7	O	RS232 line data output (to remote RS232 system)
RIN2	8	I	RS232 line data input (from remote RS232 system)
ROUT2	9	O	Logic data output (to UART)
DIN2	10	I	Logic data input (from UART)
DIN1	11	I	Logic data input (from UART)
ROUT1	12	O	Logic data output (to UART)
RIN1	13	I	RS232 line data input (from remote RS232 system)
DOUT1	14	O	RS232 line data output (to remote RS232 system)
GND	15	—	Ground
V_{CC}	16	—	Supply Voltage, Connect to external 5V power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

				MIN	MAX	UNIT
V_{CC}	Input supply voltage range[(2)]			−0.3	6	V
V_{S+}	Positive output supply voltage range			V_{CC} − 0.3	15	V
$V_{S−}$	Negative output supply voltage range			−0.3	−15	V
V_I	Input voltage range	Driver		−0.3	V_{CC} + 0.3	V
		Receiver			±30	
V_O	Output voltage range	DOUT		$V_{S−}$ − 0.3	V_{S+} + 0.3	V
		ROUT		−0.3	V_{CC} + 0.3	
	Short-circuit duration	DOUT			Unlimited	
T_J	Operating virtual junction temperature				150	°C
T_{stg}	Storage temperature range			−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

PARAMETER	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	kV

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (DIN1, DIN2)		2			V
V_{IL}	Low-level input voltage (DIN1, DIN2)				0.8	V
	Receiver input voltage (RIN1, RIN2)				±30	V
T_A	Operating free-air temperature	TRS232EC	0		70	°C
		TRS232EI	−40		85	

5.4 Thermal Information

THERMAL METRIC[1]		D (SOIC)	DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	71.7	60.6	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	37.4	48.1	38.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	36.8	40.6	53.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.	27.5	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	36.4	40.3	53.1	°C/W

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [1] and 図 8-1)

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
I_{CC}	Supply current	V_{CC} = 5.5V, All outputs open, T_A = 25°C		8	10	mA

(1)   Test conditions are C1–C4 = 1μF at V_{CC} = 5V ± 0.5V.
(2)   All typical values are at V_{CC} = 5V and T_A = 25°C.

5.6 Driver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range[1]

PARAMETER			TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	DOUT	R_L = 3kΩ to GND		5	7		V
V_{OL}	Low-level output voltage[3]	DOUT	R_L = 3kΩ to GND			−7	−5	V
r_o	Output resistance	DOUT	V_{S+} = $V_{S−}$ = 0,	V_O = ±2V	300			Ω
I_{OS} [4]	Short-circuit output current	DOUT	V_{CC} = 5.5V,	V_O = 0		±10		mA
I_{IS}	Short-circuit input current	DIN	V_I = 0				200	μA

(1)   Test conditions are C1–C4 = 1μF at V_{CC} = 5V ± 0.5V.
(2)   All typical values are at V_{CC} = 5V and T_A = 25°C.
(3)   The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
(4)   Not more than one output should be shorted at a time.

5.7 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see [1])

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R_L = 3kΩ to 7kΩ, See 図 6-2			30	V/μs
SR(t)	Driver transition region slew rate	See 図 6-3		3		V/μs
	Data rate	One DOUT switching		250		kbit/s

(1)   Test conditions are C1–C4 = 1μF at V_{CC} = 5V ± 0.5V.

5.8 Receiver Section: Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature range [1]

PARAMETER		TEST CONDITIONS		MIN	TYP[2]	MAX	UNIT
V_{OH}	High-level output voltage	ROUT	I_{OH} = −1mA	3.5			V
V_{OL}	Low-level output voltage[3]	ROUT	I_{OL} = 3.2mA			0.4	V
V_{IT+}	Receiver positive-going input threshold voltage	RIN	V_{CC} = 5V, T_A = 25°C		1.7	2.4	V
$V_{IT−}$	Receiver negative-going input threshold voltage	RIN	V_{CC} = 5V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis voltage	RIN	V_{CC} = 5V	0.2	0.5	1	V
r_i	Receiver input resistance	RIN	V_{CC} = 5V, T_A = 25°C	3	5	7	kΩ

(1)   Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.
(2)   All typical values are at V_{CC} = 5V and T_A = 25°C.
(3)   The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.
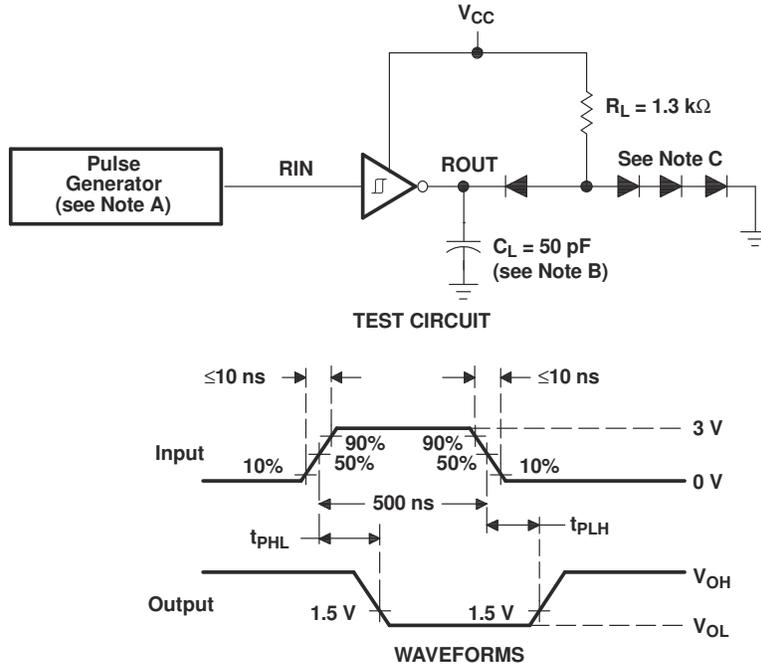
5.9 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see [1] and 図 6-1)

| PARAMETER		TYP	UNIT
$t_{PLH(R)}$	Receiver propagation delay time, low- to high-level output	500	ns
$t_{PHL(R)}$	Receiver propagation delay time, high- to low-level output	500	ns

(1)   Test conditions are C1–C4 = 1µF at V_{CC} = 5V ± 0.5V.

6 Parameter Measurement Information

A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

図 6-1. Receiver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements
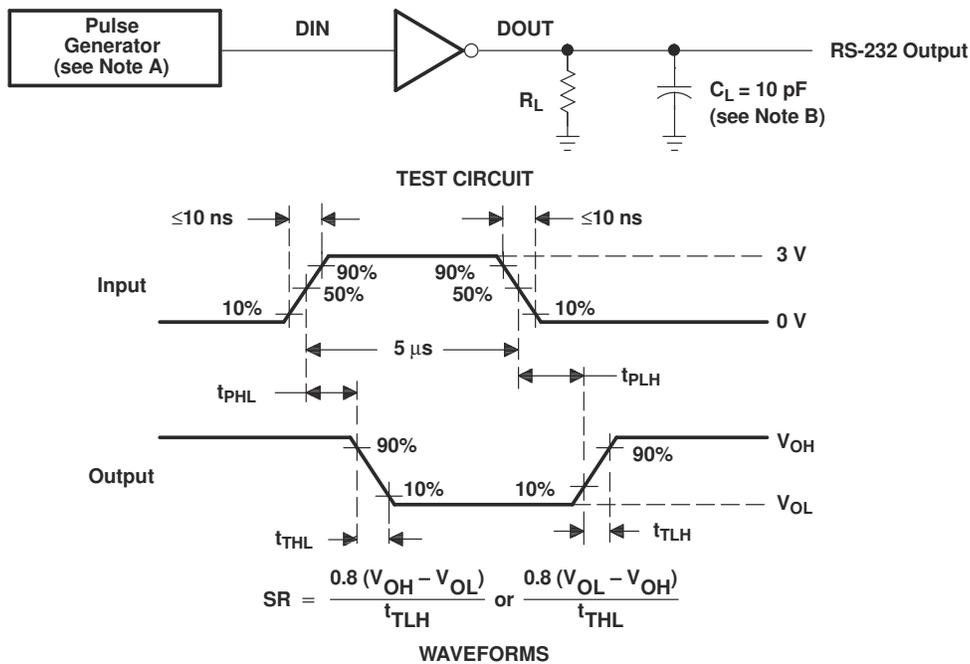
$$SR = \frac{0.8\,(V_{OH} - V_{OL})}{t_{TLH}} \text{ or } \frac{0.8\,(V_{OL} - V_{OH})}{t_{THL}}$$
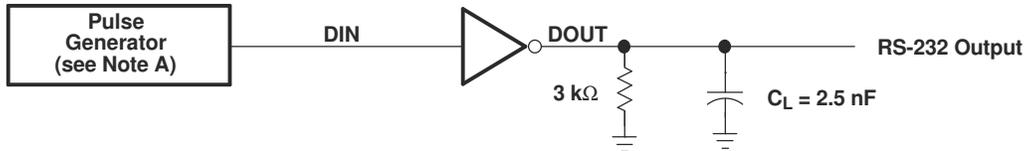
A. The pulse generator has the following characteristics: $Z_O = 50\Omega$, duty cycle ≤ 50%.
B. C_L includes probe and jig capacitance.

図 6-2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5μs Input)

資料に関するフィードバック(ご意見やお問い合わせ)を送信　　7

TEST CIRCUIT

$$SR = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$
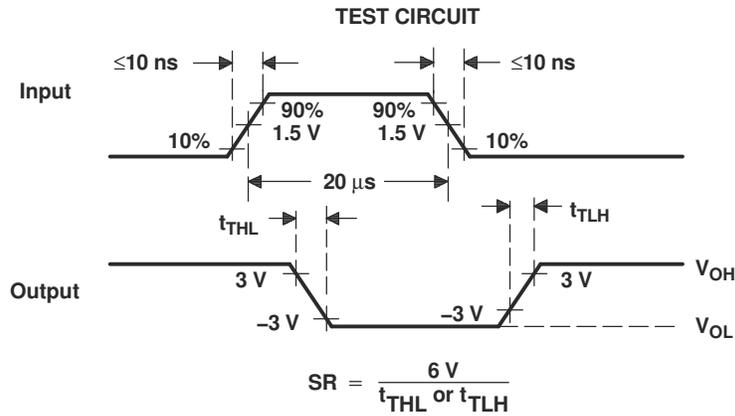
WAVEFORMS

A.   The pulse generator has the following characteristics: Z_O = 50Ω, duty cycle ≤ 50%.

図 6-3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20µs Input)

7 Detailed Description
7.1 Device Functional Modes

表 7-1. Function Tables: Each Driver

INPUT[1] DIN	OUTPUT DOUT
L	H
H	L

(1)   H = high level, L = low level

表 7-2. Each Receiver

INPUT[1] RIN	OUTPUT ROUT
L	H
H	L

(1)   H = high level, L = low level

Product Folder Links: *TRS232E*

English Data Sheet: SLLS791
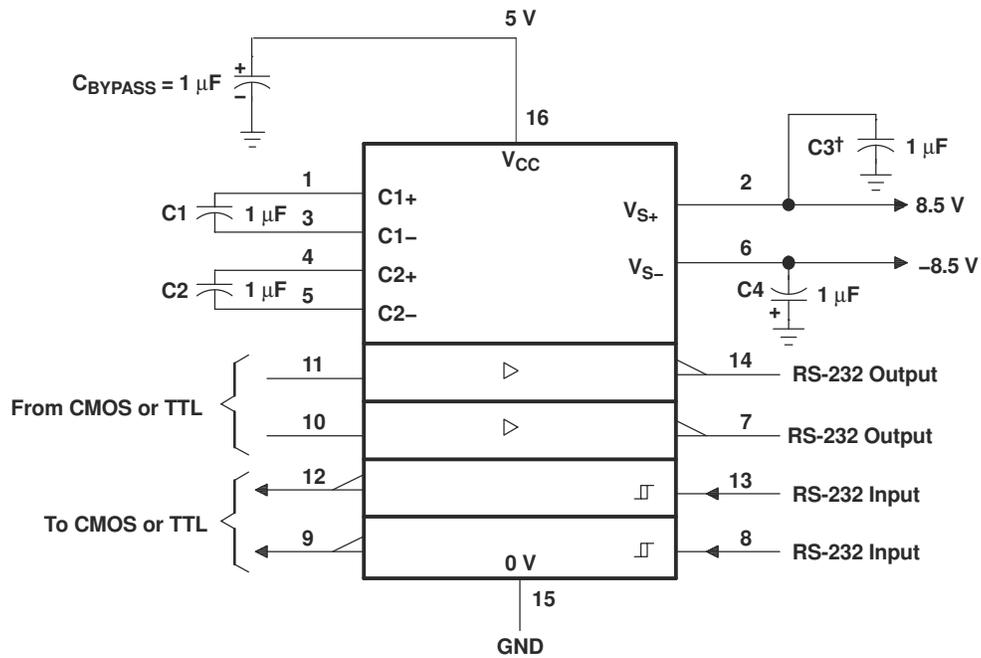
8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

† C3 can be connected to V_{CC} or GND.

A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1μF capacitors shown, the TRS202E can operate with 0.1μF capacitors.

図 8-1. Typical Operating Circuit

Product Folder Links: *TRS232E*

English Data Sheet: SLLS791

9 Device Documentation and Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

TI 用語集   この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS232ECD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	TRS232EC
TRS232ECDR	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	TRS232EC
TRS232ECDWR	Obsolete	Production	SOIC (DW) | 16	-	-	Call TI	Call TI	0 to 70	TRS232EC
TRS232ECN	Obsolete	Production	PDIP (N) | 16	-	-	Call TI	Call TI	0 to 70	TRS232ECN
TRS232ECPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	0 to 70	RU32EC
TRS232ECPWR	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	0 to 70	RU32EC
TRS232EID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	TRS232EI
TRS232EIDR	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	TRS232EI
TRS232EIDWR	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI
TRS232EIDWR.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS232EI
TRS232EIN	Obsolete	Production	PDIP (N) | 16	-	-	Call TI	Call TI	-40 to 85	TRS232EIN
TRS232EIPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	RU32EI
TRS232EIPWR	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	RU32EI

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
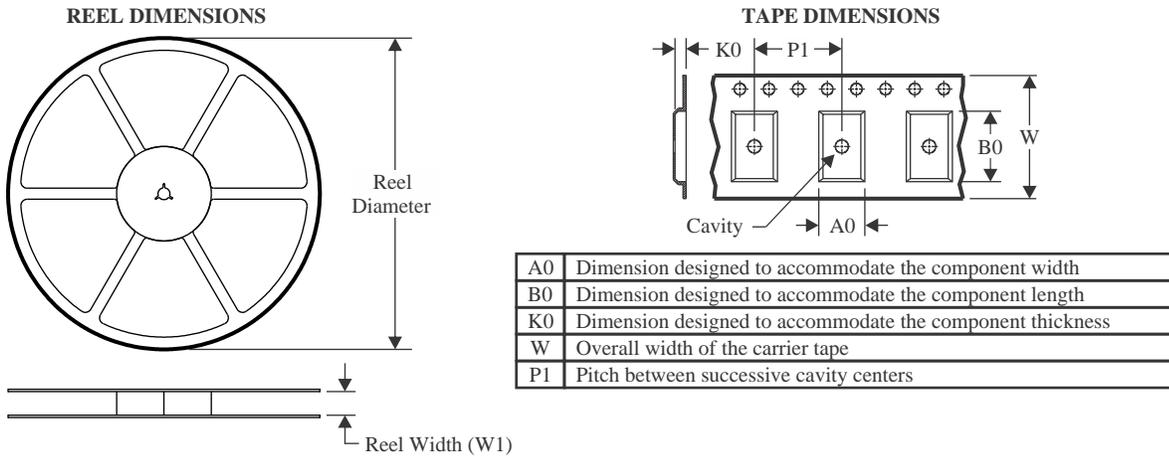
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
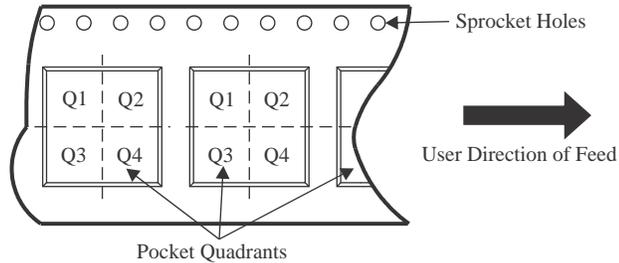
*All dimensions are nominal

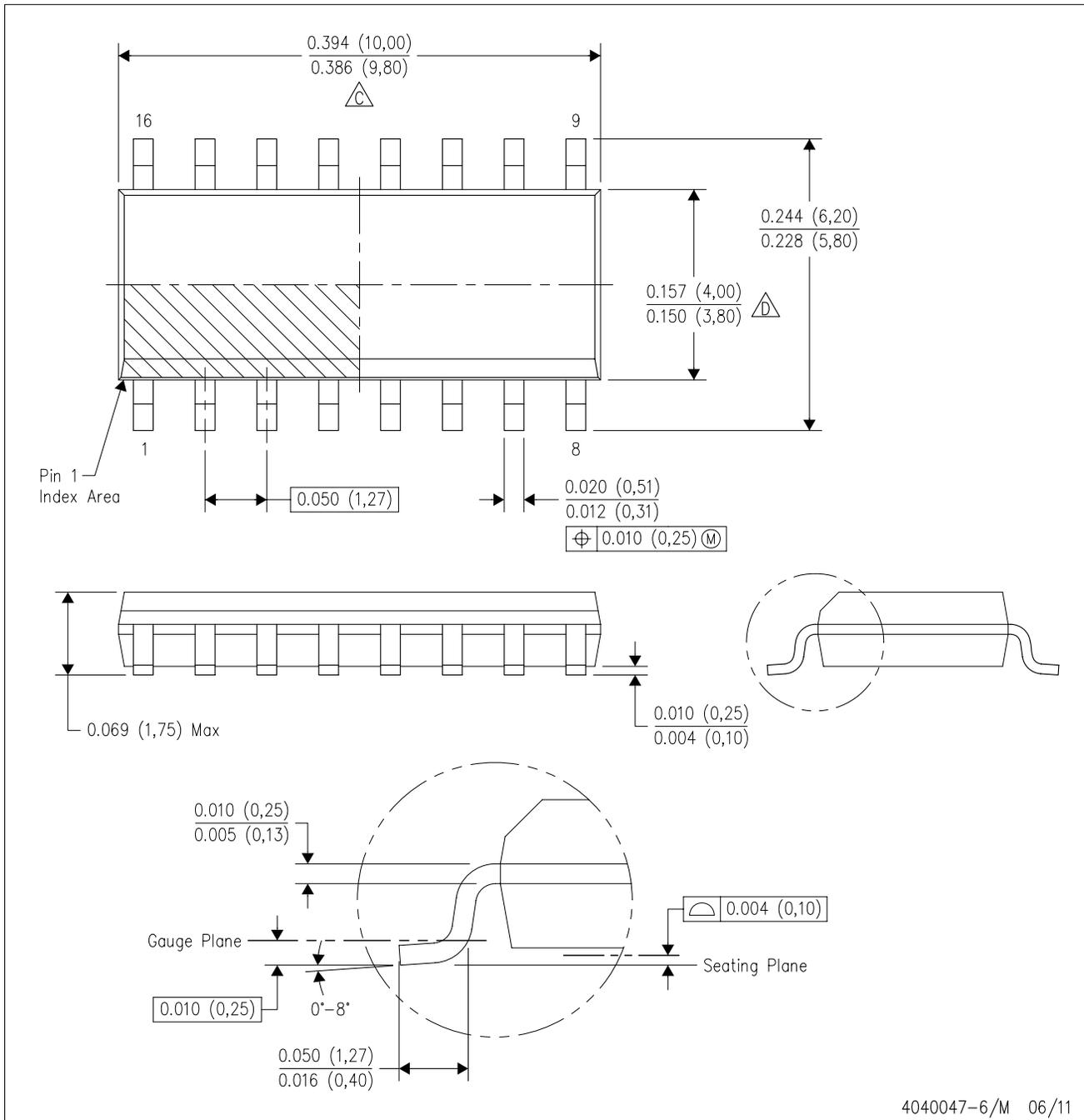| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS232EIDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS232EIDWR	SOIC	DW	16	2000	350.0	350.0	43.0

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
         D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AC.

DW 16

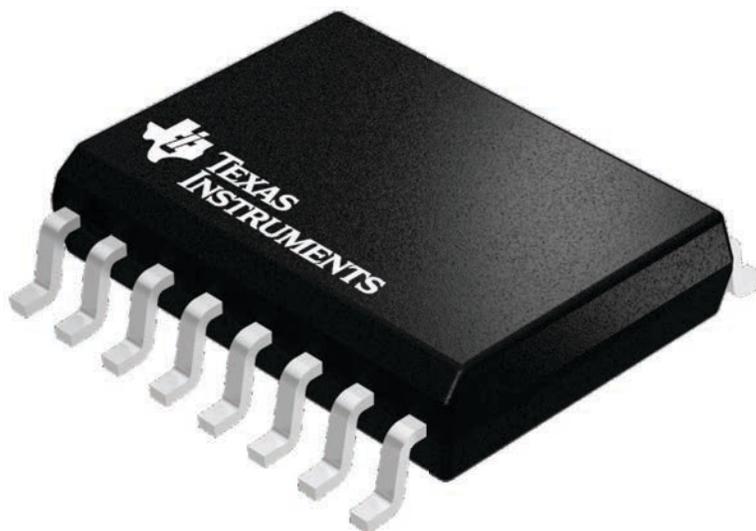**SOIC - 2.65 mm max height**

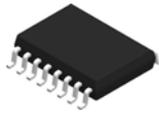**7.5 x 10.3, 1.27 mm pitch**

This image is a representation of the package family, actual package may vary.
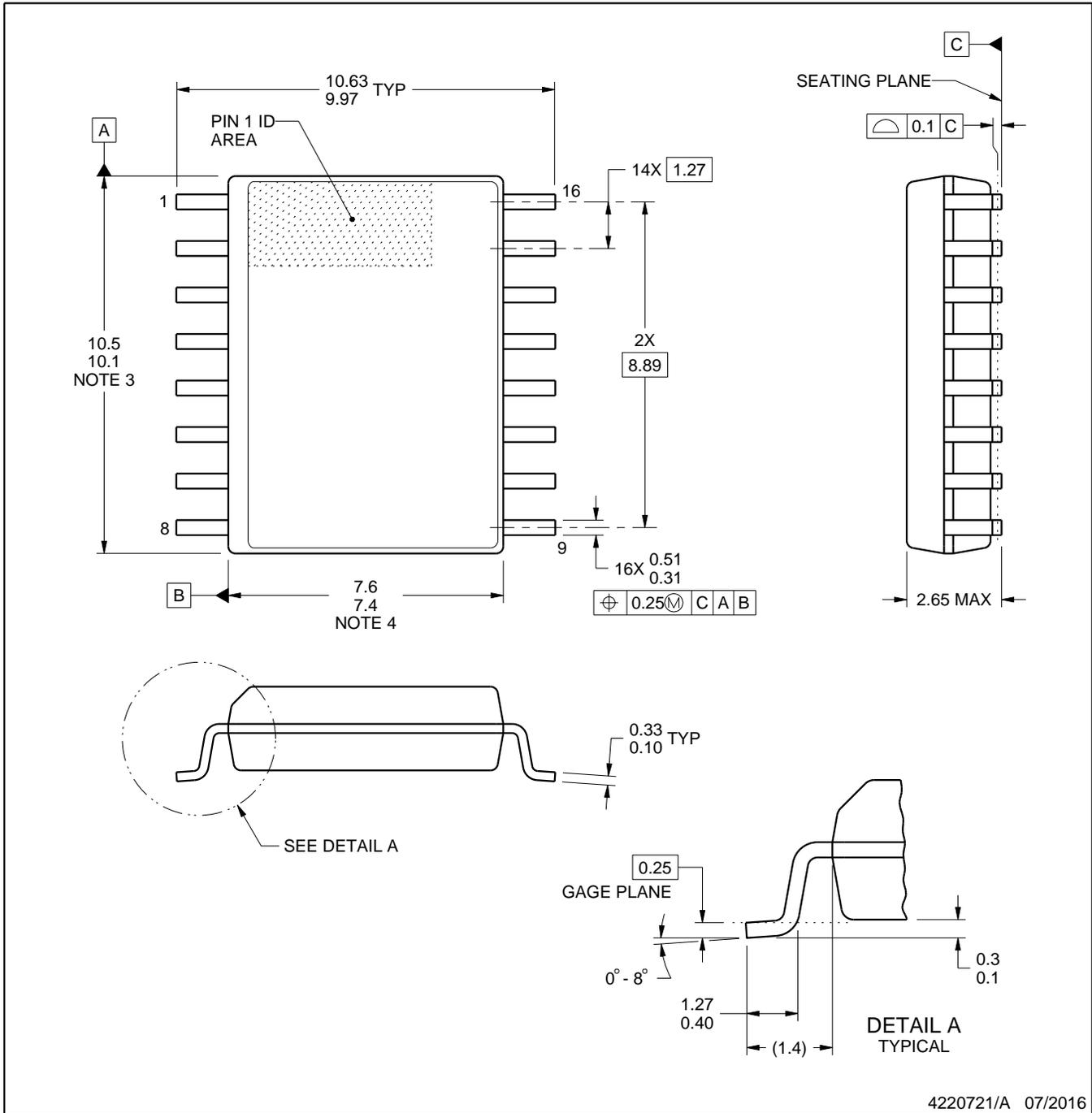Refer to the product data sheet for package details.

4224780/A

C

SEATING PLANE

⌒ | 0.1 | C

10.63
9.97 TYP

PIN 1 ID
AREA

A

1

16

14X | 1.27

2X
8.89

10.5
10.1
NOTE 3

8

9

16X 0.51
0.31

⊕ | 0.25Ⓜ | C | A | B

2.65 MAX

B

7.6
7.4
NOTE 4

0.33
0.10 TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

1.27
0.40

(1.4)

0.3
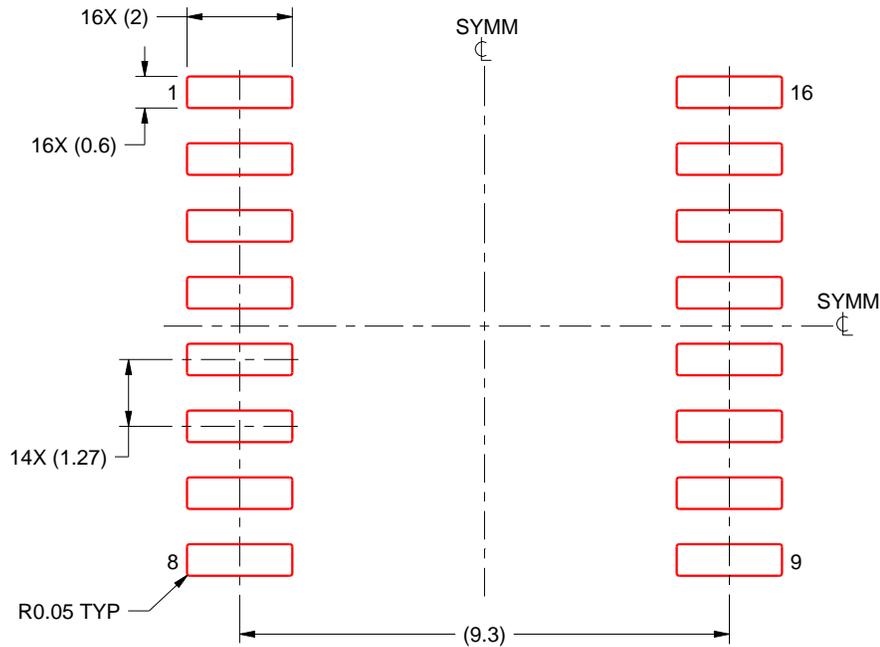0.1

DETAIL A
TYPICAL

4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

16X (2)

SYMM
℄

SEE
DETAILS

16X (0.6)

1

16

SYMM
℄

14X (1.27)

8

9

R0.05 TYP

(9.3)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220721/A   07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (2)

1

16X (0.6)
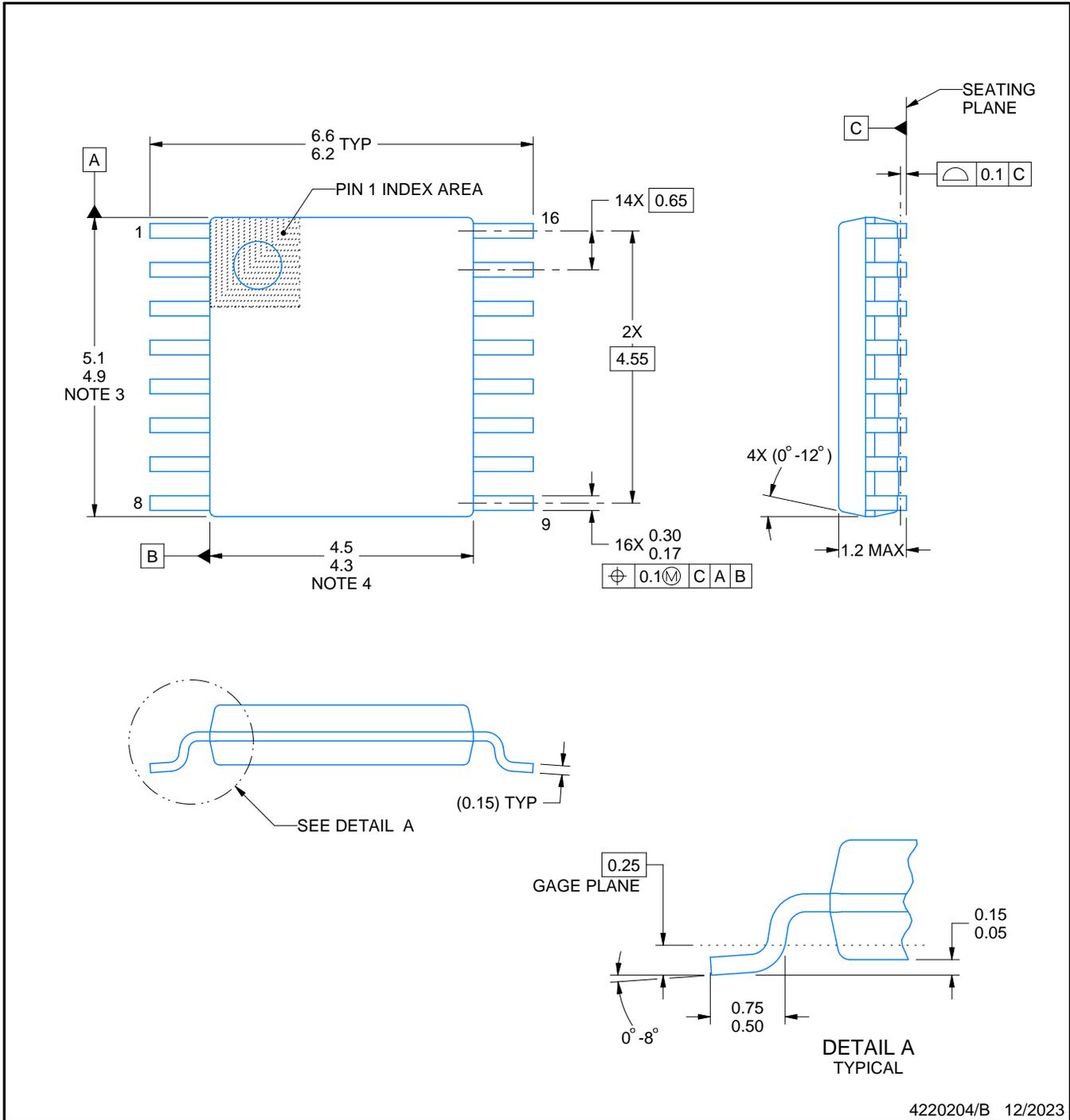
14X (1.27)

8

R0.05 TYP

SYMM

16

SYMM

9

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A   07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

SEATING PLANE

C

△ | 0.1 | C

6.6
6.2 TYP

A

PIN 1 INDEX AREA

1

14X | 0.65

16

2X

4.55

5.1
4.9
NOTE 3

8

9

B

4.5
4.3
NOTE 4

16X | 0.30
0.17

⊕ | 0.1 Ⓜ | C | A | B

4X (0° -12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0.15
0.05

0.75
0.50

0° -8°

DETAIL A
TYPICAL
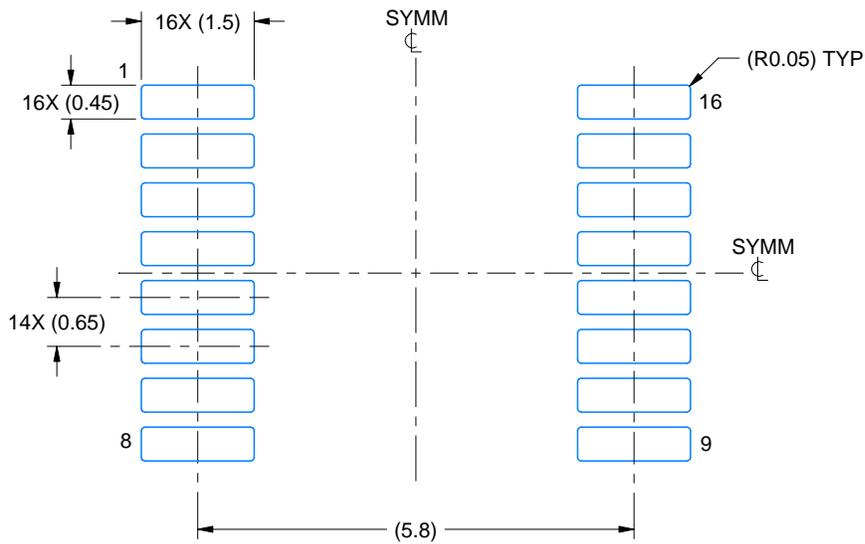
4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

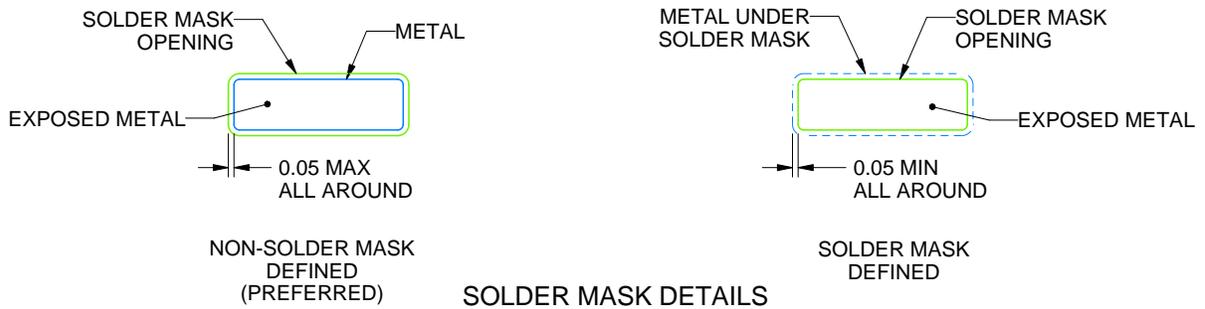16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
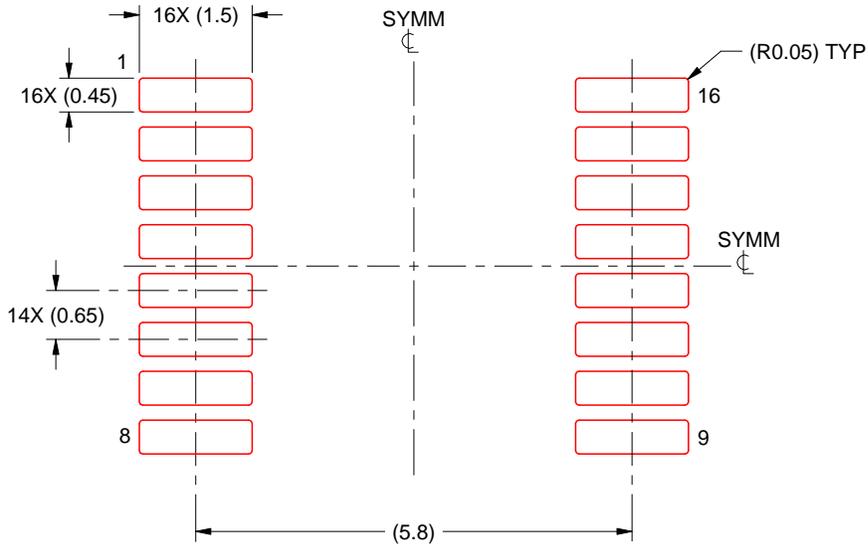
SOLDER MASK DETAILS

4220204/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS INSTRUMENTS
www.ti.com

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
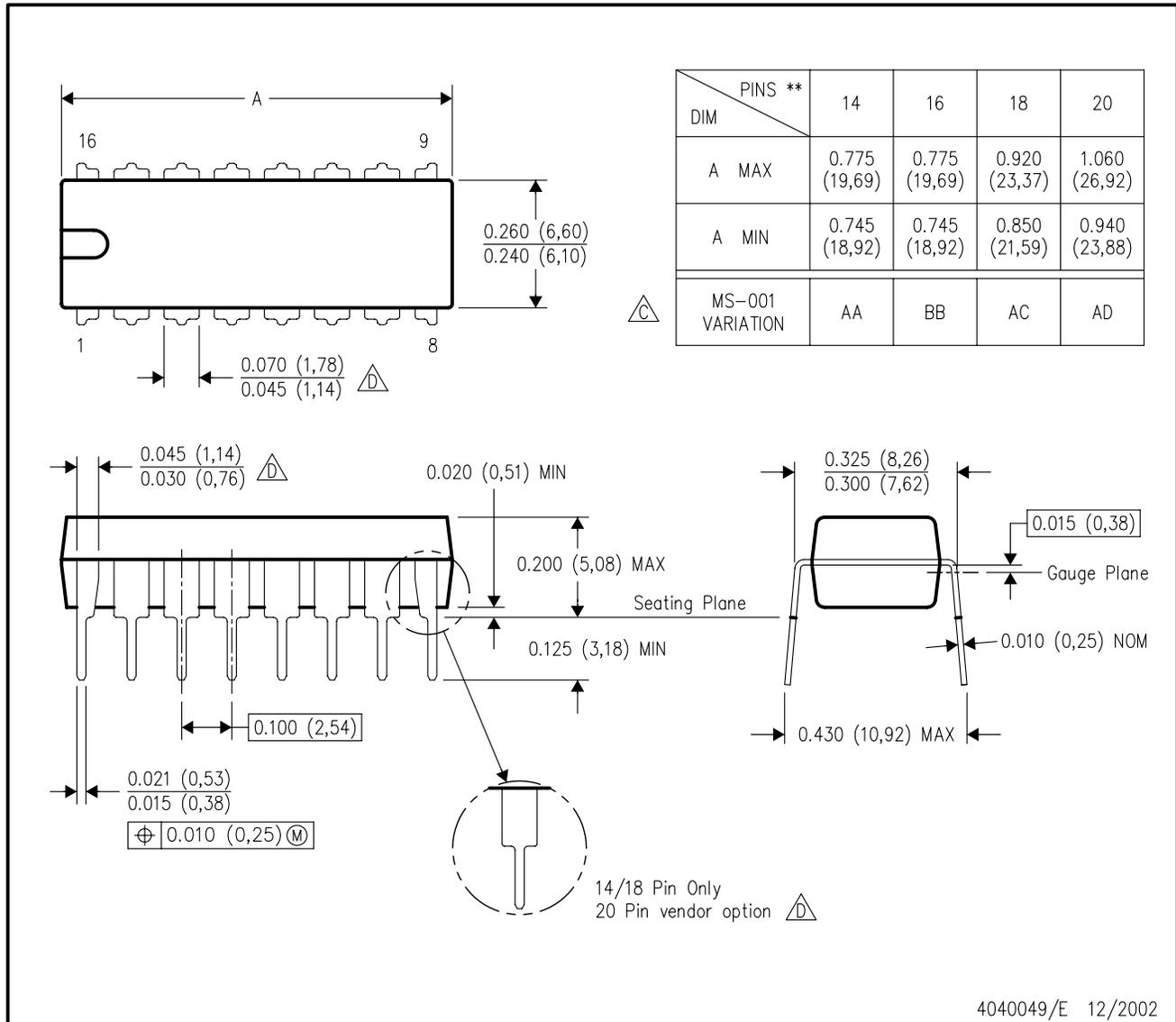BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM / PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) △D

0.045 (1,14) / 0.030 (0,76) △D

0.020 (0,51) MIN

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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