TRS3243 ±15kV ESD (HBM) 保護機能搭載、3V～5.5V マルチチャネル RS-232 ライン・ドライバ / レシーバ

1 特長

- 3V～5.5V の V_{CC} 電源で動作
- IBM® PC/AT™ シリアル・ポート用のシングルチップおよび単一電源インターフェイス
- 人体モデル (HBM) で ±15kV の RS-232 バス・ピン ESD 保護
- TIA/EIA-232-F および ITU V.28 規格の要件に適合
- 3 つのドライバと 5 つのレシーバ
- 最高 250kbps で動作
- 小さいアクティブ電流：300µA (標準値)
- 小さいスタンバイ電流：1µA (標準値)
- 外付けコンデンサ：4 × 0.1µF
- 3.3V 電源で 5V ロジック入力を許容
- 常時アクティブの非反転レシーバ出力 (ROUT2B)
- 動作温度範囲
  - TRS3243C：0℃～70℃
  - TRS3243I：-40℃～85℃
- シリアルマウス駆動可能
- 有効な RS-232 信号が検出されない場合、自動パワー・ダウン機能により ドライバ出力をディスエーブル

2 アプリケーション

- バッテリ駆動システム
- タブレット
- ノート PC
- ノート PC
- ハンドヘルド機器

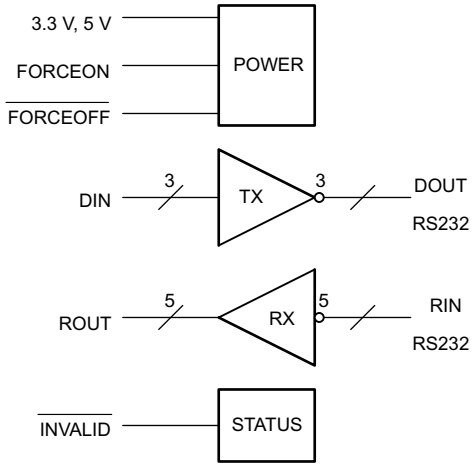
3 概要

TRS3243 デバイスは、3 つのライン・ドライバと 5 つのライン・レシーバで構成されており、DE-9 DTE インターフェイスに理想的です。±15kV のピン間 (シリアル・ポート接続ピン、GND を含む) ESD (HBM) 保護機能を備えています。フレキシブルな電源機能は自動的に電力を節約します。リング・インジケータと有効な RS232 入力をチェックできるように、特別な出力 (ROUT2B、$\overline{\text{INVALID}}$) は常に有効化されています。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TRS3243	SSOP (28)	10.20mm × 5.30mm
	TSSOP (28)	9.70mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (June 2015) to Revision C (October 2022)	Page
• Changed the *Thermal Information* table	5
• Changed the MAX value of I_{CC} Supply current auto-powerdown disabled from 1 mA to 1.2 mA in *Electrical Characteristics—Power and Status*	5

Changes from Revision A (September 2011) to Revision B (June 2015)	Page
• 「端子機能」表、「ESD 定格」表、「熱に関する情報」表、「代表的特性」セクション、「詳細説明」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
• Deleted *Ordering Information* table	3

5 Pin Configuration and Functions

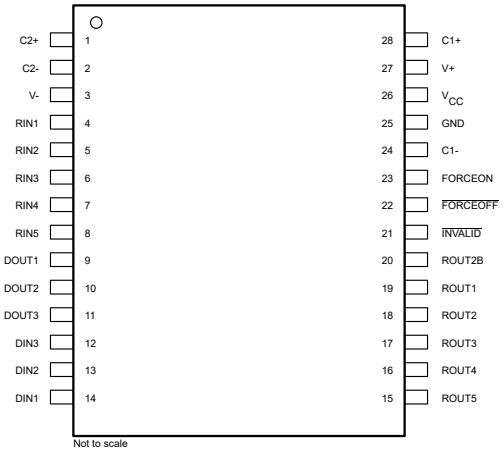


図 5-1. DB, PW Packages, 28-Pin SSOP, TSSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-		Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	$\overline{\text{INVALID}}$	O	Invalid Output Pin
22	$\overline{\text{FORCEOFF}}$	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V_{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.3	6	V
V_+	Positive output supply voltage(2)		–0.3	7	V
V_-	Negative output supply voltage(2)		0.3	–7	V
$V_+ - V_-$	Supply voltage difference(2)			13	V
V_I	Input voltage	Driver, $\overline{\text{FORCEOFF}}$, FORCEON	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage	Driver	–13.2	13.2	V
		Receiver, $\overline{\text{INVALID}}$	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN , DOUT, and GND pins (1)	±15000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 All other pins(1)	±3000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see 図 9-1)(1)

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_{CC} = 3.3 V	2		5.5	V
			V_{CC} = 5 V	2.4		5.5	
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature		TRS3243C	0		70	°C
			TRS3243I	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC[1]		{DB} (SSOP) 16 PINS	{PW} (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.1	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	21.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.0	28.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics—Power and Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1] (see 図 9-1)

PARAMETER		TEST CONDITIONS	MIN	TYP[2]	MAX	UNIT
I_{CC}	Supply current Automatic power down disabled	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}. T_A = 25°C		0.3	1.2	mA
	Supply current Powered off	No load, $\overline{FORCEOFF}$ at GND. T_A = 25°C		1	10	µA
	Supply current Automatic power down enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded, All DIN are grounded. T_A = 25°C		1	10	µA
I_I	Input leakage current of $\overline{FORCEOFF}$, FORCEON	V_I = V_{CC} or V_I at GND		±0.01	±1	µA
V_{IT+}	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			2.7	V
V_{IT-}	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7			V
V_T	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3		0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = –1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6			V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}			0.4	V

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.6 Electrical Characteristics—Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 図 9-1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND			5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND			–5	–5.4		V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3 kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA			±5			V
I_{IH}	High-level input current	$V_I = V_{CC}$				±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND				±0.01	±1	μA
V_{hys}	Input hysteresis						±1	V
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V,	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V					
r_o	Output resistance	V_{CC} = 0 V, V_+ = 0 V, and V_- = 0 V,	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND,	V_O = ±12 V,	V_{CC} = 3 to 3.6 V			±25	μA
			V_O = ±10 V,	V_{CC} = 4.5 to 5.5 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Electrical Characteristics—Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 図 9-1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OH} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – V_{IT-})			0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{FORCEOFF}$ = 0 V		±0.05	±10	μA
r_I	Input resistance	V_I = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Switching Characteristics—Power and Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 7-5)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	V_{CC} = 5 V	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	V_{CC} = 5 V	30	µs
t_{en}	Supply enable time	V_{CC} = 5 V	100	µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.9 Switching Characteristics—Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (see 図 9-1)
TRS3243C, TRS3243I

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ One DOUT switching,	C_L = 1000 pF See 図 7-1	150	250		kbps
$t_{sk(p)}$	Pulse skew(3)	R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 2500 pF See 図 7-3		100		ns
SR(tr)	Slew rate, transition region (see 図 7-1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V + 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.10 Switching Characteristics—Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	TYP(2)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See 図 7-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output		150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See 図 7-4	200	ns
t_{dis}	Output disable time		200	ns
$t_{sk(p)}$	Pulse skew(3)	See 図 7-3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.11 Typical Characteristics

V_{CC} = 3.3 V

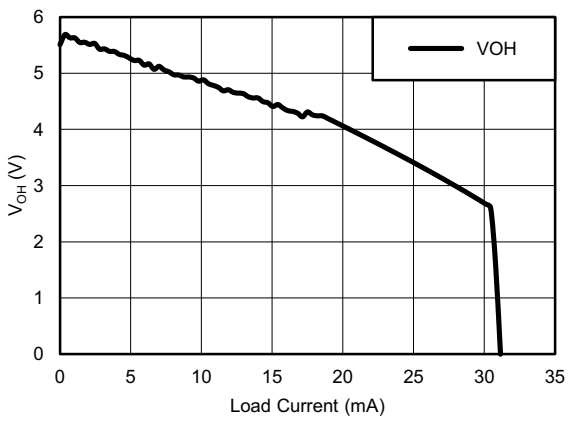


図 6-1. DOUT VOH vs Load Current

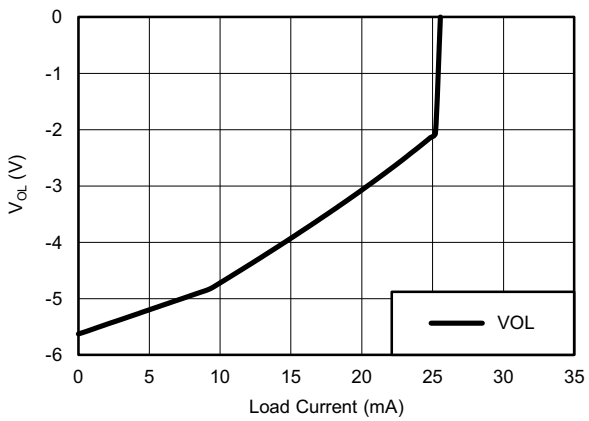
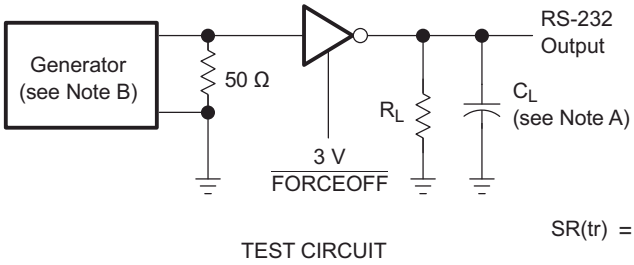


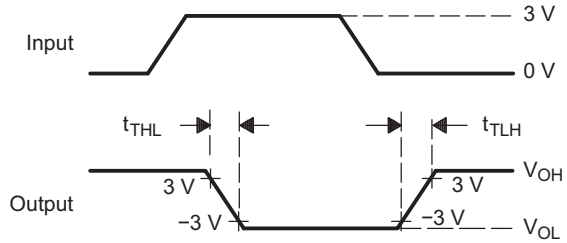
図 6-2. DOUT VOL vs Load Current

7 Parameter Measurement Information



TEST CIRCUIT

$$SR(tr) = \frac{6\ V}{t_{THL} \text{ or } t_{TLH}}$$

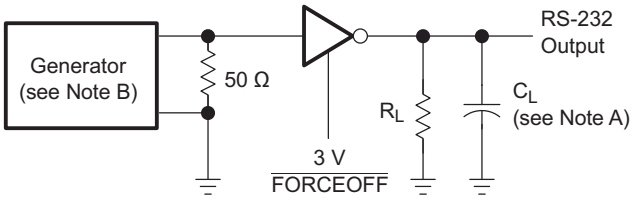


VOLTAGE WAVEFORMS

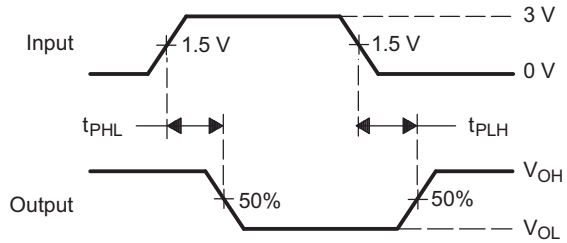
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

図 7-1. Driver Slew Rate



TEST CIRCUIT

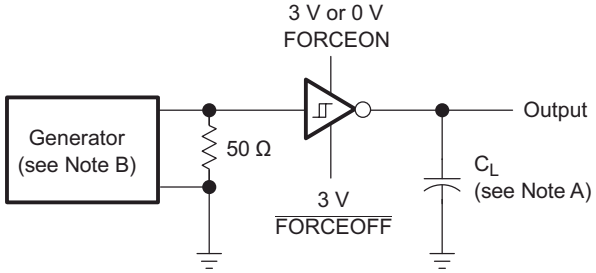


VOLTAGE WAVEFORMS

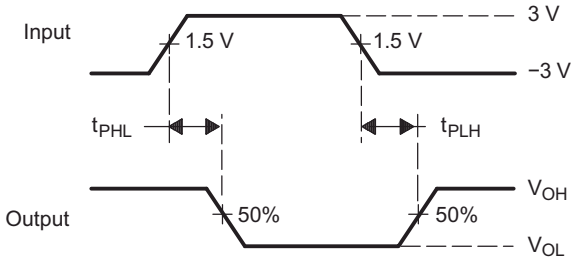
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbps, (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

図 7-2. Driver Pulse Skew



TEST CIRCUIT

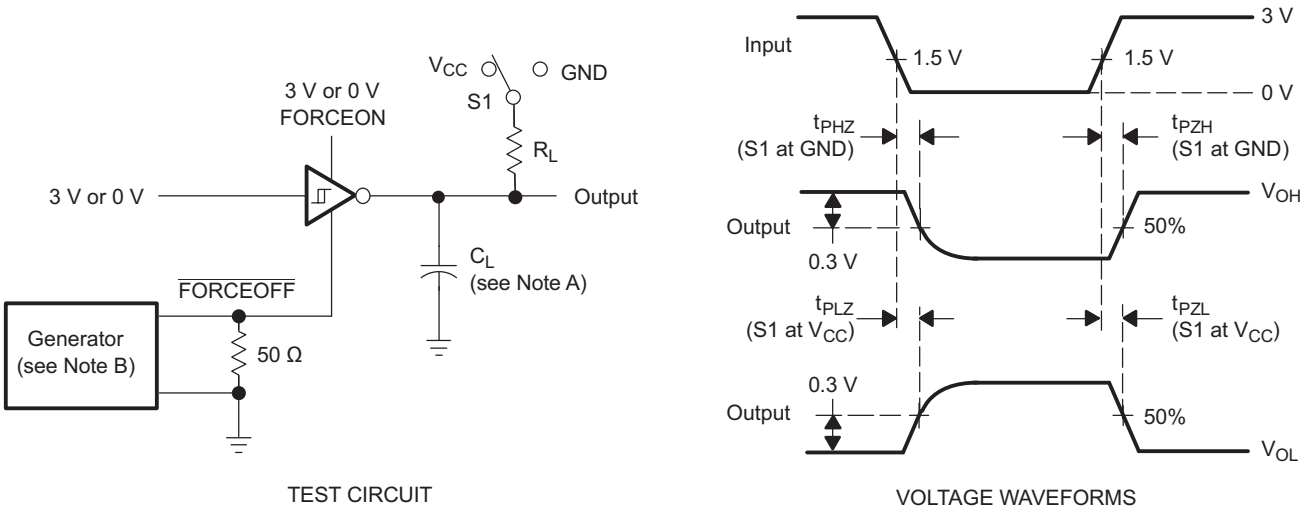


VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.

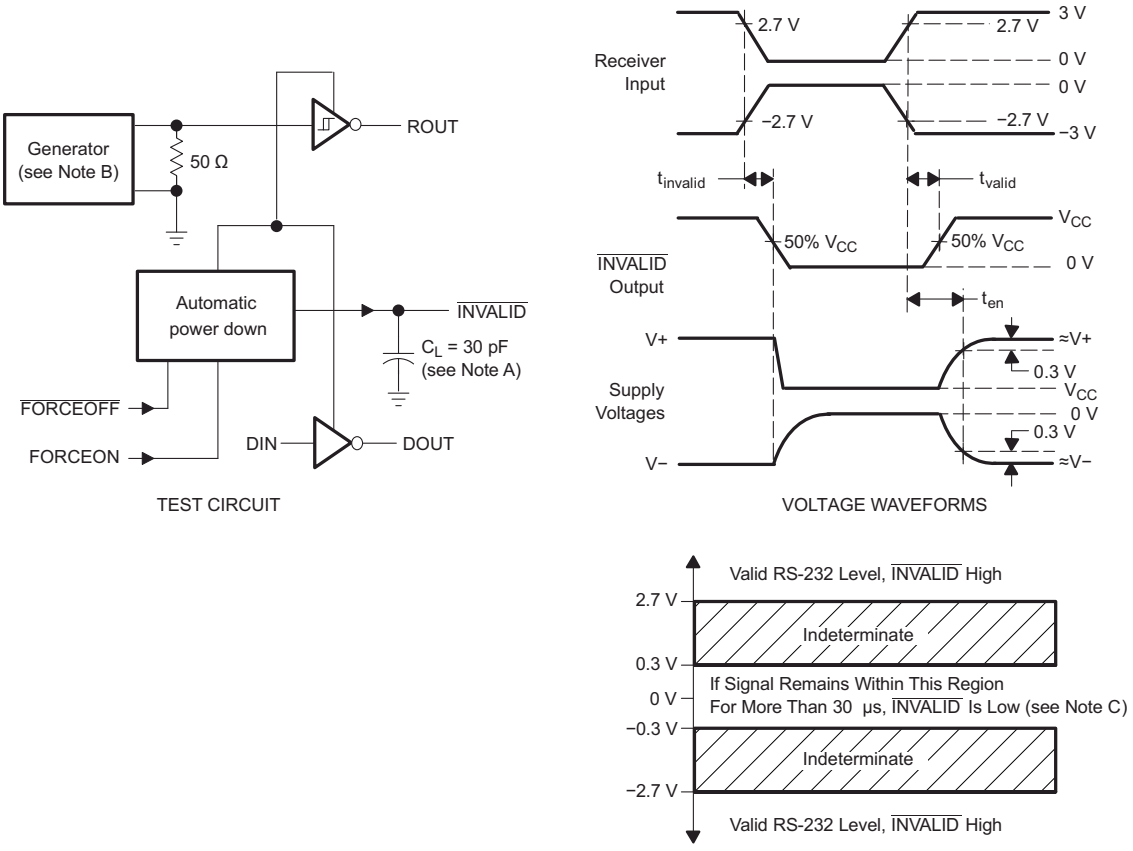
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

図 7-3. Receiver Propagation Delay Times



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

図 7-4. Receiver Enable and Disable Times



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbps, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
C. Automatic power down disables drivers and reduces supply current to 1 µA.

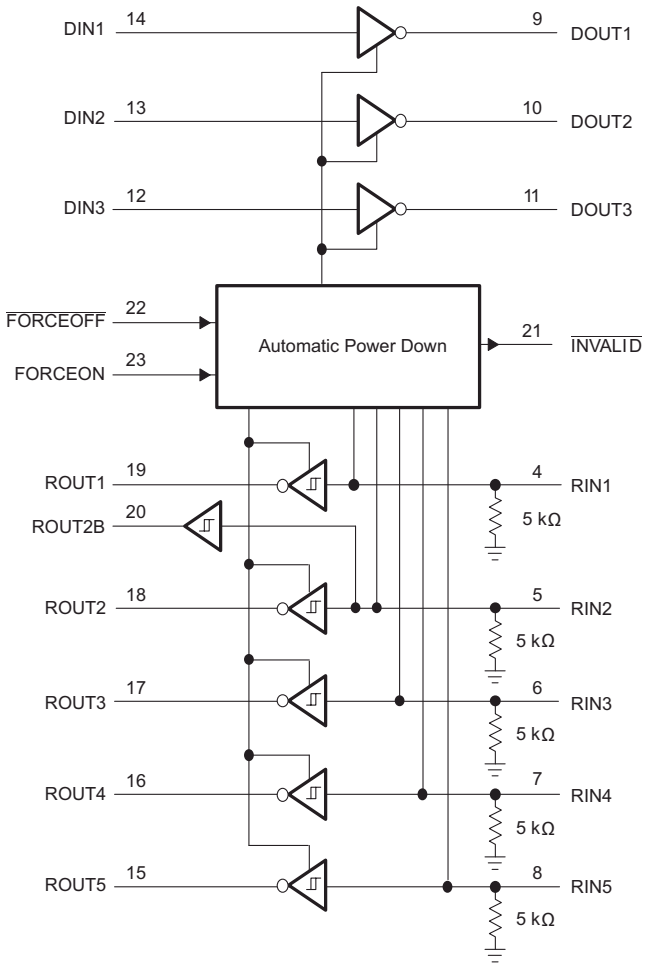
図 7-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

8 Detailed Description

8.1 Overview

The TRS3243 device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD (HBM) protection pin-to-pin (serial-port connection pins, including GND). The TRS3243 device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches what is needed for the typical serial port used in an IBM PC, AT, or compatible device. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. Flexible control options for power management are available when the serial port is inactive. The automatic power-down feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 µA. Disconnecting the serial port or turning off the peripheral drivers causes the automatic power-down condition to occur. Automatic power down can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high and must be done when driving a serial mouse. With automatic power down enabled, the device is activated automatically when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V, is less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between –0.3 V and 0.3 V for more than 30 µs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Automatic Power Down

Automatic power down can be used to automatically save power when the receivers are unconnected or when they are connected to a powered down remote RS232 port. FORCEON being high overrides automatic power down and the drivers are active. $\overline{\text{FORCEOFF}}$ being low overrides FORCEON and powers down all outputs except for ROUT2B and $\overline{\text{INVALID}}$.

8.3.2 Charge Pump

The charge pump increases, inverts, and regulates voltage at V+ and V– pins. The charge pump requires four external capacitors.

8.3.3 RS232 Driver

Three drivers interface standard logic level to RS232 levels. All DIN inputs must be valid high or low.

8.3.4 RS232 Receiver

Five receivers interface RS232 levels to standard logic levels. An open input results in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.3.5 ROUT2B Receiver

ROUT2B is an always-active, noninverting output of RIN2 input, which allows applications using the ring indicator to transmit data while the device is powered down.

8.3.6 Invalid Input Detection

The $\overline{\text{INVALID}}$ output goes active low when all RIN inputs are unpowered. The $\overline{\text{INVALID}}$ output goes inactive high when any RIN input is connected to an active RS232 voltage level.

8.4 Device Functional Modes

表 8-1. Each Driver(1)

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with automatic power down disabled
H	H	H	X	L	
L	L	H	YES	H	Normal operation with automatic power down enabled
H	L	H	YES	L	
X	L	H	NO	Z	Power off by automatic power down feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, YES = any RIN valid, NO = all RIN invalid

表 8-2. Each Receiver(1)

INPUTS			OUTPUTS	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

表 8-3. $\overline{\text{INVALID}}$ and ROUT2B Outputs(1)

INPUTS				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
YES	L	X	X	H	L	Always Active
YES	H	X	X	H	H	
YES	OPEN	X	X	H	L	Always Active
NO	OPEN	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off),
OPEN = input disconnected or connected driver off, YES = any RIN valid, NO = all RIN invalid

9 Application and Implementation

注

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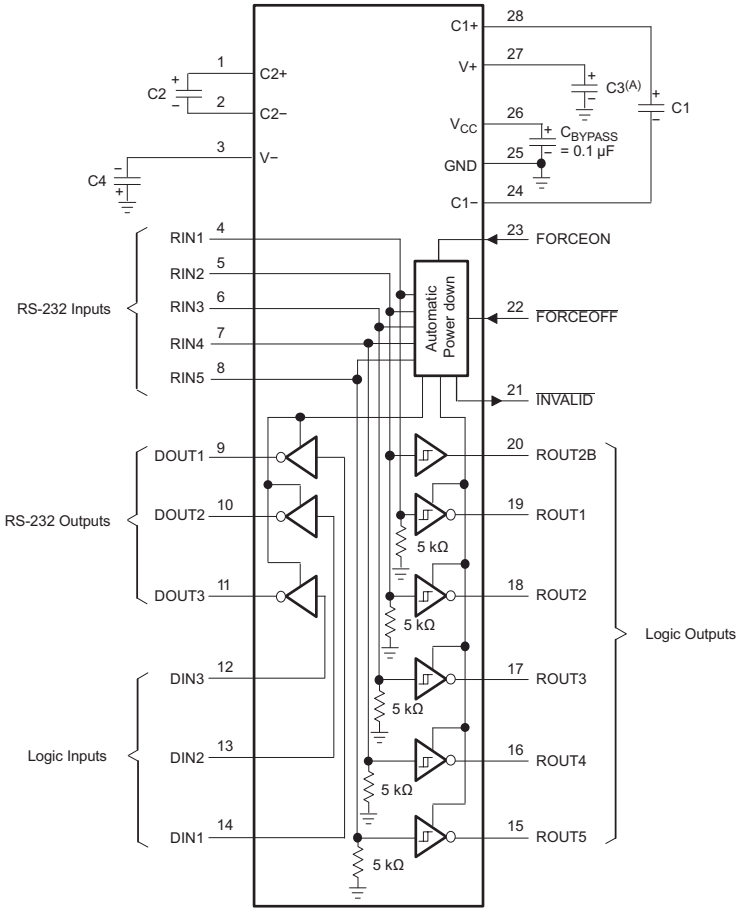
9.1 Application Information

The TRS3243 device is designed to convert single-ended signals into RS232-compatible signals, and vice-versa.

This device can be used in any application where RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector. The device also features an automatic power-down circuit.

9.2 Typical Application



A. C3 can be connected to V_{CC} or GND.
B. Resistor values shown are nominal.
C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

図 9-1. Typical Operating Circuit and Capacitor Values

9.2.1 Design Requirements

- V_{CC} minimum is 3 V and maximum is 5.5 V
- Maximum recommended bit rate is 250 kbps

表 9-1. V_{CC} versus Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

9.2.2 Detailed Design Procedure

It is recommended to add capacitors as shown in 図 9-1.

All DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curve

V_{CC}= 3.3 V

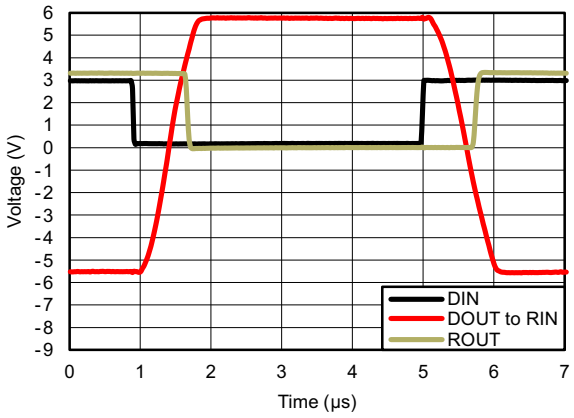


図 9-2. Driver to Receiver Loopback Timing Waveform

9.3 Power Supply Recommendations

V_{CC} must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using 表 9-1.

9.4 Layout

9.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

図 9-3 shows only critical layout sections. Input and output traces will vary in shape and size depending on the customer application. FORCEON and $\overline{\text{FORCEOFF}}$ must be pulled up to VCC or GND through a pullup resistor, depending on which configuration is desired upon powerup.

9.4.2 Layout Example

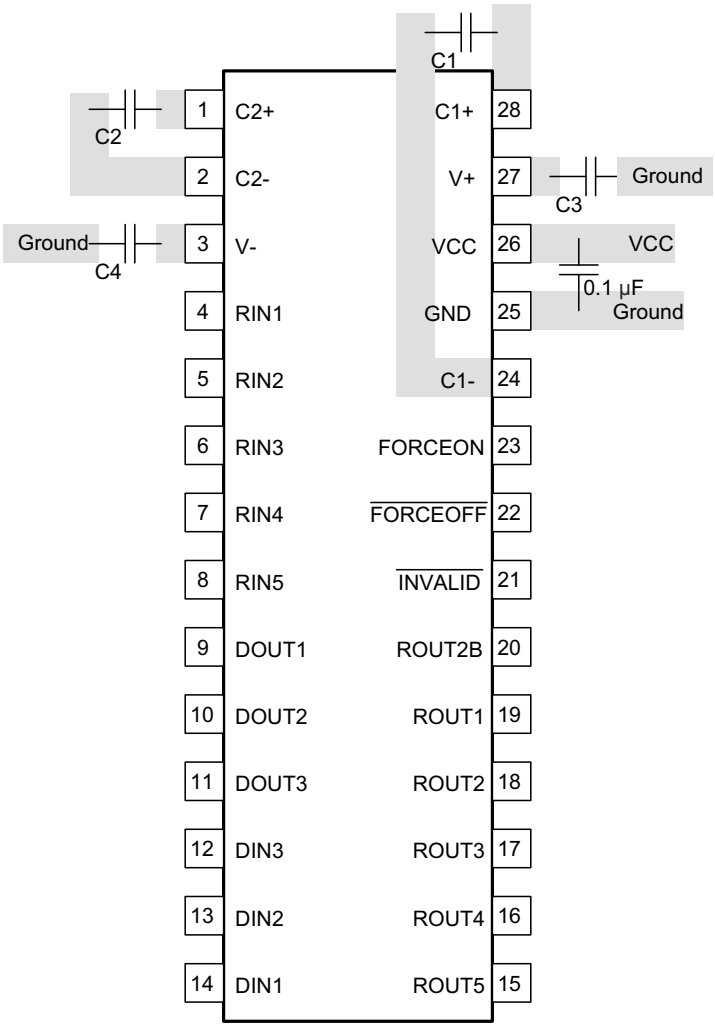


図 9-3. Layout Diagram

10 Device and Documentation Support

10.1 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.4 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRS3243CDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C
TRS3243CDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C
TRS3243CDBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C
TRS3243IDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I
TRS3243IDBR.A	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

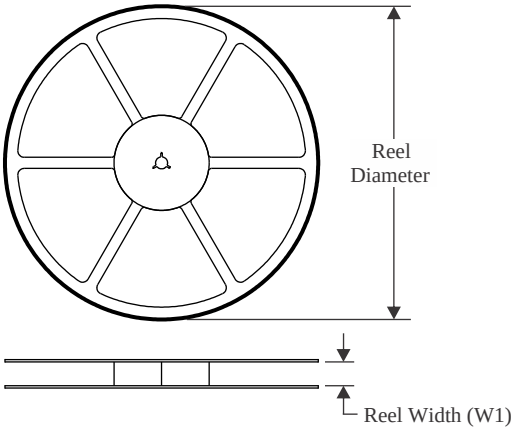
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

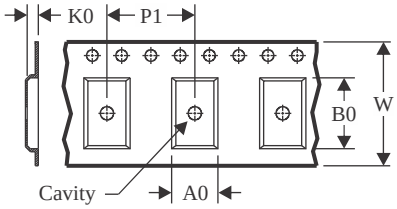
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

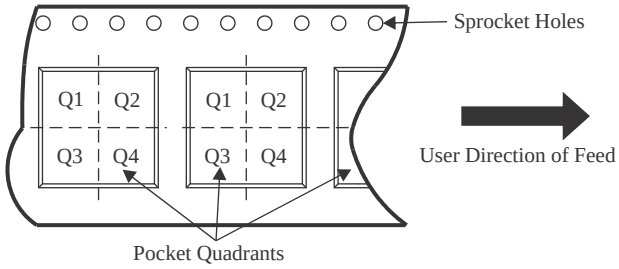


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

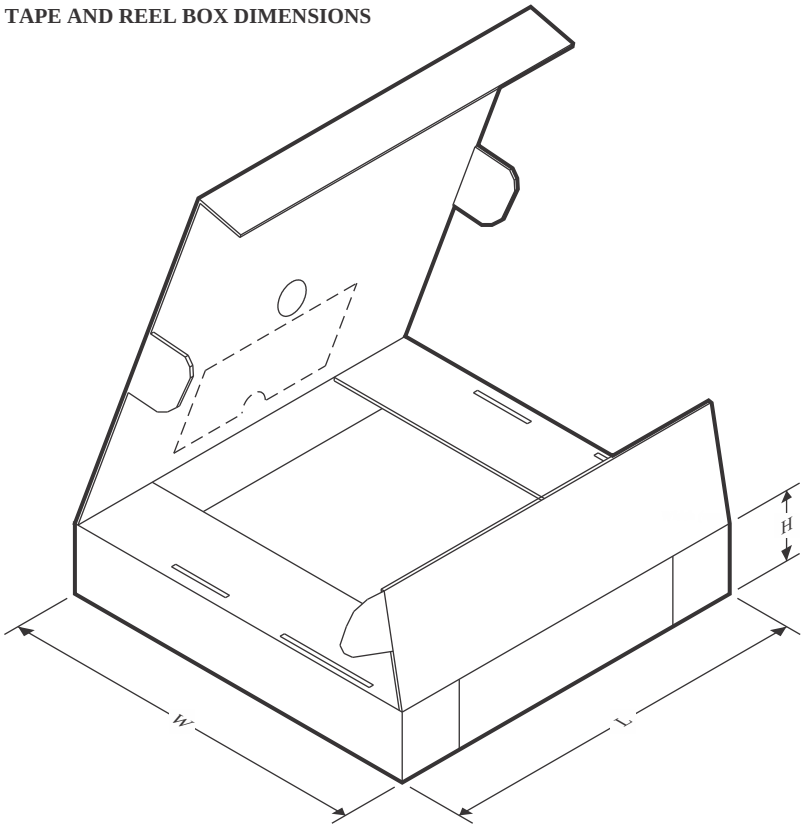
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3243CDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
TRS3243IDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

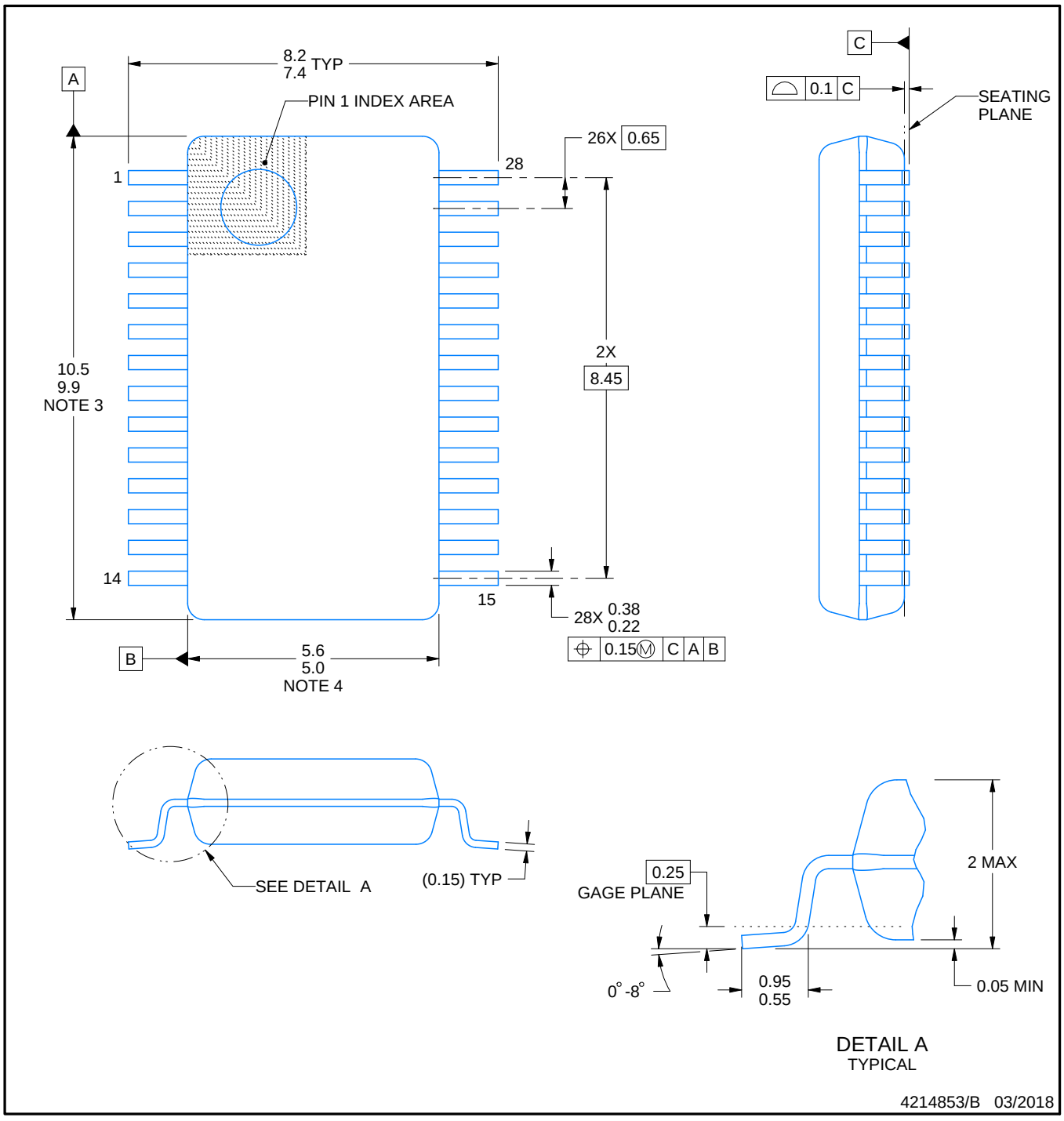
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3243CDBR	SSOP	DB	28	2000	353.0	353.0	32.0
TRS3243IDBR	SSOP	DB	28	2000	353.0	353.0	32.0

PACKAGE OUTLINE

DB0028A

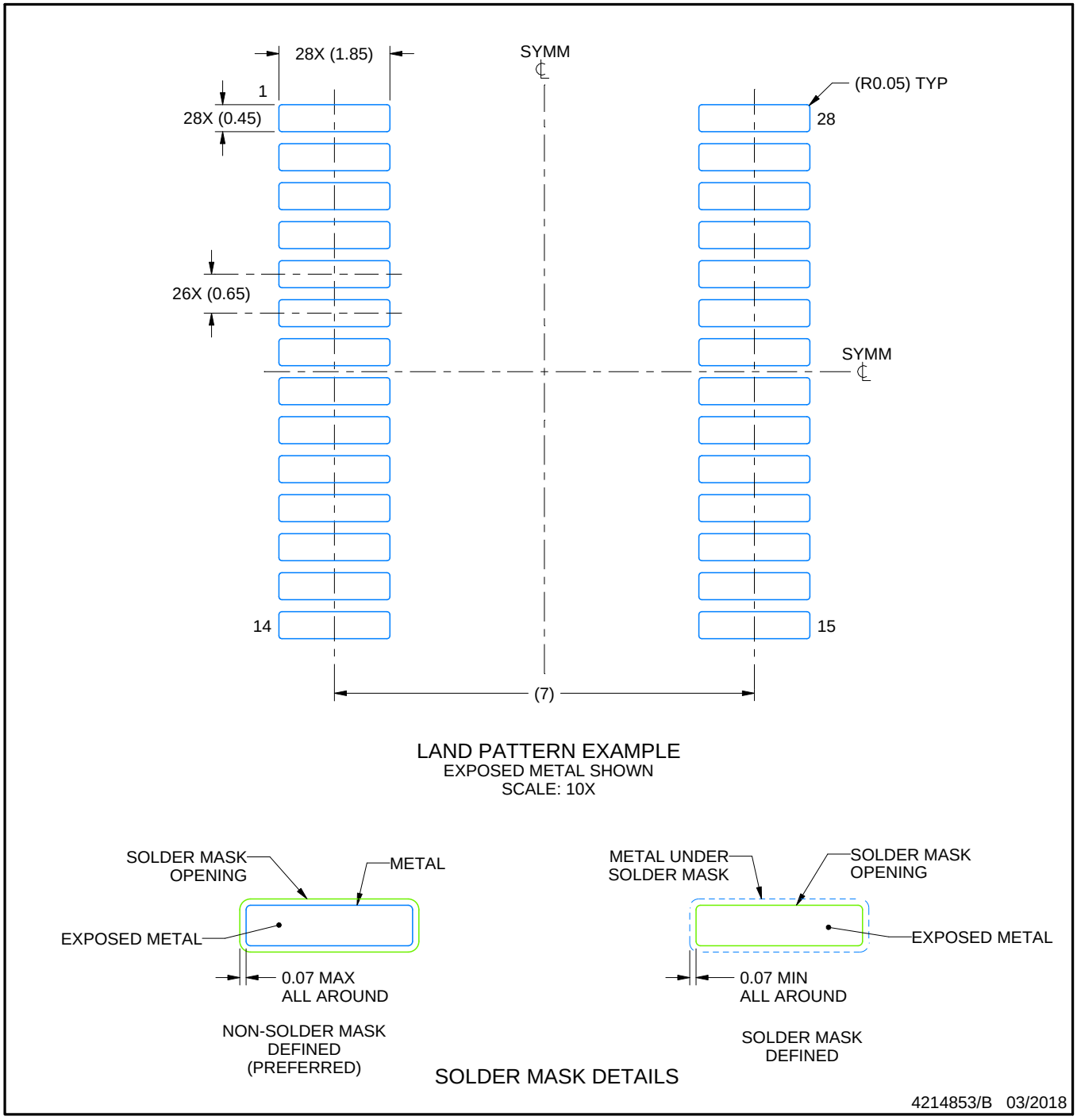
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



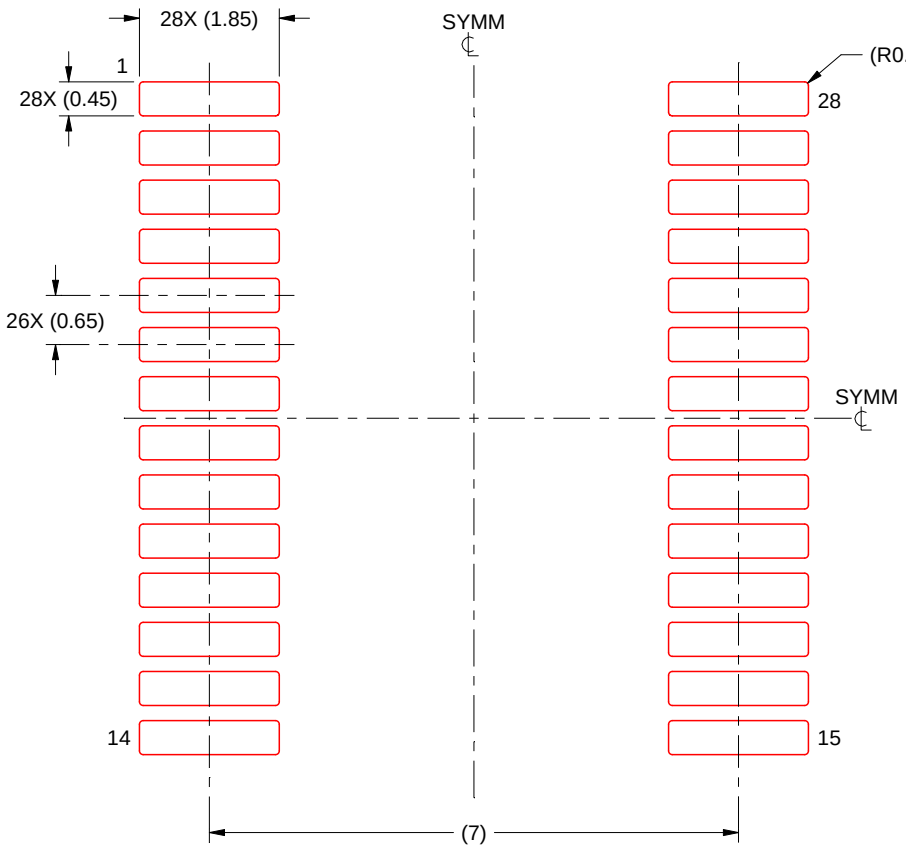
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月