

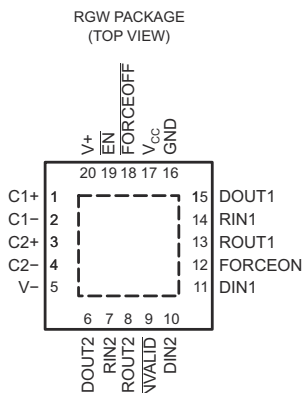
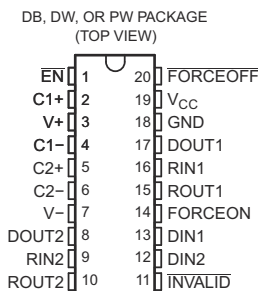
# 3V~5.5V、マルチチャネル RS-232 ラインドライバおよびレシーバ、±15kV ESD 保護

## 1 特長

- RS-232 バス・ピンの ESD 保護機能
  - ±15kV 人体モデル (HBM)
  - ±8kV IEC 61000-4-2、接触放電
  - ±15kV IEC 61000-4-2、エアギャップ放電
- TIA/EIA-232-F および ITU v.28 規格の要件に適合またはそれを上回る性能
- 3V~5.5V の V<sub>CC</sub> 電源で動作
- 最大 1000kbit/s で動作
- 2 つのドライバと 2 つのレシーバ
- 小さいスタンバイ電流: 標準値 1μA
- 外付けコンデンサ: 4 × 0.1μF
- 3.3V 電源で 5V ロジック入力を許容

## 2 アプリケーション

- バッテリー駆動システム
- PDA
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器



## 3 概要

TRSF3223E は 2 つのラインドライバ、2 つのラインレシーバ、1 つのデュアル チャージポンプ回路で構成されており、±15kV のピン間 (シリアル・ポート接続ピン、GND を含む) ESD 保護機能を備えています。このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポートコネクタの間の電気的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V~5.5V の単一電源で動作できます。TRSF3223E は、最大 1000k ビットの標準的なデータ信号速度で動作します。

シリアル・ポートが使われていない際のパワー・マネージメントを柔軟に制御できます。FORCEON が LOW かつ FORCEOFF が HIGH の場合、自動パワー・ダウン機能が動作します。この動作モード中、有効な RS-232 信号を検出しない場合、ドライバ出力はディセーブルになります。FORCEOFF を LOW に設定しかつ EN を HIGH に設定すると、ドライバとレシーバはどちらもシャットダウンされ、消費電流は 1mA に減少します。シリアルポートを切り離れた場合、またはペリフェラルドライバをオフにした場合、自動パワーダウンが作動します。FORCEON と FORCEOFF を HIGH にすると、自動パワー・ダウンを無効にできます。自動パワーダウンが有効な場合、いずれかのレシーバの入力に有効な信号が印加されると、デバイスは自動的にアクティブになります。INVALID 出力は、レシーバの入力に RS-232 信号が存在するかどうかをユーザーに通知する目的で使用されます。INVALID は、いずれかのレシーバの入力電圧が 2.7V を上回っている場合、-2.7V を下回っている場合、-0.3V と 0.3V の間にあった期間が 30μs 未満である場合のいずれかの場合、HIGH (有効データ) になります。INVALID は、レシーバの入力電圧が 30μs を超える期間 -0.3V と 0.3V の間にある場合、LOW (無効データ) になります。レシーバの入力レベルについては、図 5-4 を参照してください。

### パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
TRSF3223E	SOIC (DW, 20)	12.8mm × 10.3mm
	SSOP (DB, 20)	7.2mm × 7.8mm
	TSSOP (PW, 20)	6.5 mm × 6.4 mm
	VQFN (RGW, 20)	5mm × 5mm

- 詳細については、セクション 10 を参照してください。
- パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



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## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	-0.3	6	V	
V+	Positive-output supply voltage range <sup>(2)</sup>	-0.3	7	V	
V-	Negative-output supply voltage range <sup>(2)</sup>	0.3	-7	V	
V+ – V-	Supply voltage difference <sup>(2)</sup>		13	V	
V <sub>I</sub>	Input voltage range	Driver ( FORCEOFF, FORCEON, EN)	-0.3	6	V
		Receiver	-25	25	
V <sub>O</sub>	Output voltage range	Driver	-13.2	13.2	V
		Receiver ( INVALID)	-0.3	V <sub>CC</sub> + 0.3	
T <sub>J</sub>	Operating virtual junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 4.2 Recommended Operating Conditions

See [7-1](#) and <sup>(1)</sup>

		MIN	NOM	MAX	UNIT	
Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
		V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver and control high-level input voltage	DIN, EN, FORCEOFF, FORCEON	V <sub>CC</sub> = 3.3 V	2		V
			V <sub>CC</sub> = 5 V	2.4		
V <sub>IL</sub>	Driver and control low-level input voltage	DIN, EN, FORCEOFF, FORCEON			0.8	V
V <sub>I</sub>	Driver and control input voltage	DIN, EN, FORCEOFF, FORCEON	0		5.5	V
	Receiver input voltage		-25		25	
T <sub>A</sub>	Operating free-air temperature	TRSF3223EC	0		70	°C
		TRSF3223EI	-40		85	

- (1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

### 4.3 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000	V
			±15000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 4.4 ESD Ratings - IEC Specifications

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2 Contact Discharge <sup>(1)</sup>	±8,000	V
		IEC 61000-4-2 Air-gap Discharge <sup>(1)</sup>	±15,000	

(1) A minimum of 1-μF capacitor between V<sub>CC</sub> and GND is required to meet the specified IEC 61000-4-2 rating.

### 4.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DB (SOIC)	DW (SOIC)	PW (TSSOP)	RGW (VQFN)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	76.2	76.8	89.7	32.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	36.8	39.6	29.0	23.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	33.9	41.5	41.9	11.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.7	12.6	1.9	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	33.6	40.9	41.3	11.5	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 4.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
I <sub>I</sub>	Input leakage current	EN, FORCEOFF, FORCEON		±0.01	±1	μA	
I <sub>CC</sub>	Supply current	Auto-powerdown disabled	V <sub>CC</sub> = 3.3 V or 5 V, T <sub>A</sub> = 25°C, No load, FORCEOFF and FORCEON at V <sub>CC</sub>		0.3	1.3	mA
		Powered off	No load, FORCEOFF at GND		1	10	
		Auto-powerdown enabled	No load, FORCEOFF at V <sub>CC</sub> , FORCEON at GND, All RIN are open or grounded		1	10	μA

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 4.7 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND	5	5.4		V
V <sub>OL</sub>	Low-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND	–5	–5.4		V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub>		±0.01	±1	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at GND		±0.01	±1	μA
I <sub>OS</sub>	Short-circuit output current <sup>(3)</sup>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V		±35	±60	mA
		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V				
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = ±2 V	300	10M		Ω
I <sub>OZ</sub>	Output leakage current	FORCEOFF = GND, V <sub>CC</sub> = 3 V to 3.6 V, V <sub>O</sub> = ±12 V			±25	μA
		FORCEOFF = GND, V <sub>CC</sub> = 4.5 V to 5.5 V, V <sub>O</sub> = ±12 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

## 4.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT	
Maximum data rate (see <a href="#">5-1</a> )	R <sub>L</sub> = 3 kΩ, One DOUT switching	C <sub>L</sub> = 1000 pF		250			kbit/s	
		C <sub>L</sub> = 250 pF, V <sub>CC</sub> = 3 V to 4.5 V		1000				
		C <sub>L</sub> = 1000 pF, V <sub>CC</sub> = 4.5 V to 5.5 V		1000				
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 kΩ to 7 kΩ, See <a href="#">5-2</a>		300			ns	
SR(tr)	Slew rate, transition region (see <a href="#">5-1</a> )	R <sub>L</sub> = 7 kΩ, C <sub>L</sub> = 150 pF to 1000 pF		8		90	V/μs	
		R <sub>L</sub> = 3 kΩ	C <sub>L</sub> = 1000 pF		12			60
			C <sub>L</sub> = 150 pF to 250 pF		24			150

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## 4.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.1		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.6	2.4	V
		V <sub>CC</sub> = 5 V		1.9	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
		V <sub>CC</sub> = 5 V	0.6	1.4		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5		V
I <sub>OZ</sub>	Output leakage current	EN = V <sub>CC</sub>		±0.05		μA
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5		kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 4.10 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See <a href="#">5-3</a>	150	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See <a href="#">5-3</a>	150	ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">5-4</a>	200	ns
t <sub>dis</sub>	Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">5-4</a>	200	ns
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	See <a href="#">5-3</a>	50	ns

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

#### 4.11 Electrical Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [5-5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$	-2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$	-0.3	0.3	V
$V_{OH}$	$\overline{INVALID}$ high-level output voltage	$I_{OH} = 1\text{ mA}$ , $\overline{FORCEOFF} = V_{CC}$	$V_{CC} - 0.6$		V
$V_{OL}$	$\overline{INVALID}$ low-level output voltage	$I_{OL} = 1.6\text{ mA}$ , $\overline{FORCEOFF} = V_{CC}$		0.4	V

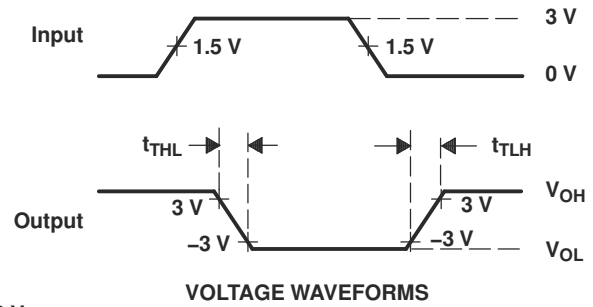
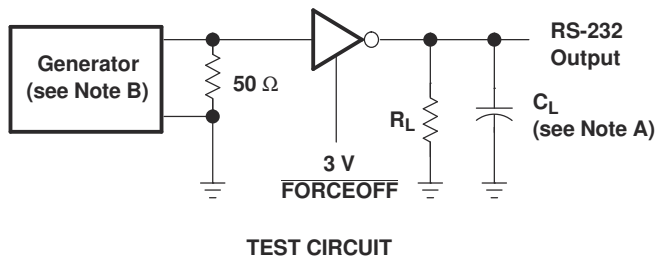
#### 4.12 Switching Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [5-5](#))

PARAMETER		TYP <sup>(1)</sup>	UNIT
$t_{valid}$	Propagation delay time, low- to high-level output	1	$\mu\text{s}$
$t_{invalid}$	Propagation delay time, high- to low-level output	30	$\mu\text{s}$
$t_{en}$	Supply enable time	100	$\mu\text{s}$

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

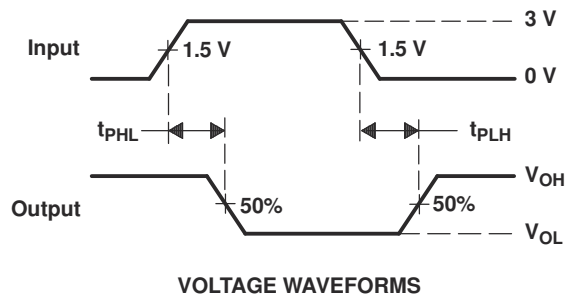
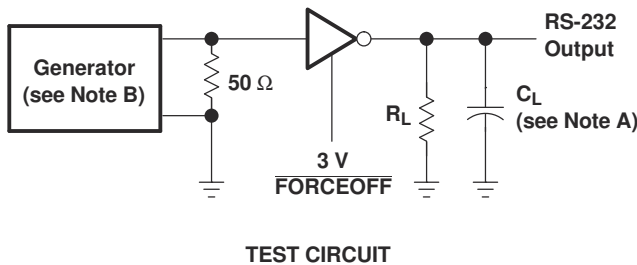
## 5 Parameter Measurement Information



$$SR(tr) = \frac{6\text{ V}}{t_{THL} \text{ or } t_{TLH}}$$

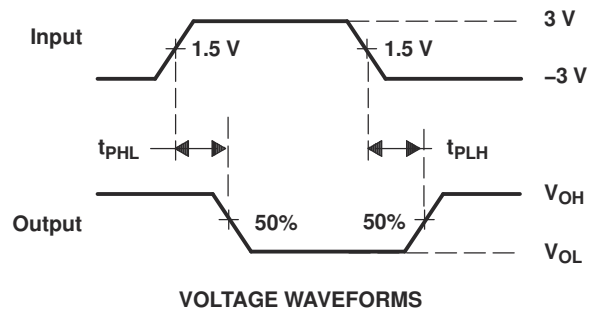
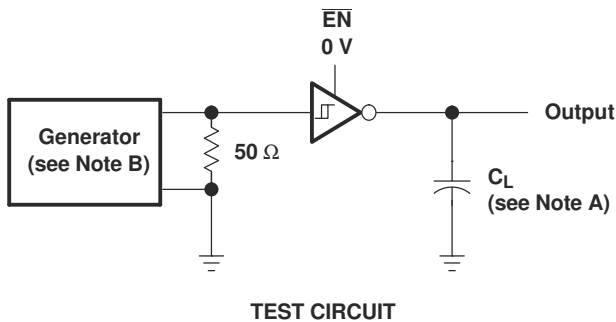
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

### 5-1. Driver Slew Rate



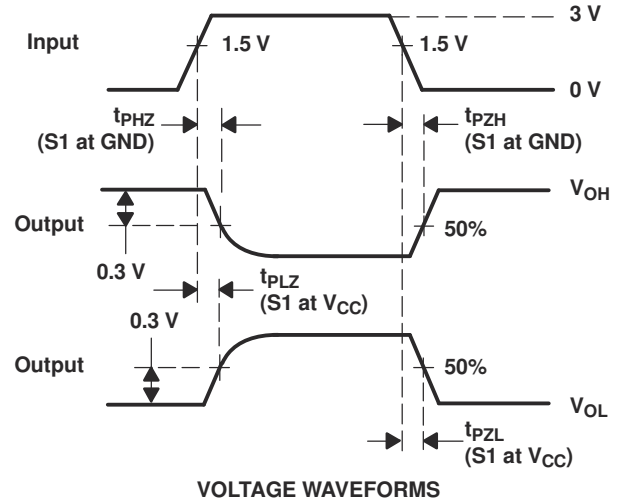
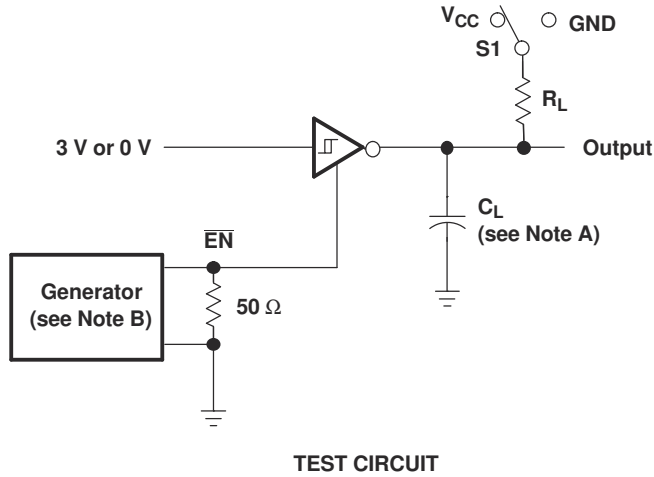
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

### 5-2. Driver Pulse Skew



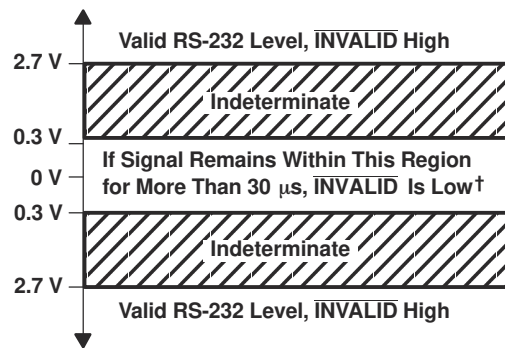
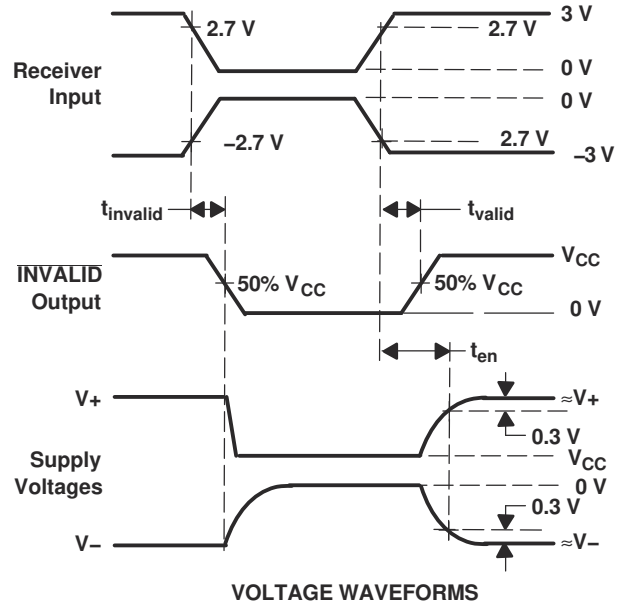
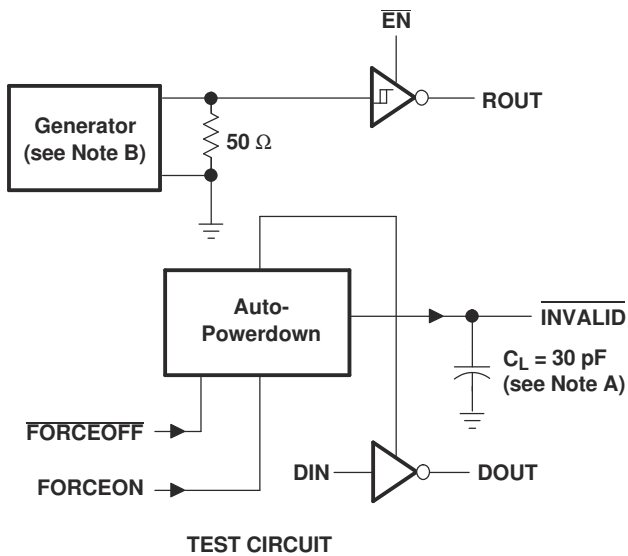
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

### 5-3. Receiver Propagation Delay Times



- A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ .

**5-4. Receiver Enable and Disable Times**



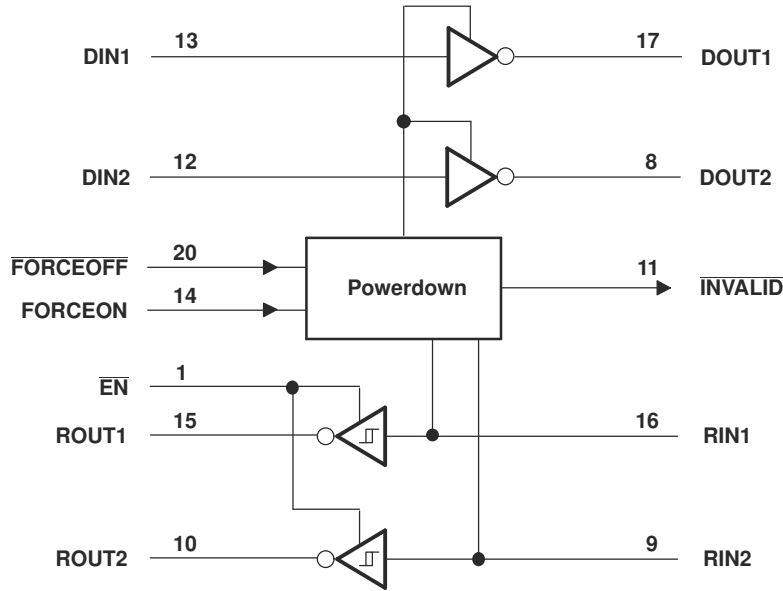
† Auto-powerdown disables drivers and reduces supply current to 1  $\mu$ A

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

**5-5. INVALID Propagation Delay Times and Supply Enabling Time**

## 6 Detailed Description

### 6.1 Functional Block Diagram



Pin numbers are for the DB, DW, and PW packages.

6-1. Logic Diagram (Positive Logic)

### 6.2 Device Functional Modes

Function Tables (Each Driver)

INPUTS <sup>(1)</sup>				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Function Tables (Each Receiver)

INPUTS <sup>(1)</sup>			OUTPUT ROUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

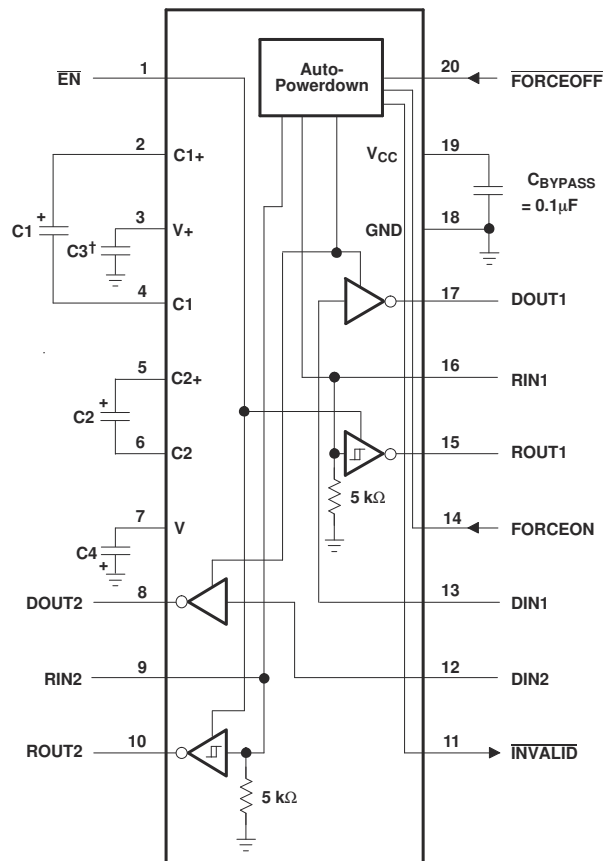
(1) H = high level, L = low level, X = irrelevant,  
Z = high impedance (off),  
Open = input disconnected or connected driver off

## 7 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 7.1 Typical Application



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

**図 7-1. Typical Operating Circuit and Capacitor Values**

#### 7.1.1 Detailed Design Procedure

TRSF3223E has integrated charge-pump that generates positive and negative rails needed for RS-232 signal levels. Main design requirement is that charge-pump capacitor terminals must be connected with recommended capacitor values. Charge-pump rail voltages and device supply pin must be properly bypassed with ceramic capacitors.

## 8 Device and Documentation Support

### 8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

### 8.2 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 8.5 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision A (September 2011) to Revision B (December 2023)

	Page
ドキュメント全体にわたって表、図、相互参照の採番方法を変更.....	1
Added the <i>ESD Ratings</i> tables.....	3
Added the <i>Thermal Information</i> table.....	4
Changed the I <sub>CC</sub> Auto-powerdown disabled max value from 1 mA to 1.3 mA in the <i>Electrical Characteristics</i>	4

### Changes from Revision \* (August 2007) to Revision A (September 2011)

	Page
RGW パッケージをデータシートに追加.....	1
RHL パッケージをデータシートから削除.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TRSF3223ECPWR</a>	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	0 to 70	RT23EC
<a href="#">TRSF3223EIDBR</a>	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIDBR.A	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
<a href="#">TRSF3223EIDWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3223EI
TRSF3223EIDWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3223EI
<a href="#">TRSF3223EIPW</a>	Obsolete	Production	TSSOP (PW)   20	-	-	Call TI	Call TI	-40 to 85	RT23EI
<a href="#">TRSF3223EIPWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIPWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIPWRG4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIPWRG4.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
<a href="#">TRSF3223EIRGWR</a>	Active	Production	VQFN (RGW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RT23EI
TRSF3223EIRGWR.A	Active	Production	VQFN (RGW)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RT23EI

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3223EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3223EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRSF3223EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TRSF3223EIPWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TRSF3223EIRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3223EIDBR	SSOP	DB	20	2000	353.0	353.0	32.0
TRSF3223EIDWR	SOIC	DW	20	2000	356.0	356.0	45.0
TRSF3223EIPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
TRSF3223EIPWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
TRSF3223EIRGWR	VQFN	RGW	20	3000	353.0	353.0	32.0



# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

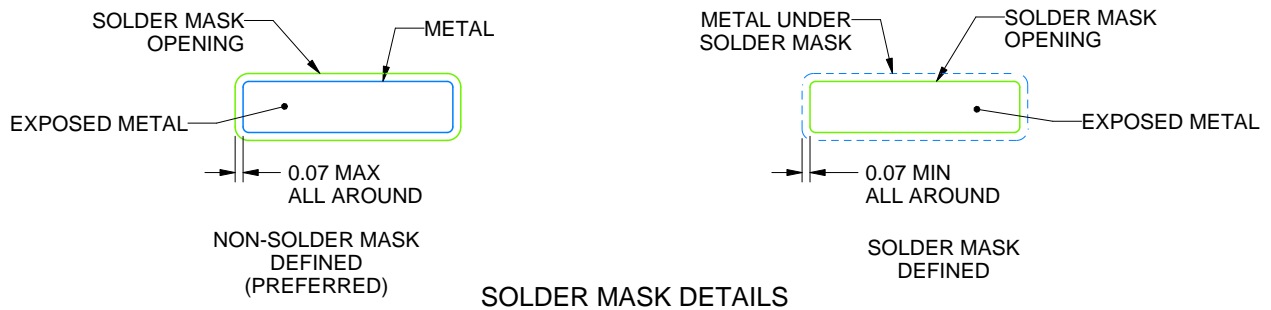
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

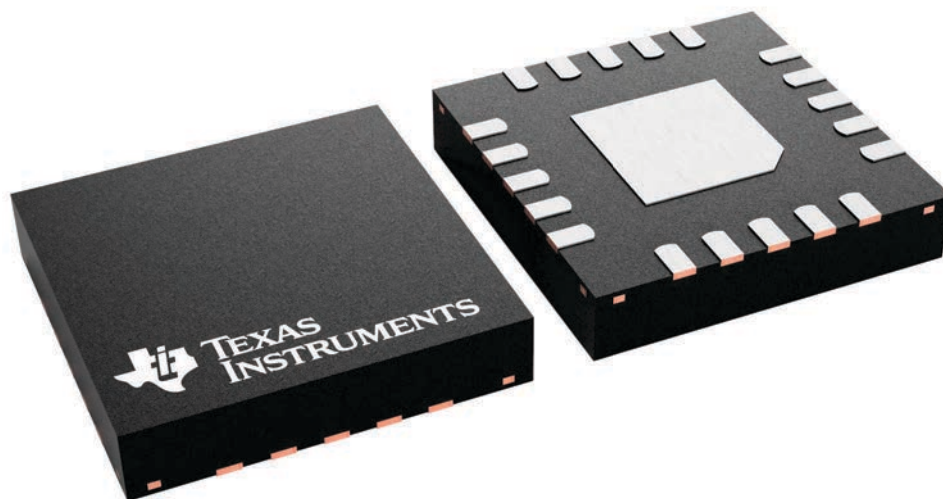
**RGW 20**

**VQFN - 1 mm max height**

5 x 5, 0.65 mm pitch

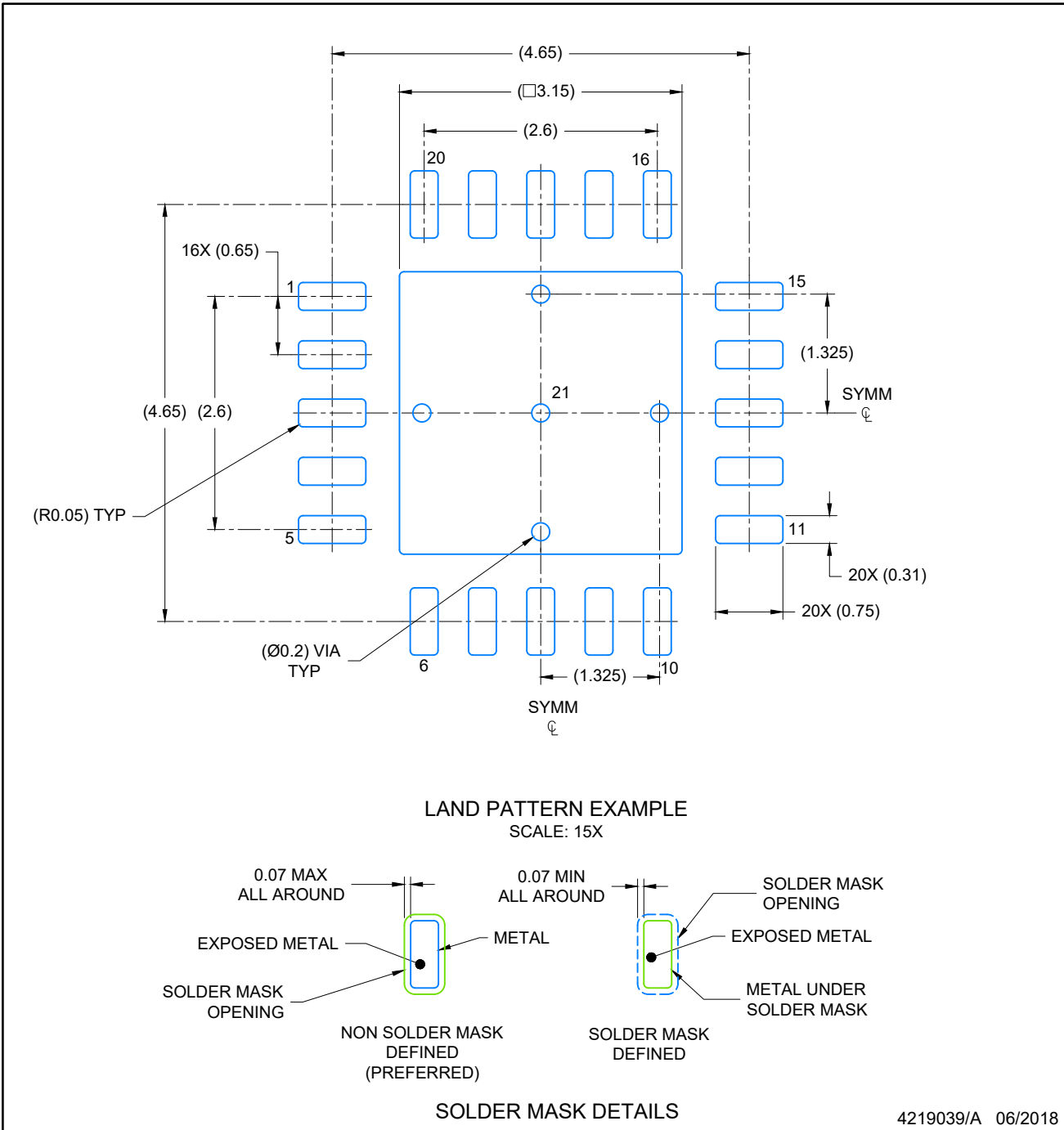
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227157/A





NOTES: (continued)

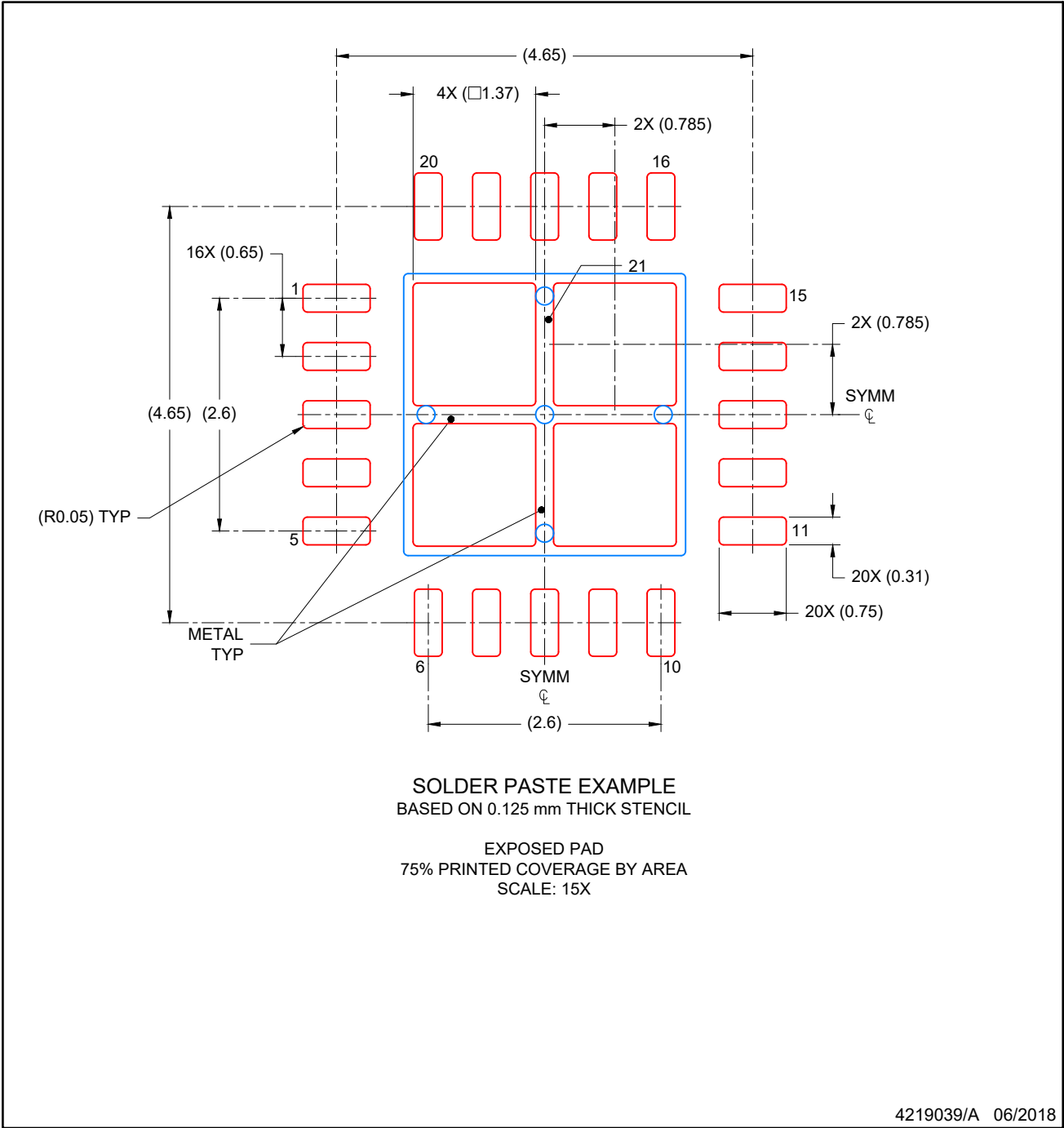
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGW0020A

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日 : 2025 年 10 月