



TS3A5017-Q1 2チャンネル、4:1の車載アプリケーション用アナログ・スイッチ

1 特長

- 車載アプリケーション用にAEC-Q100認定済み
 - デバイス温度: T_A -40°C ~ 125°C
 - デバイスHBM分類レベル: $\pm 1500V$
 - デバイスCDM分類レベル: $\pm 1000V$
- 電源オフ保護に対応: $V_{CC} = 0V$ 時、I/OピンはHi-Z
- 低いオン抵抗
- 低い電荷注入
- 1Ωのオン抵抗マッチング
- 全高調波歪(THD+N): 0.25%
- 2.3V~3.6Vの単電源で動作
- JESD 78, Class II準拠で100mA超のラッチアップ性能

2 アプリケーション

- サンプル・アンド・ホールド回路
- インフォテインメントのオーディオおよびビデオ信号のルーティング
- テレマティクス制御ユニット

3 概要

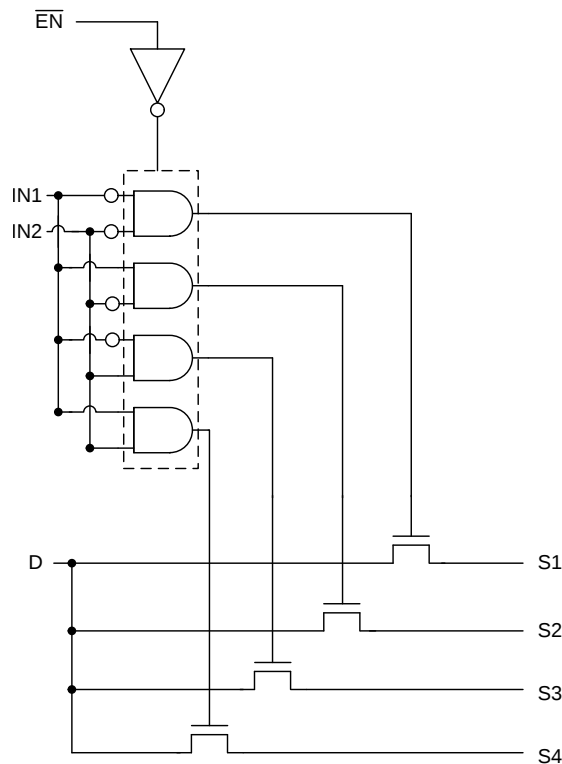
TS3A5017-Q1デバイスは2チャンネル、4:1のマルチプレクサで、2.3V~3.6Vで動作するように設計されています。このデバイスは双方向で、デジタルとアナログ両方の信号を処理できます。このデバイスの電源オフ保護機能により、 $V_{CC} = 0V$ のときは信号パスが高インピーダンスになることが保証され、電源シーケンシングが簡単になり、システムの信頼性が向上します。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TS3A5017-Q1	VQFN (16)	4.00mm×3.50mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



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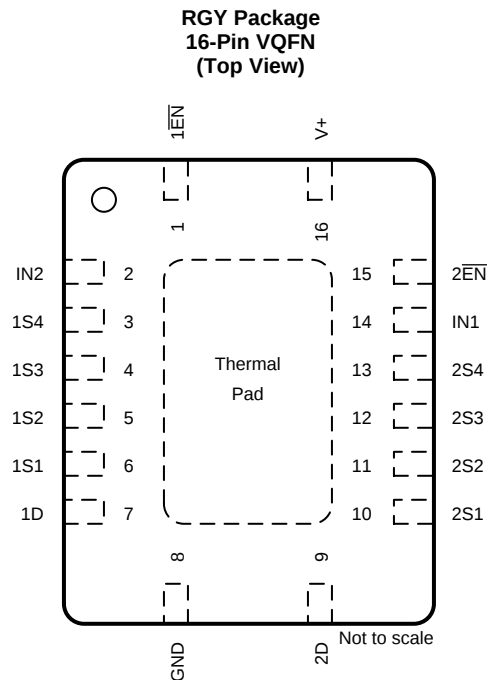
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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2018年10月	*	初版

5 Pin Configuration and Functions



If exposed thermal pad is used, it must be connected as a secondary ground or left electrically open.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
7	1D	I/O	Common path for switch 1
1	$\overline{1EN}$	I	Active-low enable for switch 1
6	1S1	I/O	Switch 1 channel 1
5	1S2	I/O	Switch 1 channel 2
4	1S3	I/O	Switch 1 channel 3
3	1S4	I/O	Switch 1 channel 4
9	2D	I/O	Common path for switch 2
15	$\overline{2EN}$	I	Active-low enable for switch 2
10	2S1	I/O	Switch 2 channel 1
11	2S2	I/O	Switch 2 channel 2
12	2S3	I/O	Switch 2 channel 3
13	2S4	I/O	Switch 2 channel 4
8	GND	–	Ground
14	IN1	I	Switch 1 input select
2	IN2	I	Switch 2 input select
16	V+	–	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

			MIN	MAX	UNIT
V ₊	Supply voltage ⁽³⁾		–0.5	4.6	V
V _S , V _D	Analog voltage ^{(3) (4)}		–0.5	4.6	V
I _{SK} , I _{DK}	Analog port clamp current	V _S , V _D < 0	–50		mA
I _S , I _D	ON-state switch current	V _S , V _D = 0 to 7 V	–128	128	mA
V _I	Digital input voltage		–0.5	4.6	V
I _{IK}	Digital input clamp current ^{(3) (4)}	V _I < 0	–50		mA
I ₊	Continuous current through V ₊			100	mA
I _{GND}	Continuous current through GND		–100		mA
T _{stg}	Storage temperature		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{I/O}	Switch input/output voltage range	0	3.6	V
V ₊	Supply voltage range	2.3	3.6	V
V _I	Control input voltage range	0	3.6	V
T _A	Operating Temperature Range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TS3A5017-Q1	UNIT
		RGY (VQFN)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	47.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	58.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	24.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	24.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics for 3.3-V Supply

 $V_+ = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Analog Switch								
V _D , V _S	Analog signal range				0		V ₊	V
r _{on}	ON-state resistance	0 ≤ V _S ≤ V ₊ , I _D = −32 mA,	Switch ON, see Figure 12	T _A = 25°C V ₊ = 3 V	11			Ω
				T _A = Full V ₊ = 3 V	16			
Δr _{on}	ON-state resistance match between channels	V _S = 2.1 V, I _D = −32 mA,	Switch ON, see Figure 12	T _A = 25°C V ₊ = 3 V	1			Ω
				T _A = Full V ₊ = 3 V	5			
r _{on(flat)}	ON-state resistance flatness	0 ≤ V _S ≤ V ₊ , I _D = −32 mA,	Switch ON, see Figure 12	T _A = 25°C V ₊ = 3 V	7			Ω
				T _A = Full V ₊ = 3 V	12			
I _{S(OFF)}	S OFF leakage current	V _S = 1 V, V _D = 3 V, or V _S = 3 V, V _D = 1 V,	Switch OFF, see Figure 13	T _A = 25°C V ₊ = 3.6 V	0.05			μA
I _{SPWR(OFF)}		V _S = 0 to 3.6 V, V _D = 3.6 V to 0,		T _A = Full V ₊ = 3.6 V	−0.3		0.3	
				T _A = 25°C V ₊ = 0 V	0.5			
				T _A = Full V ₊ = 0 V	−10		10	
I _{D(OFF)}	D OFF leakage current	V _S = 1 V, V _D = 3 V, or V _S = 3 V, V _D = 1 V,	Switch OFF, see Figure 13	T _A = 25°C V ₊ = 3.6 V	0.05			μA
I _{DPWR(OFF)}		V _D = 0 to 3.6 V, V _S = 3.6 V to 0,		T _A = Full V ₊ = 3.6 V	−0.3		0.3	
				T _A = 25°C V ₊ = 0 V	0.5			
				T _A = Full V ₊ = 0 V	−20		20	
I _{S(ON)}	S ON leakage current	V _S = 1 V, V _D = Open, or V _S = 3 V, V _D = Open,	Switch ON, see Figure 14	T _A = 25°C V ₊ = 3.6 V	0.05			μA
				T _A = Full V ₊ = 3.6 V	−0.3		0.3	
I _{D(ON)}	D ON leakage current	V _D = 1 V, V _S = Open, or V _D = 3 V, V _S = Open,	Switch ON, see Figure 14	T _A = 25°C V ₊ = 3.6 V	0.05			μA
				T _A = Full V ₊ = 3.6 V	−0.3		0.3	
Digital Control Inputs (IN1, IN2, $\overline{\text{EN}}$) ⁽²⁾								
V _{IH}	Input logic high			T _A = Full	2		V ₊	V
V _{IL}	Input logic low			T _A = Full	0		0.8	V
I _{IH} , I _{IL}	Input leakage current	V _I = V ₊ or 0		T _A = 25°C V ₊ = 3.6 V	0.05			μA
				T _A = Full V ₊ = 3.6 V	−1		1	
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0, C _L = 0.1 nF,	See Figure 21	T _A = 25°C V ₊ = 3.3 V	5			pC
C _{S(OFF)}	S OFF capacitance	V _S = V ₊ or GND, Switch OFF,	See Figure 15	T _A = 25°C V ₊ = 3.3 V	4.5			pF
C _{D(OFF)}	D OFF capacitance	V _D = V ₊ or GND, Switch OFF,	See Figure 15	T _A = 25°C V ₊ = 3.3 V	19			pF
C _{S(ON)}	S ON capacitance	V _S = V ₊ or GND, Switch ON,	See Figure 15	T _A = 25°C V ₊ = 3.3 V	27			pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 3.3-V Supply (continued)

 $V_+ = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$C_{D(ON)}$	D ON capacitance	$V_D = V_+$ or GND, Switch ON,	See Figure 15	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		27		pF
C_I	Digital input capacitance	$V_I = V_+$ or GND,	See Figure 15	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		3		pF
BW	Bandwidth	$R_L = 50 \Omega$, Switch ON,	See Figure 17	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		165		MHz
O_{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See Figure 18	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		-69		dB
O_{ISO}	OFF isolation	$R_L = 50 \Omega$, $f = 10 \text{ MHz}$,	See Figure 18	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		-49		dB
X_{TALK}	Crosstalk	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See Figure 19	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		-69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	$R_L = 50 \Omega$, $f = 1 \text{ MHz}$,	See Figure 20	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		-80		dB
THD	Total harmonic distortion	$R_L = 600 \Omega$, $C_L = 50 \text{ pF}$,	$f = 20 \text{ Hz to } 20 \text{ kHz}$, see Figure 22	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		0.25		%
Supply								
I_+	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	$T_A = 25^\circ\text{C}$ $V_+ = 3.6 \text{ V}$		2.5	7	μA
				$T_A = \text{Full}$ $V_+ = 3.6 \text{ V}$			10	

6.6 Electrical Characteristics for 2.5-V Supply

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Analog Switch								
V _D , V _S	Analog signal range				0		V ₊	V
r _{on}	ON-state resistance	0 ≤ V _S ≤ V ₊ , I _D = −24 mA,	Switch ON, see Figure 12	T _A = 25°C V ₊ = 2.3 V	22		Ω	
				T _A = Full V ₊ = 2.3 V	28			
Δr _{on}	ON-state resistance match between channels	V _S = 1.6 V, I _D = −24 mA,	Switch ON, see Figure 12	T _A = 25°C V ₊ = 2.3 V	1		Ω	
				T _A = Full V ₊ = 2.3 V	5			
r _{on(flat)}	ON-state resistance flatness	0 ≤ V _S ≤ V ₊ , I _D = −24 mA,	Switch ON, see Figure 12	T _A = 25°C V ₊ = 2.3 V	18		Ω	
				T _A = Full V ₊ = 2.3 V	24			
I _{S(OFF)}	S OFF leakage current	V _S = 0.5 V, V _D = 2.2 V, or V _S = 2.2 V, V _D = 0.5 V,	Switch OFF, see Figure 13	T _A = 25°C V ₊ = 2.7 V	0.05		μA	
T _A = Full V ₊ = 2.7 V				−0.3	0.3			
I _{SPWR(OFF)}		V _S = 0 to 2.7 V, V _D = 2.7 V to 0,		T _A = 25°C V ₊ = 0 V	0.5			
				T _A = Full V ₊ = 0 V	−15	15		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply (continued)

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{D(OFF)}	D OFF leakage current	V _S = 0.5 V, V _D = 2.2 V, or V _S = 2.2 V, V _D = 0.5V,	Switch OFF, see § 13	T _A = 25°C V ₊ = 2.7 V	0.05		μA	
I _{DPWR(OFF)}		V _D = 0 to 2.7 V, V _S = 2.7 V to 0,		T _A = Full V ₊ = 2.7 V	-0.3	0.3		
				T _A = 25°C V ₊ = 0 V	0.5			
				T _A = Full V ₊ = 0 V	-20	20		
I _{S(ON)}	S ON leakage current	V _S = 0.5 V, V _D = Open, or V _S = 2.2 V, V _D = Open,	Switch ON, see § 14	T _A = 25°C V ₊ = 2.7 V	0.05		μA	
I _{D(ON)}	D ON leakage current	V _D = 0.5 V, V _S = Open, or V _D = 2.2 V, V _S = Open,		T _A = Full V ₊ = 2.7 V	-0.3	0.3		
			T _A = 25°C V ₊ = 2.7 V	0.05		μA		
			Switch ON, see § 14	T _A = Full V ₊ = 2.7 V	-0.3		0.3	
				Logic Inputs (IN1, IN2, $\overline{\text{EN}}$)⁽²⁾				
V _{IH}	Input logic high			T _A = Full	1.7		V ₊	V
V _{IL}	Input logic low			T _A = Full	0		0.7	V
I _{IH} , I _{IL}	Input leakage current	V _I = V ₊ or 0		T _A = 25°C V ₊ = 2.7 V	0.05		μA	
				T _A = Full V ₊ = 2.7 V	-1	1		
Q _C	Charge injection	V _{GEN} = 0, R _{GEN} = 0, C _L = 0.1 nF,	See § 21	T _A = Full V ₊ = 2.5 V	3			pC
C _{S(OFF)}	S OFF capacitance	V _S = V ₊ or GND, Switch OFF,	See § 15	T _A = Full V ₊ = 2.5 V	4.5			pF
C _{D(OFF)}	D OFF capacitance	V _D = V ₊ or GND, Switch OFF,	See § 15	T _A = Full V ₊ = 2.5 V	18.5			pF
C _{S(ON)}	S ON capacitance	V _S = V ₊ or GND, Switch ON,	See § 15	T _A = Full V ₊ = 2.5 V	26			pF
C _{D(ON)}	D ON capacitance	V _D = V ₊ or GND, Switch ON,	See § 15	T _A = Full V ₊ = 2.5 V	26			pF
C _I	Digital input capacitance	V _I = V ₊ or GND,	See § 15	T _A = Full V ₊ = 2.5 V	3			pF
BW	Bandwidth	R _L = 50 Ω, Switch ON,	See § 17	T _A = Full V ₊ = 2.5 V	165			MHz
O _{ISO}	OFF isolation	R _L = 50 Ω, f = 1 MHz,	See § 18	T _A = Full V ₊ = 2.5 V	-69			dB
O _{ISO}	OFF isolation	R _L = 50 Ω, f = 10 MHz,	See § 18	T _A = Full V ₊ = 2.5 V	-49			dB
X _{TALK}	Crosstalk	R _L = 50 Ω, f = 1 MHz,	See § 19	T _A = Full V ₊ = 2.5 V	-69			dB
X _{TALK(ADJ)}	Crosstalk adjacent	R _L = 50 Ω, f = 1 MHz,	See § 20	T _A = Full V ₊ = 2.5 V	-85			dB
THD	Total harmonic distortion	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, see § 22	T _A = Full V ₊ = 2.5 V	0.3			%
Supply								

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics for 2.5-VSupply (continued)

 $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_+	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$		2.5	7	μA
				$T_A = \text{Full}$ $V_+ = 2.7 \text{ V}$			10	

6.7 Switching Characteristics for 3.3-VSupply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turnon time ⁽¹⁾	$V_D = 2 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, see 16	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		5	9.5	ns
				$T_A = \text{Full}$ $V_+ = 3 \text{ V to } 3.6 \text{ V}$			10.5	
t_{OFF}	Turnoff time ⁽¹⁾	$V_D = 2 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, see 16	$T_A = 25^\circ\text{C}$ $V_+ = 3.3 \text{ V}$		1.5	3.5	ns
				$T_A = \text{Full}$ $V_+ = 3 \text{ V to } 3.6 \text{ V}$			4.5	

(1) Specified by design, not tested in production

6.8 Switching Characteristics for 2.5-VSupply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turnon time ⁽¹⁾	$V_{\text{COM}} = 2 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, see 16	$T_A = 25^\circ\text{C}$ $V_+ = 2.5 \text{ V}$		5	8	ns
				$T_A = \text{Full}$ $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$			10	
t_{OFF}	Turnoff time ⁽¹⁾	$V_{\text{COM}} = 2 \text{ V}$, $R_L = 300 \Omega$,	$C_L = 35 \text{ pF}$, see 16	$T_A = 25^\circ\text{C}$ $V_+ = 2.5 \text{ V}$		2	4.5	ns
				$T_A = \text{Full}$ $V_+ = 2.3 \text{ V to } 2.7 \text{ V}$			6	

(1) Specified by design, not tested in production.

6.9 Typical Characteristics

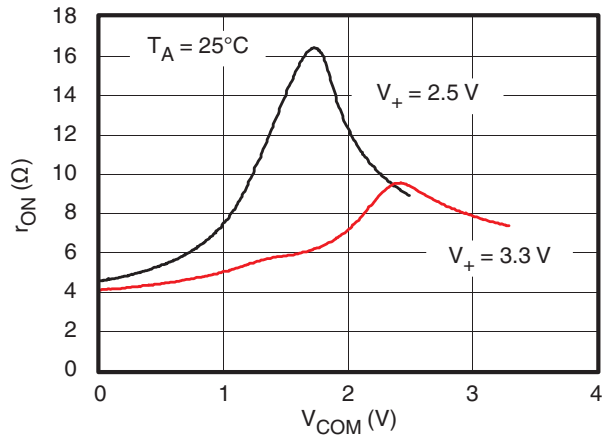


FIG 1. r_{ON} VS V_{COM}

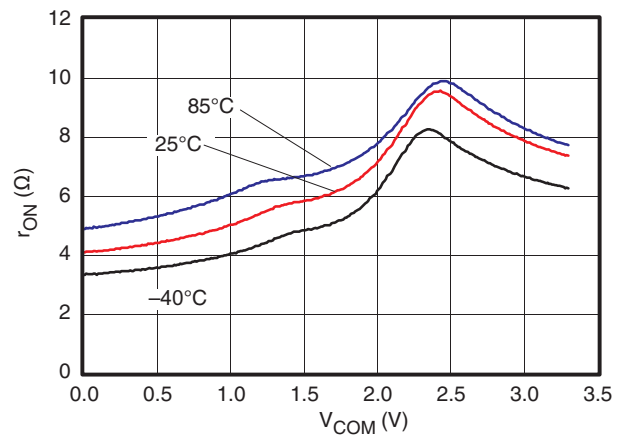


FIG 2. r_{ON} VS V_{COM} ($V_+ = 3.3\text{ V}$)

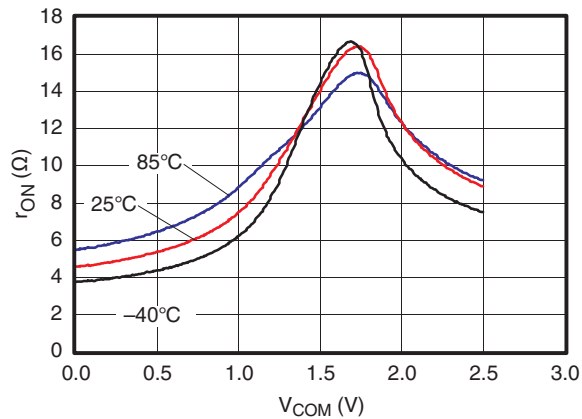


FIG 3. r_{ON} VS V_{COM} ($V_+ = 2.5\text{ V}$)

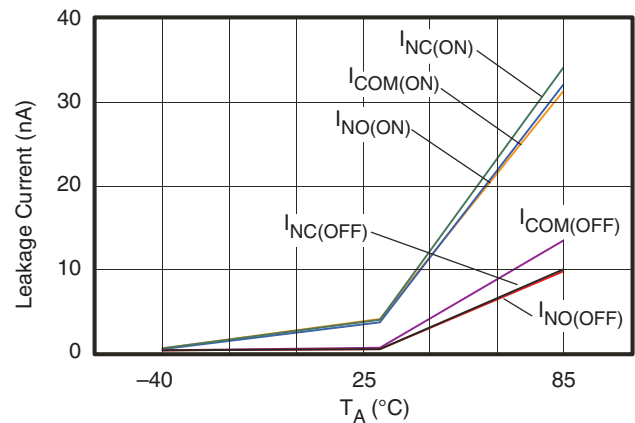


FIG 4. Leakage Current vs Temperature ($V_+ = 3.6\text{ V}$)

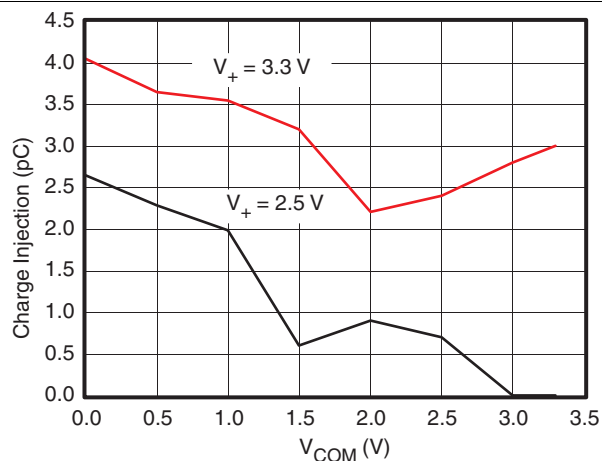


FIG 5. Charge Injection (Q_C) VS V_{COM}

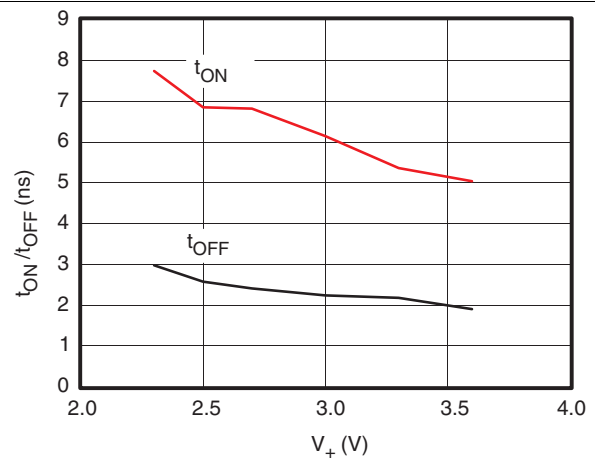


FIG 6. t_{ON} and t_{OFF} VS Supply Voltage

Typical Characteristics (continued)

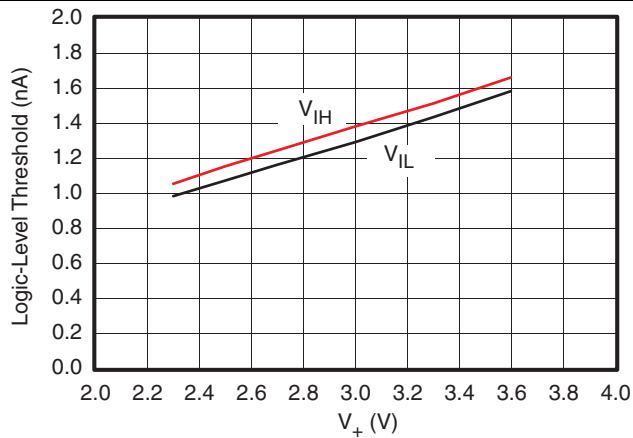


图 7. Logic-Level Threshold vs V_+

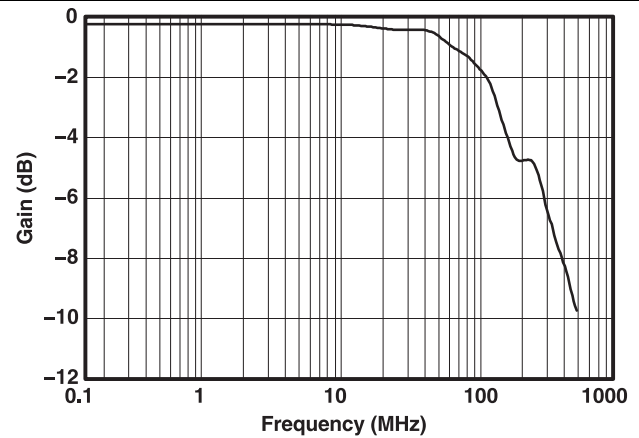


图 8. Bandwidth (Gain vs Frequency) ($V_+ = 3.3$ V)

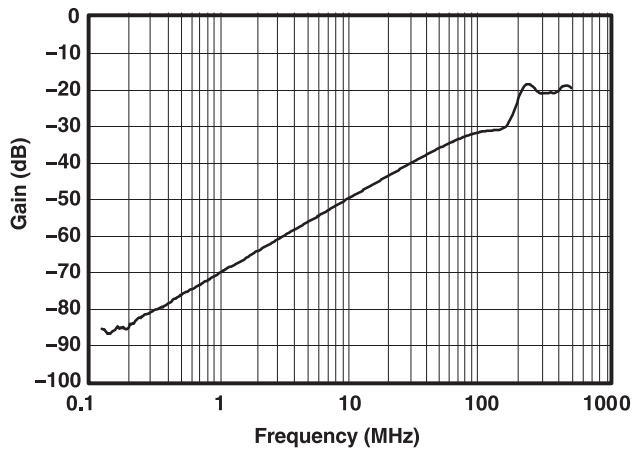


图 9. OFF Isolation and Crosstalk vs Frequency ($V_+ = 3.3$ V)

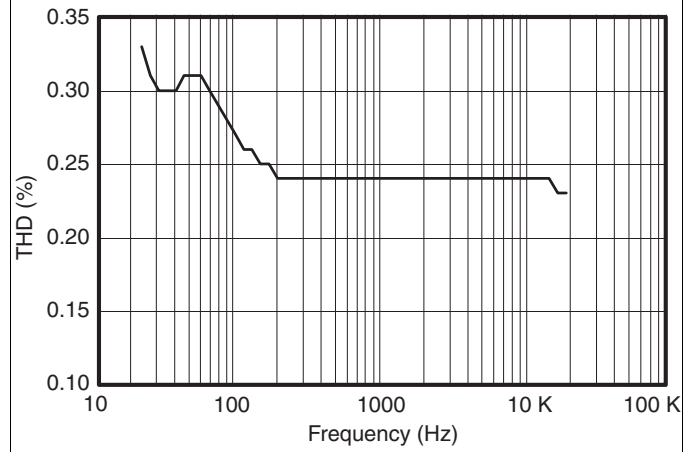


图 10. Total Harmonic Distortion vs Frequency

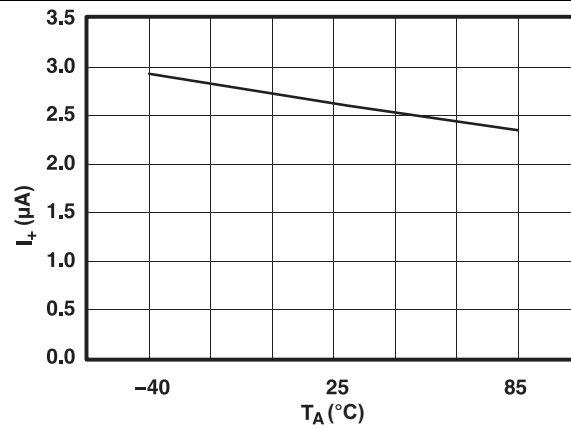


图 11. Power-Supply Current vs Temperature ($V_+ = 3.6$ V)

7 Parameter Measurement Information

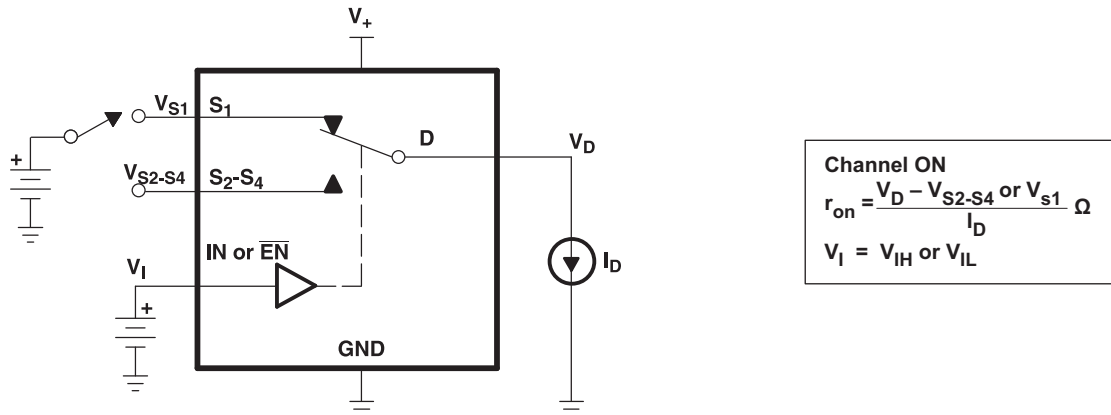


FIG 12. ON-State Resistance (r_{on})

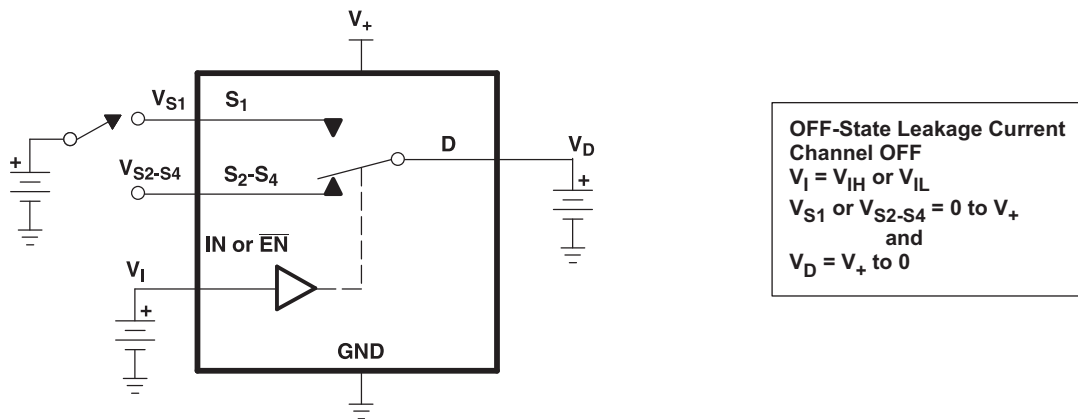


FIG 13. OFF-State Leakage Current ($I_{D(OFF)}$, $I_{S(OFF)}$)

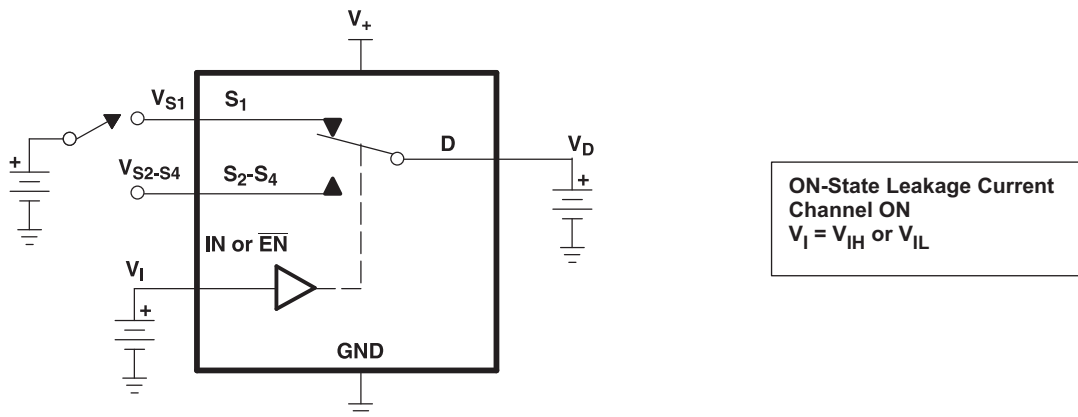
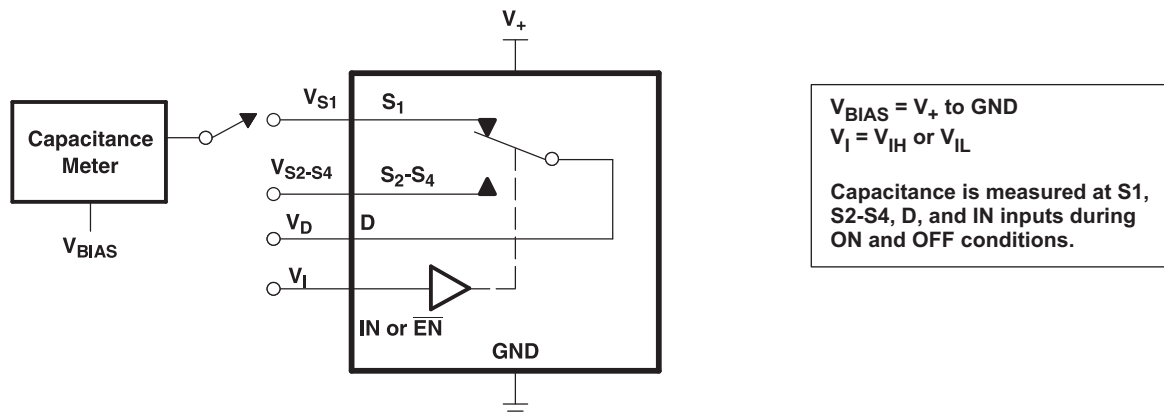
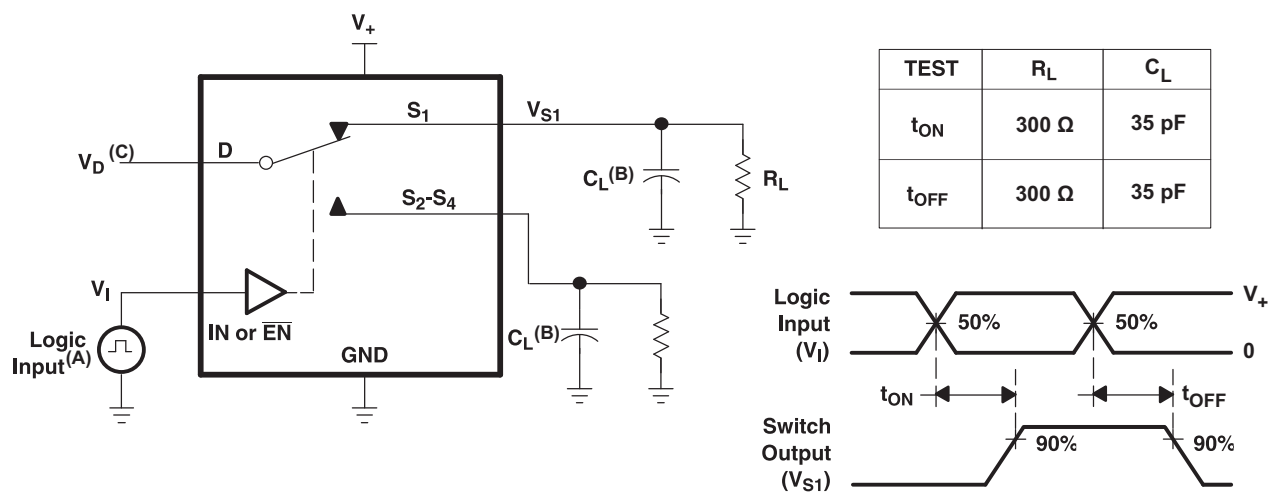
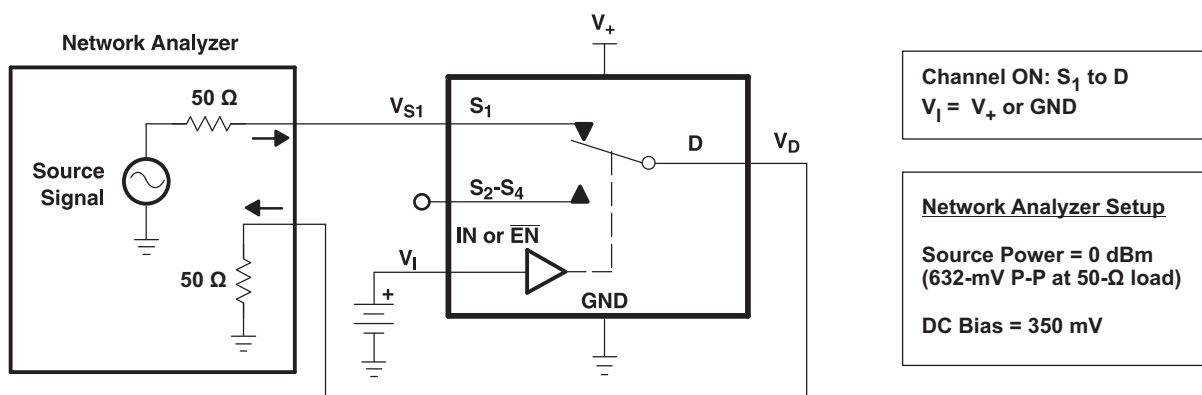


FIG 14. ON-State Leakage Current ($I_{D(ON)}$, $I_{S(ON)}$)

Parameter Measurement Information (continued)

FIG 15. Capacitance (C_I , $C_{D(OFF)}$, $C_{D(ON)}$, $C_{S(OFF)}$, $C_{S(ON)}$)


- A. All input pulses are supplied by generators having the following characteristics:
 PRR $\leq$ 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.
- C. See Electrical Characteristics for V_D .

FIG 16. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

FIG 17. Bandwidth (BW)

Parameter Measurement Information (continued)

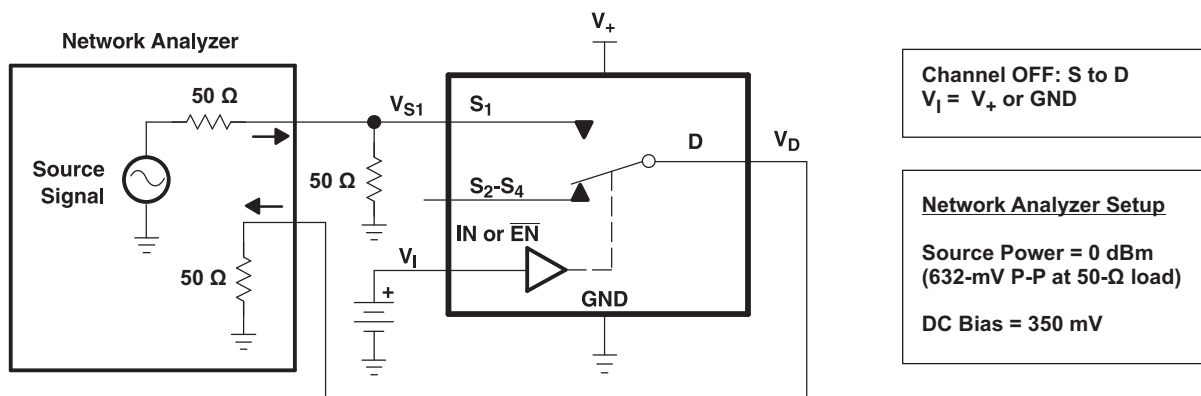


图 18. OFF Isolation (O_{ISO})

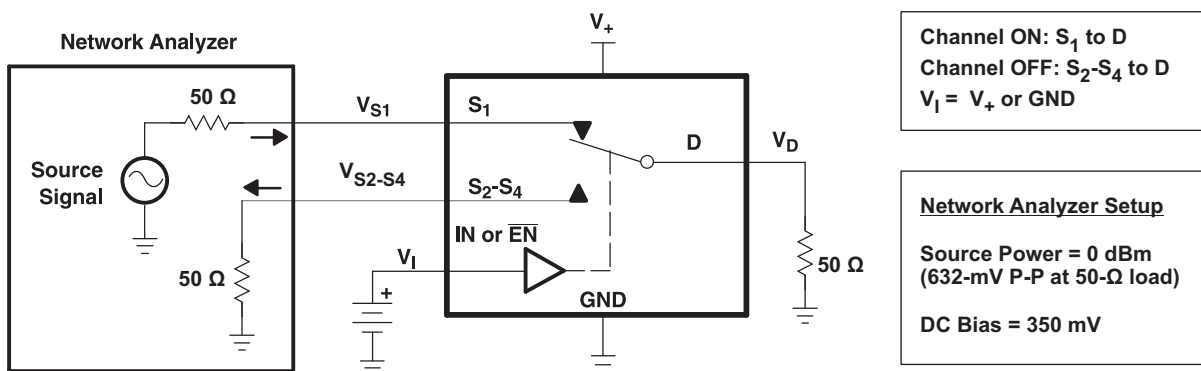


图 19. Crosstalk (X_{TALK})

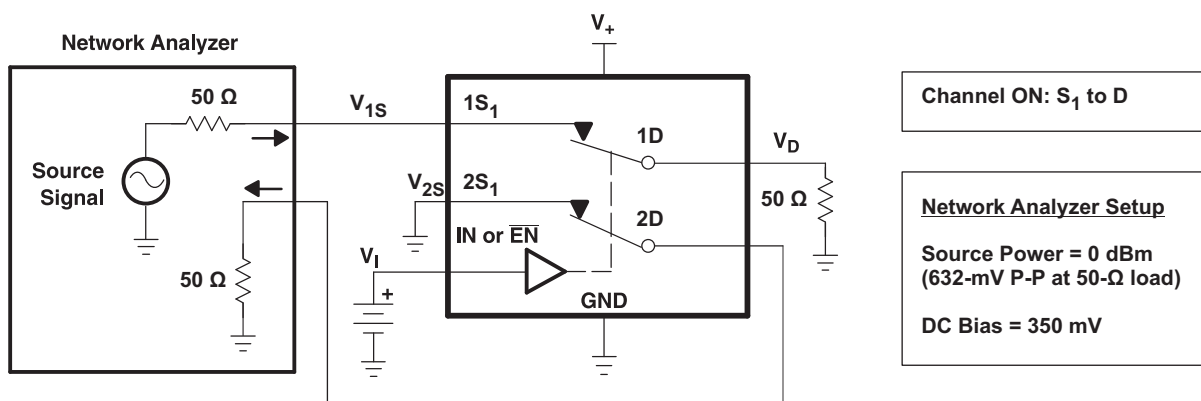
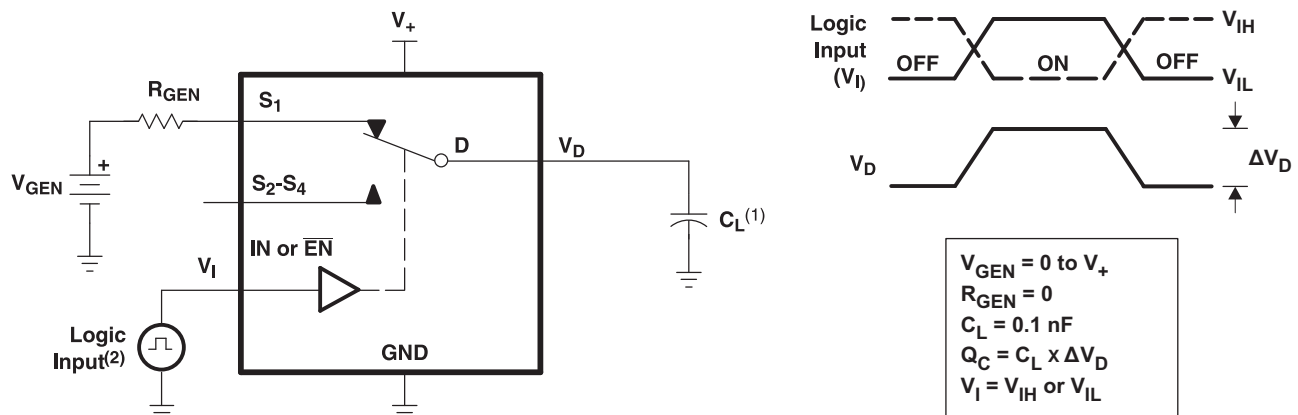


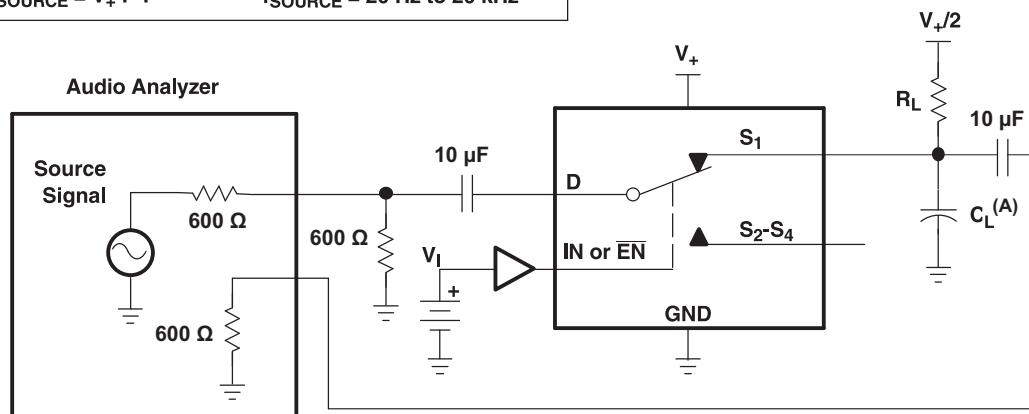
图 20. Adjacent Crosstalk (X_{TALK})

Parameter Measurement Information (continued)


- A. All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- B. C_L includes probe and jig capacitance.

⊠ 21. Charge Injection (Q_C)

Channel ON: D to S	$V_I = V_{IH} \text{ or } V_{IL}$
$V_{SOURCE} = V_+$ P-P	$f_{SOURCE} = 20 \text{ Hz to } 20 \text{ kHz}$



- A. C_L includes probe and jig capacitance.

⊠ 22. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A5017-Q1 is a dual Single-Pole-4-Throw (SP4T) solid-state analog switch. The TS3A5017-Q1, like all analog switches, is bidirectional. Each D pin connects to its four respective S pins, with the switch connection dependent on the status of $\overline{\text{EN}}$, IN2, and IN1. See 表 1 for the switch configuration truth table.

8.2 Functional Block Diagram

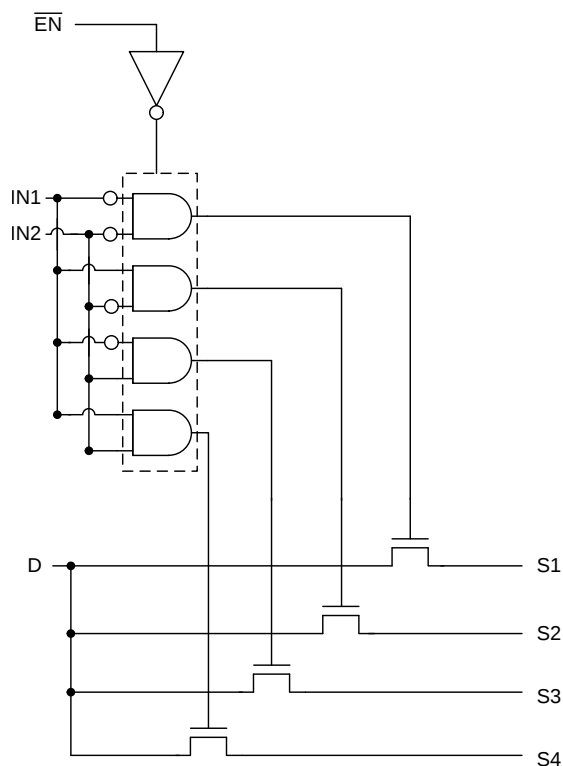


図 23. Functional Block Diagram (Each Switch)

8.3 Feature Description

Isolation in powered-down mode allows signals to be present at the inputs while the switch is powered off without causing damage to the device. The low ON-state resistance and low charge injection give the TS3A5017-Q1 better performance at higher speeds.

8.4 Device Functional Modes

表 1. Function Table

$\overline{\text{EN}}$	IN2	IN1	D TO S, S TO D
L	L	L	D = S ₁
L	L	H	D = S ₂
L	H	L	D = S ₃
L	H	H	D = S ₄
H	X	X	OFF

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3A5017-Q1 can be used in a variety of customer systems. The TS3A5017-Q1 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

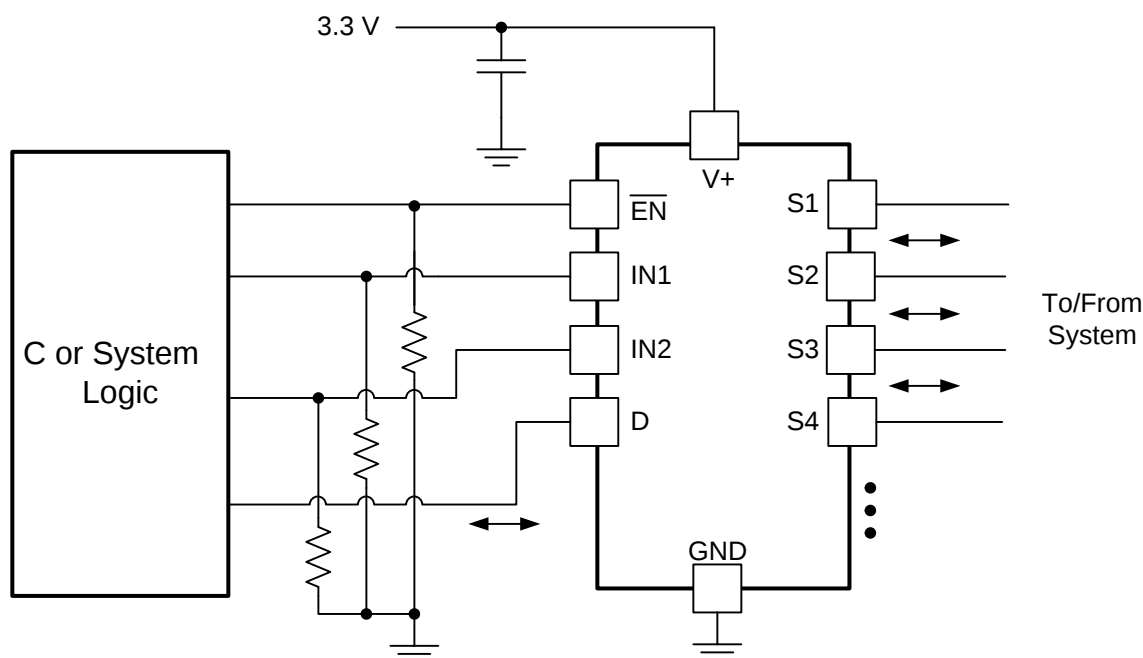


图 24. System Schematic for TS3A5017-Q1

9.2.1 Design Requirements

In this particular application, V+ was 3.3 V, although V+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See [Power Supply Recommendations](#) for more details.

9.2.2 Detailed Design Procedure

In this application, EN, IN1, and IN2 are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

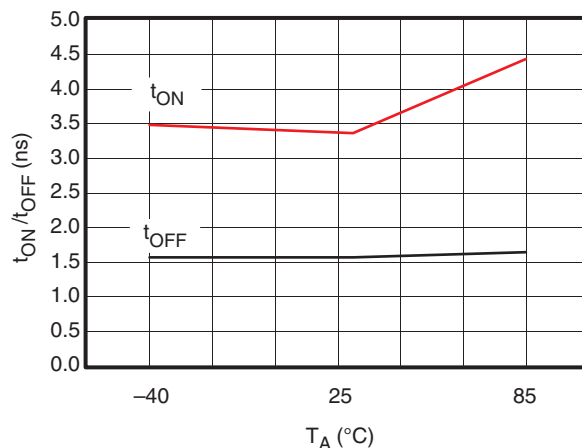


图 25. t_{ON} and t_{OFF} vs Temperature (V₊ = 3.3 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operation Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and the traces will turn corners. [Figure 26](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN1, IN2, and $\overline{\text{EN}}$ pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states. See *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#) for more details.

11.2 Layout Example

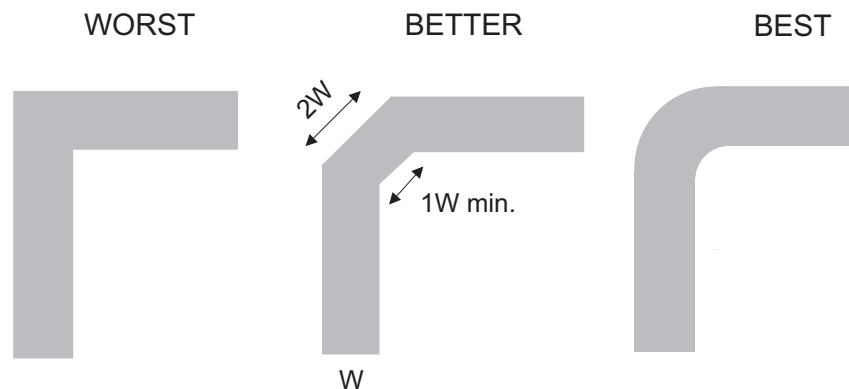


Figure 26. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

表 2. パラメータの説明

記号	説明
V_{COM}	COM電圧
V_{NC}	NC電圧
V_{NO}	NO電圧
r_{on}	チャンネルがオンのときのCOMとNCポート間、またはCOMとNOポート間の抵抗
Δr_{on}	特定デバイスでのチャンネル間の r_{on} の差
$r_{on(flat)}$	規定の条件の範囲における、チャンネルの r_{on} の最大値と最小値との差
$I_{NC(OFF)}$	対応チャンネル(NCからCOM)がオフ状態のとき、NCポートで測定されるリーク電流
$I_{NC(ON)}$	対応チャンネル(NCからCOM)がオン状態、出力(COM)がオープンのとき、NCポートで測定されるリーク電流
$I_{NO(OFF)}$	対応チャンネル(NOからCOM)がオフ状態のとき、NOポートで測定されるリーク電流
$I_{NO(ON)}$	対応チャンネル(NOからCOM)がオン状態、出力(COM)がオープンのとき、NOポートで測定されるリーク電流
$I_{COM(OFF)}$	対応チャンネル(COMからNCまたはNO)がオフ状態のとき、COMポートで測定されるリーク電流
$I_{COM(ON)}$	対応チャンネル(COMからNCまたはNO)がオン状態、出力(NCまたはNO)がオープン/のとき、COMポートで測定されるリーク電流
V_{IH}	制御入力(IN, $\overline{EN}$)の論理HIGHの最小入力電圧
V_{IL}	制御入力(IN, $\overline{EN}$)の論理LOWの最大入力電圧
V_I	制御入力(IN, $\overline{EN}$)の電圧
I_{IH}, I_{IL}	制御入力(IN, $\overline{EN}$)で測定されるリーク電流
t_{ON}	スイッチのターンオン時間。このパラメータは、規定された条件の範囲で、スイッチがオンになるときのデジタル制御(IN)信号とアナログ出力(NCまたはNO)信号との間の伝搬遅延により測定されます。
t_{OFF}	スイッチのターンオフ時間。このパラメータは、規定された条件の範囲で、スイッチがオフになるときのデジタル制御(IN)信号とアナログ出力(NCまたはNO)信号との間の伝搬遅延により測定されます。
Q_C	電荷注入は、制御(IN)入力からアナログ(NCまたはNO)出力への、望ましくない信号のカップリングの測定値です。この値はクーロン(C)単位で、制御入力のスイッチングによって誘導される合計電荷により測定されます。電荷注入 $Q_C = C_L \times \Delta V_{COM}$ で、 C_L は負荷容量、 ΔV_{COM} はアナログ出力電圧の変化です。
$C_{NC(OFF)}$	対応チャンネル(NCからCOM)がオフのときのNCポートの容量
$C_{NC(ON)}$	対応チャンネル(NCからCOM)がオンのときのNCポートの容量
$C_{NO(OFF)}$	対応チャンネル(NOからCOM)がオフのときのNCポートの容量
$C_{NO(ON)}$	対応チャンネル(NOからCOM)がオンのときのNCポートの容量
$C_{COM(OFF)}$	対応チャンネル(COMからNC)がオフのときのCOMポートの容量
$C_{COM(ON)}$	対応チャンネル(COMからNC)がオンのときのCOMポートの容量
C_I	制御入力(IN, $\overline{EN}$)の容量
O_{ISO}	スイッチのオフ絶縁は、オフ状態のスイッチのインピーダンス測定値です。これは、対応チャンネル(NCからCOM)がオフ状態のとき、特定の周波数についてdB単位で測定されます。
X_{TALK}	クロストークは、オンのチャンネルからオフのチャンネル(NC1からNO1)への、望ましくない信号カップリングの測定値です。隣接クロストークは、オンのチャンネルから隣接するオンのチャンネル(NC1からNC2)への、望ましくない信号カップリングの測定値です。この値は特定の周波数において、dB単位で測定されます。
BW	スイッチの帯域幅。オン状態のチャンネルのゲインがDCゲインより-3dB低くなる周波数です。
THD	全高調波歪は、アナログ・スイッチにより発生する信号の歪みを示します。この値は、2次、3次、およびさらに高次の高調波の二乗平均(RMS)値と、基本波の絶対振幅との比として定義されます。
I_+	制御(IN)ピンが V_+ またはGNDであるときの静的消費電流

12.2 ドキュメントのサポート

12.2.1 関連資料

- 『低速またはフローティングCMOS入力の影響』SCBA004

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.5 商標

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12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3A5017QRGYRQ1	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5017Q
TS3A5017QRGYRQ1.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5017Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS3A5017-Q1 :

- Catalog : [TS3A5017](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5017QRGYRQ1	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5017QRGYRQ1	VQFN	RGY	16	3000	367.0	367.0	35.0

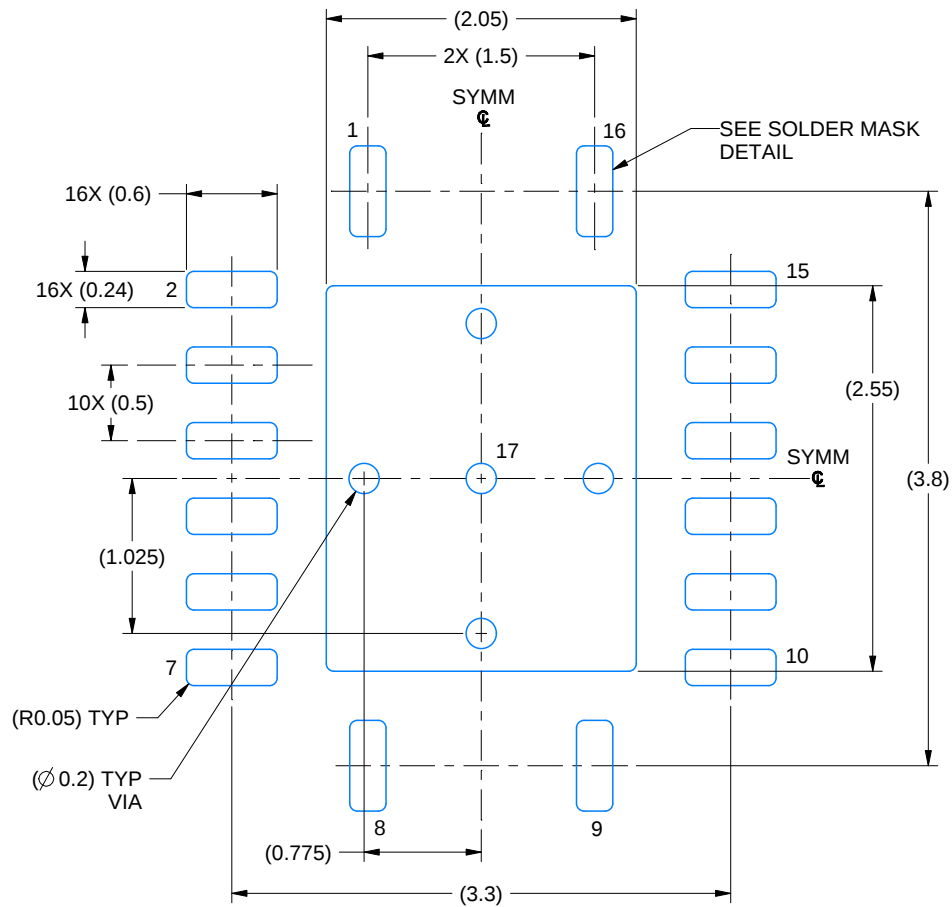
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

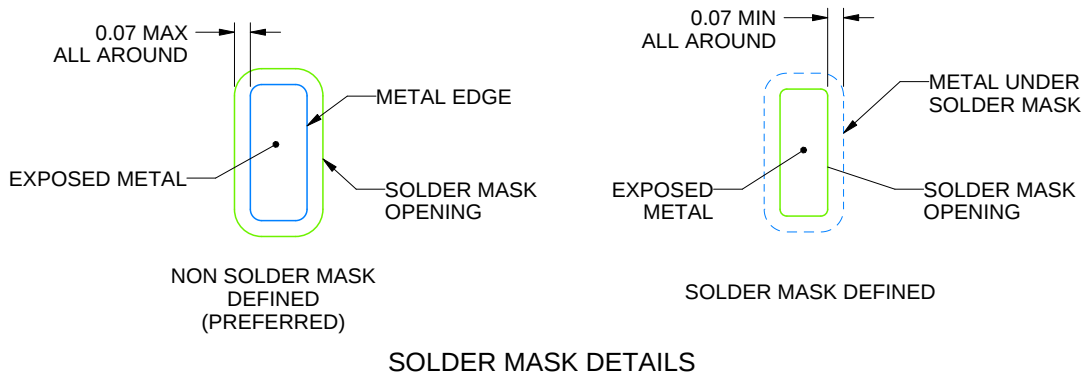
RGY0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4225140/A 07/2019

NOTES: (continued)

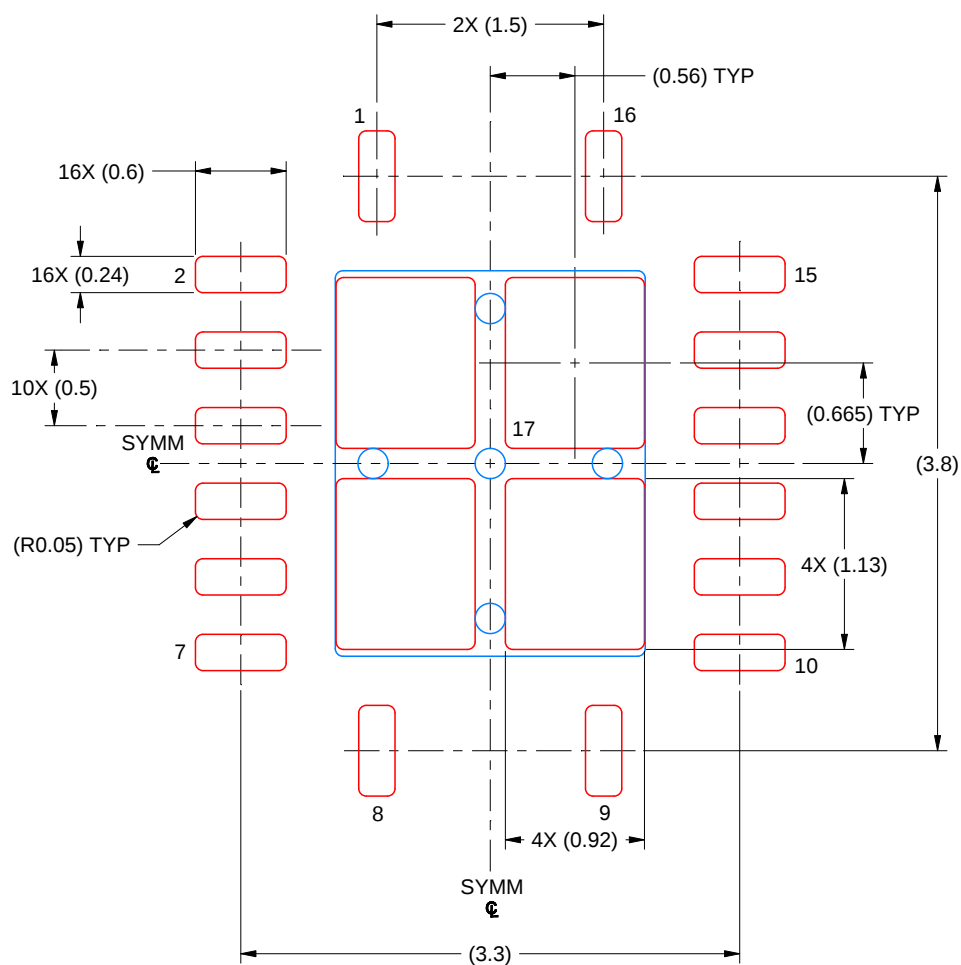
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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