TS3L110 クワッド SPDT 高帯域幅 10/100 Base-T LAN スイッチ 差動 8:4 マルチプレクサ/デマルチプレクサ

1 特長

- 広い帯域幅 (標準値 BW = 500MHz)
- 小さいクロストーク (標準値 X_{TALK} = -30dB)
- 伝播遅延がゼロに近い双方向データ・フロー
- 低くフラットなオン抵抗
  (r_{on} = 4Ω (標準値)、$r_{on(flat)}$ = 1Ω)
- データ I/O ポートでのスイッチング (0～5V)
- 3V～3.6V の範囲の V_{CC} で動作
- I_{off} により部分的パワーダウン・モード動作をサポート
- データおよび制御入力にアンダーシュート・クランプ・ダイオードを内蔵
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- ESD 性能は JESD 22 に準拠しテスト済み
  - 2000V、人体モデル (A114-B、クラス II)
  - 1000V、デバイス帯電モデル (C101)
- 10 Base-T と 100 Base-T の両方の信号処理に最適

2 アプリケーション

- 10 および 100 Base-T 信号のスイッチング

3 概要

TS3L110 ローカル・エリア・ネットワーク (LAN) スイッチは、1 つのスイッチ・イネーブル ($\overline{E}$) 入力を備えた 4 ビット 1:2 マルチプレクサ/デマルチプレクサです。$\overline{E}$ が LOW のとき、スイッチはオンになり、I ポートは Y ポートに接続されます。$\overline{E}$ が HIGH のとき、スイッチはオフになり、I と Y のポート間は高インピーダンス状態になります。セレクト (S) 入力は、マルチプレクサ/デマルチプレクサのデータ・パスを制御します。

TS3L110 デバイスを使用して、LAN アプリケーションの機械式リレーを置き換えることができます。このデバイスはオン抵抗 (r_{on}) が低くかつフラットで、帯域幅が広く、クロストークが小さいため、10/100 Base-T や他の各種 LAN アプリケーションに適しています。TS3L110 デバイスは、10/100 Base-T のイーサネット・トランシーバからの信号を、ラップトップやドッキング・ステーションの RJ-45 LAN コネクタへ転送するために使用できます。このデバイスは、チャネル間のスキューとクロストークが小さくなるよう設計されています。

このデバイスは、I_{off}を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。I_{off}機能により、パワーダウン時に損傷を引き起こすような電流がデバイスに逆流しないことが保証されます。デバイスは、電源オフ時は絶縁されています。

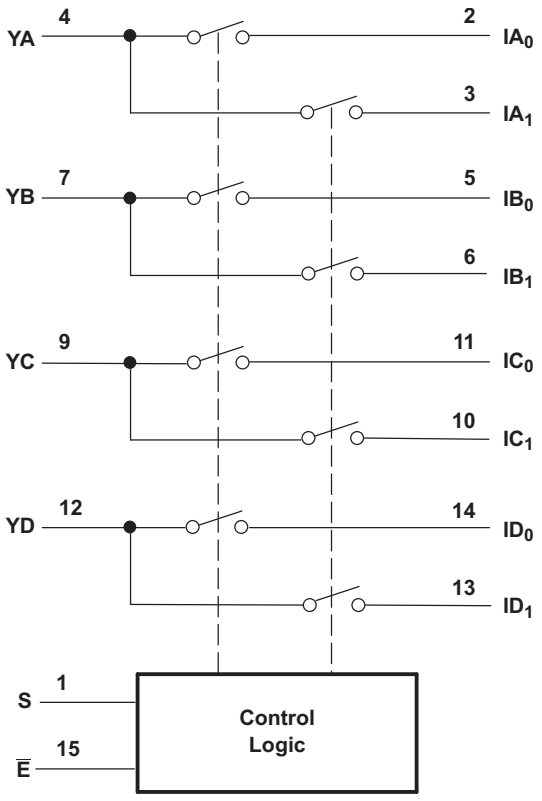
電源オンまたは電源オフ時に確実に高インピーダンス状態になるように、$\overline{E}$ はプルアップ抵抗経由で V_{CC} に接続します。この抵抗の最小値は、ドライバの電流シンク能力によって決定されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TS3L110	SOIC (D) 16	9.90mm×3.91mm
	SSOP (DBQ) 16	4.90mm × 3.90mm
	TVSOP (DGV) 16	3.60mm × 4.40mm
	TSSOP (PW) 16	5.00mm×4.40mm
	VQFN (RGV) 16	4.00mm×4.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ロジック図(正論理)



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (May 2019) から **Revision B** に変更 **Page**

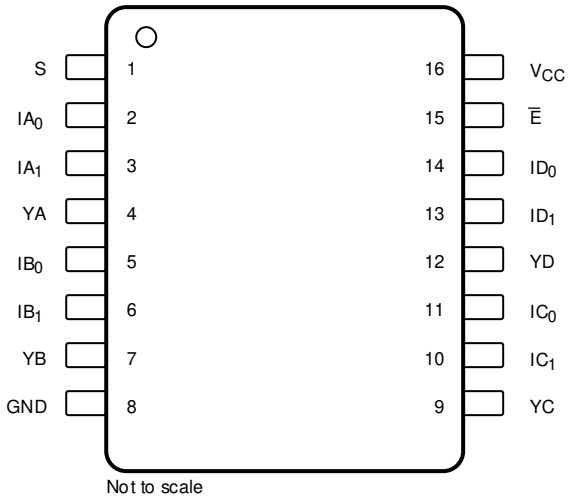
- Change pin 10 to IC_1, pin 11 to IC_0, pin 13 to ID_1, and pin 14 to ID_0 in the *Pin Configuration and Functions* ... 3

2004年**9**月発行のものから更新 **Page**

- 「*製品情報*」表、「*ESD 定格*」表、「*熱に関する情報*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

5 Pin Configuration and Functions

D, DBQ, DGV, or PW Package
SOIC, SSOP, TVSOP, TSSOP 16 Pins
Top View



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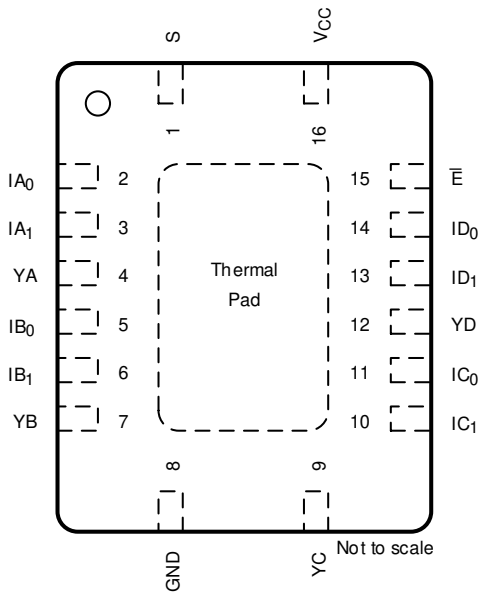
RGY Package
VQFN 16 Pins
Top View



Not to scale

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
S	1	Select input
IA_0	2	Data I/Os
IA_1	3	Data I/Os
YA	4	Data I/Os
IB_0	5	Data I/Os
IB_1	6	Data I/Os
YB	7	Data I/Os
GND	8	Ground (0 V) reference
YC	9	Data I/Os
IC_1	10	Data I/Os
IC_0	11	Data I/Os
YD	12	Data I/Os
ID_1	13	Data I/Os
ID_0	14	Data I/Os
$\overline{E}$	15	Enable input
V_{CC}	16	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±128	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance	D package(6)		73	°C/W
		DBQ package(6)		90	
		DGV package(6)		120	
		PW package(6)		108	
		RGY package(7)		39	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.
(7) The package thermal impedance is calculated in accordance with JESD 51-5.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. e.

6.3 Recommended Operating Conditions(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage ($\overline{E}$, S)	2	5.5	V
V_{IL}	Low-level control input voltage ($\overline{E}$, S)	0	0.8	V
$V_{I/O}$	Input/output voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		TS3L110					UNIT
		D (SOIC)	DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGV (VQFN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.0	114.5	139.3	111.5	50.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	60.5	57.4	42.0	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.3	58.2	73.7	57.8	26.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.3	15.3	7.2	4.2	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.0	57.6	73.0	57.2	26.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	-	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics[1]

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}	$\overline{E}$, S	V_{CC} = 3.6 V,	I_{IN} = –18 mA				–1.8	V
I_{IH}	$\overline{E}$, S	V_{CC} = 3.6 V,	V_{IN} = 5.5 V				±1	µA
I_{IL}	$\overline{E}$, S	V_{CC} = 3.6 V,	V_{IN} = GND				±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0,	Switch ON or OFF		0.7	1.5	mA
C_{in}	$\overline{E}$, S	f = 1 MHz,	V_{IN} = 0			2.5	3.5	pF
$C_{io(OFF)}$	I port	V_I = 0,	f = 1 MHz, Outputs open,	Switch OFF		3.5	5	pF
	Y port	V_I = 0,	f = 1 MHz, Outputs open,	Switch OFF		5.5	7	
$C_{io(ON)}$	I or Y port	V_I = 0,	f = 1 MHz, Outputs open,	Switch ON		10.5	13	pF
r_{on}		V_{CC} = 3 V,	1.25 V ≤ V_I ≤ V_{CC},	I_O = –10 mA to –30 mA		4	8	Ω
$r_{on(flat)}$[3]		V_{CC} = 3 V,	V_I = 1.25 V and V_{CC},	I_O = –10 mA to –30 mA		1		Ω
Δr_{on}[4]		V_{CC} = 3 V,	1.25 V ≤ V_I ≤ V_{CC},	I_O = –10 mA to –30 mA		0.9	2	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{on(flat)}$ is the difference of r_{on} in a given channel at specified voltages.
(4) Δr_{on} is the difference of r_{on} in a given device.

6.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figure 5 and Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	I or Y	Y or I		0.25		ns
t_{PZH}, t_{PZL}	$\overline{E}$ or S	I or Y	0.5		7	ns
t_{PHZ}, t_{PLZ}	$\overline{E}$ or S	I or Y	0.5		5	ns
$t_{sk(p)}$(3)	I or Y	Y or I		0.1	0.2	ns

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Skew between opposite transitions of the same output $|t_{PHL} – t_{PLH}|$. This parameter is not production tested.

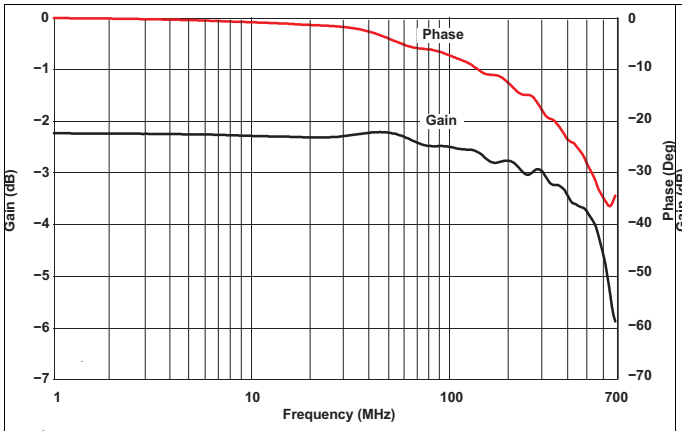
6.7 Dynamic Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP(1)	UNIT
X_{TALK}	R_L = 100 Ω,	f = 250 MHz,	See Figure 7	–26	dB
O_{IRR}	R_L = 100 Ω,	f = 250 MHz,	See Figure 8	–28	dB
BW	R_L = 100 Ω,		See Figure 6	500	MHz

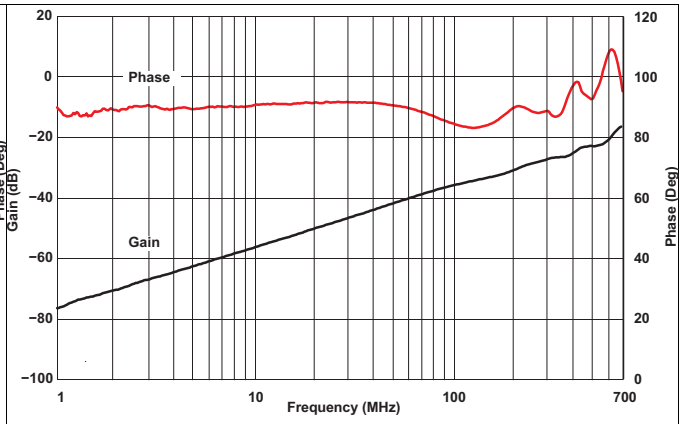
(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

6.8 Typical Characteristics



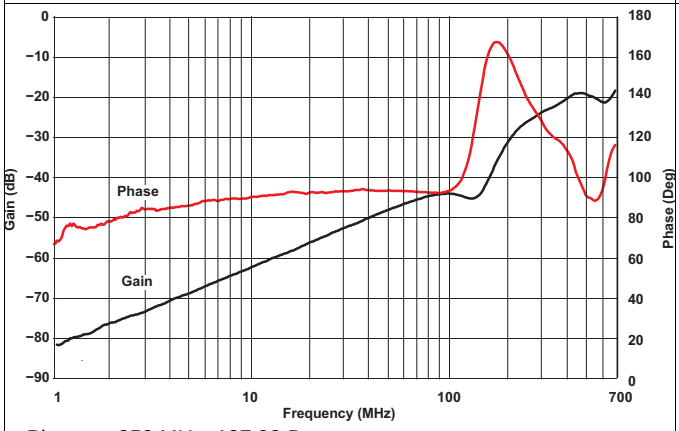
Phase at 627 MHz, −36 Deg
Gain −3 dB at 627 MHz

Figure 1. Gain and Phase vs Frequency



Phase at 250 MHz, 88.2 Deg
Gain −28.5 dB at 250 MHz

Figure 2. OFF Isolation vs Frequency



Phase at 250 MHz, 137.92 Deg
Gain −26 dB at 250 MHZ

Figure 3. Crosstalk vs Frequency

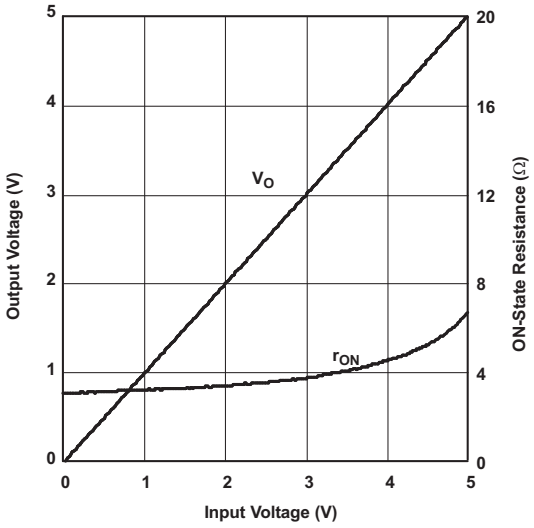
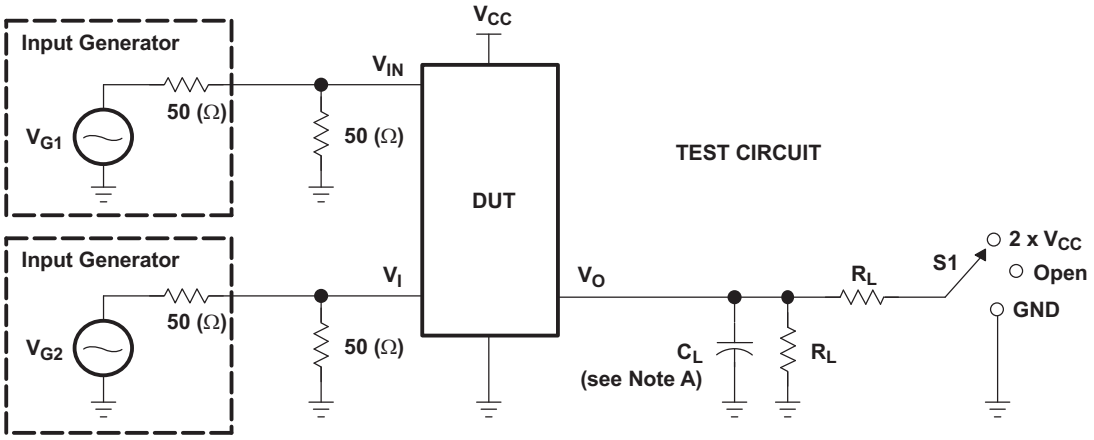
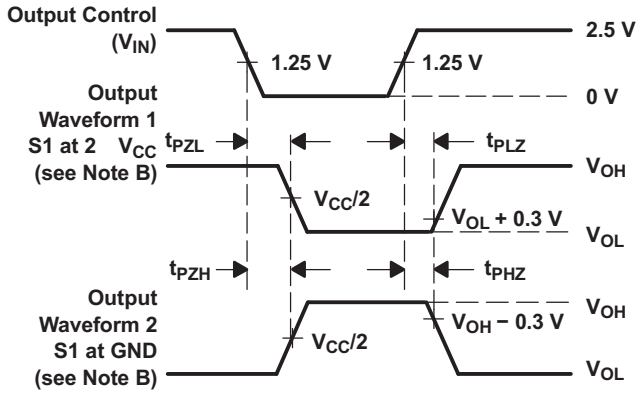


Figure 4. Output Voltage and ON-State Resistance vs Input Voltage

7 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 x V_{CC}	200 (Ω)	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	200 (Ω)	V_{CC}	10 pF	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

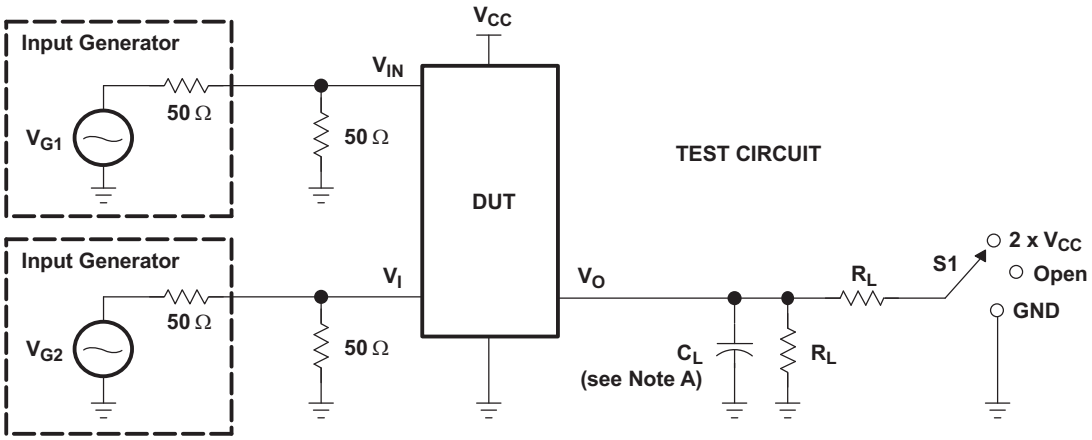
D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

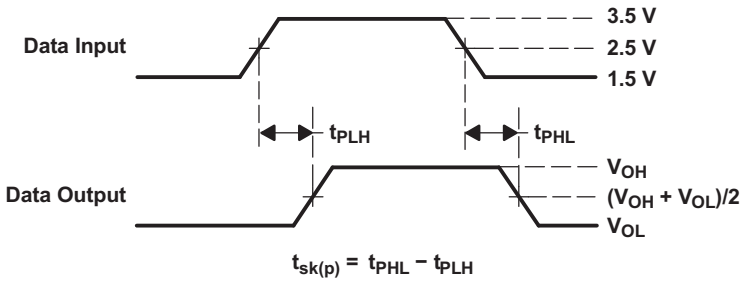
F. t_{PLZ} and t_{PHH} are the same as t_{en}.

Figure 5. Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



TEST	V_{CC}	S1	R_L	V_{IN} (see Note B)	C_L
$t_{sk(p)}$	3.3 V ± 0.3 V	GND	200 Ω	V_{CC} or GND	10 pF



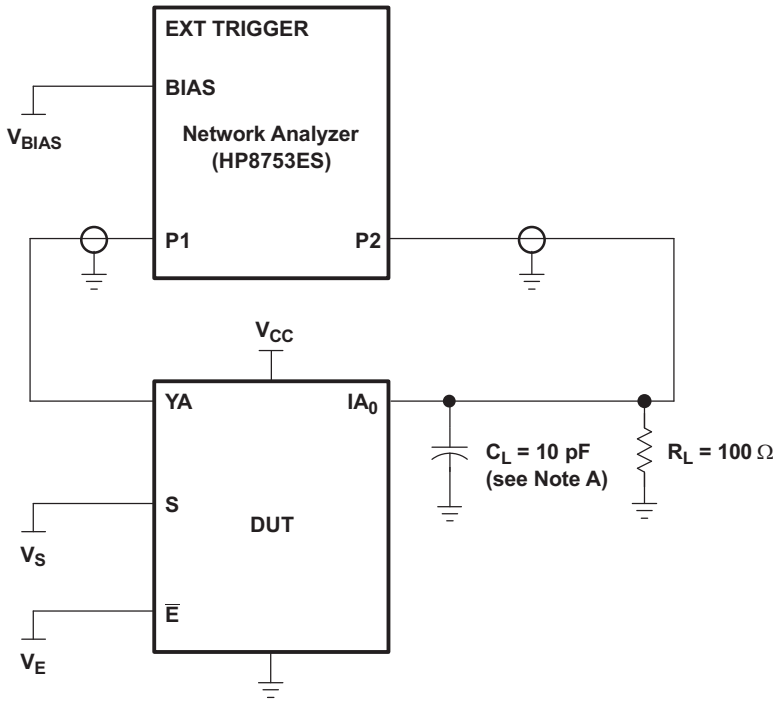
VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

A. C_L includes probe and jig capacitance.

B. Switch is ON during the measurement of $t_{sk(p)}$, that is, voltage at E = 0 and S = V_{CC} or GND.

Figure 6. Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

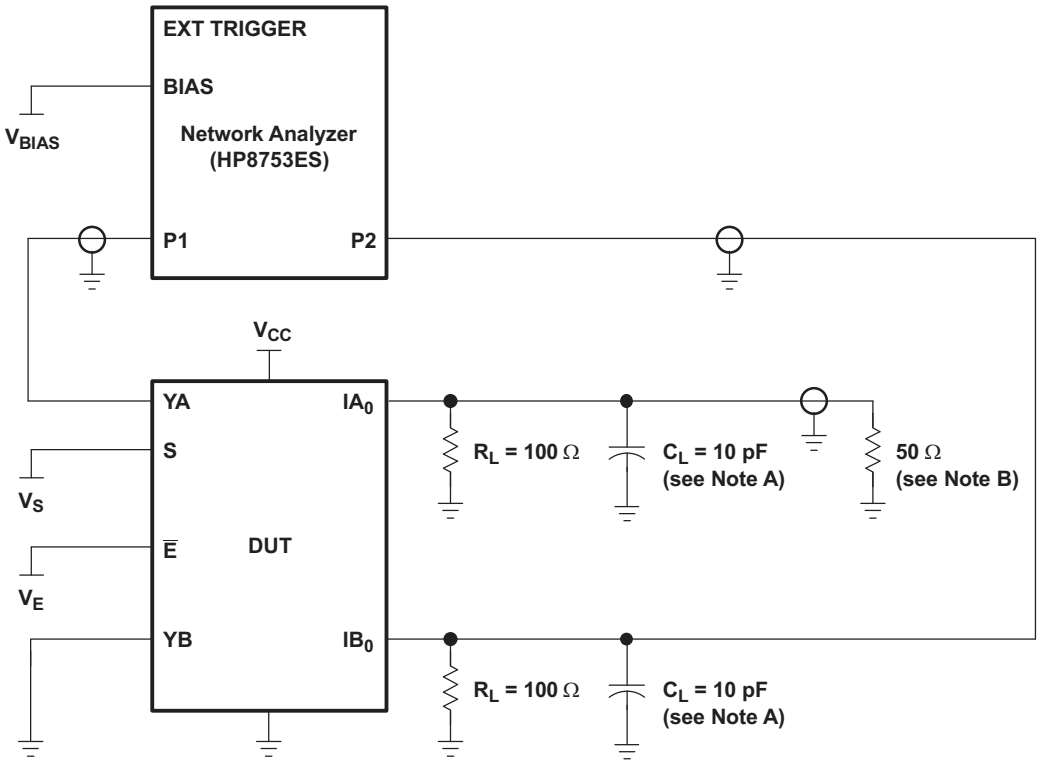
Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_S = 0, V_E = 0, and YA is the input, the output is measured at IA_0. All unused analog I/O ports are left open.

HP8753ES Setup

- Average = 4
- RBW = 3 kHz
- V_{BIAS} = 0.35 V
- ST = 2 s
- P1 = 0 dBM

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer

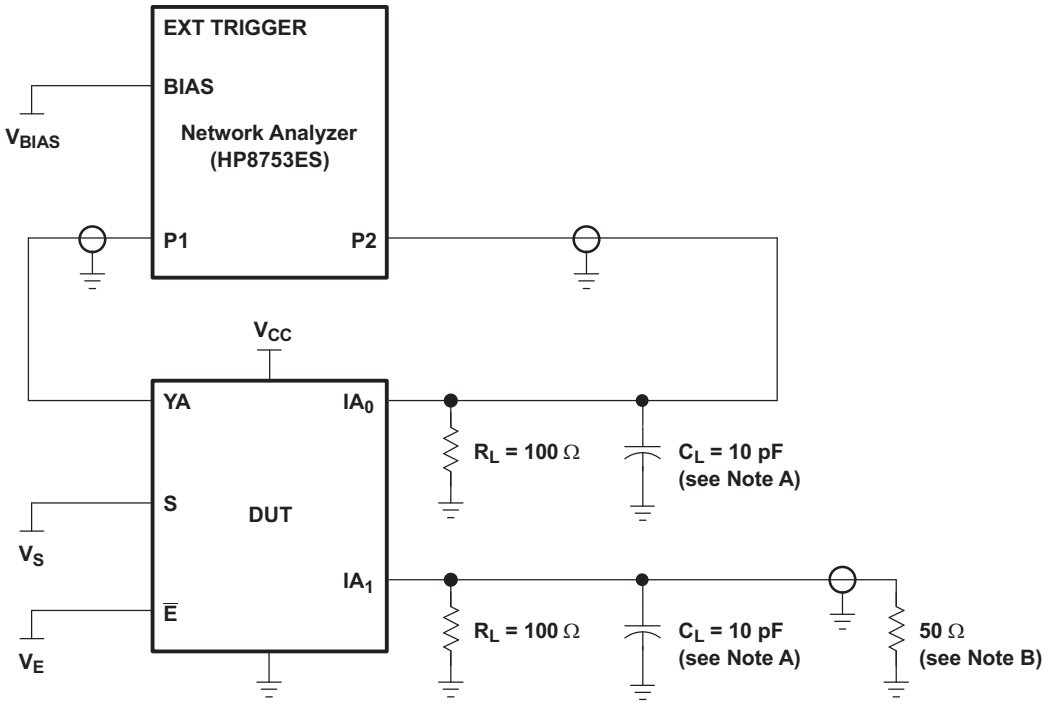
Figure 8. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_S = 0, V_E = 0, and YA is the input, the output is measured at IB_0. All unused analog input (Y) ports are connected to GND, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

- Average = 4
- RBW = 3 kHz
- V_{BIAS} = 0.35 V
- ST = 2 s
- P1 = 0 dBM

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer

Figure 9. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when $V_S = V_{CC}$, $V_E = 0$, and YA is the input, the output is measured at IA_0. All unused analog input (Y) ports are left open, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

HP8753FS Setup

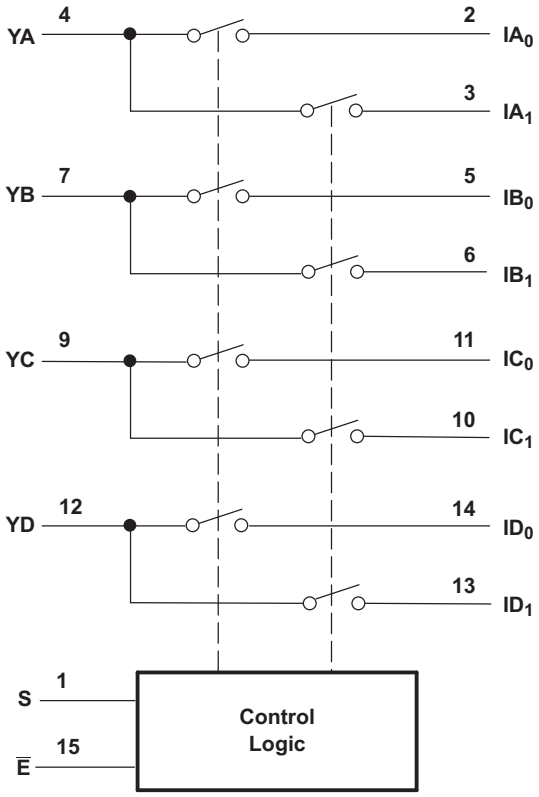
- Average = 4
- RBW = 3 kHz
- V_{BIAS} = 0.35 V
- ST = 2 s
- P1 = 0 dBM

8 Detailed Description

8.1 Overview

The TI TS3L110 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable (E) input. When E is low, the switch is enabled, and the I port is connected to the Y port. When E is high, the switch is disabled, and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

8.2 Functional Block Diagram



8.3 Feature Description

I_{off} supports Partial-Power-Down Mode Operation.

The TS3L110 device ensures the signal path is high impedance state when V_{CC} = 0 V.

8.4 Device Functional Modes

The TS3L110 supports a power down mode which reduces the current consumption of the device and places all the signal paths in a high impedance state. To place the TS3L100 in power down mode, set the $\overline{E}$ pin with a logic high voltage as seen in Table 1.

Table 1. Function Table

INPUTS		INPUT/OUTPUT YX	FUNCTION
$\overline{E}$	S		
L	L	IX_0	$YX = IX_0$
L	H	IX_1	$YX = IX_1$
H	X	Z	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many Local Area Network (LAN) applications in which the ethernet hubs or controllers have a limited number of I/Os or need to route signals from a single ethernet PHY to multiple ethernet jacks. The TS3L110 solution can effectively expand the limited I/Os by switching between multiple Ethernet jacks to interface them to a single Ethernet PHY.

9.2 Typical Application

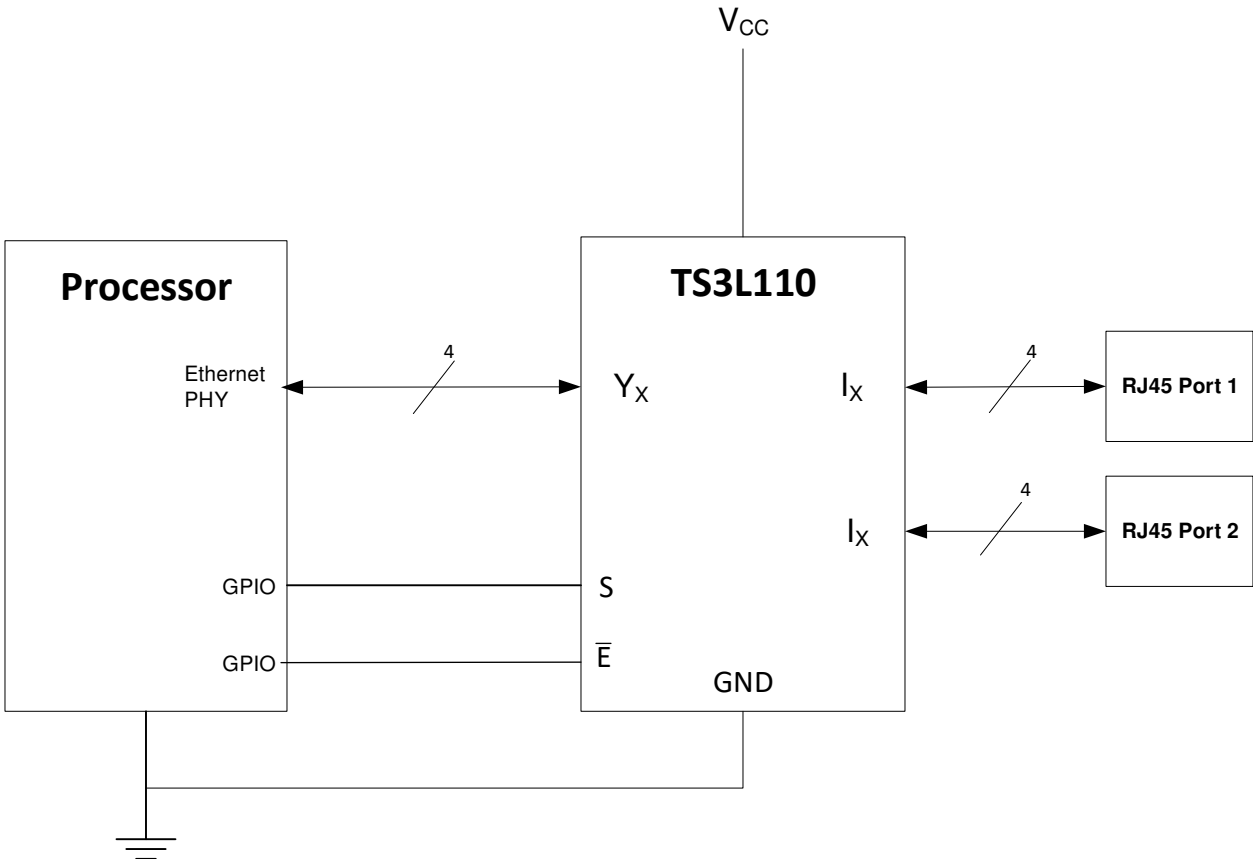


Figure 10. Typical Application Schematic

9.2.1 Design Requirements

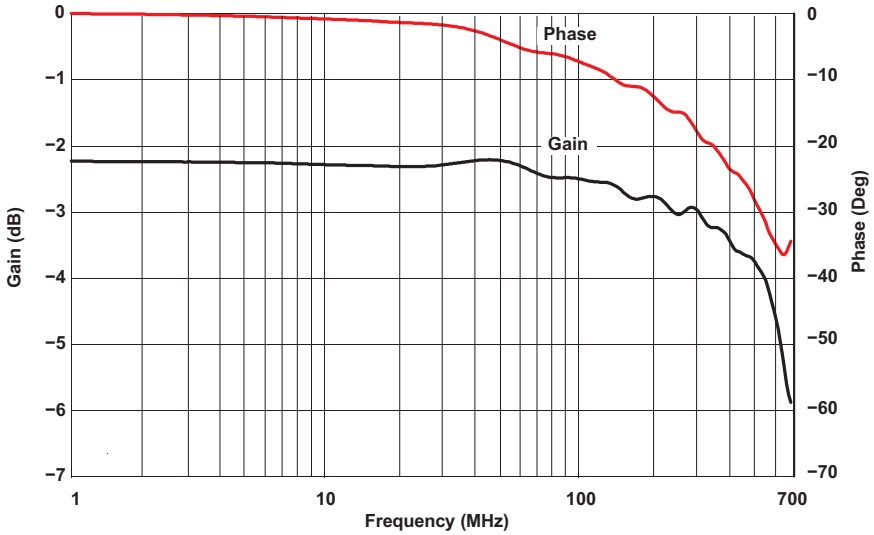
Ensure that all of the signals passing through the switch are within the recommended operating ranges. To ensure proper performance, see Recommended Operating Conditions.

9.2.2 Detailed Design Procedure

The TS3L110 can be properly operated without any external components. TI recommends that the digital control pins S and $\overline{E}$ be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin. Connect the exposed thermal pad to ground.

Typical Application (continued)

9.2.3 Application Curves



Phase at 627 MHz, −36 Deg

Gain −3 dB at 627 MHz

Figure 11. Gain and Phase vs Frequency

10 Power Supply Recommendations

Power to the device is supplied through the VCC pins. TI recommends placing a bypass capacitor as close to the supply pin (VCC) as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

- TI recommends keeping the high-speed signals as short as possible.
- Each via introduces discontinuities in the transmission line of the signal and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
- Avoid stubs on the high-speed signals because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.
- Route all high-speed signal traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.
- Due to high-frequency signals, a printed-circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 12.
- The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

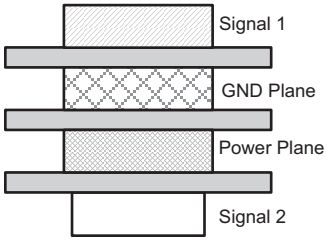


Figure 12. Four-Layer Board Stackup

11.2 Layout Example

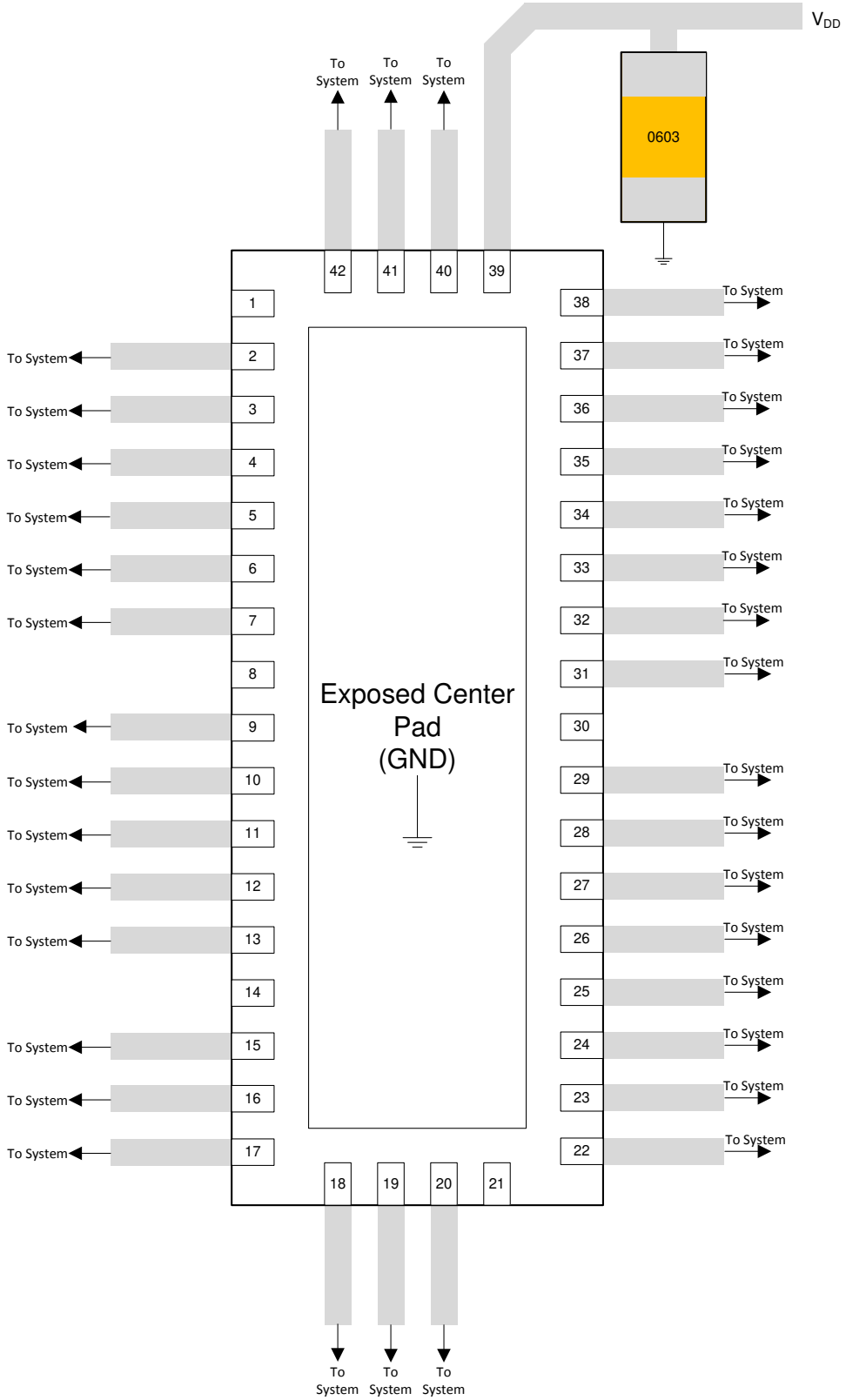


Figure 13. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 商標

E2E is a trademark of Texas Instruments.
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12.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TS3L110D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110
TS3L110D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110
TS3L110DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110
TS3L110DBQR.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110
TS3L110DBQRG4	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110
TS3L110DBQRG4.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110
TS3L110DE4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110
TS3L110DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110
TS3L110DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110
TS3L110DGVR.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110
TS3L110DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110
TS3L110DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TS3L110
TS3L110PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	TK110
TS3L110PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110
TS3L110PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TK110
TS3L110RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110
TS3L110RGYR.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110
TS3L110RGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110
TS3L110RGYRG4.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TK110

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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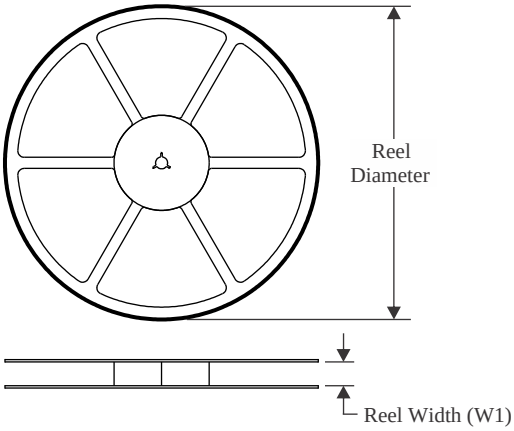
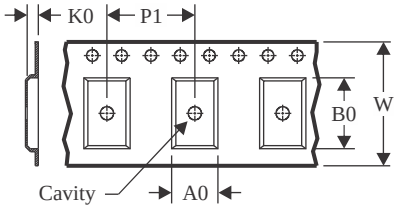
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

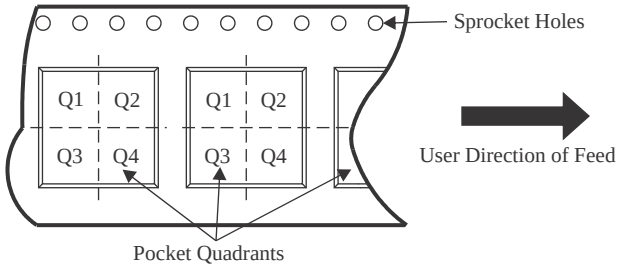


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

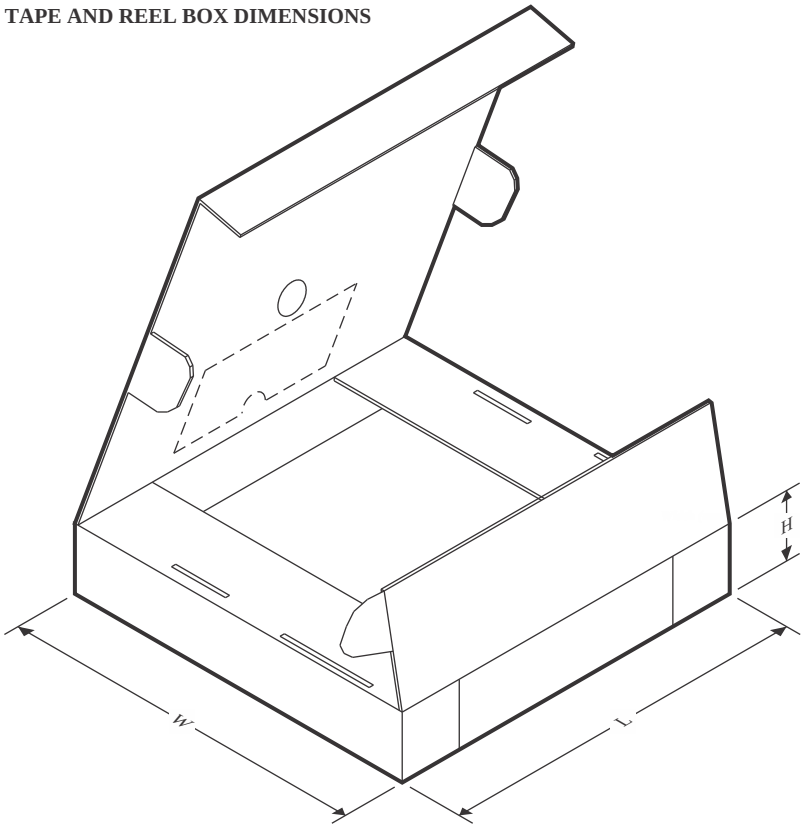
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3L110DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS3L110DBQRG4	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS3L110DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
TS3L110DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS3L110PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TS3L110RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
TS3L110RGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

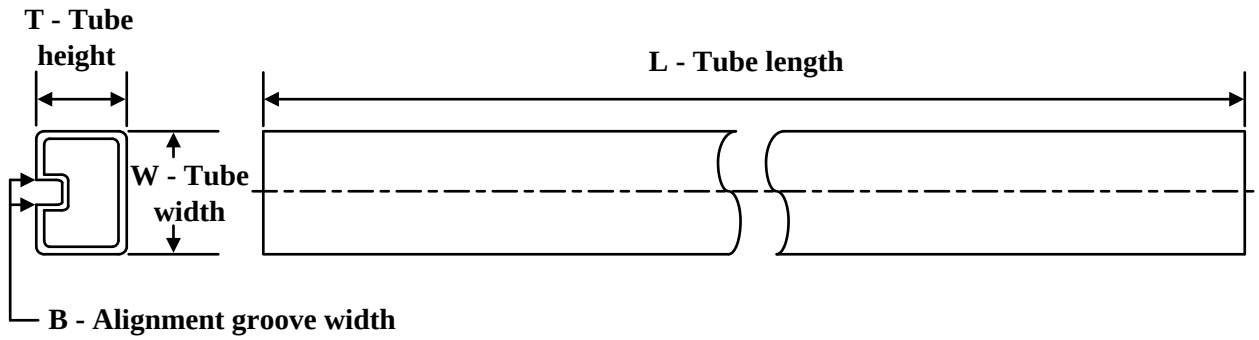
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3L110DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
TS3L110DBQRG4	SSOP	DBQ	16	2500	353.0	353.0	32.0
TS3L110DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
TS3L110DR	SOIC	D	16	2500	340.5	336.1	32.0
TS3L110PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TS3L110RGYR	VQFN	RGY	16	3000	353.0	353.0	32.0
TS3L110RGYRG4	VQFN	RGY	16	3000	353.0	353.0	32.0

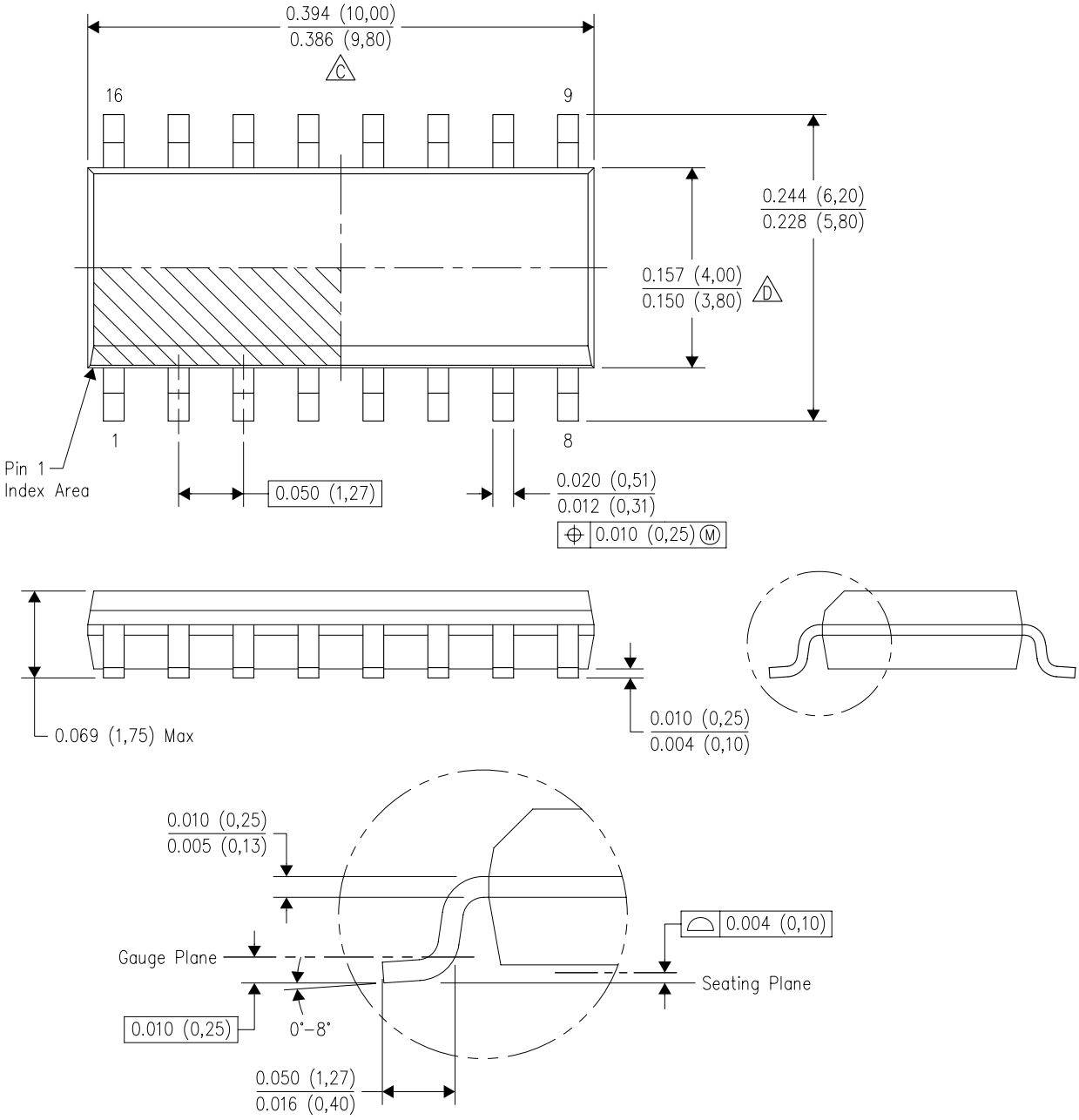
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TS3L110D	D	SOIC	16	40	507	8	3940	4.32
TS3L110D.B	D	SOIC	16	40	507	8	3940	4.32
TS3L110DE4	D	SOIC	16	40	507	8	3940	4.32
TS3L110DG4	D	SOIC	16	40	507	8	3940	4.32

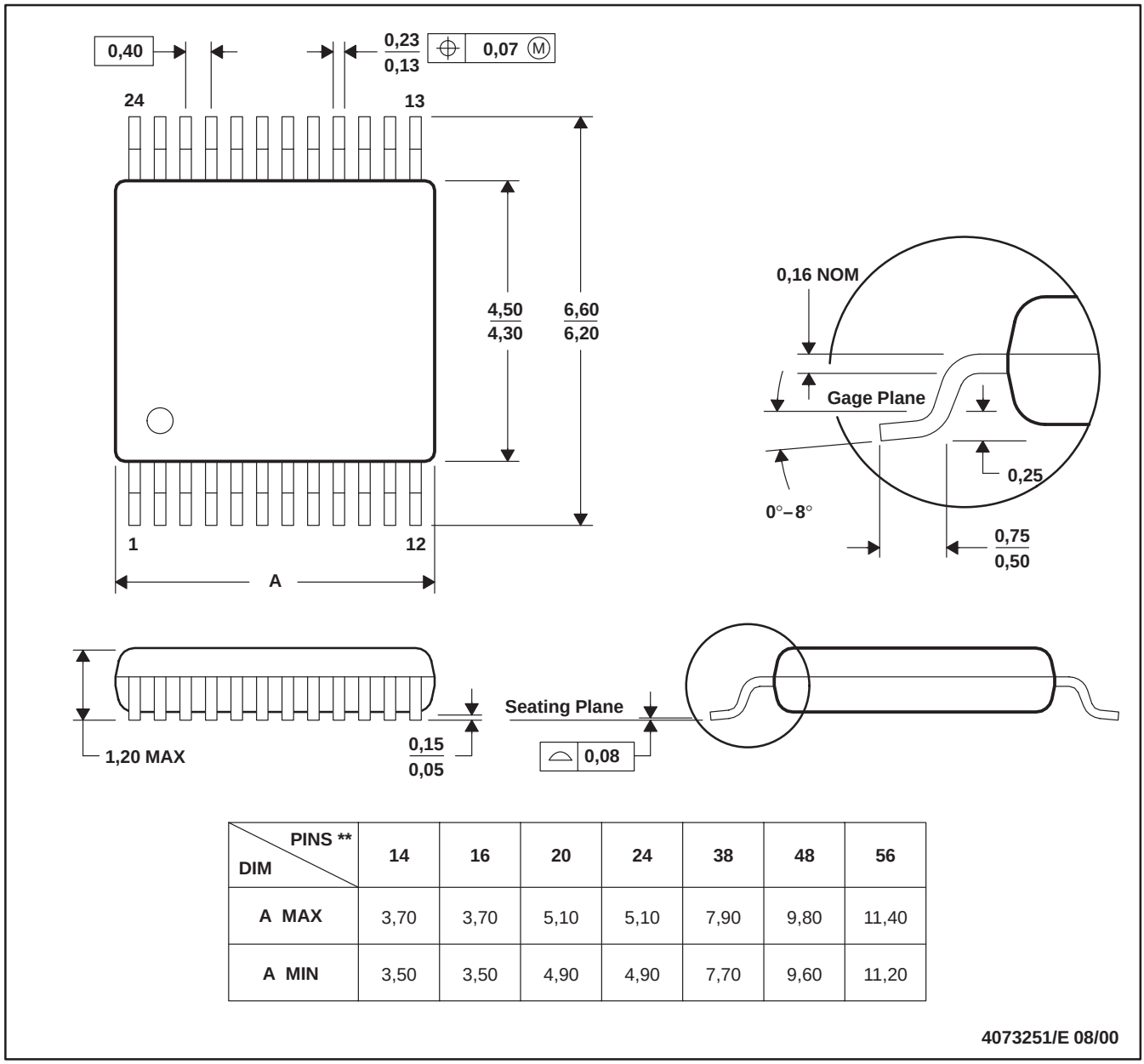
D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

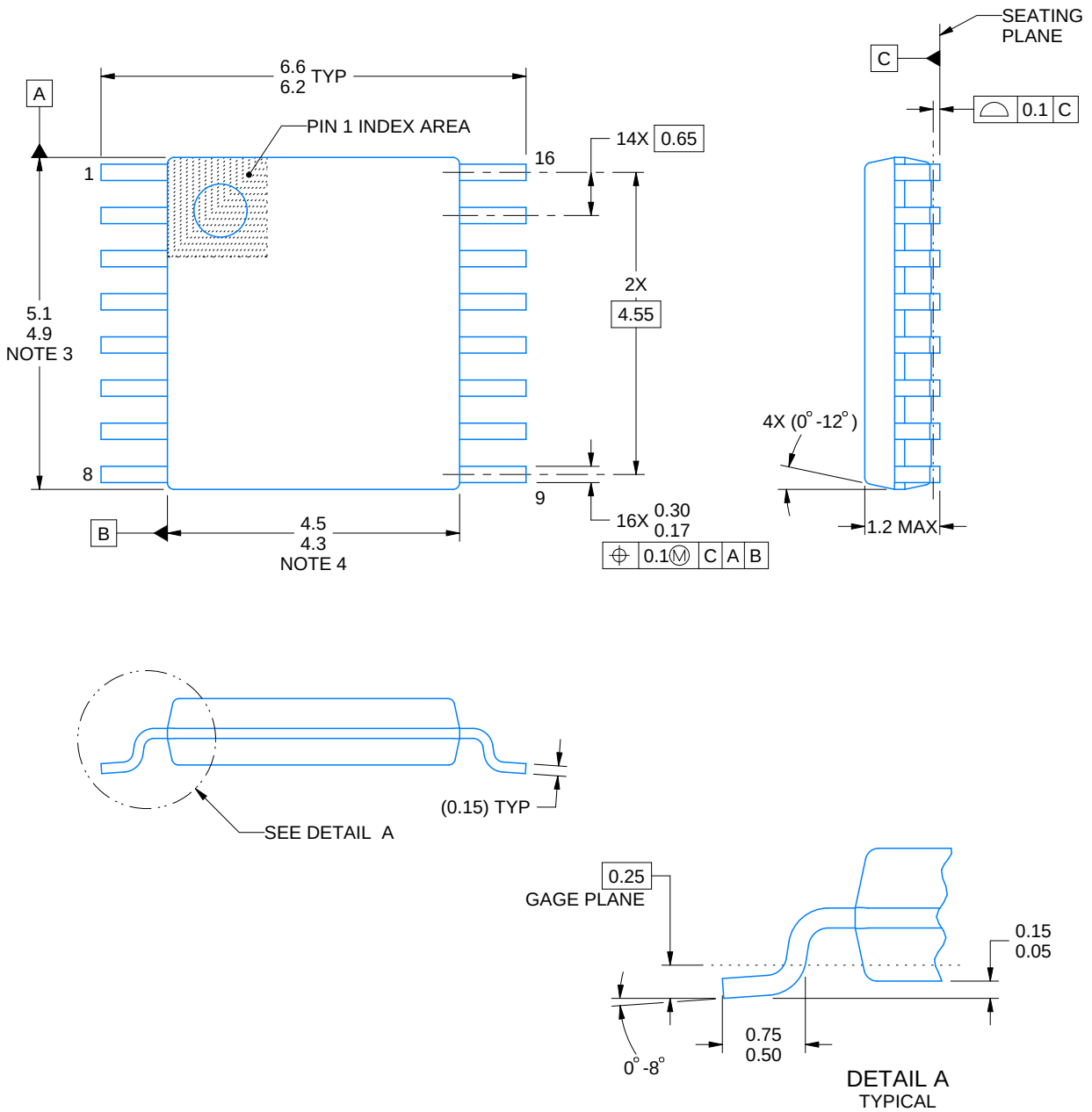
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

PW0016A

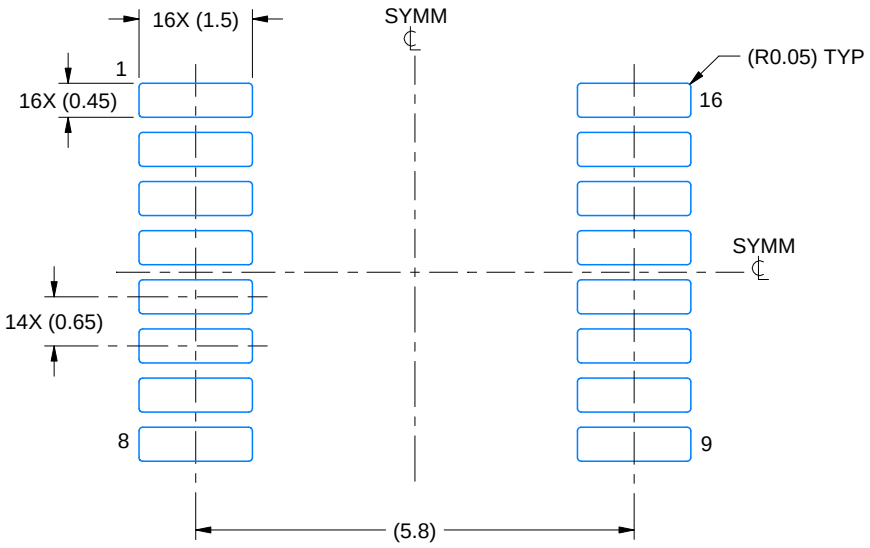
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



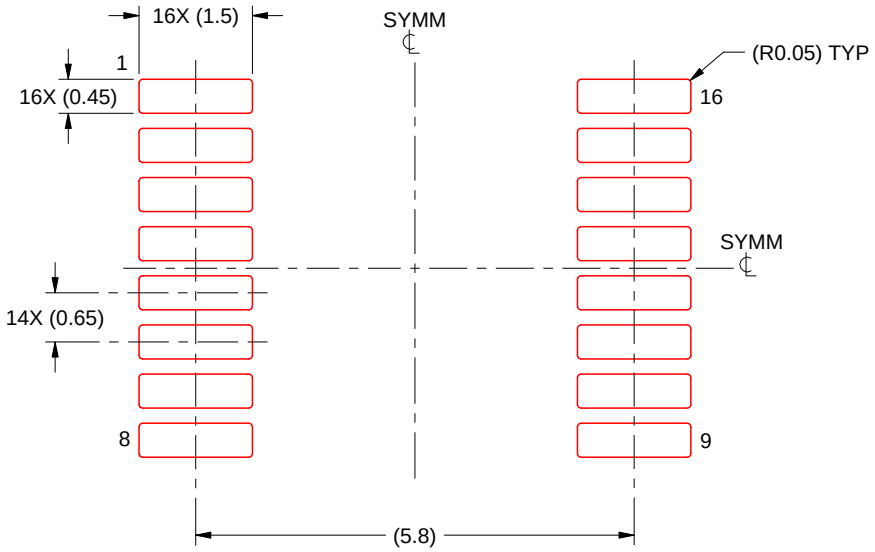
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

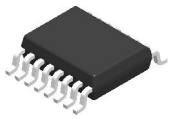


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

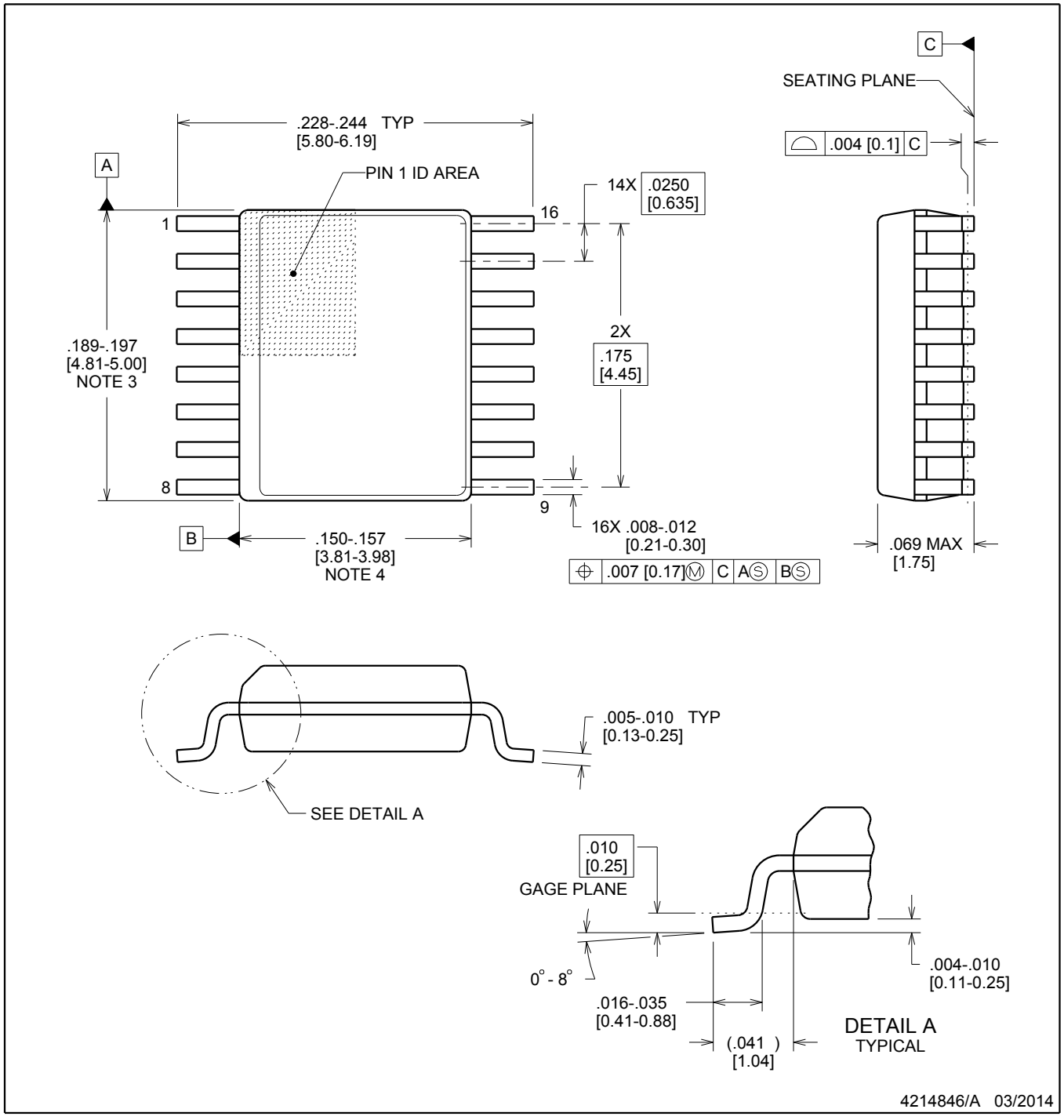


PACKAGE OUTLINE

DBQ0016A

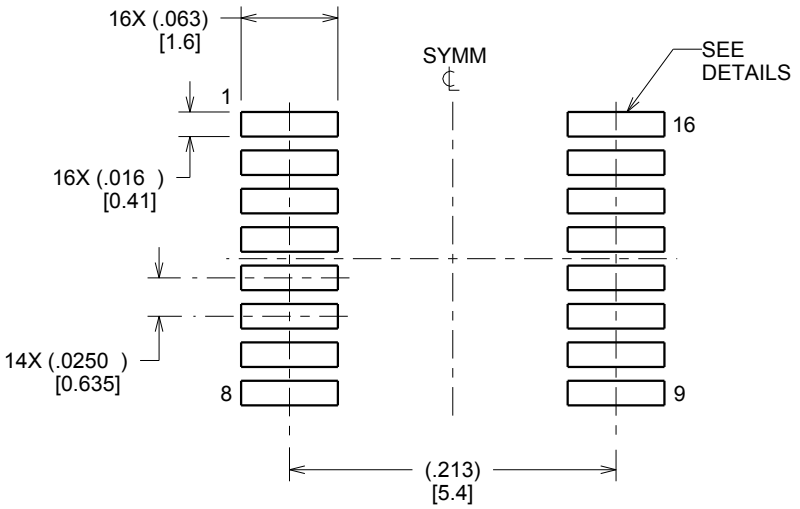
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

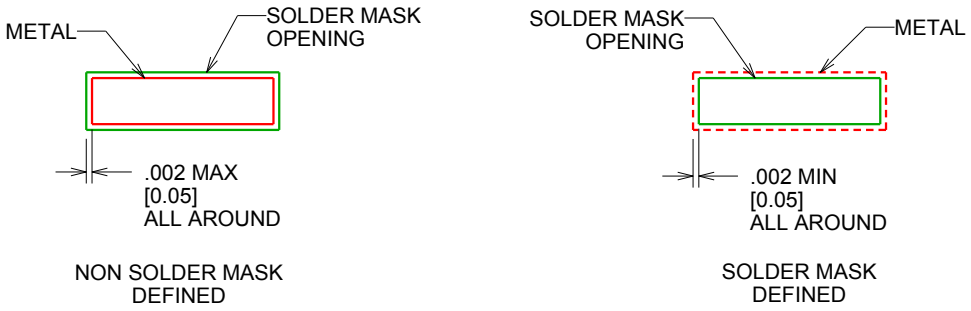


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

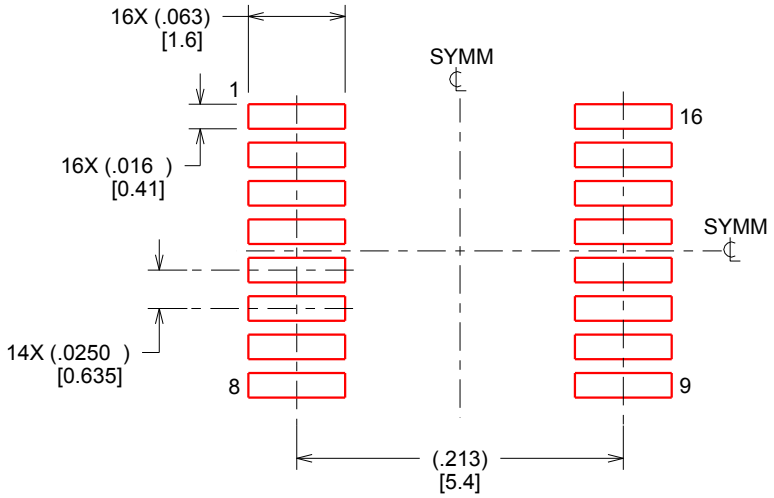
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



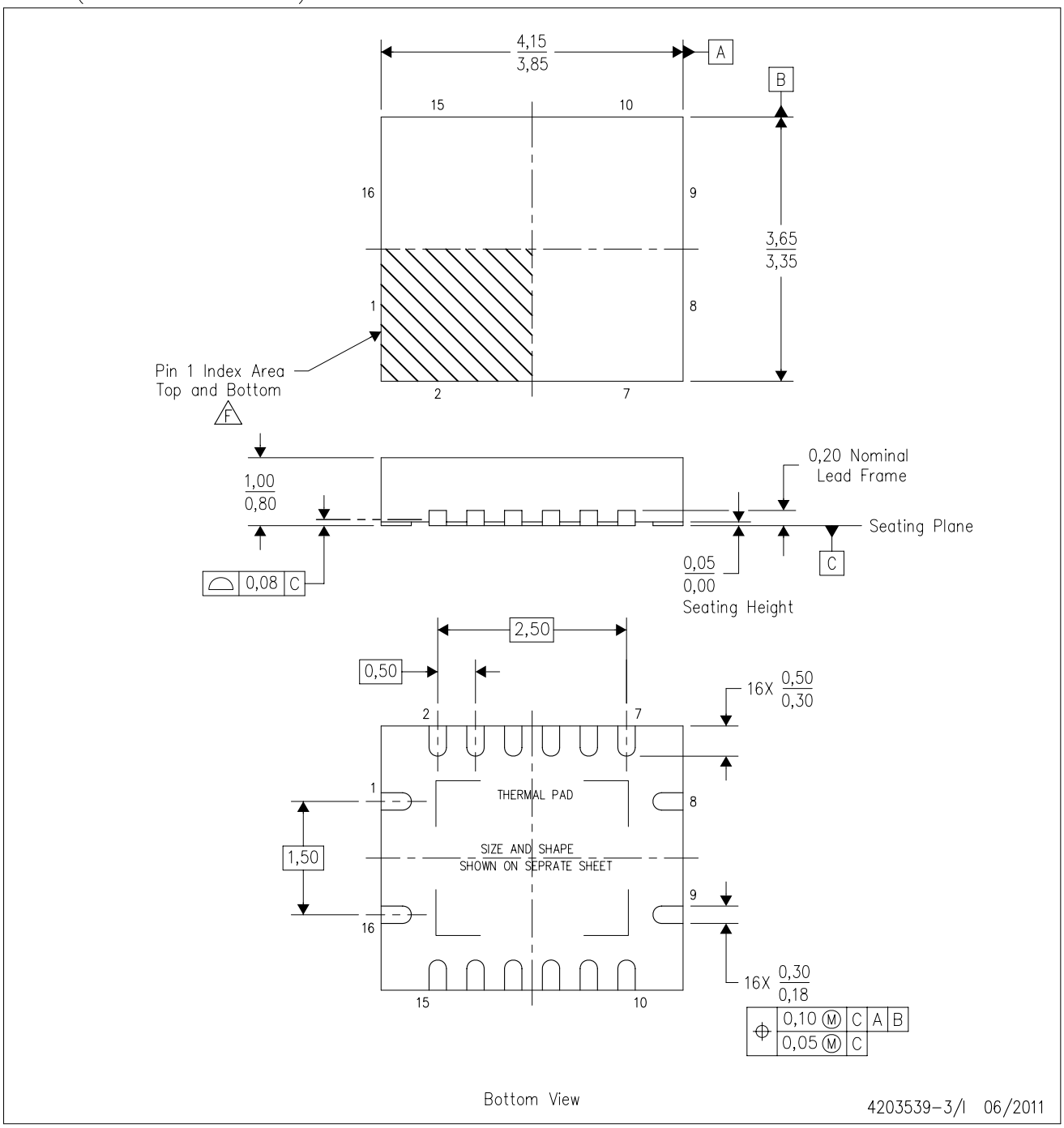
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

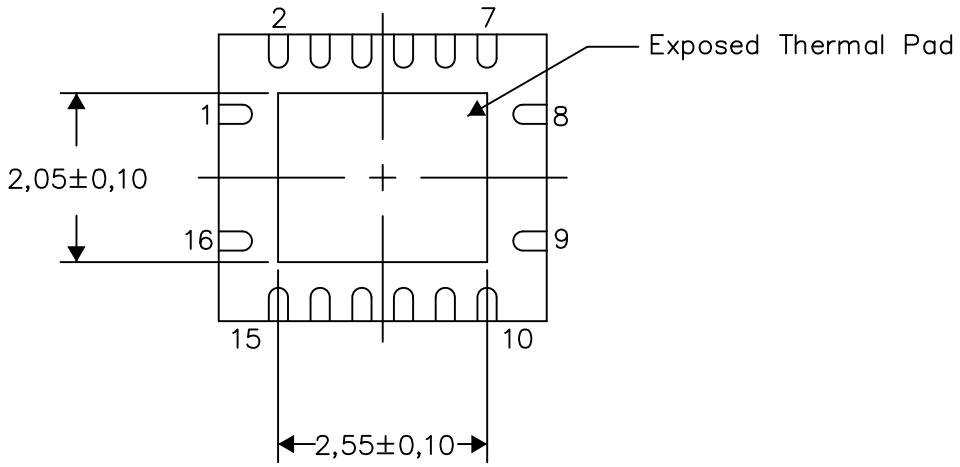
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



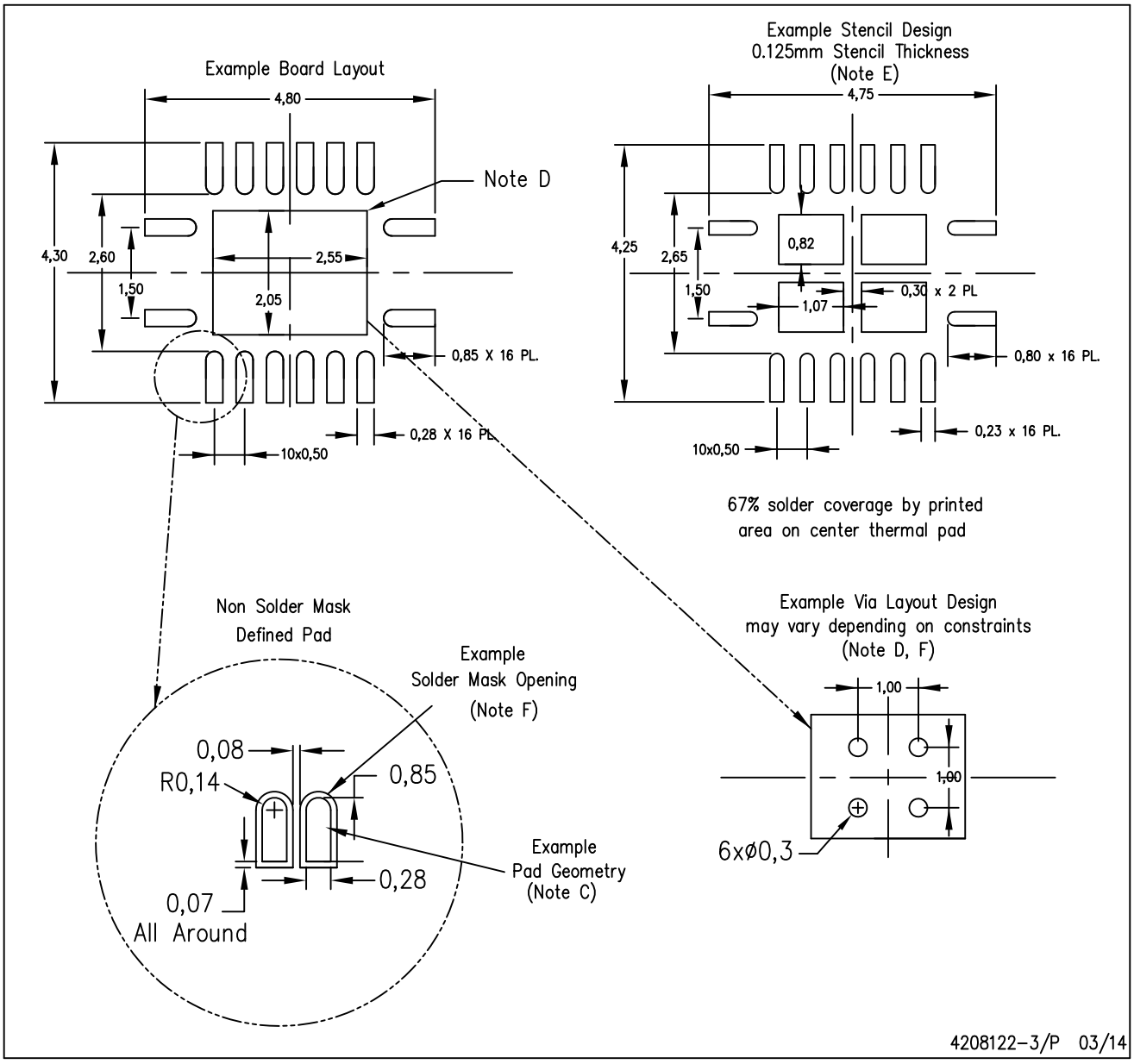
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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最終更新日：2025 年 10 月