# TUSB217A-Q1 USB 2.0 High-Speed シグナル・コンディショナ、DCP および CDP コントローラ付き

## 1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - デバイス温度グレード 2:
    -40℃～105℃、$T_A$
- 広い電源電圧範囲:2.3～6.5V
- USB 切断時およびシャットダウン時の非常に低い消費電力
- USB 2.0 High Speed 信号のコンディショニング
- USB 2.0、OTG 2.0、BC 1.2 に対応
- Low-Speed、Full-Speed、High-Speed 信号処理のサポート
- BC 1.2 充電ダウンストリーム・ポート (CDP) および専用充電ポート (DCP) コントローラを内蔵、DCP/CDP ピンにより動的に変更可能
- 特定のホストやデバイスに非依存
- 最大 5m のケーブルをサポート
  - 外付けのプルダウン抵抗により 4 つの信号ブースト (エッジ・ブーストと DC ブースト) 設定を選択可能
  - プルアップまたはプルダウンで選択可能な 3 つの RX イコライズ設定により、損失が大きいアプリケーションの ISI ジッタを補償
- 2 つの TUSB217A-Q1 デバイスを使って最大 10m のケーブル長に対応
- スケーラブルなソリューション - 損失が大きいアプリケーションに対応するため、デバイスをデイジー・チェーン接続可能
- RWB は TUSB211/212/214/216 とピン互換

## 2 アプリケーション

- 車載用インフォテインメントおよびクラスタ
- 車載用ヘッド・ユニット
- アクティブ・ケーブル、延長ケーブル、バックプレーン

## 3 概要

TUSB217A-Q1 は第 3 世代 USB 2.0 High Speed 信号コンディショナーで、伝送チャネルでの AC 損失 (容量性負荷による) および DC 損失 (抵抗損失による) を補償するように設計されています。

TUSB217A-Q1 には、エッジ・ブースタにより USB 2.0 High Speed 信号の遷移エッジを高速化し、DC ブースト機能により静的電圧レベルを上げる特許取得済みの設計が採用されています。また、TUSB217A-Q1 はプリイコライゼーション機能を備えているため、レシーバ感度を高め、長いケーブルを使用するアプリケーションで ISI (符号間干渉) ジッタを補償できます。USB Low Speed および Full Speed 信号特性は、TUSB217A-Q1 による影響を受けません。

TUSB217A-Q1 は、パケット・タイミングを変更せず、また、伝搬遅延やレイテンシを追加せずに、信号品質を向上させることができます。

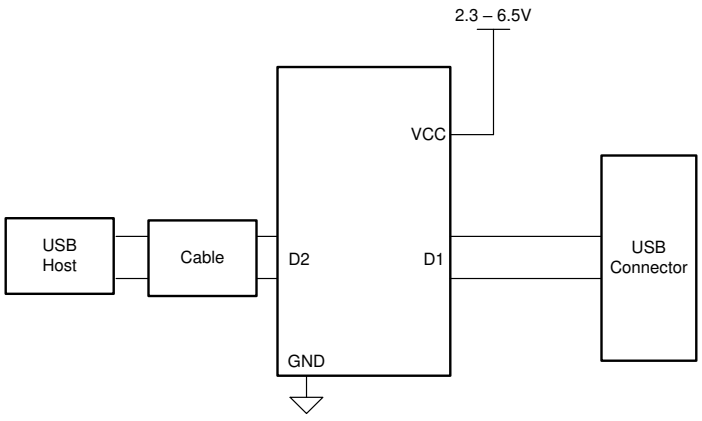
TUSB217A-Q1 により、最長 5 メートルのケーブルを使用したシステムで、USB 2.0 High Speed 近端アイ・コンプライアンスに合格することが可能になります。

TUSB217A-Q1 は USB On-The-Go (OTG) および Battery Charging (BC 1.2) プロトコルにも対応しています。内蔵の BC 1.2 バッテリ充電コントローラは、制御ピンを使って有効化できます。

**デバイス情報** (1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| TUSB217A-Q1 | X2QFN (12RWB) | 1.60mm x 1.60mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**簡略回路図**

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## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| September 2021 | * | Initial Release |

## 5 Device Comparison

| | TUSB211 | TUSB212 | TUSB214 | TUSB216I | TUSB217A |
|---|---|---|---|---|---|
| Supply (V) | 3.3 | 3.3 | 3.3 | 2.3 to 6.5 | 2.3 to 6.5 |
| DC Boost | | 3 levels | 3 levels | Tandem with AC Boost | Tandem with AC Boost |
| RX pre-equalization for ISI compensation | | | | 3 levels | 3 levels |
| Charging Downstream Port (CDP) controller | | | Always ON | Pin Controlled | Always ON. Dynamically selected by DCP/CDP pin |
| Dedicated Charging Port (DCP) controller | | | | | Always ON. Dynamically selected by DCP/CDP pin |
| Cable length compensation for near-end high-speed eye mask Compliance (pre-channel before redriver/post-channel after redriver) (meter - gauge) | 2/1 - 28AWG | 4/2 - 28AWG | 4/2 - 28AWG | 6/3 - 28AWG (10 - 24AWG with one redriver on each end) | 6/3 - 28AWG (10 - 24AWG with one redriver on each end) |
| Cable length compensation for far-end high-speed eye mask Compliance (pre-channel before redriver/post-channel after redriver) (meter - gauge) | 5/3 - 28AWG | 8/6 - 28AWG | 8/6 - 28AWG | 10/8 - 26AWG (10 - 28AWG with one redriver on each end) | 10/8 - 26AWG (10 - 28AWG with one redriver on each end) |

## 6 Pin Configuration and Functions

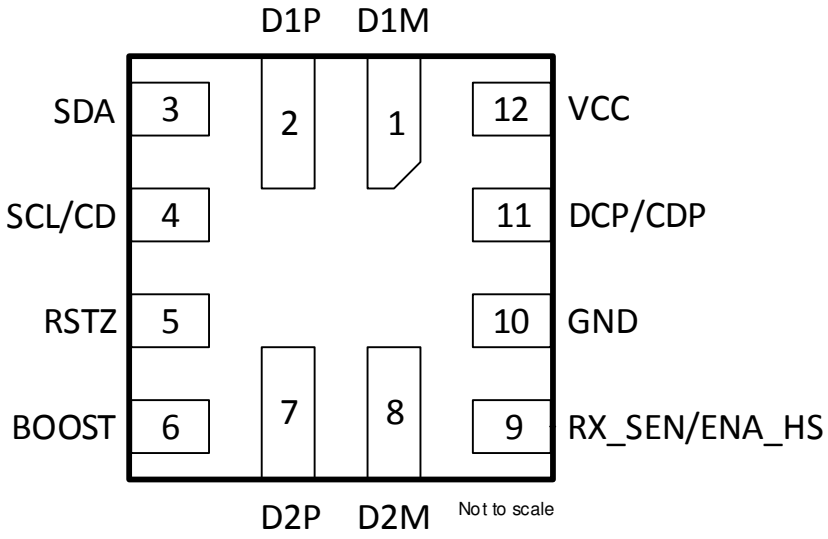



**図 6-1. TUSB217A-Q1 RWB 12-Pin X2QFN Top View**

**表 6-1. Pin Functions**

| PIN (RWB) | | I/O | INTERNAL PULLUP/PULLDOWN | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. (RWB) | | | |
| BOOST | 6 | I | N/A | USB High-speed boost select through the external pull down resistor. Both edge boost and DC boost are controlled by a single pin in non-I2C mode. In I2C mode edge boost and DC boost can be individually controlled.<br>Sampled upon power up. Does not recognize real time adjustments. Auto selects BOOST LEVEL = 3 when left floating. |
| DCP/CDP | 11 | I | 500 kΩ PU | DCP or CDP mode selection. Low=DCP and High=CDP<br>TUSB217A-Q1RWB BC1.2 controller is always enabled. |
| RX_SEN(2)/ENA_HS | 9 | I/O | N/A | In I2C mode:<br>Reserved for TI test purpose.<br>In non-I2C mode:<br>At reset: 3-level input signal RX_SEN. USB High-speed RX Equalization Setting to Compensate ISI Jitter<br>H (pin is pulled high) – high RX equalization (high loss channel)<br>M (pin is left floating) – medium RX equalization (medium loss channel)<br>L (pin is pulled low) – low RX equalization (low loss channel)<br>After reset: Output signal ENA_HS. Flag indicating that channel is in High-speed mode. Asserted upon:<br>1. Detection of USB-IF High-speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern.<br>2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 µs – 128 µs]. |
| D2P | 7 | I/O | N/A | USB High-speed positive port. |
| D2M | 8 | I/O | N/A | USB High-speed negative port. |
| GND | 10 | P | N/A | Ground |
| D1M | 1 | I/O | N/A | USB High-speed negative port.. |
| D1P | 2 | I/O | N/A | USB High-speed positive port. |
| SDA(1) | 3 | I/O | 500 kΩ PU<br>1.8 MΩ PD | I2C Mode:<br>Bidirectional I2C data pin [7-bit I2C slave address = 0x2C].<br>In non I2C mode:<br>Reserved for TI test purpose. |
| VCC | 12 | P | N/A | Supply power |

**表 6-1. Pin Functions (continued)**

| PIN (RWB) | | I/O | INTERNAL PULLUP/PULLDOWN | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. (RWB) | | | |
| RSTN | 5 | I | 500 kΩ PU<br>1.8 MΩ PD | Device disable/enable.<br>Low – Device is at reset and in shutdown, and<br>High - Normal operation.<br>Recommend 0.1-µF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications. |
| SCL(1)/CD | 4 | I/O | When RSTN asserted there is a 500 kΩ PD | In I2C mode:<br>I2C clock pin [I2C address = 0x2C].<br>Non I2C mode:<br>After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect. |

(1) Pull-up resistors for SDA and SCL pins in $I^2C$ mode should be $R_{Pull-up}$ (depending on I2C bus voltage). If both SDA and SCL are pulled up at power-up the device enters into $I^2C$ mode.
(2) Pull-down and pull-up resistors for RX_SEN pin must follow $R_{RXSEN1}$ and $R_{RXSEN2}$ resistor recommendations in non $I^2C$ mode.

# 7 Specifications

## 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range | VCC | –0.3 | 7 | V |
| Voltage range USB data | DxP, DxM | –0.3 | 5.5 | V |
| Voltage range on BOOST pin | BOOST | -0.3 | 1.98 | V |
| Voltage range other pins | RX_SEN, DCP/CDP,SDA,SCL, RSTN | -0.3 | 5.5 | V |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |
| Maximum junction temperature, $T_{J\ (max)}$ | | | 125 | °C |

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002((1)) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011((4)) | ±750 | |

(1) AEC Q100-002 HBM ESD Classification Level 2
(2) AEC Q100- 011 CDM ESD Classification Level C4A

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 2.3 | 5 | 6.5 | V |
| $T_A$ | Operating free-air temperature (AEC-Q100) | –40 | | 105 | °C |
| $T_J$ | Junction temperature (AEC-Q100) | | | 115 | °C |
| $V_{I2C\_BUS}$ | I2C Bus Voltage | 1.62 | | 3.6 | V |
| DxP, DxM | Voltage range USB data | 0 | | 3.6 | V |
| BOOST | Voltage range BOOST pin | 0 | | 1.98 | V |
| DIGITAL | Voltage range other pins (SCL, SDA, RSTN, DCP/CDP) | 0 | | 3.6 | V |
| RX_SEN | Voltage range RX_SEN pin | 0 | | 5.0 | V |

## 7.4 Thermal Information

| THERMAL METRIC (1) | | RWB (X2QFN) 12 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 137.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 62 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 67.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 67.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP (1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER** | | | | | | |
| $I_{ACTIVE\_HS}$ | High Speed Active Current | USB channel = HS mode. 480 Mbps traffic. $V_{CC}$ supply stable, with Boost = Max | | 22 | 36 | mA |
| $I_{IDLE\_HS}$ | High Speed Idle Current | USB channel = HS mode, no traffic. $V_{CC}$ supply stable, Boost = Max | | 22 | 36 | mA |
| $I_{HS\_SUPSPEND}$ | High Speed Suspend Current | USB channel = HS Suspend mode. $V_{CC}$ supply stable | | 0.75 | 1.4 | mA |
| $I_{FS}$ | Full-Speed Current | USB channel = FS mode, 12 Mbps traffic, $V_{cc}$ supply stable | | 0.75 | 1.4 | mA |
| $I_{DISCONN}$ | Disconnect Power | Host side application. No device attachment. | | 0.80 | 1.4 | mA |
| $I_{SHUTDN}$ | Shutdown Power | RSTN driven low, $V_{CC}$ supply stable | | 60 | 115 | µA |
| **CONTROL PIN LEAKAGE** | | | | | | |
| $I_{LKG\_FS}$ | Pin failsafe leakage current for SDA, RSTN | $V_{CC}$ = 0 V, pin at $V_{IH, max}$ | | 10 | 15 | µA |
| $I_{LKG\_FS}$ | Pin failsafe leakage current for RX_SEN | $V_{CC}$ = 0 V, pin at $V_{IH, max}$ | | 6 | 15 | µA |
| $I_{LKG\_FS}$ | Pin failsafe leakage current for SCL | $V_{CC}$ = 0 V, pin at $V_{IH, max}$ | | | 70 | nA |
| **INPUT RSTN** | | | | | | |
| $V_{IH}$ | High level input voltage | | 1.5 | | 3.6 | V |
| $V_{IL}$ | Low-level input voltage | | 0 | | 0.5 | V |
| $I_{IH}$ | High level input current | $V_{IH}$ = 3.6 V, $R_{PU}$ enabled | | | ±15 | µA |
| $I_{IL}$ | Low level input current | $V_{IL}$ = 0V, $R_{PU}$ enabled | | | ±20 | µA |
| **INPUT DIGITAL** | | | | | | |
| $V_{IH}$ | High level input voltage (DCP/ CDP) | | 1.5 | | 3.6 | V |
| $V_{IL}$ | Low-level input voltage (DCP/ CDP) | | 0 | | 0.5 | V |
| $I_{IL}$ | Low level input current | $V_{IL}$ = 0V | | | ±20 | µA |
| $I_{IH}$ | High level input current | $V_{IH}$ = 3.6 V | | | ±15 | µA |
| **INPUT RX_SEN (3-level input, for mid level leave pin floating)** | | | | | | |
| $V_{IH(Max)}$ | Maximum High level input voltage | VCC = 2.3V to 6.5V | | | 5.0 | V |
| $V_{IH(Min)}$ | Minimum High level input voltage | VCC > 4.5V | 3.3 | | | V |
| | | VCC = 2.3V to 4.5V (% of VCC) | 75 | | | % |
| $V_{IL}$ | Low level input voltage | VCC > 4.5V | | | 0.75 | V |
| | | VCC = 2.3V to 4.5V (% of VCC) | | | 15 | % |
| **INPUT BOOST** | | | | | | |
| $R_{BOOST\_LVL0}$ | External pulldown resistor for BOOST Level 0 | | | | 160 | Ω |
| $R_{BOOST\_LVL1}$ | External pulldown resistor for BOOST Level 1 | | 1.5 | 1.8 | 2 | kΩ |
| $R_{BOOST\_LVL2}$ | External pulldown resistor for BOOST Level 2 | | 3.4 | 3.6 | 3.96 | kΩ |
| $R_{BOOST\_LVL3}$ | External pulldown resistor for BOOST Level 3 to remove upper limit for resistor value, can be left open | | 7.5 | | | kΩ |
| **OUTPUTS CD, ENA_HS** | | | | | | |
| $V_{OH}$ | High level output voltage for CD and ENA_HS | $I_O$ = –50 µA, VCC >= 3.0V | 2.5 | | | V |
| $V_{OH}$ | High level output voltage for CD | $I_O$ = –25 µA, VCC = 2.3V | 1.7 | | | V |

## 7.5 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP (1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High level output voltage for ENA_HS | $I_O$ = –25 µA, VCC = 2.3V | 1.8 | | | V |
| $V_{OL}$ | Low level output voltage for CD and ENA_HS | $I_O$ = 50 µA | | | 0.3 | V |
| **I2C** | | | | | | |
| $C_{I2C\_BUS}$ | $I^2C$ Bus Capacitance | | 4 | | 150 | pF |
| $I_{OL}$ | $I^2C$ open drain output current | $V_{OL}$ = 0.4V | 1.5 | | | mA |
| $V_{IL}$ | 2.3V<= VCC<= 4.3V, $V_{I2C\_BUS}$ = 1.8V +/-10% | $R_{Pull-up}$ =1.6kΩ to 2.5kΩ, % of $V_{I2C\_BUS}$ | | | 25 | % |
| $V_{IL}$ | $V_{I2C\_BUS}$ = 3.3V +/-10% | $R_{Pull-up}$ =2.8kΩ to 7kΩ, % of $V_{I2C\_BUS}$ | | | 25 | % |
| $V_{IH}$ | 2.3V<= VCC<= 4.3V, $V_{I2C\_BUS}$ = 1.8V +/-10% | $R_{Pull-up}$ =1.6kΩ to 2.5kΩ, % of $V_{I2C\_BUS}$ | 80 | | | % |
| $V_{IH}$ | $V_{I2C\_BUS}$ = 3.3V +/-10% | $R_{Pull-up}$ =2.8kΩ to 7kΩ, % of $V_{I2C\_BUS}$ | 75 | | | % |
| $R_{Pull-up}$ | $V_{I2C\_BUS}$ = 1.8V +/-10% | | 1.6 | 2 | 2.5 | kΩ |
| $R_{Pull-up}$ | $V_{I2C\_BUS}$ = 3.3V +/-10% | | 2.8 | 4.7 | 7 | kΩ |
| SCL Frequency | | | | | 100 | kHz |
| **DxP, DxM** | | | | | | |
| $C_{IO\_DXX}$ | Capacitance to GND | Measured with VNA at 240 MHz, $V_{CC}$ supply stable, Redriver off | | 2.5 | | pF |

(1) All typical values are at $V_{CC}$ = 5 V, and $T_A$ = 25°C.

## 7.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP (1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DxP, DxM USB Signals** | | | | | | |
| $F_{BR\_DXX}$ | Bit Rate | USB channel = HS mode. 480 Mbps traffic. $V_{CC}$ supply stable | | | 480 | Mbps |
| $t_{R/F\_DXX}$ | Rise/Fall time | | 100 | | | ps |

(1) All typical values are at $V_{CC}$ = 5 V, and $T_A$ = 25°C.

## 7.7 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **POWER UP TIMING** | | | | | |
| $T_{RSTN\_PW}$ | Minimum width to detect a valid RSTN signal assert when the pin is actively driven low | 100 | | | µs |
| $T_{STABLE}$ | VCC must be stable before RSTN de-assertion | 300 | | | µs |
| $T_{READY}$ | Maximum time needed for the device to be ready after RSTN is de-asserted. | | | 500 | µs |
| $T_{RAMP}$ | $V_{CC}$ ramp time | | | 100 | ms |
| $T_{RAMP}$ | $V_{CC}$ ramp time | 0.2 | | | ms |
| **I2C (STD)** | | | | | |
| $t_{SUSTO}$ | Stop setup time, SCL ($T_r$=600ns-1000ns), SDA ($T_f$=6.5ns-106.5ns), 100kHz STD | 4 | | | µs |
| $t_{HDSTA}$ | Start hold time, SCL (Tr=600ns-1000ns), SDA (Tf=6.5ns-106.5ns), 100kHz STD | 4 | | | µs |
| $t_{SUSTA}$ | Start setup time, SCL ($T_r$=600ns-1000ns), SDA ($T_f$=6.5ns-106.5ns), 100kHz STD | 4.7 | | | µs |
| $t_{SUDAT}$ | Data input or False start/stop, setup time, SCL ($T_r$=600ns-1000ns), SDA ($T_f$=6.5ns-106.5ns), 100kHz STD | 250 | | | ns |
| $t_{HDDAT}$ | Data input or False start/stop, hold time, SCL ($T_r$=600ns-1000ns), SDA ($T_f$=6.5ns-106.5ns), 100kHz STD | 5 | | | µs |
| $t_{BUF}$ | Bus free time between START and STOP conditions | 4.7 | | | µs |
| $t_{LOW}$ | Low period of the $I_{2C}$ clock | 4.7 | | | µs |
| $t_{HIGH}$ | High period of the $I_{2C}$ clock | 4 | | | µs |
| $t_F$ | Fall time of both SDA and SCL signals | | | 300 | ns |
| $t_R$ | Rise time of both SDA and SCL signals | | | 1000 | ns |

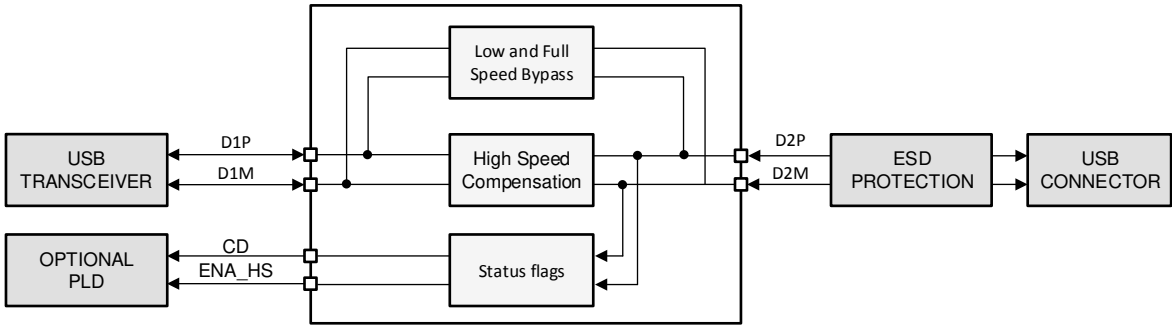
# 8 Detailed Description

## 8.1 Overview

The TUSB217A-Q1 is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB217A-Q1 has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. Additional RX sensitivity, tuned by external pull-up resistor and pull-down resistor, allows to overcome attenuation in cables. The TUSB217A-Q1 allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

## 8.2 Functional Block Diagram






## 8.3 Feature Description

### 8.3.1 High-Speed Boost

The high-speed booster (combination of edge boost and DC boost) improves the eye width for USB2.0 high-speed signals. It is direction independent and by that is compatible to OTG systems. The BOOST pin is configuring the booster strength with different values of pull down resistors to set 4 levels of boosts, alternatively the boost level can be set through the I2C register according to セクション 8.4.6. Internal circuitry of the signal conditioner reduces possible overshoot.

### 8.3.2 RX Sensitivity

The RX_SEN pin is a tri-level pin. It is used to set the equalization gain of the device according to system channel inter-symbol interference (ISI) loss. RX equalization can be increased to compensate for the higher ISI loss of the channel for example due to a long cable.

## 8.4 Device Functional Modes

### 8.4.1 Low-Speed (LS) Mode

TUSB217A-Q1 automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

### 8.4.2 Full-Speed (FS) Mode

TUSB217A-Q1 automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low

### 8.4.3 High-Speed (HS) Mode

TUSB217A-Q1 automatically detects a HS connection and will enable signal compensation as determined by the configuration of the RX_SEN pin and the external pull down resistance on its BOOST pin.

CD pin and ENA_HS pin are asserted high when high-speed boost is active.

### 8.4.4 High-Speed Downstream Port Electrical Compliance Test Mode

TUSB217A-Q1 will detect HS compliance test fixture and enter downstream port high-speed eye diagram test mode. CD pin will be low and ENA_HS pin is asserted high when TUSB217A-Q1 is in HS eye compliance test mode.

If RSTN pin is asserted low and de-asserted high while TUSB217A-Q1 is operating in HS functional mode, TUSB217A-Q1 may transition to HS eye compliance test mode and CD asserts low and ENA_HS remains high. When this occurs signal compensation is enabled.

### 8.4.5 Shutdown Mode

TUSB217A-Q1 can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

**表 8-1. CD and ENA_HS Pins in Different Modes**

| MODE | CD | ENA_HS |
|---|---|---|
| Low-speed | HIGH | LOW |
| Full-speed | HIGH | LOW |
| High-speed | HIGH | HIGH |
| High-speed downstream port electrical test | LOW | HIGH |
| Shutdown | LOW | LOW |

### 8.4.6 $I^2C$ Mode

TUSB217A-Q1 supports 100 KHz I2C for device configuration, status read back and test purposes. For detail electrical and functional specifications refer to I2C Bus Specification 2.1, 2001 – STANDARD MODE. This controller is enabled after SCL and SDA pins are sampled high shortly after return from shutdown. In this mode, the CSR can be accessed by I2C read/write transaction to 7-bit slave address 0x2C. It is advised to set CFG_ACTIVE bit before changing values. This halts the FSM, and reset it after all changes are made. This ensure proper startup into high-speed mode.

### 8.4.7 BC 1.2 Battery Charging Controller

Battery charging controller feature is always enabled in TUSB217A-Q1 RWB and supports both CDP charging downstream port functionality and DCP dedicated charging port functionality depending on DCP/CDP pin. When DCP/CDP pin is high the BC 1.2 controller supports CDP mode and when DCP/CDP pin is low BC 1.2 controller supports DCP mode. DCP/CDP pin can be dynamically controlled. When host or hub is disabled DCP/CDP pin can be set low to support DCP mode and when host or hub is enabled DCP/CDP pin can be set to high to support CDP. Downstream VBUS should be toggled after the DCP/CDP pin change so BC 1.2 handshake starts over to indicate charging mode change.

DCP/CDP pin has an internal pull up resistor. When DCP/CDP pin is left unconnected the BC 1.2 controller will be in CDP mode.

**表 8-2. TUSB217A-Q1 RWB Battery Charging Controller Modes**

| Pin 11 (DCP/CDP) | CDP | DCP |
|---|---|---|
| Low | NO | YES |
| High | YES | NO |

## 8.5 TUSB217A-Q1 Registers

表 8-3 lists the memory-mapped registers for the TUSB217A-Q1 registers. All register offset addresses not listed in 表 8-3 should be considered as reserved locations and the register contents should not be modified.

**表 8-3. TUSB217A-Q1 Registers**

| Offset | Acronym | Register Name | Section |
|---|---|---|---|
| 0x1 | EDGE_BOOST | This register is setting EDGE BOOST level. | Go |
| 0x3 | CONFIGURATION | This register is selecting device mode. | Go |
| 0xE | DC_BOOST | This register is setting DC BOOST level. | Go |
| 0x25 | RX_SEN | This register is setting RX Sensitivity level. | Go |

Complex bit access types are encoded to fit into small table cells. 表 8-4 shows the codes that are used for access types in this section.

**表 8-4. TUSB217A-Q1 Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| Read Type | | |
| RH | H<br>R | Set or cleared by hardware<br>Read |
| Write Type | | |
| W | W | Write |
| Reset or Default Value | | |
| *-n* | | Value after reset or the default value |

### 8.5.1 EDGE_BOOST Register (Offset = 0x1) [reset = X]

EDGE_BOOST is shown in 図 8-1 and described in 表 8-5.

Return to Summary Table.

This register is setting EDGE BOOST level.

**図 8-1. EDGE_BOOST Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ACB_LVL | | | | RESERVED | | | |
| RH/W-X | | | | RH/W-X | | | |

**表 8-5. EDGE_BOOST Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | ACB_LVL | RH/W | X | XXXXb (sampled at startup from BOOST pin)<br>0000b to 1111b range<br>0x0 = BOOST PIN LEVEL 0 (lowest edge boost setting)<br>0x3 = BOOST PIN LEVEL 1<br>0x6 = BOOST PIN LEVEL 2<br>0xA = BOOST PIN LEVEL 3<br>0xF = (highest edge boost setting) |

表 8-5. EDGE_BOOST Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | RESERVED | RH/W | X | These bits are reserved bits and set by hardware at reset.<br>When this register is modified the software should first read these reserved bits and rewrite with the same values |

### 8.5.2 CONFIGURATION Register (Offset = 0x3) [reset = X]

CONFIGURATION is shown in 図 8-2 and described in 表 8-6.

Return to Summary Table.

This register is selecting device mode.

図 8-2. CONFIGURATION Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | CFG_ACTIVE |
| RH/W-X | | | | | | | RH/W-0x1 |

表 8-6. CONFIGURATION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | RH/W | X | These bits are reserved bits and set by hardware at reset.<br>When this register is modified the software should first read these reserved bits and rewrite with the same values |
| 0 | CFG_ACTIVE | RH/W | 0x1 | Configuration mode<br>After reset, if I2C mode is true (SCL and SDA are both pulled high) set the bit to get into configuration mode and clear to return to normal mode.<br>0x0 = NORMAL MODE<br>0x1 = CONFIGURATION MODE |

### 8.5.3 DC_BOOST Register (Offset = 0xE) [reset = X]

DC_BOOST is shown in 図 8-3 and described in 表 8-7.

Return to Summary Table.

This register is setting DC BOOST level.

図 8-3. DC_BOOST Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | DCB_LVL | | | |
| RH/W-X | | | | RH/W-X | | | |

表 8-7. DC_BOOST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | RH/W | X | These bits are reserved bits and set by hardware at reset.<br>When this register is modified the software should first read these reserved bits and rewrite with the same values |

表 8-7. DC_BOOST Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | DCB_LVL | RH/W | X | XXXXb (sampled at startup from BOOST pin)<br>0000b to 1111b range<br>0x0 = BOOST PIN LEVEL 0 (lowest dc boost setting)<br>0x2 = BOOST PIN LEVEL 1 and 2<br>0x6 = BOOST PIN LEVEL 3<br>0xF = (highest dc boost setting) |

### 8.5.4 RX_SEN Register (Offset = 0x25) [reset = X]

RX_SEN is shown in 図 8-4 and described in 表 8-8.

Return to Summary Table.

This register is setting RX Sensitivity level.

図 8-4. RX_SEN Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RX_SEN | | | | | | | |
| RH/W-X | | | | | | | |

表 8-8. RX_SEN Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | RX_SEN | RH/W | X | XXXXb (sampled at startup from RX_SEN pin)<br>00000000b to 11111111b range<br>0x0 = RX_SEN LEVEL LOW<br>0x33 = RX_SEN LEVEL MID<br>0x66 = RX_SEN LEVEL HIGH<br>0xFF = (highest setting) |

# 9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 9.1 Application Information

The purpose of the TUSB217A-Q1 is to re-store the signal integrity of a USB High-speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB217A-Q1 can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB217A-Q1 to control other blocks on the customer platform, if so desired.

## 9.2 Typical Application

A typical application for TUSB217A-Q1 with dynamic mode change between DCP and CDP is shown in 図 9-1. BC 1.2 controller mode will be based on host/hub active state in this application. When host/hub is not active the controller will be in DCP mode and when the host/hub is active the controller will be in CDP mode. Downstream VBUS needs to be toggled by the power controller to change advertisement and for portable device to re-detect the BC 1.2 controller charging mode. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed (that is, D2 faces transceiver and D1 faces connector).

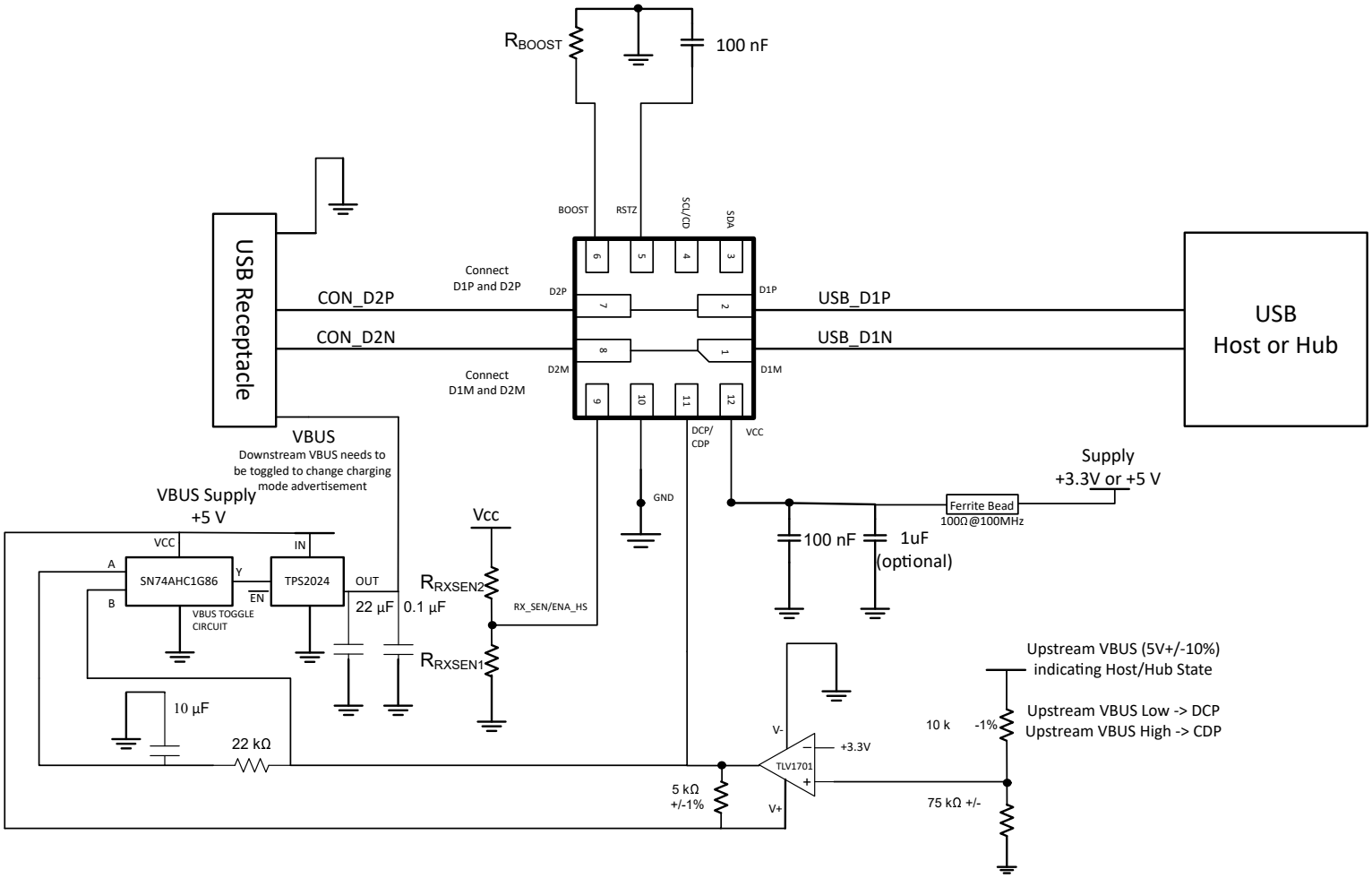





**図 9-1. TUSB217A-Q1: A Reference Schematic (Design Example with DCP/CDP Dynamic Switching). Downstream VBUS Needs to be Toggled if Upstream VBUS State Changes for BC 1.2 Controller to Change DCP/CDP Advertisement.**

### 9.2.1 Design Requirements

TUSB217A-Q1 requires a valid reset signal as described in the *Power Supply Recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters shown in 表 9-1, 表 9-2 and 表 9-3.

**表 9-1. Design Parameters for 5-V Supply With High Loss System**

| PARAMETER | | | | VALUE(1) |
|---|---|---|---|---|
| $V_{CC}$ | | | | 5 V ±10% |
| $I^2C$ support required in system (Yes/No) | | | | No |
| Edge and DC Boost | | $R_{BOOST}$ | BOOST Level | Boost Level 1: $R_{BOOST}$ = 1.8 kΩ |
| | | 0-Ω | 0 | |
| | | 1.8 kΩ ±1% | 1 | |
| | | 3.6 kΩ ± 1% | 2 | |
| | | Do Not Install (DNI) | 3 | |
| RX Sensitivity | $R_{RXSEN1}$ | $R_{RXSEN2}$ | RX_SEN Level | High RX Sensitivity Level: $R_{RXSEN1}$ = 37.5 kΩ $R_{RXSEN2}$ = 12.5 kΩ |
| | 22 kΩ - 40 kΩ (27 kΩ typical) | Do Not Install (DNI) | Low | |
| | Do Not Install (DNI) | Do Not Install (DNI) | Medium | |
| | 37.5 kΩ(2) | 12.5 kΩ | High | |

(1) These parameters are starting values for a high loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 5 V supply system could be applicable to 3.3 V supply system as well.
(2) This resistor is needed for a 5 V supply to divide the voltage down so the RX_SEN pin voltage does not exceed 5.0 V.

**表 9-2. Design Parameters for 3.3-V Supply With Low to Medium Loss System**

| PARAMETER | | | | VALUE(1) |
|---|---|---|---|---|
| $V_{CC}$ | | | | 3.3 V ±10% |
| $I^2C$ support required in system (Yes/No) | | | | No |
| Edge and DC Boost | | $R_{BOOST}$ | BOOST Level | Boost Level 0: $R_{BOOST}$ = 0-Ω |
| | | 0-Ω | 0 | |
| | | 1.8 kΩ ±1% | 1 | |
| | | 3.6 kΩ ±1% | 2 | |
| | | Do Not Install (DNI) | 3 | |
| RX Sensitivity | $R_{RXSEN1}$ | $R_{RXSEN2}$ | RX_SEN Level | Medium RX Sensitivity Level: $R_{RXSEN1}$ = DNI $R_{RXSEN2}$ = DNI |
| | 22 kΩ – 40 kΩ (27 kΩ typical) | Do Not Install (DNI) | Low | |
| | Do Not Install (DNI) | Do Not Install (DNI) | Medium | |
| | Do Not Install (DNI) | 22 kΩ – 40 kΩ (27 kΩ typical) | High | |

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 3.3 V supply system could be applicable to 5 V supply system as well.

**表 9-3. Design Parameters for 2.3-V to 4.3-V VBAT Supply With Low to Medium Loss System**

| PARAMETER | | | | VALUE(1) |
|---|---|---|---|---|
| $V_{CC}$ | | | | 2.3 V to 4.3V |
| $I^2C$ support required in system (Yes/No) | | | | No |
| Edge and DC Boost | | $R_{BOOST}$ | BOOST Level | Boost Level 0: $R_{BOOST}$ = 0-Ω |
| | | 0-Ω | 0 | |
| | | 1.8 kΩ ±1% | 1 | |
| | | 3.6 kΩ ±1% | 2 | |
| | | Do Not Install (DNI) | 3 | |
| RX Sensitivity | $R_{RXSEN1}$ | $R_{RXSEN2}$ | RX_SEN Level | Medium RX Sensitivity Level: $R_{RXSEN1}$ = DNI $R_{RXSEN2}$ = DNI |
| | 22 kΩ – 40 kΩ (27 kΩ typical) | Do Not Install (DNI) | Low | |
| | Do Not Install (DNI) | Do Not Install (DNI) | Medium | |
| | 37.5 kΩ(2) | 12.5 kΩ | High | |

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 2.3 V – 4.3 V supply system could be applicable to 5 V supply system as well.
(2) This resistor is needed for a VBAT supply (2.3 V – 4.3 V) to divide the voltage down so the RX_SEN pin voltage does not exceed 5.0 V.

### 9.2.2 Detailed Design Procedure

The ideal BOOST setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with BOOST level 0, and then increment to BOOST level 1, and so on. Same applies to the RX sensitivity setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with RX sensitivity level Low.

In order for the TUSB217A-Q1 to recognize any change to the BOOST setting, the RSTN pin must be toggled. This is because the BOOST pin is latched on power up and the pin is ignored thereafter.

注

The TUSB217A-Q1 compensates for extra attenuation in the signal path according to the configuration of the RX_SEN pin. This maximum recommended voltage for this pin is 5 V when selecting the highest RX sensitivity level.

Placement of the device is also dependent on the application goal. 表 9-4 summarizes our recommendations.

**表 9-4. Platform Placement Guideline**

| PLATFORM GOAL | SUGGESTED TUSB217A-Q1 PLACEMENT |
|---|---|
| Pass USB Near End Mask at the receptacle | Close to measurement point (connector) |
| Pass USB Far End Eye Mask at the plug | Close to USB PHY |
| Cascade multiple TUSB217A-Q1s to improve device enumeration | Midway between each USB interconnect |

**表 9-5. Table of Recommended Settings**

| BOOST and RX_SEN settings (1) for channel loss | | |
|---|---|---|
| **Pre-channel cable length (Between USB PHY and TUSB217A-Q1)** | **BOOST** | **RX_SEN** |
| 0-3 meter | Level 0 | Medium or High |
| 2-5 meter | Level 1 | Medium or High |
| **Post-channel cable length (Between TUSB217A-Q1 and inter-connect)** | **BOOST** | **RX_SEN** |
| 0-2 meter | Level 0 | Medium or High |
| 1-4 meter | Level 1 | Medium or High |

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host or device as well as cable length and loss profile.

#### *9.2.2.1 Test Procedure to Construct USB High-speed Eye Diagram*

注

USB-IF certification tests for High-speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High-speed Eye Mask:

##### 9.2.2.1.1 For a Host Side Application

1. Configure the TUSB217A-Q1 to the desired BOOST setting.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB217A-Q1.
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB217A-Q1.
4. Enable the host to transmit USB TEST_PACKET.
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to retest TUSB217A-Q1 with a different BOOST setting (must reset to change).

##### 9.2.2.1.2 For a Device Side Application

1. Configure the TUSB217A-Q1 to the desired BOOST setting.
2. Power on (or toggle the RSTN pin if already powered on) the TUSB217A-Q1.
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB217A-Q1. Ensure that the USB-IF device test fixture is configured to the ‘INIT’ position.
4. Allow the host to enumerate the device.
5. Enable the device to transmit USB TEST_PACKET.
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the ‘TEST’ position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB217A-Q1 with a different BOOST setting (must reset to change).

### 9.2.3 Application Curves

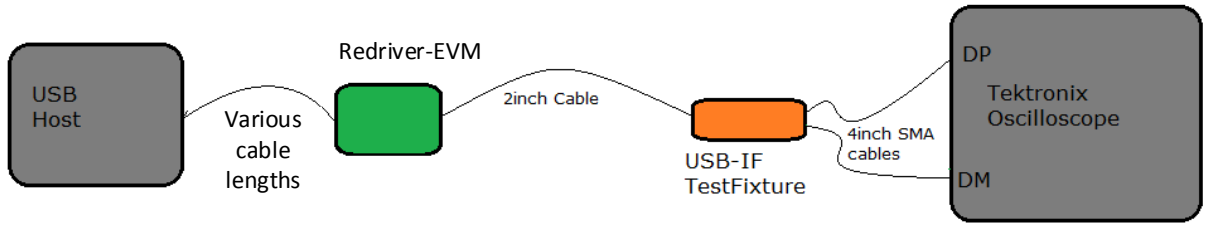



**図 9-2. Near End Eye Measurement Set-Up With Pre-Channel Cable**

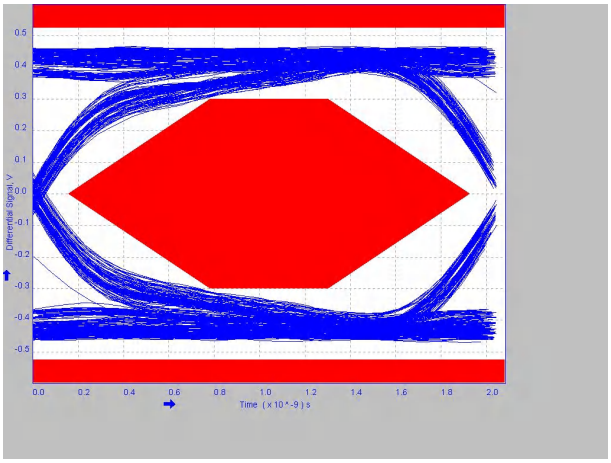


**図 9-3. 2 Meter Pre-Channel Without TUSB217A-Q1**

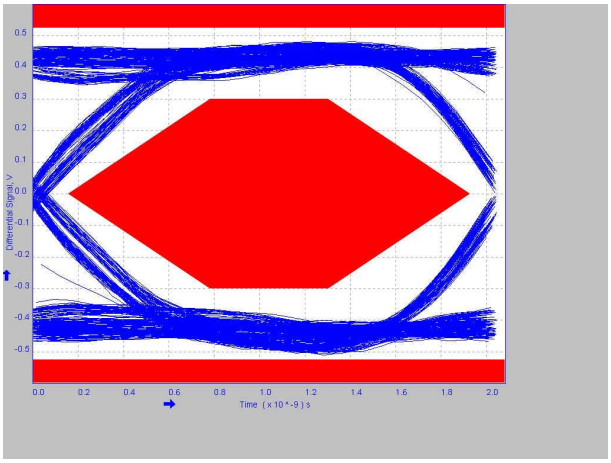


**図 9-4. 2 Meter Pre-Channel With TUSB217A-Q1 BOOST=1 RX_SEN=MED**

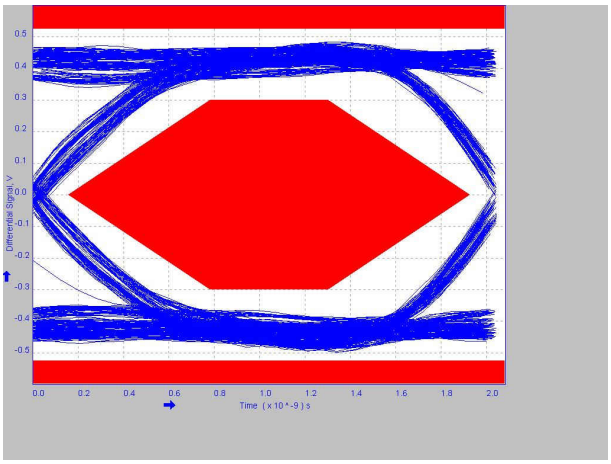


**図 9-5. 2 Meter Pre-Channel With TUSB217A-Q1 BOOST=0 RX_SEN=HIGH**

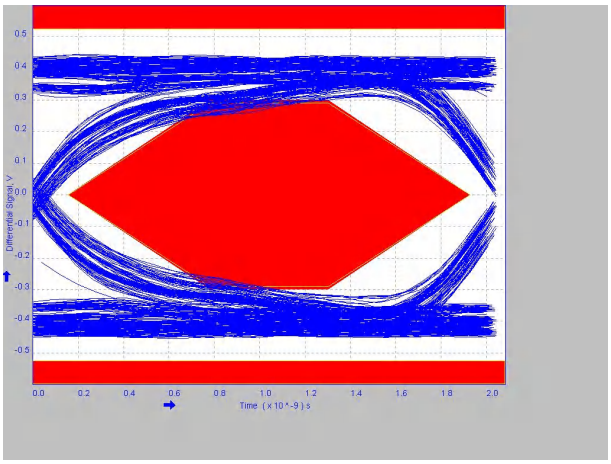


**図 9-6. 3 Meter Pre-Channel Without TUSB217A-Q1**

### 9.2.3 Application Curves (continued)

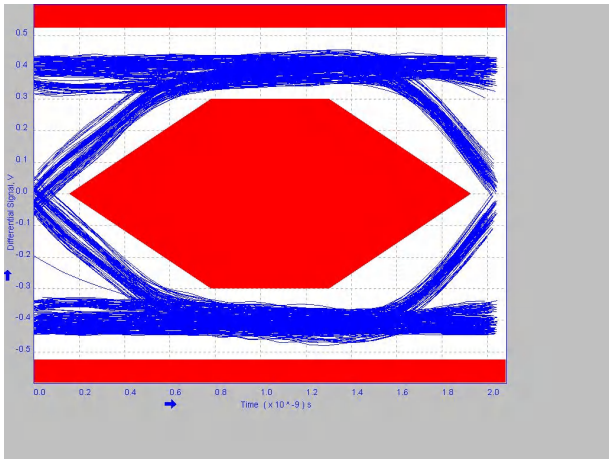


図 9-7. 3 Meter Pre-Channel With TUSB217A-Q1 BOOST=0 RX_SEN=HIGH

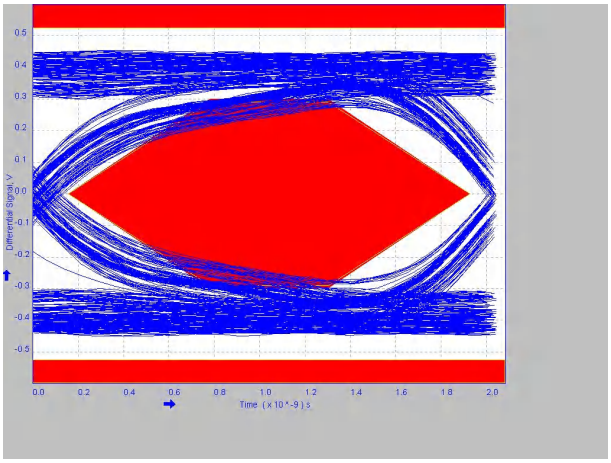


図 9-8. 5 Meter Without TUSB217A-Q1

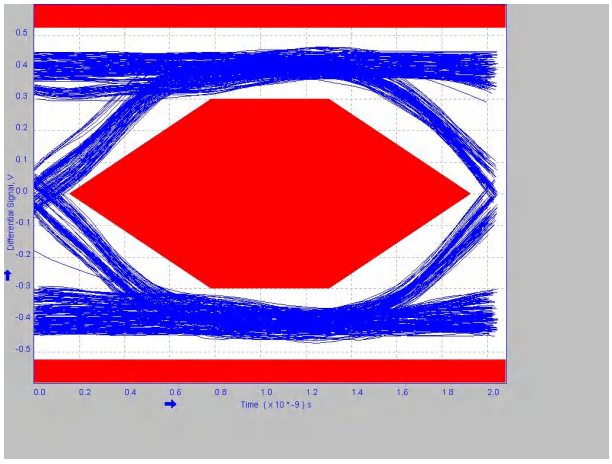


図 9-9. 5 Meter Pre-Channel With TUSB217A-Q1 BOOST=1 RX_SEN=MED

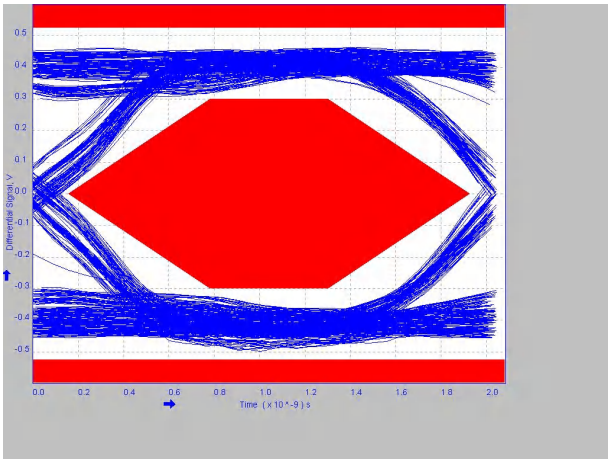


図 9-10. 5 Meter Pre-Channel With TUSB217A-Q1 BOOST=2 RX_SEN=MED

### 9.2.3 Application Curves

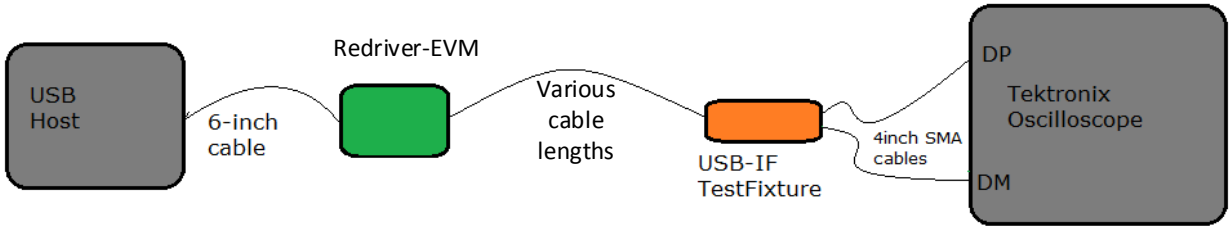



**図 9-11. Near End Eye Measurement Set-Up With Post-Channel Cable**

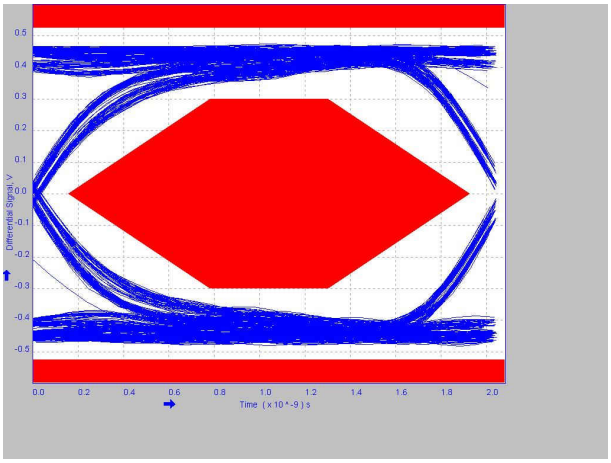


**図 9-12. 6 Inches Post Channel Without TUSB217A-Q1**

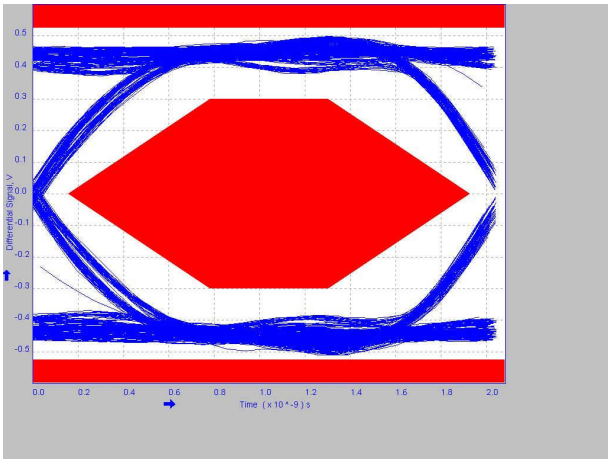


**図 9-13. 6 Inches Post-Channel With TUSB217A-Q1 BOOST=0 RX_SEN=HIGH**

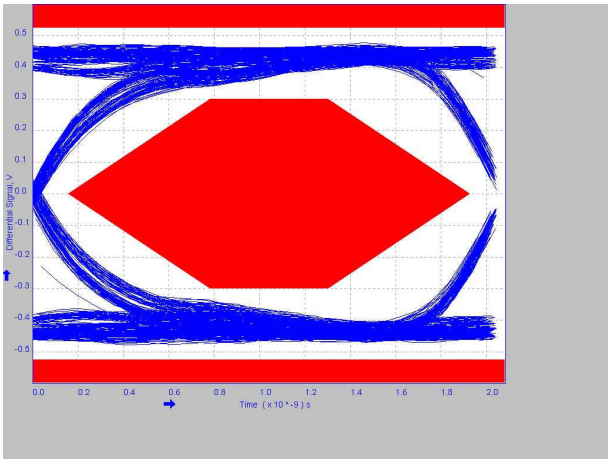


**図 9-14. 1 Meter Post-Channel Without TUSB217A-Q1**

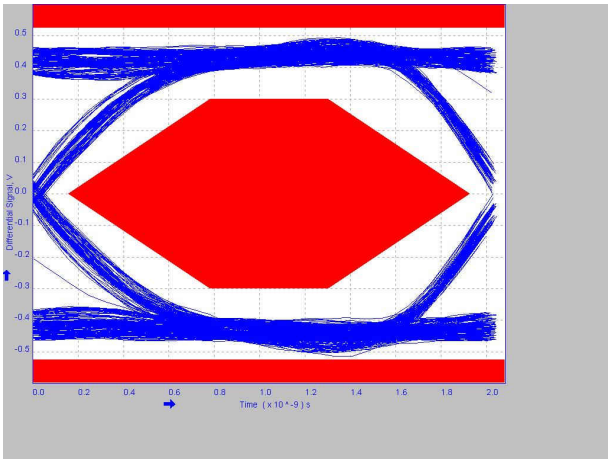


**図 9-15. 1 Meter Post-Channel With TUSB217A-Q1 BOOST=0 RX_SEN=MED**

### 9.2.3 Application Curves (continued)

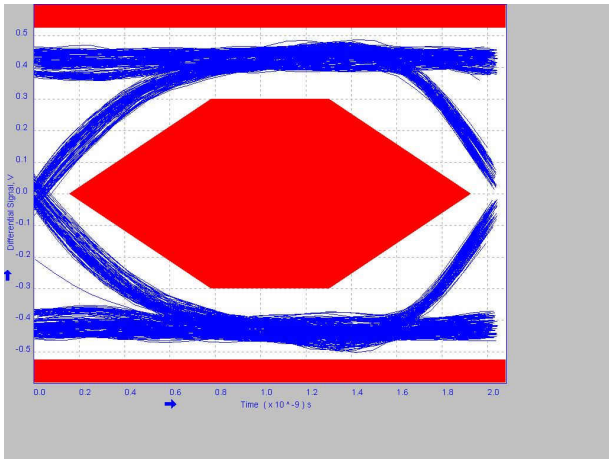


図 9-16. 1 Meter Post-Channel With TUSB217A-Q1 BOOST=0 RX_SEN=HIGH

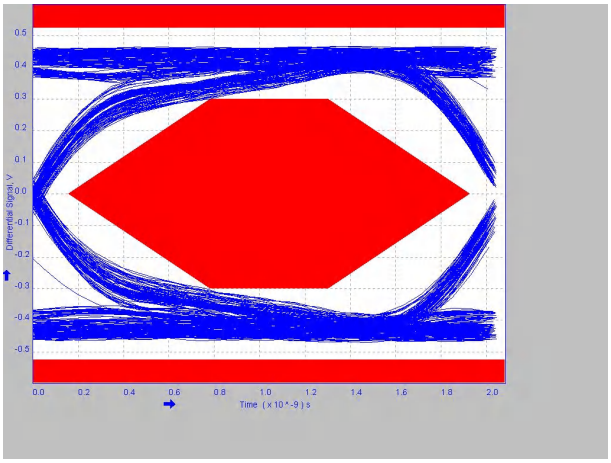


図 9-17. 2 Meter Post-Channel Without TUSB217A-Q1

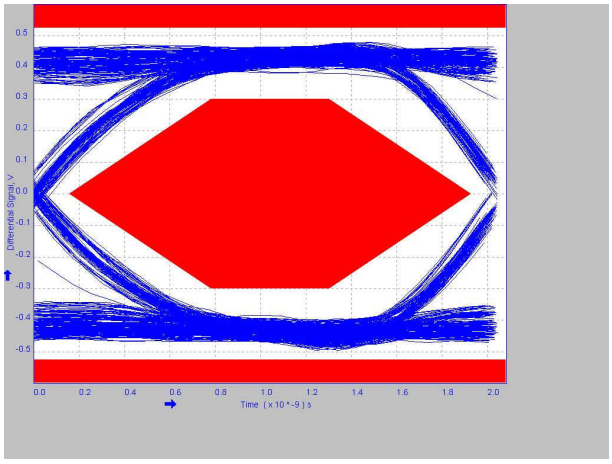


図 9-18. 2 Meter Post-Channel With TUSB217A-Q1 BOOST=1 RX_SEN=MED

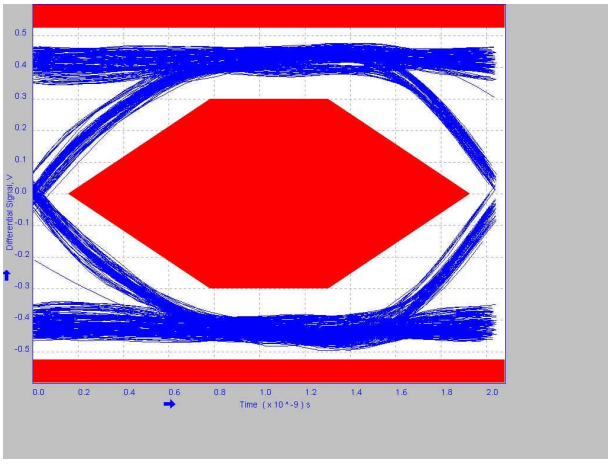


図 9-19. 2 Meter Post-Channel With TUSB217A-Q1 BOOST=1 RX_SEN=HIGH

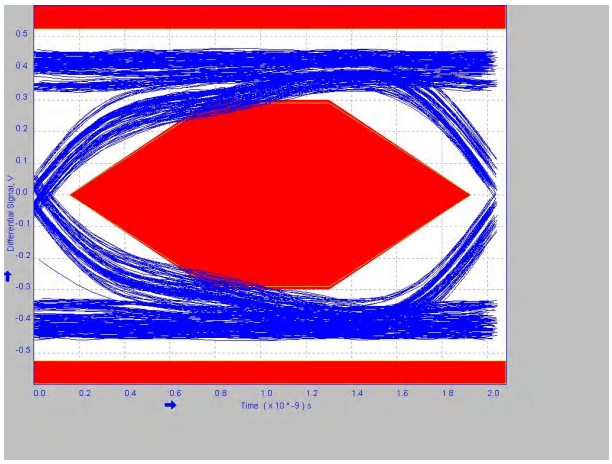


図 9-20. 4 Meter Post-Channel Without TUSB217A-Q1

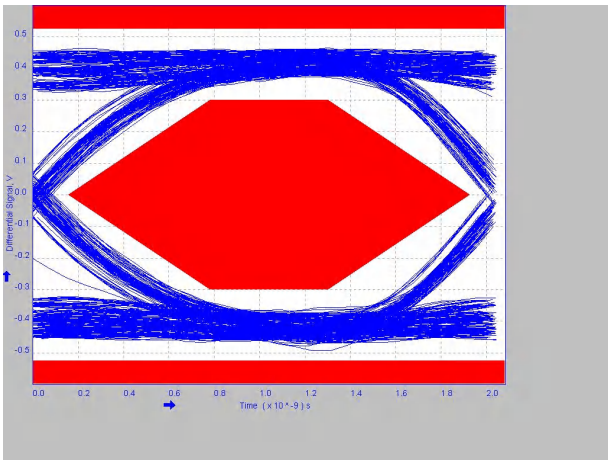


図 9-21. 4 Meter Post-Channel With TUSB217A-Q1 BOOST=2 RX_SEN=MED

# 10 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to minimum recommended supply voltage or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to $V_{CC}$). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

[Ramp Time x 5] ÷ [500 kΩ] (1)

# 11 Layout

## 11.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90 Ω differential routing underneath the device.

## 11.2 Layout Example

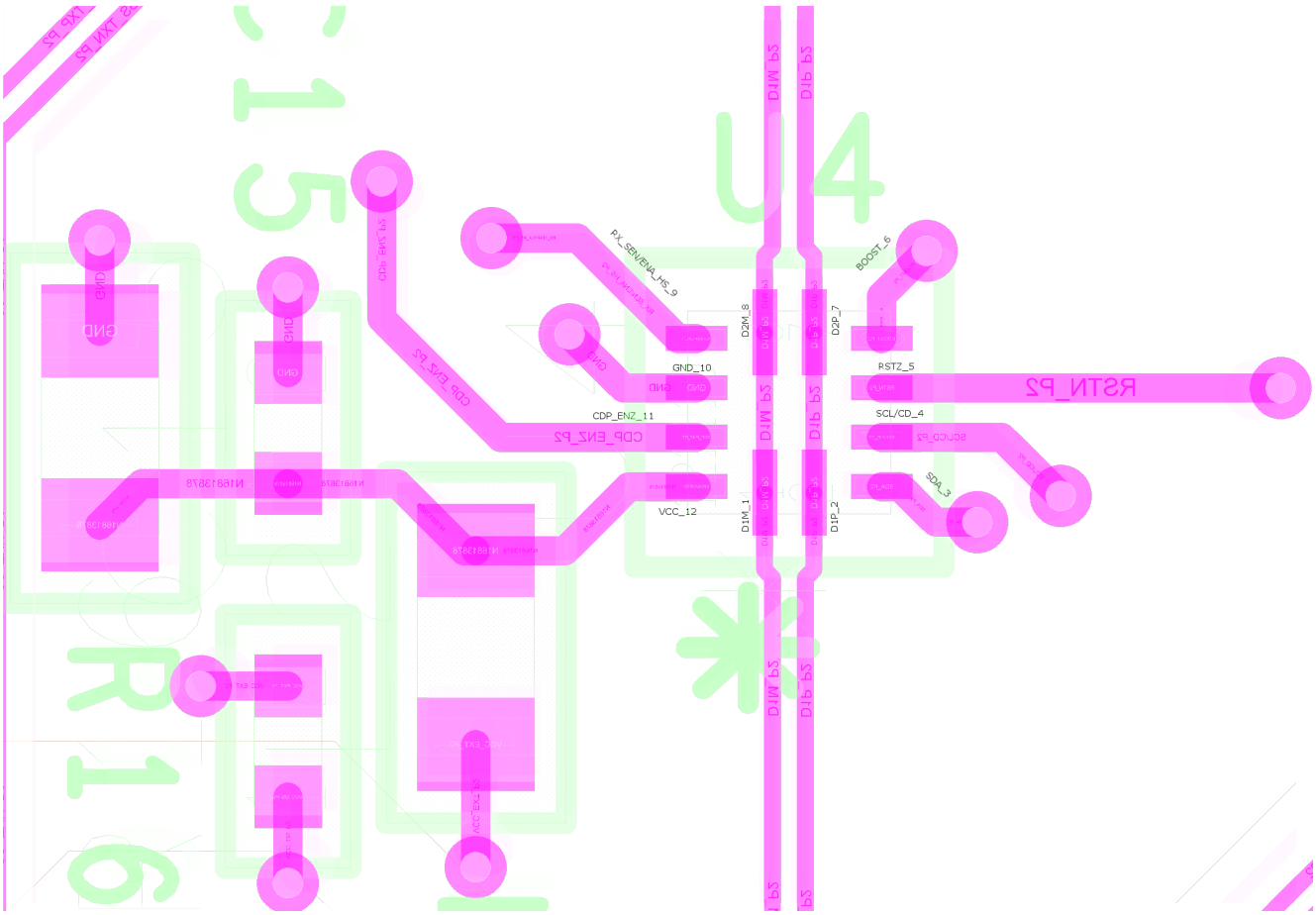



**図 11-1. Layout Example**

# 12 Device and Documentation Support

## 12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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## 12.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 12.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TUSB217ARWBRQ1 | Active | Production | X2QFN (RWB) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 7A |
| TUSB217ARWBRQ1.A | Active | Production | X2QFN (RWB) \| 12 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 7A |
| TUSB217ARWBTQ1 | Active | Production | X2QFN (RWB) \| 12 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 7A |
| TUSB217ARWBTQ1.A | Active | Production | X2QFN (RWB) \| 12 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 7A |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF TUSB217A-Q1 :**

- Catalog : TUSB217A

NOTE: Qualified Version Definitions:

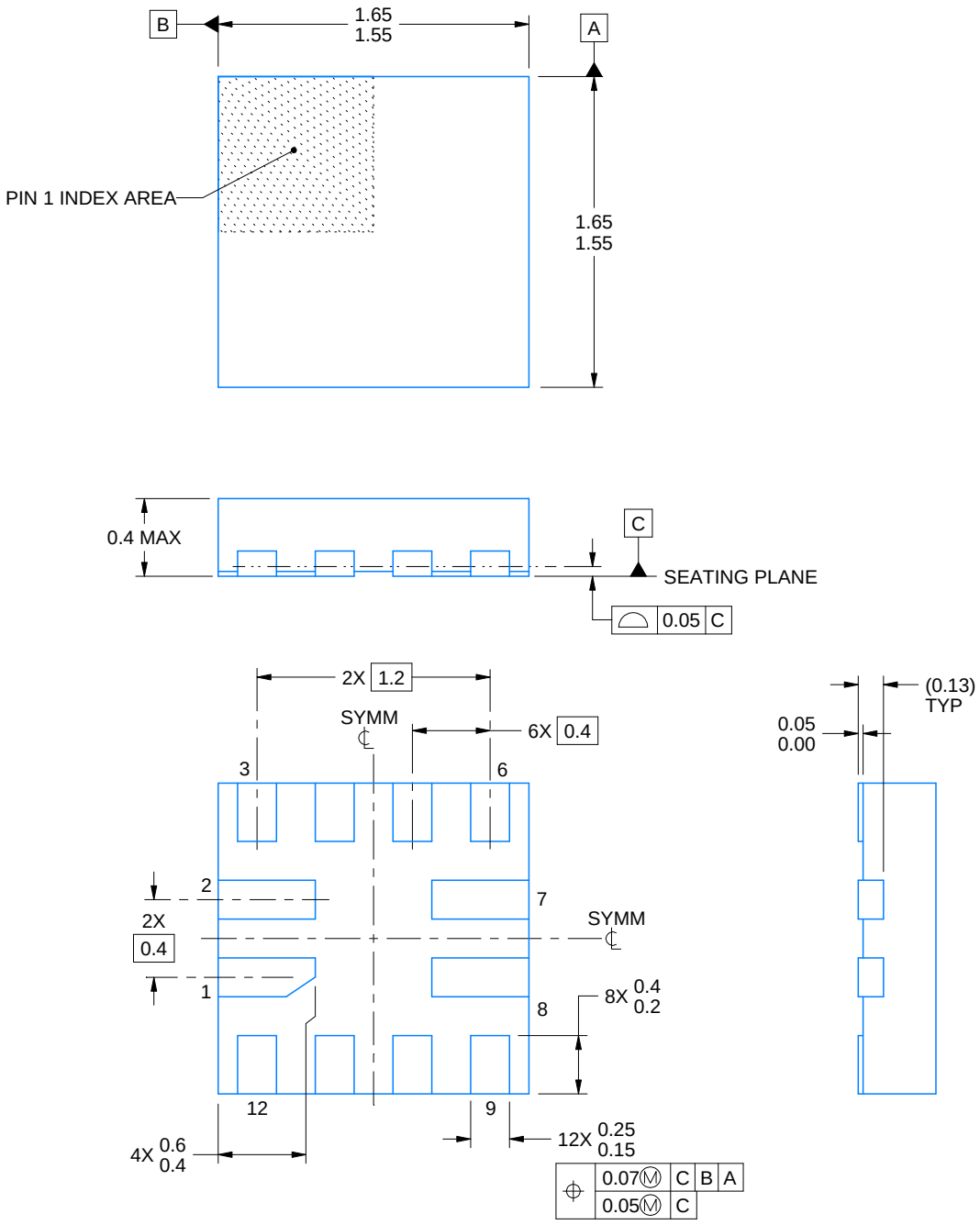
- Catalog - TI's standard catalog product

# PACKAGE OUTLINE

## RWB0012A

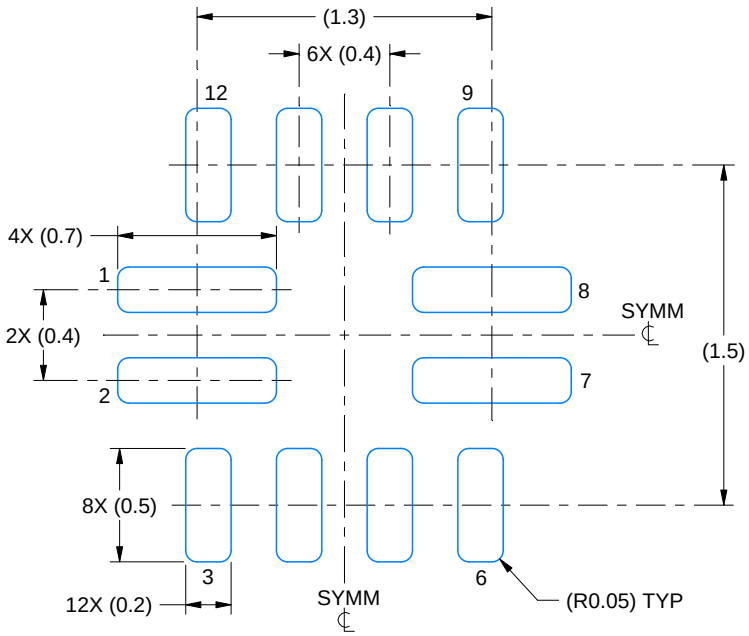
## X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

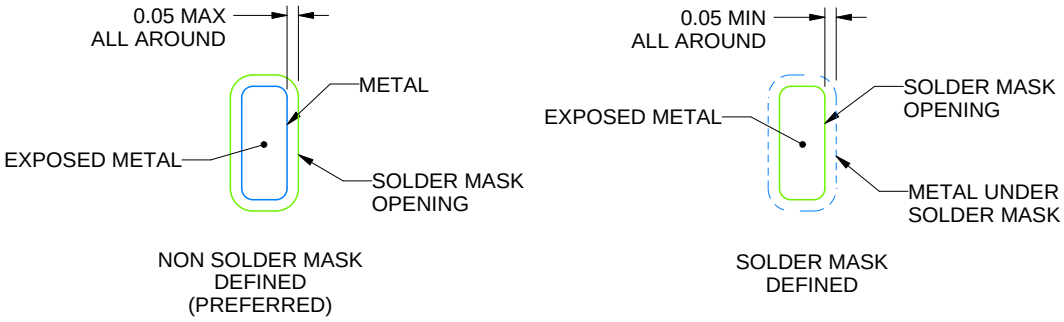



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X




SOLDER MASK DETAILS

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NOTES: (continued)

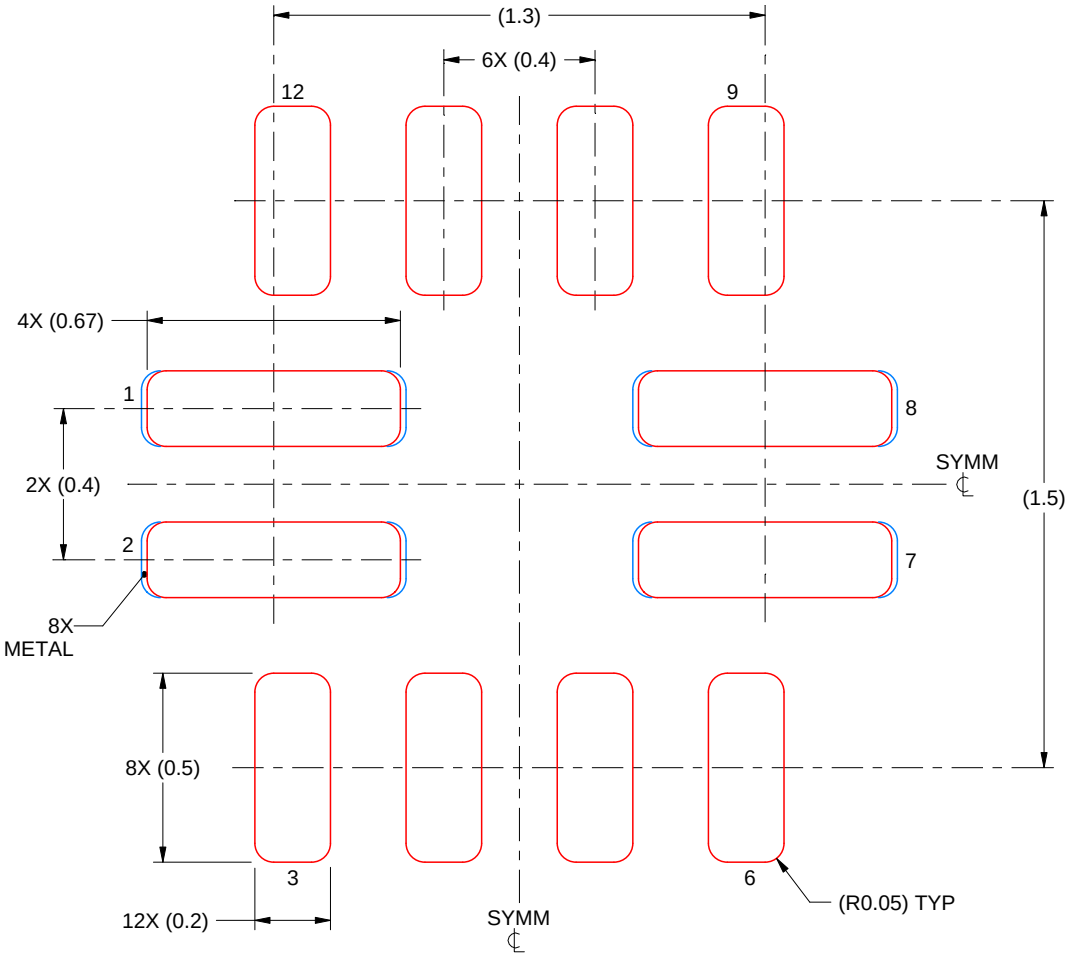
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

# EXAMPLE STENCIL DESIGN

## RWB0012A

## X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月