

UCC21732-Q1 アクティブ保護および絶縁アナログ センシング機能搭載、高 CMTI、車載用 10A ソース / シンク、SiC/IGBT 向け、強化絶縁シングル チャネル ゲート ドライバ

1 特長

- 5.7kV_{RMS} のシングル チャネル絶縁型ゲートドライバ
- 車載アプリケーション向けに AEC-Q100 認定済み
 - デバイス温度グレード 1: 動作時周囲温度範囲: -40°C ~ +125°C
 - デバイス HBM ESD 分類レベル 3A
 - デバイス CDM ESD 分類レベル C3
- 最高 2121V_{pk} の SiC MOSFET および IGBT
- 出力駆動電圧 (VDD-VEE): 33V (最大値)
- ±10A の駆動能力と分割出力
- 最小 CMTI: 150V/ns
- 270ns の応答時間による高速過電流保護
- 外部アクティブ ミラー クランプ
- フォルト発生時の内部 2 レベル ターンオフ
- PWM 出力を備えた絶縁アナログ センサで
 - NTC、PTC、サーマル ダイオードによる温度センシング
 - 高電圧 DC リンクまたは相電圧
- 過電流 FLT アラームと RST/EN からのリセット
- RST/EN での高速イネーブル / ディセーブル応答
- 入力ピンの 40ns 未満のノイズ過渡およびパルスを除く
- 12V VDD UVLO (RDY のパワー グッド付き)
- 最大 5V のオーバー/アンダー シュート過渡電圧に耐える入力/出力
- 伝搬遅延時間: 130ns (最大値)、パルス / 部品スキュー: 30ns (最大値)
- 沿面距離と空間距離が 8mm を超える SOIC-16 DW パッケージ
- 動作時の接合部温度: -40°C ~ 150°C
- 安全関連認証:
 - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁: 8000V_{PK} (V_{IOTM})、2121V_{PK} (V_{IORM})
 - UL 1577 に準拠した絶縁耐圧: 5700V_{RMS} (1 分間)

2 アプリケーション

- EV 用トラクション インバータ
- オンボード充電器と充電ステーション
- HEV/EV 用 DC/DC コンバータ

3 概要

UCC21732-Q1 は、先進の保護機能、クラス最高の動的性能、堅牢性を持ち合わせ、最高 2121V (DC) で動作する SiC MOSFET および IGBT 用に設計されたガルバニック絶縁型シングル チャネル ゲート ドライバです。UCC21732-Q1 は最大 ±10A のピーク 電流をソースおよびシンクできます。

入力側は SiO₂ 容量性絶縁技術によって出力側から絶縁されており、最大 1.5kV_{RMS} の動作電圧、絶縁バリア寿命が 40 年を超える 12.8kV_{PK} のサージ耐性を備えるとともに、小さい部品間スキューと 150V/ns を超える同相ノイズ耐性 (CMTI) を実現しています。

UCC21732-Q1 は、高速の過電流および短絡検出、シャント電流センシング、フォルト通知、アクティブ ミラー クランプ、入力側および出力側電源 UVLO などの最新の保護機能を備えているため、SiC および IGBT のスイッチング動作や堅牢性を最適化できます。アナログから PWM へ信号を変換する、この絶縁型センサは、温度または電圧のセンシングを簡単に行えるため、ドライバの汎用性をさらに高め、システムの設計工数、サイズ、およびコストを簡素化できます。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
UCC21732-Q1	DW (SOIC, 16)	10.3mm × 7.5mm

(1) 供給されているすべてのパッケージについては、[セクション 13](#) を参照してください。

デバイスのピン構成

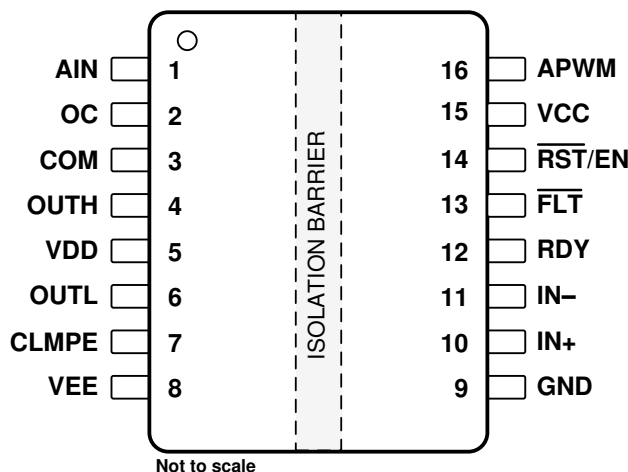


Table of Contents

1 特長	1	7 Detailed Description	23
2 アプリケーション	1	7.1 Overview.....	23
3 概要	1	7.2 Functional Block Diagram.....	24
4 Pin Configuration and Functions	3	7.3 Feature Description.....	24
5 Specifications	4	7.4 Device Functional Modes.....	31
5.1 Absolute Maximum Ratings.....	4	8 Applications and Implementation	32
5.2 ESD Ratings.....	4	8.1 Application Information.....	32
5.3 Recommended Operating Conditions.....	4	8.2 Typical Application.....	33
5.4 Thermal Information.....	5	9 Power Supply Recommendations	47
5.5 Power Ratings.....	5	10 Layout	48
5.6 Insulation Specifications.....	6	10.1 Layout Guidelines.....	48
5.7 Safety-Related Certifications.....	7	10.2 Layout Example.....	49
5.8 Safety Limiting Values.....	7	11 Device and Documentation Support	50
5.9 Electrical Characteristics.....	8	11.1 サード・パーティ製品に関する免責事項.....	50
5.10 Switching Characteristics.....	10	11.2 Documentation Support.....	50
5.11 Insulation Characteristics Curves.....	11	11.3 ドキュメントの更新通知を受け取る方法.....	50
5.12 Typical Characteristics.....	12	11.4 サポート・リソース.....	50
6 Parameter Measurement Information	16	11.5 Trademarks.....	50
6.1 Propagation Delay.....	16	11.6 静電気放電に関する注意事項.....	50
6.2 Input Deglitch Filter.....	18	11.7 用語集.....	50
6.3 Active Miller Clamp.....	19	12 Revision History	51
6.4 Under Voltage Lockout (UVLO).....	20	13 Mechanical, Packaging, and Orderable Information	51
6.5 OC (Over Current) Protection.....	22		

4 Pin Configuration and Functions

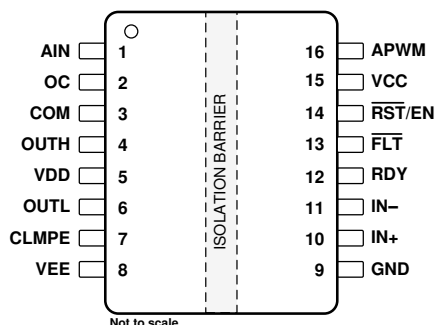


図 4-1. UCC21732-Q1 DW SOIC (16) Top View

表 4-1. Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
AIN	1	I	Isolated analog sensing input, parallel a small capacitor to COM for better noise immunity. Tie to COM if unused.
OC	2	I	Over current detection pin, support lower threshold for SenseFET, DESAT, and Shunt resistor sensing. Tie to COM if unused.
COM	3	P	Common ground reference, connecting to emitter pin for IGBT and source pin for SiC-MOSFET
OUTH	4	O	Gate driver output pull up
VDD	5	P	Positive supply rail for gate drive voltage, Bypassing a >10-μF capacitor to COM to support specified gate driver source peak current capability. Place decoupling capacitor close to the pin.
OUTL	6	O	Gate driver output pull down
CLMPE	7	O	External Active miller clamp, connecting this pin to the gate of the external miller clamp MOSFET. Leave floating if unused.
VEE	8	P	Negative supply rail for gate drive voltage. Bypassing a >10-μF capacitor to COM to support specified gate driver sink peak current capability. Place decoupling capacitor close to the pin.
GND	9	P	Input power supply and logic ground reference
IN+	10	I	Non-inverting gate driver control input. Tie to VCC if unused.
IN-	11	I	Inverting gate driver control input. Tie to GND if unused.
RDY	12	O	Power good for VCC-GND and VDD-COM. RDY is open drain configuration and can be paralleled with other RDY signals
FLT	13	O	Active low fault alarm output upon overcurrent or short circuit. FLT is in open drain configuration and can be paralleled with other faults
RST/EN	14	I	The RST/EN serves two purposes: 1) Enable / shutdown of the output side. The FET is turned off by a regular turn-off, if terminal EN is set to low; 2) Resets the OC condition signaled on FLT pin. if terminal RST/EN is set to low for more than 1000 ns. A reset of signal FLT is asserted at the rising edge of terminal RST/EN. For automatic RESET function, this pin only serves as an EN pin. Enable / shutdown of the output side. The FET is turned off by a general turn-off, if terminal EN is set to low.
VCC	15	P	Input power supply from 3 V to 5.5 V, bypassing a >1-μF capacitor to GND. Place decoupling capacitor close to the pin.
APWM	16	O	Isolated Analog Sensing PWM output. Leave floating if unused.

(1) P = Power, G = Ground, I = Input, O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		MIN	MAX	UNIT
VCC	VCC – GND	–0.3	6	V
VDD	VDD – COM	–0.3	36	V
VEE	VEE – COM	–17.5	0.3	V
V _{MAX}	VDD – VEE	–0.3	36	V
IN+, IN–, $\overline{\text{RST/EN}}$	DC	GND–0.3	VCC	V
	Transient, less than 100 ns ⁽²⁾	GND–5.0	VCC+5.0	V
AIN	Reference to COM	–0.3	5	V
OC	Reference to COM	–0.3	6	V
OUTH, OUTL	DC	VEE–0.3	VDD	V
	Transient, less than 100 ns ⁽²⁾	VEE–5.0	VDD+5.0	V
CLMPE	Reference to VEE	–0.3	5	V
RDY, FLT, APWM		GND–0.3	VCC	V
I _{FLT} , I _{RDY}	FLT, and RDY pin input current		20	mA
I _{APWM}	APWM pin output current		20	mA
T _J	Junction temperature range	–40	150	°C
T _{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Values are verified by characterization on bench.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±4000
		Charged-device model (CDM), per AEC Q100-011	±1500

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

PARAMETER		MIN	MAX	UNIT
VCC	VCC–GND	3.0	5.5	V
VDD	VDD–COM	13	33	V
V _{MAX}	VDD–VEE	–	33	V
IN+, IN–, $\overline{\text{RST/EN}}$	Reference to GND	High level input voltage	0.7×VCC	V
		Low level input voltage	0	0.3×VCC
AIN	Reference to COM	0.6	4.5	V
t _{RST/EN}	Minimum pulse width that reset the fault	1000		ns
T _A	Ambient Temperature	–40	125	°C
T _J	Junction temperature	–40	150	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UCC21732-Q1	UNIT
		DW (SOIC)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	68.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	27.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	32.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	14.1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	32.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P _D	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 150kHz, 50% Duty Cycle for 10nF load, T _a =25°C	985	mW
P _{D1}	Maximum power dissipation by transmitter side		20	mW
P _{D2}	Maximum power dissipation by receiver side		965	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage ⁽¹⁾	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (Internal clearance) of the double insulation (2 × 0.0085 mm)	> 17	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V _{PK}
V _{IOWM}	Maximum isolation working voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1500	V _{RMS}
		DC voltage	2121	V _{DC}
V _{IMP}	Maximum impulse voltage	Tested in air, 1.2/50-μs waveform per IEC 62368-1	8000	V _{PK}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} =V _{IOTM} , t = 60 s (qualification test)	8000	V _{PK}
		V _{TEST} =1.2 x V _{IOTM} , t = 1 s (100% production test)		
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 62368-1, 1.2/50 μs waveform	12800	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a: After I/O safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} = 2545 V _{PK} , t _m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.6 × V _{IORM} = 3394 V _{PK} , t _m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) V _{ini} = V _{IOTM} , t _{ini} = 1 s; V _{pd(m)} = 1.875 × V _{IORM} = 3977 V _{PK} , t _m = 1 s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.5 sin (2πft), f = 1 MHz	~ 1	pF
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V, T _A = 25°C	≥ 10 ¹²	Ω
		V _{IO} = 500 V, 100°C ≤ T _A ≤ 125°C	≥ 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	≥ 10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 5700 V _{RMS} , t = 60 s (qualification); V _{TEST} = 1.2 × V _{ISO} = 6840 V _{RMS} , t = 1 s (100% production)	5700	V _{RMS}

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
- (2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier tied together creating a two-terminal device

5.7 Safety-Related Certifications

VDE	UL
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Recognized under UL 1577 Component Recognition Program, CSA Component Acceptance Notice 5A
Reinforced insulation Maximum transient isolation voltage, 8000 V _{PK} ; Maximum repetitive peak isolation voltage, 2121 V _{PK} ; Maximum surge isolation voltage, 8000 V _{PK}	Single protection, 5700 V _{RMS}
Certificate number: 40040142	File Number: E181974

Safety limiting⁽¹⁾ intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

5.8 Safety Limiting Values

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _S Safety input, output, or supply current	R _{θJA} = 68.3°C/W, V _{DD} = 15V, V _{EE} = -5V, T _J = 150°C, T _A = 25°C			61	mA
	R _{θJA} = 68.3°C/W, V _{DD} = 20V, V _{EE} = -5V, T _J = 150°C, T _A = 25°C			49	
P _S Safety input, output, or total power	R _{θJA} = 68.3°C/W, V _{DD} = 20V, V _{EE} = -5V, T _J = 150°C, T _A = 25°C			1220	mW
T _S Safety temperature				150	°C

- (1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the [セクション 5.4](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance. These limits vary with the ambient temperature, the junction-to-air thermal resistance, and the power supply voltages in different applications.

5.9 Electrical Characteristics

VCC=3.3V or 5.0V, 1μF capacitor from VCC to GND, VDD–COM=20V, 18V or 15V, COM–VEE =0V, 5V, 8V or 15V, C_L=100pF, –40°C<T_J<150°C (unless otherwise noted)^{(1) (2)}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC UVLO THRESHOLD AND DELAY						
V _{VCC_ON}	VCC–GND		2.55	2.7	2.85	V
V _{VCC_OFF}			2.35	2.5	2.65	
V _{VCC_HYS}				0.2		
t _{VCCFIL}	VCC UVLO Deglitch time			10		μs
t _{VCC+ to OUT}	VCC UVLO on delay to output high	IN+ = VCC, IN– = GND	28	37.8	50	
t _{VCC– to OUT}	VCC UVLO off delay to output low		5	10	15	
t _{VCC+ to RDY}	VCC UVLO on delay to RDY high	RST/EN = VCC	30	37.8	50	
t _{VCC– to RDY}	VCC UVLO off delay to RDY low		5	10	15	
VDD UVLO THRESHOLD AND DELAY						
V _{VDD_ON}	VDD–COM		10.5	12.0	12.8	V
V _{VDD_OFF}			9.9	10.7	11.8	
V _{VDD_HYS}				0.8		
t _{VDDFIL}	VDD UVLO Deglitch time			5		μs
t _{VDD+ to OUT}	VDD UVLO on delay to output high	IN+ = VCC, IN– = GND	2	5	8	
t _{VDD– to OUT}	VDD UVLO off delay to output low			5	10	
t _{VDD+ to RDY}	VDD UVLO on delay to RDY high	RST/EN = FLT=High		10	15	
t _{VDD– to RDY}	VDD UVLO off delay to RDY low			10	15	
VCC, VDD QUIESCENT CURRENT						
I _{VCCQ}	VCC quiescent current	OUT(H) = High, f _S = 0Hz, AIN=2V	2.5	3	4	mA
		OUT(L) = Low, f _S = 0Hz, AIN=2V	1.45	2	2.75	
I _{VDDQ}	VDD quiescent current	OUT(H) = High, f _S = 0Hz, AIN=2V	3.6	4	5.9	mA
		OUT(L) = Low, f _S = 0Hz, AIN=2V	3.1	3.7	5.3	
LOGIC INPUTS — IN+, IN– and RST/EN						
V _{INH}	Input high threshold	V _{CC} =3.3V		1.85	2.31	V
V _{INL}	Input low threshold	V _{CC} =3.3V	0.99	1.52		V
V _{INHYS}	Input threshold hysteresis	V _{CC} =3.3V		0.33		V
I _{IH}	Input high level input leakage current	V _{IN} = VCC		90		μA
I _{IL}	Input low level input leakage	V _{IN} = GND		–90		μA
R _{IND}	Input pins pull down resistance	see セクション 7 for more information	28.5	55	113	kΩ
R _{INU}	Input pins pull up resistance	see セクション 7 for more information	28.5	55	113	
T _{INFIL}	IN+, IN– and RST/EN deglitch (ON and OFF) filter time	f _S = 50kHz	28	40	50	ns
T _{RSTFIL}	Deglitch filter time to reset /FLT		400	650	800	ns
GATE DRIVER STAGE						
I _{OUT} , I _{OUTH}	Peak source current	C _L =0.18μF, f _S =1kHz		10		A
I _{OUT} , I _{OUTL}	Peak sink current			10		A
R _{OUTH} ⁽³⁾	Output pull-up resistance	I _{OUT} = –0.1A	1.5	2.5	4.9	Ω
R _{OUTL}	Output pull-down resistance	I _{OUT} = 0.1A	0.1	0.3	0.7	Ω
V _{OUTH}	High level output voltage	I _{OUT} = –0.2A, V _{DD} =18V		17.5		V
V _{OUTL}	Low level output voltage	I _{OUT} = 0.2A		60		mV
ACTIVE PULLDOWN						
V _{OUTPD}	Output active pull down on OUTL	I _{OUTL} or I _{OUT} = 0.1×I _{OUT(L)(typ)} , VDD=OPEN, VEE=COM	1.5	2.0	2.5	V
EXTERNAL MILLER CLAMP						
V _{CLMPH}	Miller clamp threshold voltage	Reference to VEE	1.5	2.0	2.5	V
V _{CLMPE}	Output high voltage	Reference to VEE	4.8	5	5.3	V

5.9 Electrical Characteristics (続き)

VCC=3.3V or 5.0V, 1uF capacitor from VCC to GND, VDD-COM=20V, 18V or 15V, COM-VEE =0V, 5V, 8V or 15V, C_L=100pF, -40°C<T_J<150°C (unless otherwise noted)^{(1) (2)}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{CLMPEH}	Peak source current	C _{CLMPE} = 10nF ; ensured by design		0.25		A
I _{CLMPEL}	Peak sink current	C _{CLMPE} = 10nF	0.12	0.25	0.37	A
t _{CLMPER}	Rising time	C _{CLMPE} = 330pF		20	40	ns
t _{DCLMPE}	Miller clamp ON delay time			40	70	ns
SHORT CIRCUIT CLAMPING						
V _{CLP-OUT(H)}	V _{OUT} –VDD, V _{OUTH} –VDD	OUT = Low, I _{OUT(H)} = 500mA, t _{CLP} =10us		0.9		V
V _{CLP-OUT(L)}	V _{OUT} –VDD, V _{OUTL} –VDD	OUT = High, I _{OUT(L)} = 500mA, t _{CLP} =10us		1.8		V
OC PROTECTION						
I _{DCHG}	OC pull down current when	V _{OC} = 1V		40		mA
V _{OCTH}	Detection Threshold		0.63	0.7	0.77	V
V _{OCL}	Voltage when OUT(L) = LOW, Reference to COM	I _{OC} = 5mA		0.13		V
t _{OCFIL}	OC fault deglitch filter		95	120	180	ns
t _{OCOFF}	OC propagation delay to OUT(L) 90%		150	270	400	ns
t _{OCFLT}	OC to FLT low delay		300	530	750	ns
2-LEVEL TURNOFF (Triggered by OC)						
V _{2LOFF}	2LOFF voltage threshold		8.3	9.0	10.0	V
t _{2LOFF}	2LOFF voltage duration		500		1000	ns
I _{TL1}	High to 2-Level transition sink current			900		mA
I _{TL3}	Soft turn-off current on fault conditions	V _{DD} -V _{EE} =20V, V _{OUTL} -COM=8V	500	900	1200	mA
ISOLATED TEMPERATURE SENSE AND MONITOR (A _{IN} –A _{PWM})						
V _{A_{IN}}	Analog sensing voltage range		0.6		4.5	V
I _{A_{IN}}	Internal current source	V _{A_{IN}} =2.5V, -40°C< T _J < 150°C	196	203	209	μA
f _{A_{PWM}}	A _{PWM} output frequency	V _{A_{IN}} =2.5V	360	400	440	kHz
BW _{A_{IN}}	A _{IN} –A _{PWM} bandwidth			10		kHz
D _{A_{PWM}}	A _{PWM} Dutycycle	V _{A_{IN}} = 0.6V	85	88	91	%
		V _{A_{IN}} = 2.5V	47	50	53	
		V _{A_{IN}} = 4.5V	7	10	13	
FLT AND RDY REPORTING						
t _{RDYHLD}	VDD UVLO RDY low minimum holding time		0.55		1	ms
t _{FLTMUTE}	Output mute time on fault	Reset fault through $\overline{\text{RST}}/\text{EN}$	0.55		1	ms
R _{ODON}	Open drain output on resistance	I _{ODON} = 5mA		30		Ω
V _{ODL}	Open drain low output voltage	I _{ODON} = 5mA			0.3	V
COMMON MODE TRANSIENT IMMUNITY						
CMTI	Common-mode transient immunity	V _{CM} = 1500 V	150			V/ns

- (1) Current are positive into and negative out of the specified terminal.
(2) All voltages are referenced to COM unless otherwise notified.
(3) For internal PMOS only. Refer to [セクション 7.3](#) for effective pull-up resistance.

5.10 Switching Characteristics

VCC=5.0V, 1uF capacitor from VCC to GND, VDD–COM=20V, 18V or 15V, COM–VEE = 3V, 5V or 8V, C_L=100pF, –40°C<T_J<150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PDHL}	Propagation delay time – High to Low		60	90	130	ns
t _{PDLH}	Propagation delay time – Low to High		60	90	130	
PWD	Pulse width distortion t _{PDHL} – t _{PDLH}				30	
t _{sk-pp}	Part to Part skew	Rising or Falling Propagation Delay			30	
t _r	Driver output rise time	C _L =10nF		33		
t _f	Driver output fall time	C _L =10nF		27		
f _{MAX}	Maximum switching frequency				1	MHz

5.11 Insulation Characteristics Curves

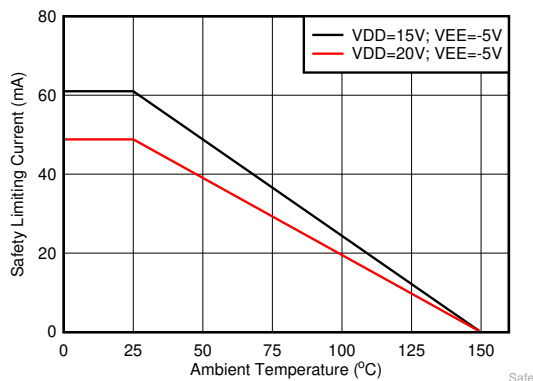


Figure 5-1. Thermal Derating Curve for Limiting Current per VDE

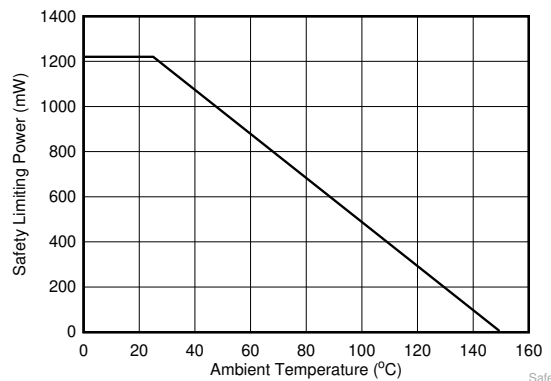


Figure 5-2. Thermal Derating Curve for Limiting Power per VDE

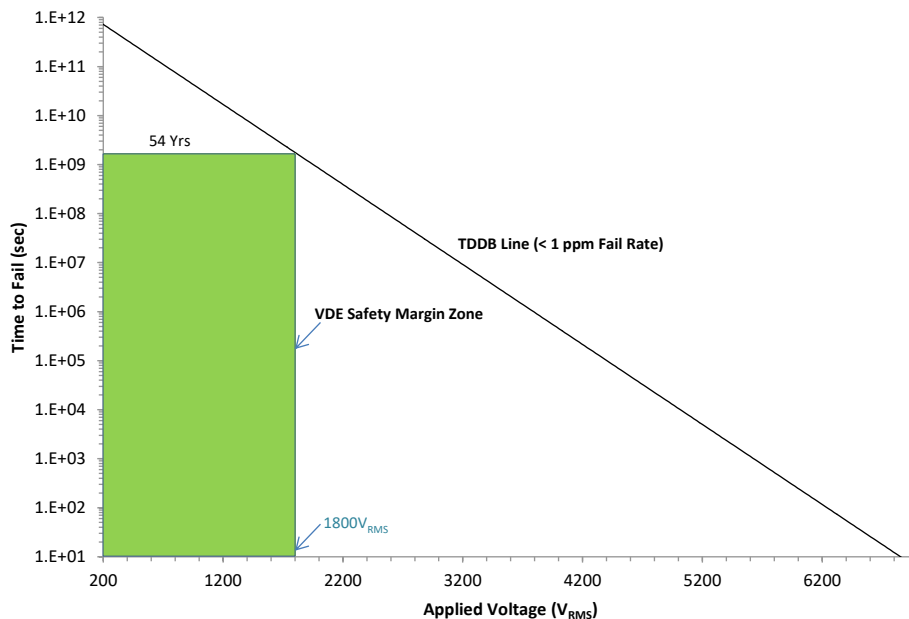


Figure 5-3. Reinforced Isolation Capacitor Life Time Projection

5.12 Typical Characteristics

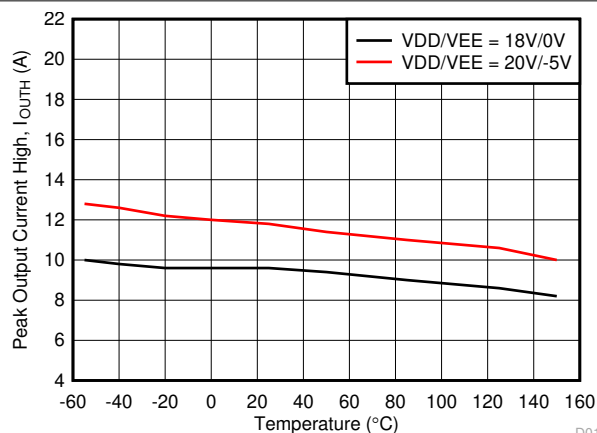


図 5-4. Output High Drive Current vs Temperature

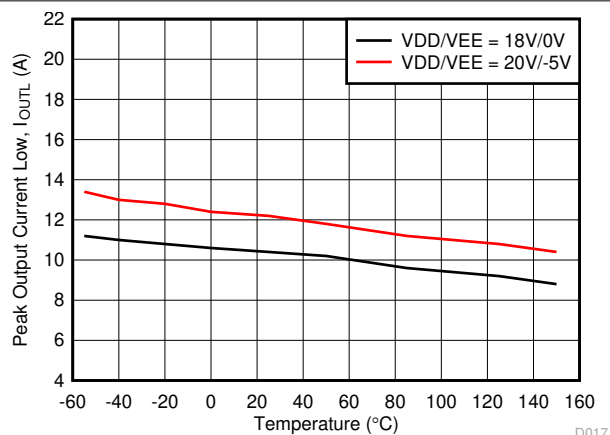


図 5-5. Output Low Driver Current vs Temperature

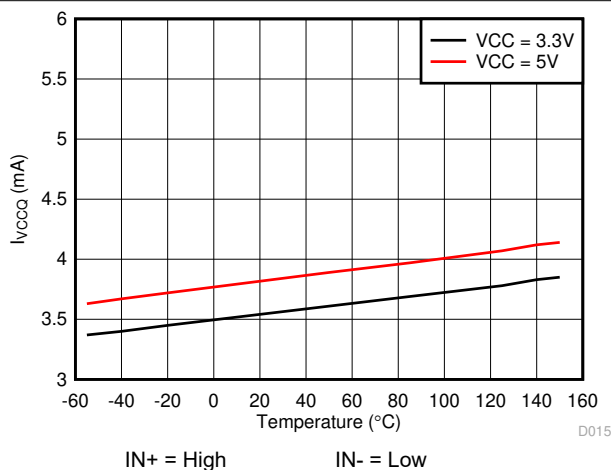


図 5-6. I_{VCCQ} Supply Current vs Temperature

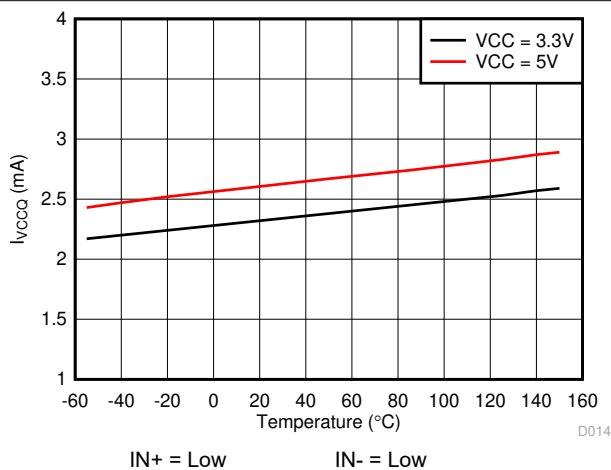


図 5-7. I_{VCCQ} Supply Current vs Temperature

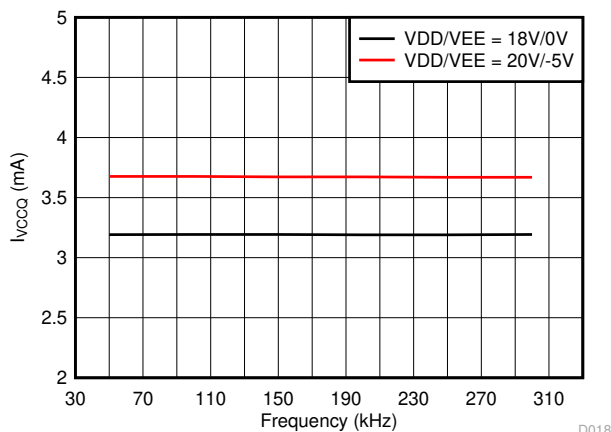


図 5-8. I_{VCCQ} Supply Current vs Input Frequency

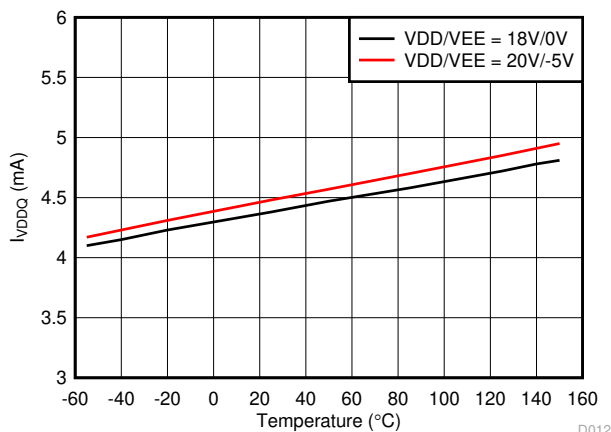


図 5-9. I_{VDDQ} Supply Current vs Temperature

5.12 Typical Characteristics (continued)

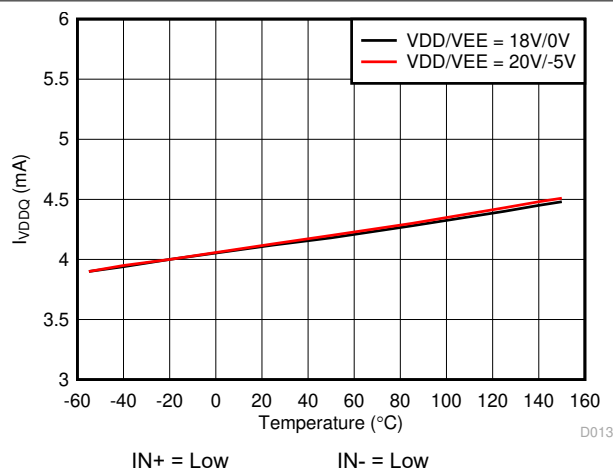


図 5-10. I_{VDDQ} Supply Current vs Temperature

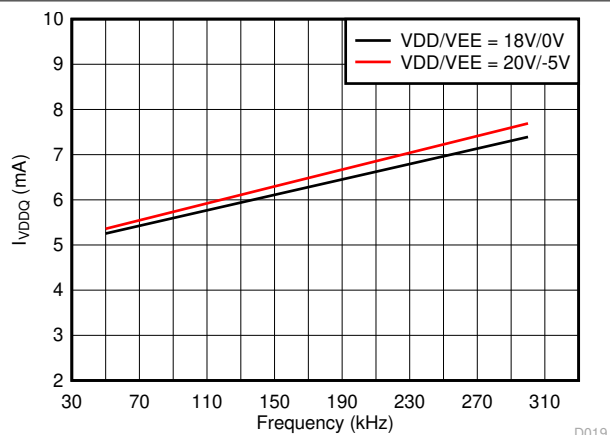


図 5-11. I_{VDDQ} Supply Current vs Input Frequency

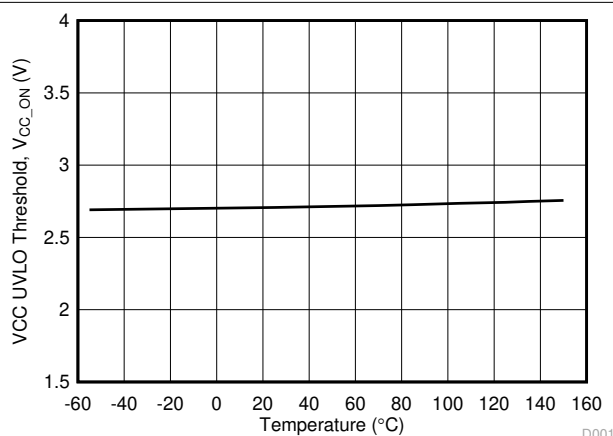


図 5-12. VCC UVLO vs Temperature

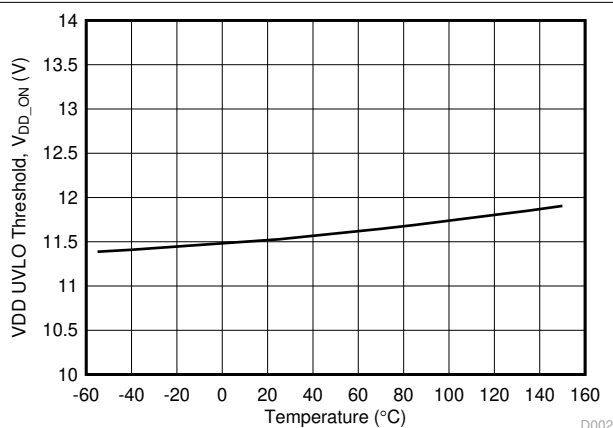


図 5-13. VDD UVLO vs Temperature

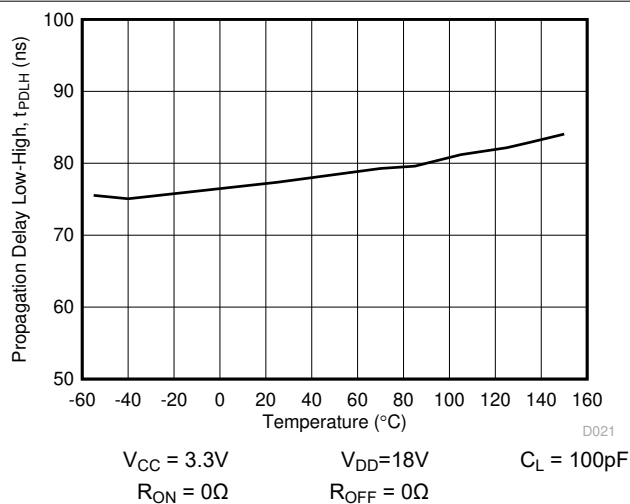


図 5-14. Propagation Delay t_{PDLH} vs Temperature

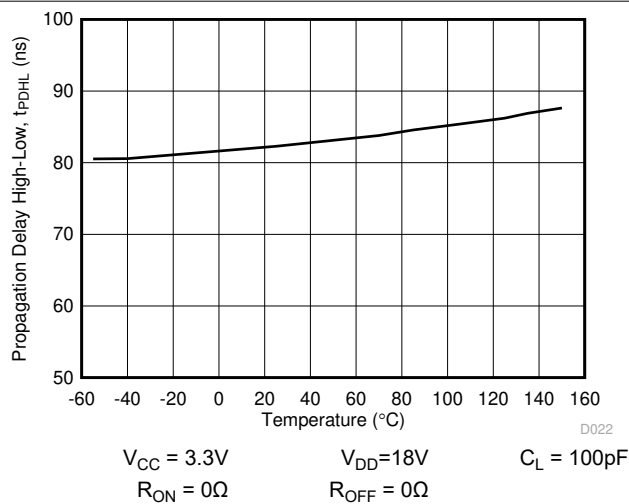


図 5-15. Propagation Delay t_{PDHL} vs Temperature

5.12 Typical Characteristics (continued)

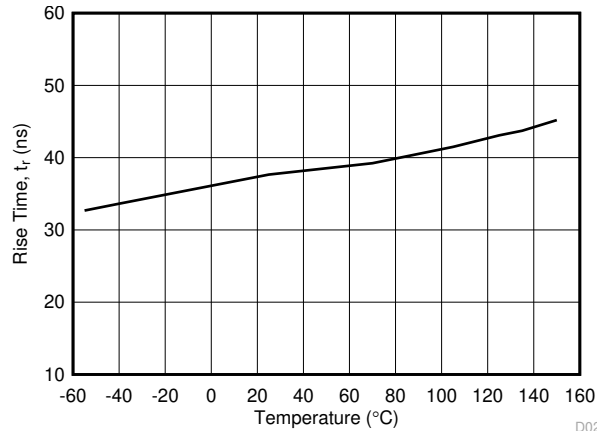


图 5-16. t_r Rise Time vs Temperature

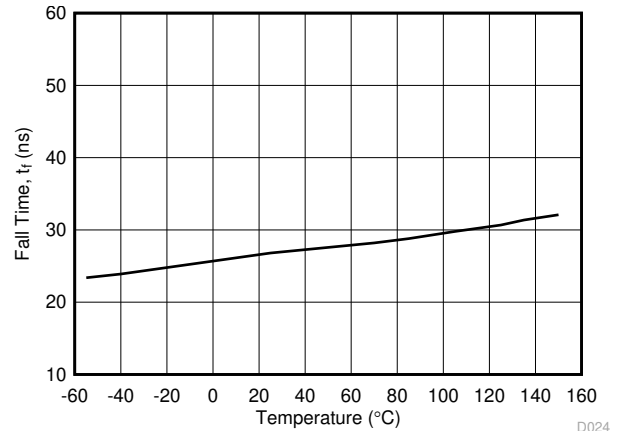


图 5-17. t_f Fall Time vs Temperature

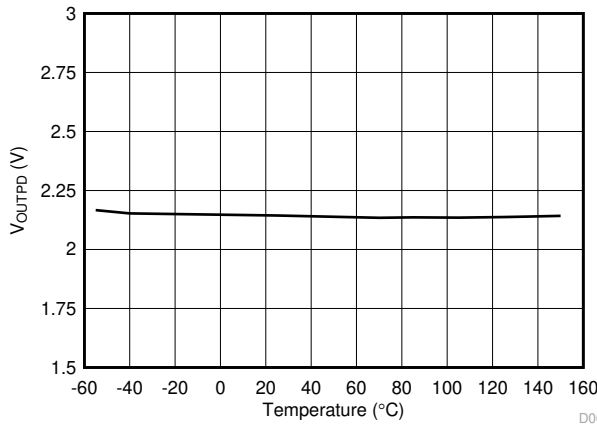


图 5-18. V_{OUTPD} Output Active Pulldown Voltage vs Temperature

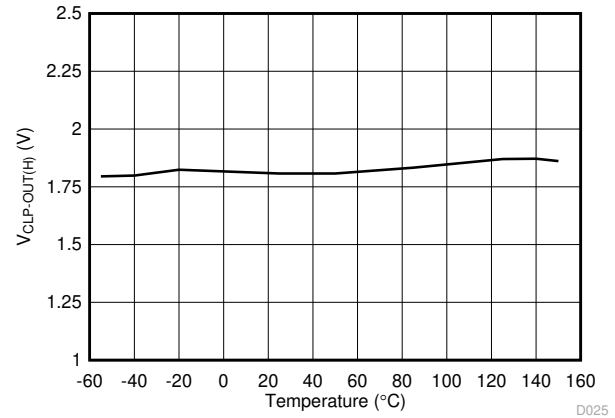


图 5-19. $V_{CLP-OUT(H)}$ Short Circuit Clamping Voltage vs Temperature

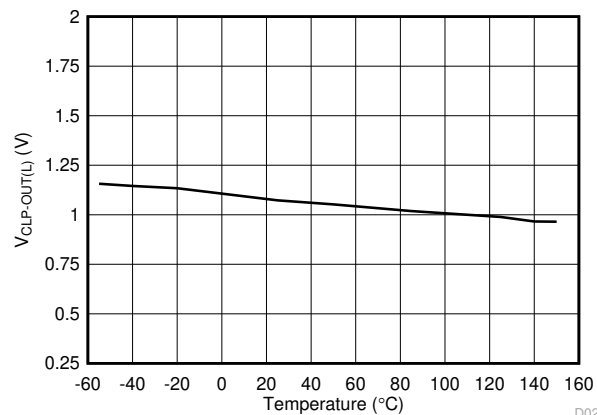


图 5-20. $V_{CLP-OUT(L)}$ Short Circuit Clamping Voltage vs Temperature

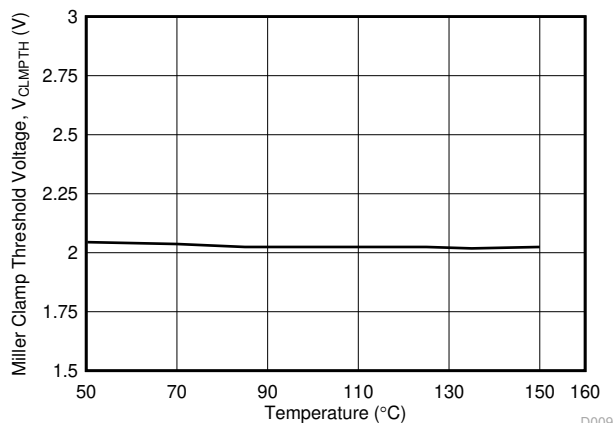


图 5-21. V_{CLMPH} Miller Clamp Threshold Voltage vs Temperature

5.12 Typical Characteristics (continued)

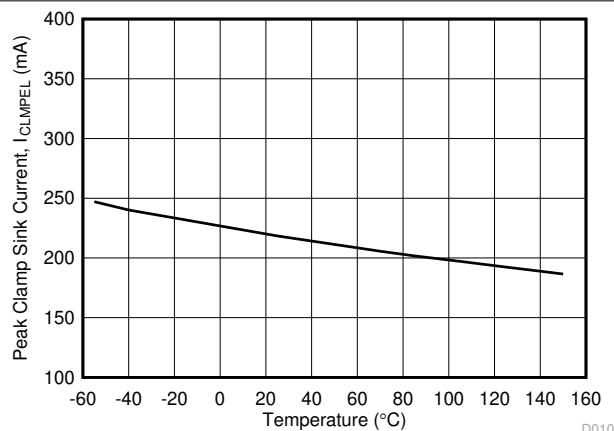


FIG 5-22. I_{CLMPEL} Miller Clamp Sink Current vs Temperature

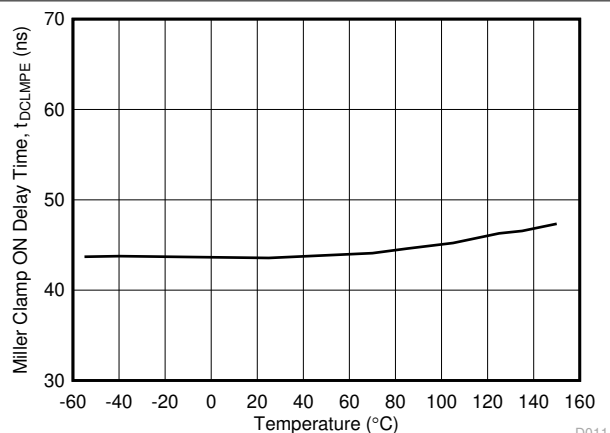


FIG 5-23. t_{DCLMPE} Miller Clamp ON Delay Time vs Temperature

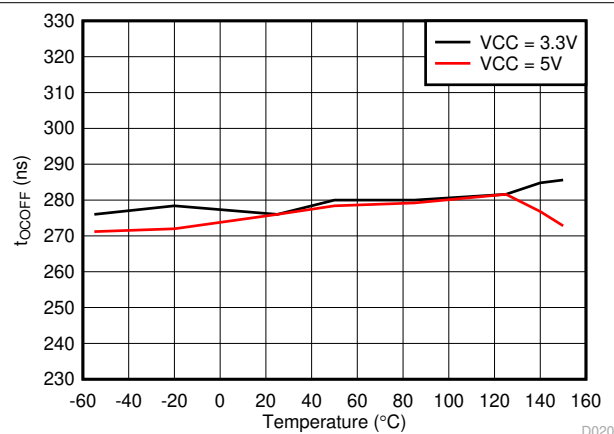


FIG 5-24. t_{OCOFF} OC Propagation Delay vs Temperature

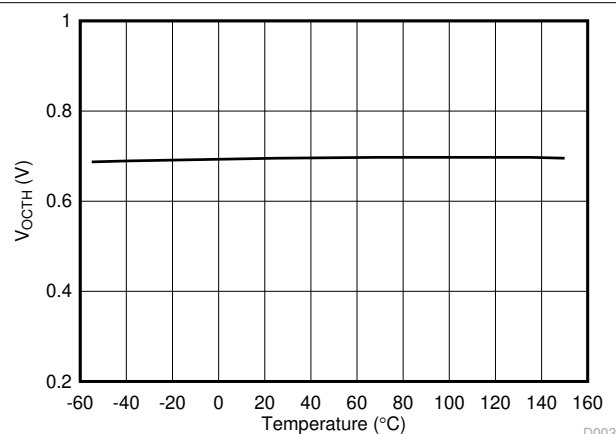


FIG 5-25. V_{OCTH} OC Detection Threshold vs Temperature

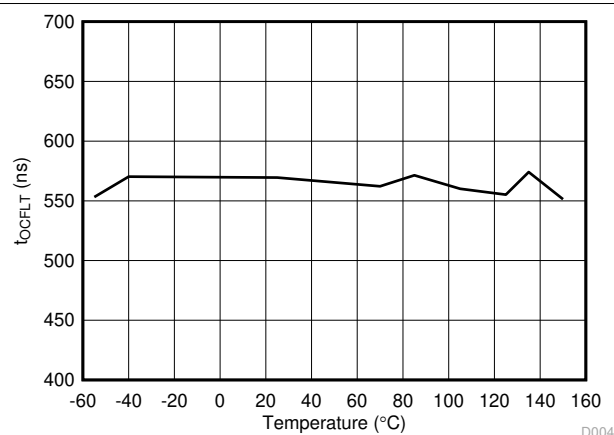


FIG 5-26. t_{OCFLT} OC to FLT Low Delay Time vs Temperature

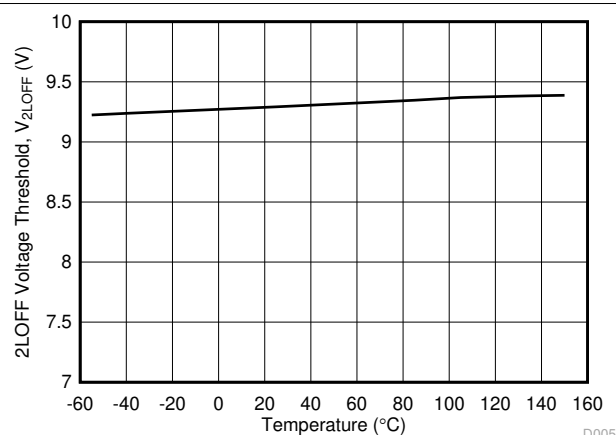


FIG 5-27. V_{2LOFF} 2-Level Turn Off Voltage Threshold vs Temperature

5.12 Typical Characteristics (continued)

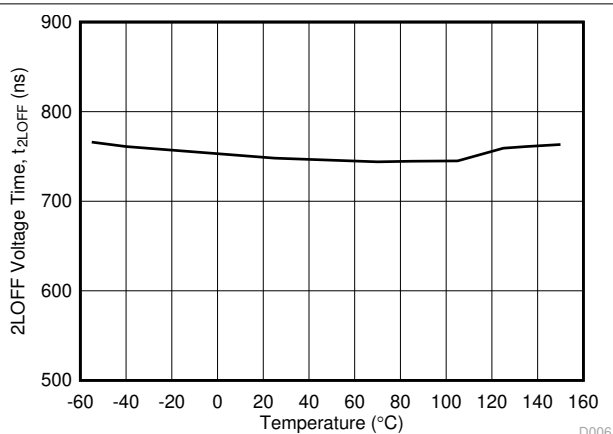


图 5-28. t_{2LOFF} 2-Level Turn Off Time vs Temperature

6 Parameter Measurement Information

6.1 Propagation Delay

6.1.1 Regular Turn-OFF

图 6-1 shows the propagation delay measurement for non-inverting configurations. 图 6-2 shows the propagation delay measurement with the inverting configurations.

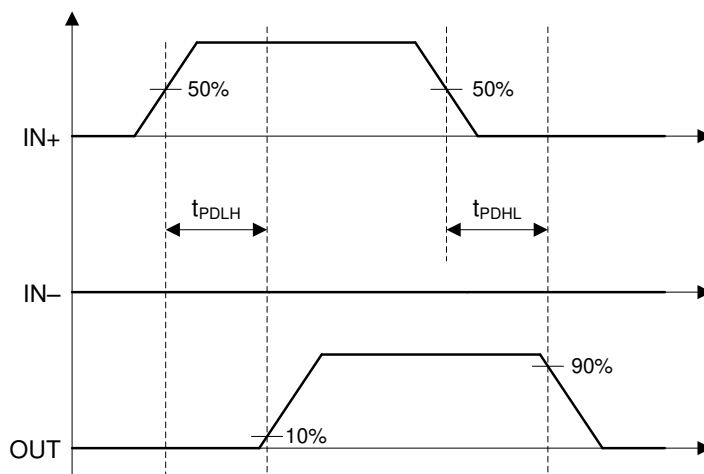


图 6-1. Non-inverting Logic Propagation Delay Measurement

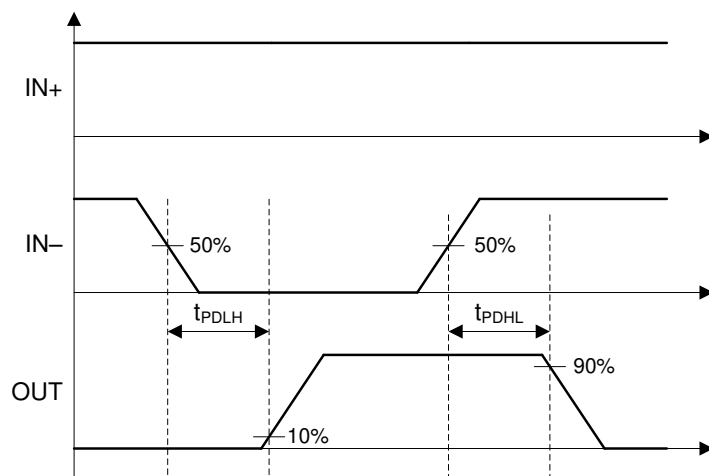


図 6-2. Inverting Logic Propagation Delay Measurement

6.2 Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, for example IN+, IN–, $\overline{\text{RST/EN}}$, a 40-ns deglitch filter is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN– PWM pulse is smaller than the input deglitch filter width, T_{INFIL} , there will be no responses on OUT drive signal. 図 6-3 and 図 6-4 shows the IN+ pin ON and OFF pulse deglitch filter effect. 図 6-5 and 図 6-6 shows the IN– pin ON and OFF pulse deglitch filter effect.

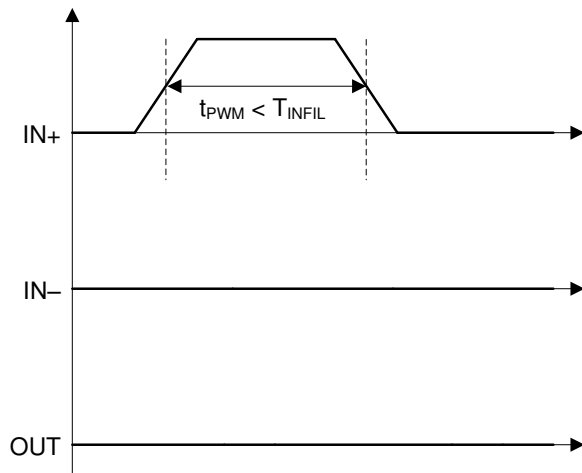


図 6-3. IN+ ON Deglitch Filter

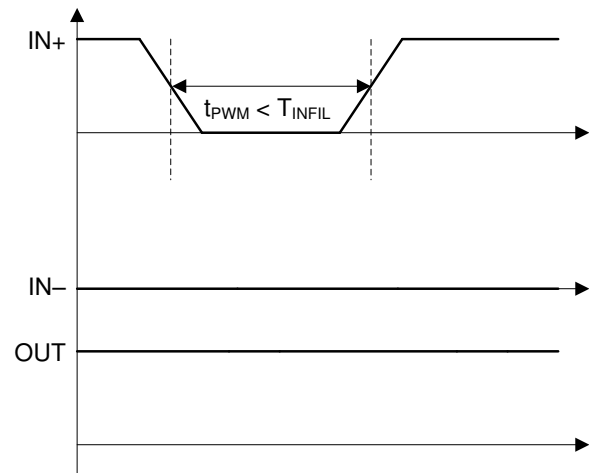


図 6-4. IN+ OFF Deglitch Filter

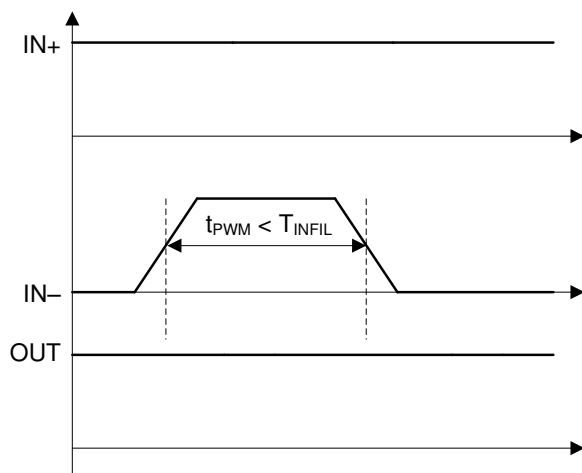


図 6-5. IN– ON Deglitch Filter

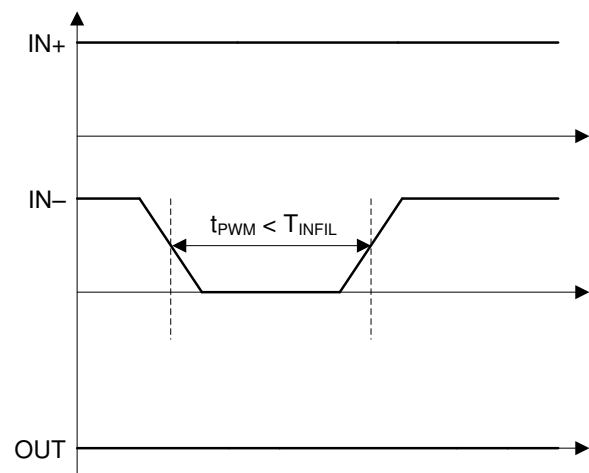
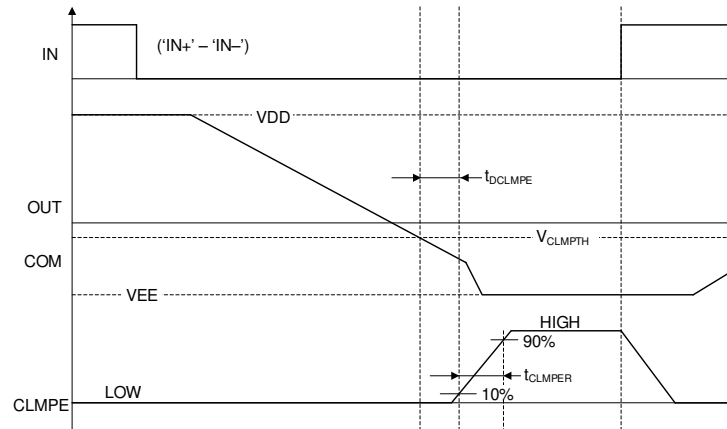


図 6-6. IN– OFF Deglitch Filter

6.3 Active Miller Clamp

6.3.1 External Active Miller Clamp

For gate driver application with unipolar bias supply or bipolar supply with small negative turn-off voltage, active miller clamp can help add an additional low impedance path to bypass the miller current and prevent the high dV/dt introduced unintentional turn-on through the miller capacitance. Different from the internal active miller clamp, external active miller clamp function is used for applications where the gate driver may not be close to the power device or power module due to system layout considerations. External active miller clamp function provide a 5-V gate drive signal to turn-on the external miller clamp FET when the gate driver voltage is less than miller clamp threshold, V_{CLMPH} . 6-7 shows the timing diagram for external active miller clamp function.



6-7. Timing Diagram for External Active Miller Clamp Function

6.4 Under Voltage Lockout (UVLO)

UVLO is one of the key protection features designed to protect the system in case of bias supply failures on VCC — primary side power supply, and VDD — secondary side power supply.

6.4.1 VCC UVLO

The VCC UVLO protection details are discussed in this section. [Figure 6-8](#) shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

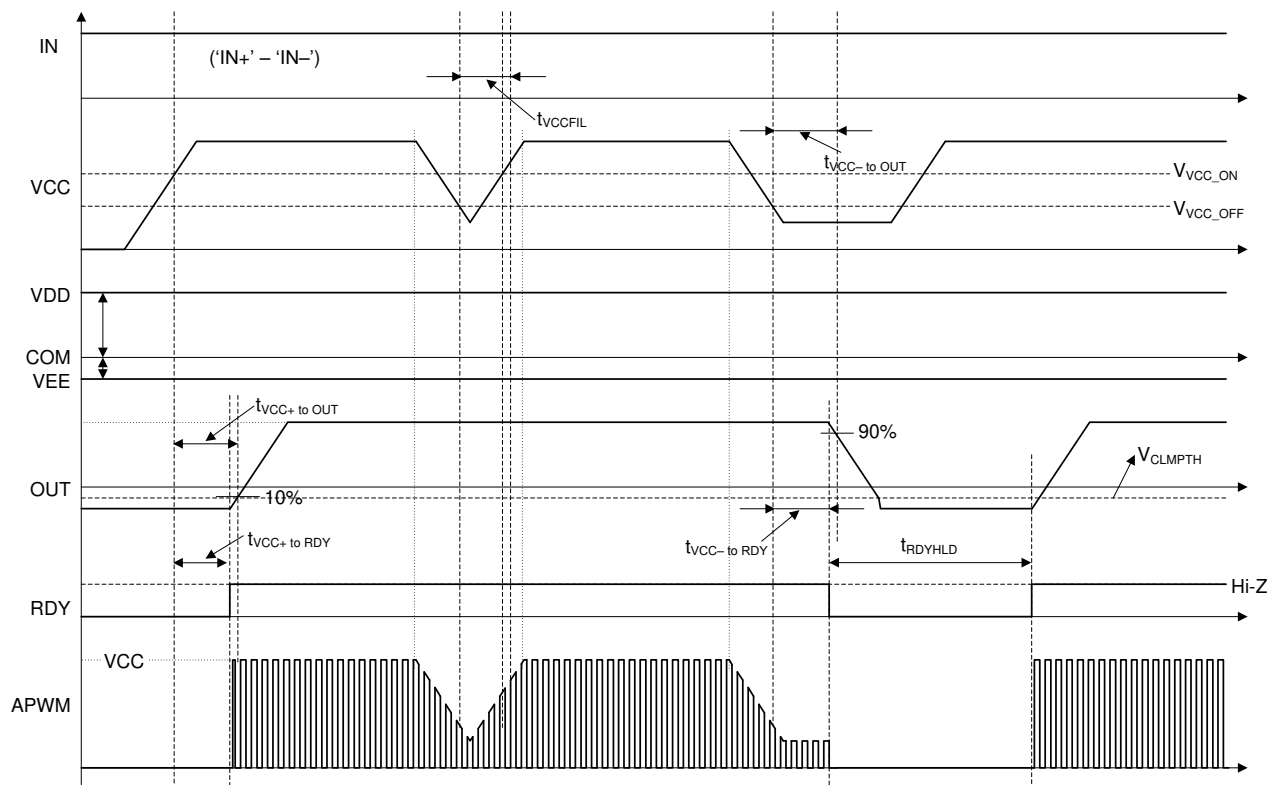


Figure 6-8. VCC UVLO Protection Timing Diagram

6.4.2 VDD UVLO

The VDD UVLO protection details are discussed in this section. 図 6-9 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN-APWM.

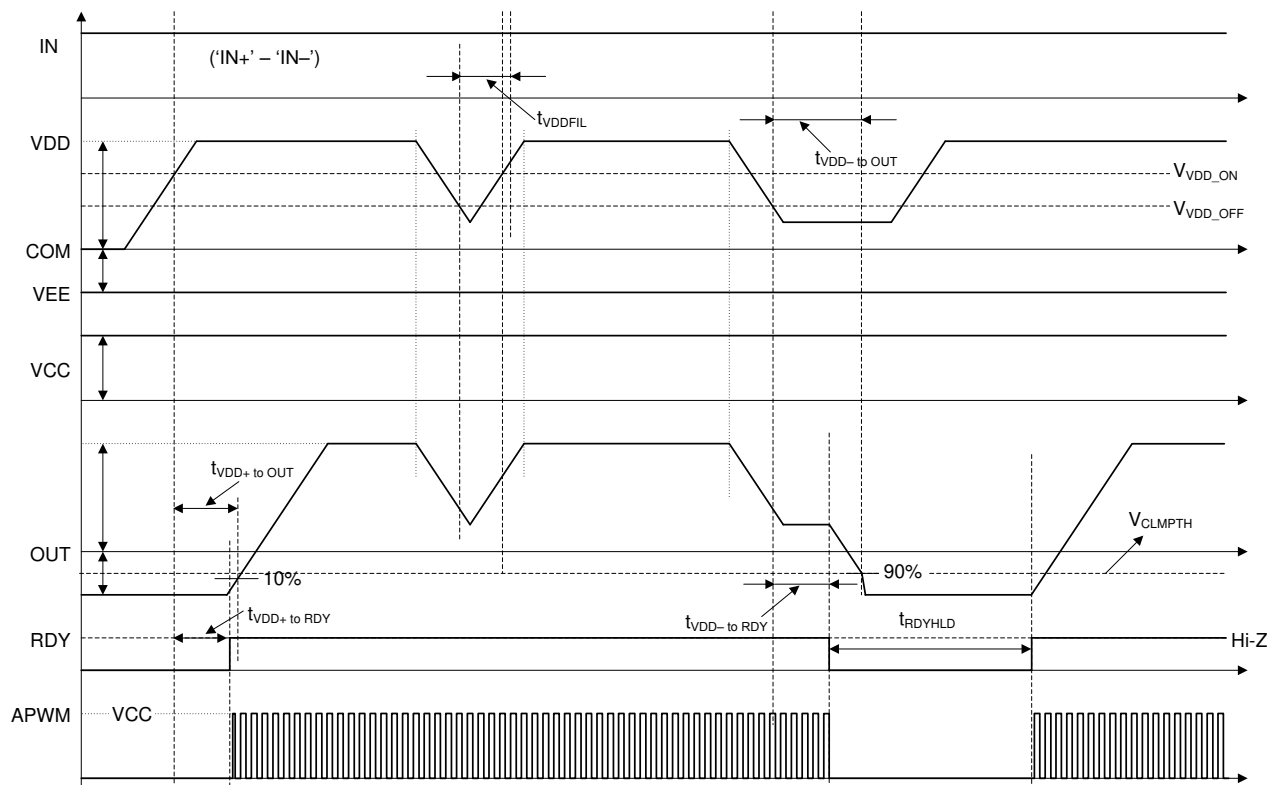


図 6-9. VDD UVLO Protection Timing Diagram

6.5 OC (Over Current) Protection

6.5.1 OC Protection with 2-Level Turn-OFF

OC Protection is used to sense the current of SiC-MOSFETs and IGBTs under over current or shoot-through condition. 図 6-10 shows the timing diagram of OC operation with 2-level turn-off.

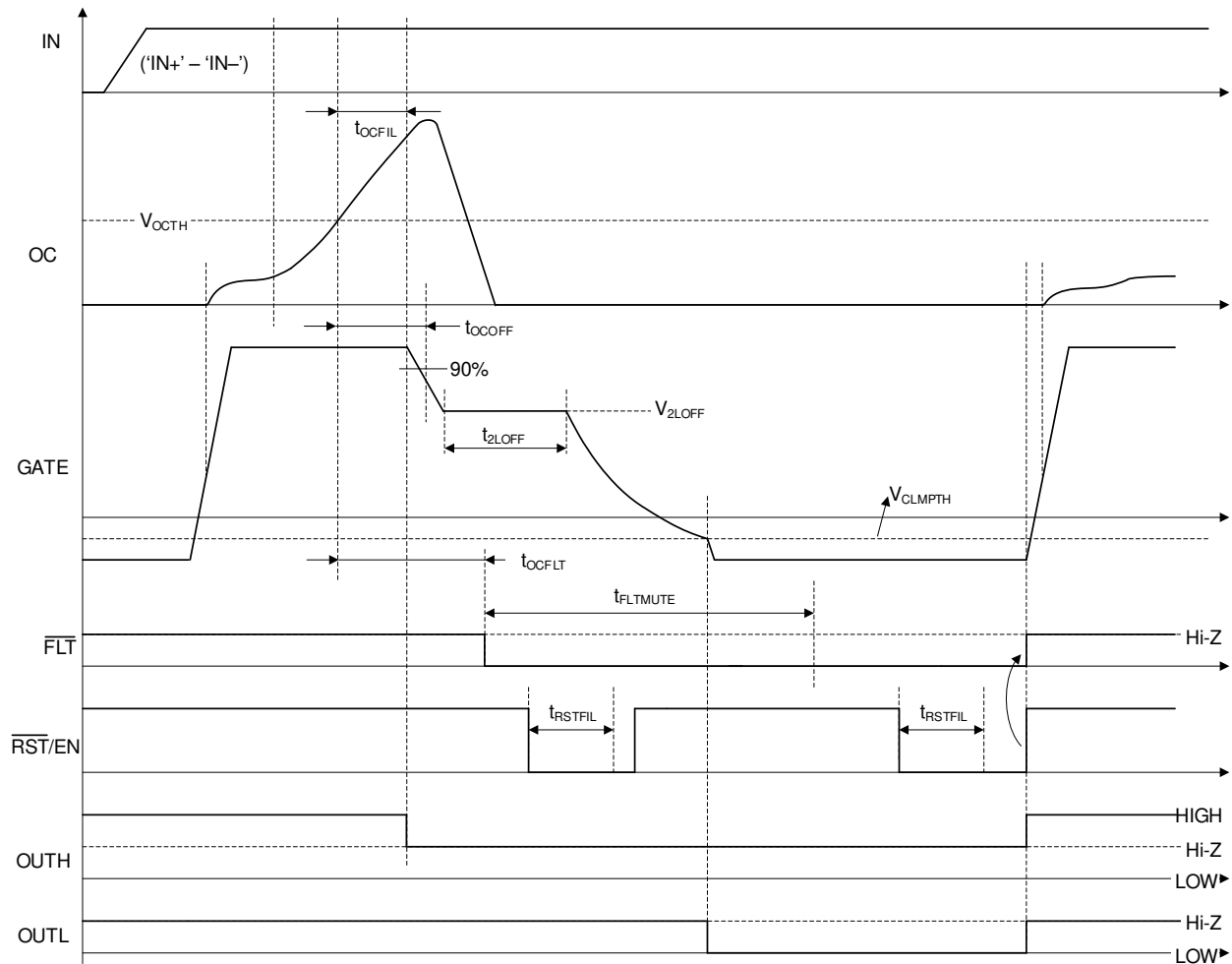


図 6-10. OC Protection with 2-Level Turn-OFF

7 Detailed Description

7.1 Overview

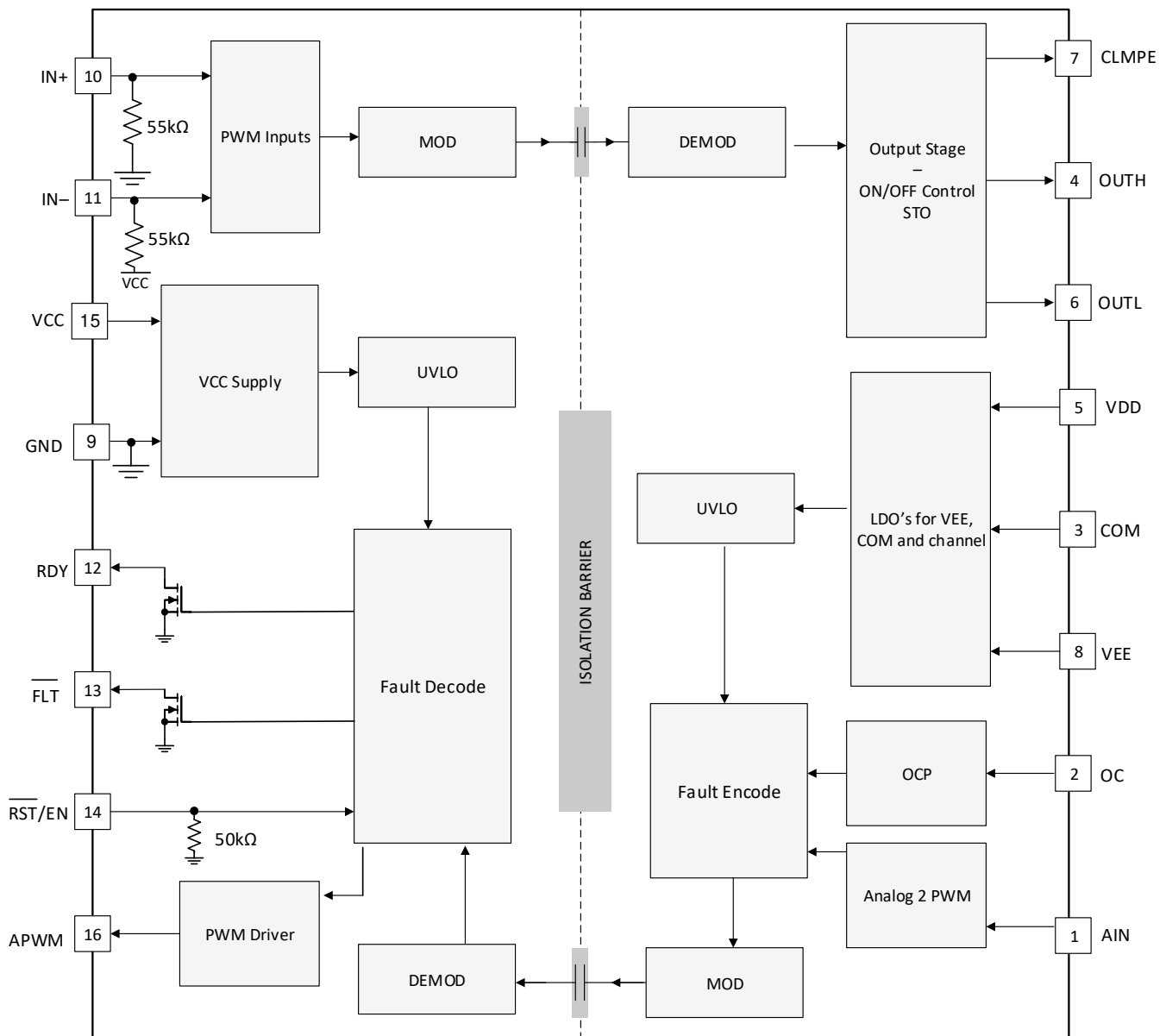
The UCC21732-Q1 device is an advanced isolated gate driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device can support up to 2121V DC operating voltage based on SiC MOSFETs and IGBTs, and can be used to above 10-kW applications such as HEV/EV traction inverter, motor drive, on-board and off-board battery charger, solar inverter, etc. The galvanic isolation is implemented by the capacitive isolation technology, which can realize a reliable reinforced isolation between the low voltage DSP/MCU and high voltage side.

The ± 10 -A peak sink and source current of UCC21732-Q1 can drive the SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with external buffer stage. The input side is isolated with the output side with a reinforced isolation barrier based on capacitive isolation technology. The device can support up to 1.5-kV_{RMS} working voltage, 12.8-kV_{PK} surge immunity with longer than 40 years isolation barrier life. The strong drive strength helps to switch the device fast and reduce the switching loss. While the 150-V/ns minimum CMTI ensures the reliability of the system with fast switching speed. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitor features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. The 12-V output side power supply UVLO is suitable for switches with gate voltage ≥ 15 V. The active miller clamp feature prevents the false turn on causing by miller capacitance during fast switching. External miller clamp FET can be used, providing more versatility to the system design. The device has the state-of-art overcurrent and short circuit detection time, and fault reporting function to the low voltage side DSP/MCU. The 2-level turn-off with soft turn off is triggered when the overcurrent or short circuit fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches.

The isolated analog to PWM sensor can be used as switch temperature sensing, DC bus voltage sensing, auxiliary power supply sensing, and so forth. The PWM signal can be fed directly to DSP/MCU or through a low-pass filter as an analog signal.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supply

The input side power supply VCC can support a wide voltage range from 3 V to 5.5 V. The device supports both unipolar and bipolar power supply on the output side, with a wide range from 13 V to 33 V from VDD to VEE. The negative power supply with respect to switch source or emitter is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. The negative voltage is especially important for SiC MOSFET due to its fast switching speed.

7.3.2 Driver Stage

UCC21732-Q1 has ± 10 -A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. UCC21732-Q1 can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 10 A. The driver features an

important safety function wherein, when the input pins are in floating condition, the OUTH/OUTL is held in LOW state. The split output of the driver stage is depicted in . The driver has rail-to-rail output by implementing a hybrid pull-up structure with a P-Channel MOSFET in parallel with an N-Channel MOSFET, and an N-Channel MOSFET to pulldown. The pull-up NMOS is the same as the pull down NMOS, so the on resistance R_{NMOS} is the same as R_{OL} . The hybrid pull-up structure delivers the highest peak-source current when it is most needed, during the miller plateau region of the power semiconductor turn-on transient. The R_{OH} in represents the on-resistance of the pull-up P-Channel MOSFET. However, the effective pull-up resistance is much smaller than R_{OH} . Since the pull-up N-Channel MOSFET has much smaller on-resistance than the P-Channel MOSFET, the pull-up N-Channel MOSFET dominates most of the turn-on transient, until the voltage on OUTH pin is about 3V below VDD voltage. The effective resistance of the hybrid pull-up structure during this period is about $2 \times R_{OL}$. Then the P-Channel MOSFET pulls up the OUTH voltage to VDD rail. The low pull-up impedance results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

The pull-down structure of the driver stage is implemented solely by a pull-down N-Channel MOSFET. This MOSFET can ensure the OUTL voltage be pulled down to VEE rail. The low pull-down impedance not only results in high sink current to reduce the turn-off time, but also helps to increase the noise immunity considering the miller effect.

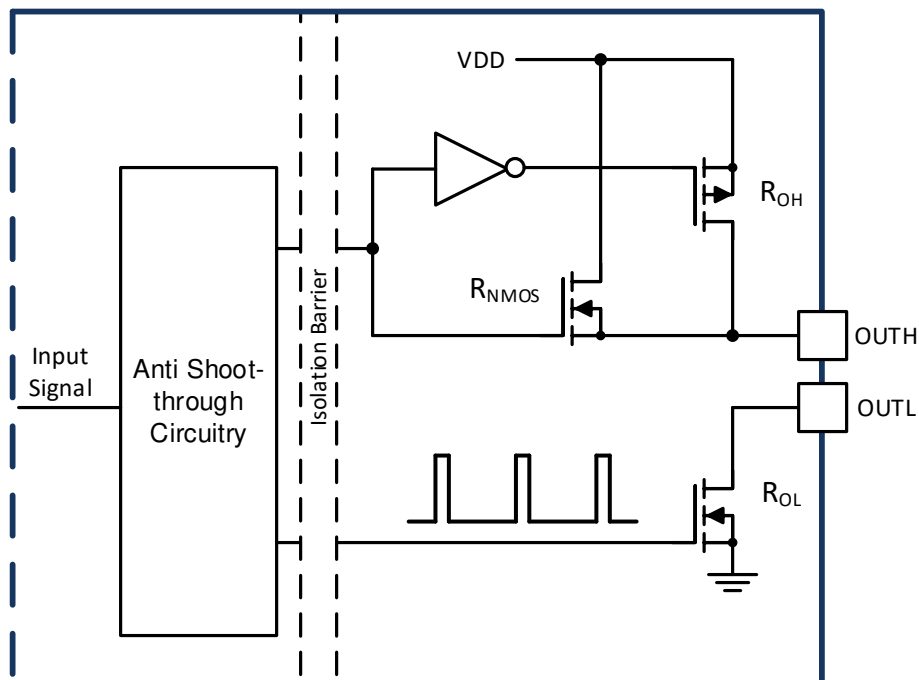


図 7-1. Gate Driver Output Stage

7.3.3 VCC and VDD Undervoltage Lockout (UVLO)

UCC21732-Q1 implements the internal UVLO protection feature for both input and output power supplies VCC and VDD. When the supply voltage is lower than the threshold voltage, the driver output is held as LOW. The output only goes HIGH when both VCC and VDD are out of the UVLO status. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. For SiC MOSFET and IGBT, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage. UCC21732-Q1 implements 12-V threshold voltage of VDD UVLO, with 800-mV hysteresis. This threshold voltage is suitable for both SiC MOSFET and IGBT.

The UVLO protection block features with hysteresis and deglitch filter, which help to improve the noise immunity of the power supply. During the turn on and turn off switching transient, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filter, the internal UVLO protection block will ignore small noises during the normal switching transients.

The timing diagrams of the UVLO feature of VCC and VDD are shown in [Figure 6-8](#), and [Figure 6-9](#). The RDY pin on the input side is used to indicate the power good condition. The RDY pin is open drain. During UVLO condition, the RDY pin is held in low status and connected to GND. Normally the pin is pulled up externally to VCC to indicate the power good. The AIN-APWM function stops working during the UVLO status. The APWM pin on the input side will be held LOW.

7.3.4 Active Pulldown

UCC21732-Q1 implements an active pulldown feature to ensure the OUTH/OUTL pin clamping to VEE when the VDD is open. The OUTH/OUTL pin is in high-impedance status when VDD is open, the active pulldown feature can prevent the output be false turned on before the device is back to control.

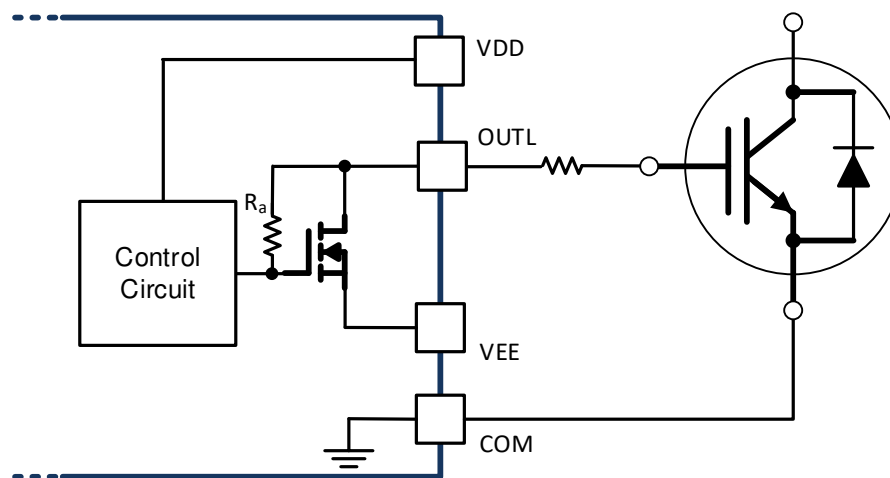


Figure 7-2. Active Pulldown

7.3.5 Short Circuit Clamping

During short circuit condition, the miller capacitance can cause a current sinking to the OUTH/OUTL pin due to the high dV/dt and boost the OUTH/OUTL voltage. The short circuit clamping feature of UCC21732-Q1 can clamp the OUTH/OUTL pin voltage to be slightly higher than VDD, which can protect the power semiconductors from a gate-source and gate-emitter overvoltage breakdown. This feature is realized by an internal diode from the OUTH/OUTL to VDD.

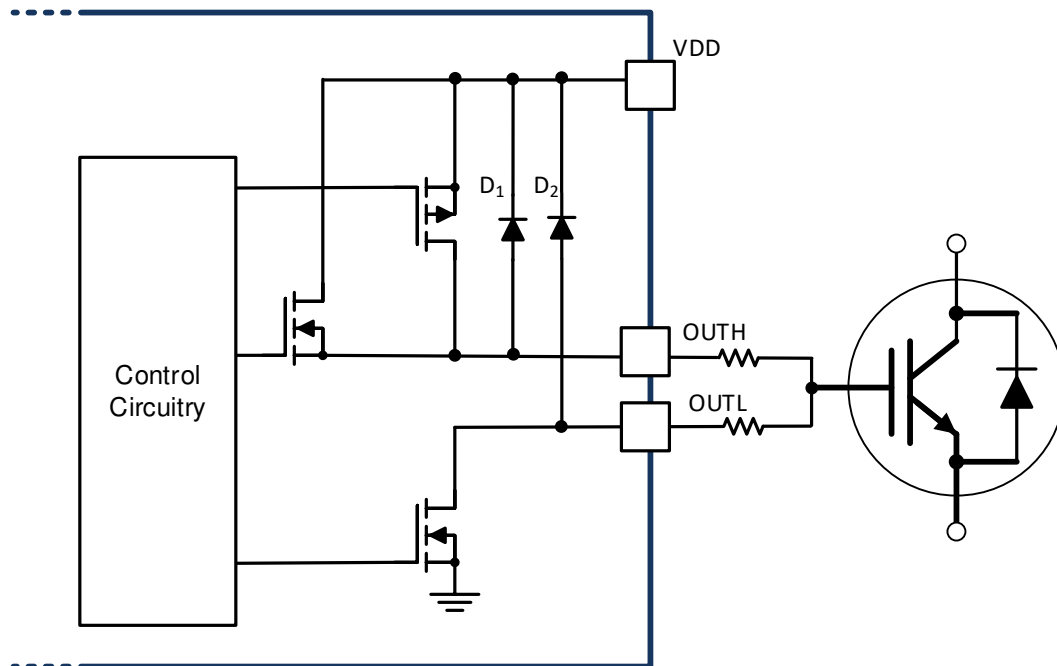


図 7-3. Short Circuit Clamping

7.3.6 External Active Miller Clamp

Active miller clamp feature is important to prevent the false turn-on while the driver is in OFF state. In applications which the device can be in synchronous rectifier mode, the body diode conducts the current during the deadtime while the device is in OFF state, the drain-source or collector-emitter voltage remains the same and the dV/dt happens when the other power semiconductor of the phase leg turns on. The low internal pull-down impedance of UCC21732-Q1 can provide a strong pulldown to hold the OUTL to VEE. However, external gate resistance is usually adopted to limit the dV/dt . The miller effect during the turn on transient of the other power semiconductor can cause a voltage drop on the external gate resistor, which boost the gate-source or gate-emitter voltage. If the voltage on V_{GS} or V_{GE} is higher than the threshold voltage of the power semiconductor, a shoot through can happen and cause catastrophic damage. The active miller clamp feature of UCC21732-Q1 drives an external MOSFET, which connects to the device gate. The external MOSFET is triggered when the gate voltage is lower than V_{CLMPH} , which is 2 V above VEE, and creates a low impedance path to avoid the false turn on issue.

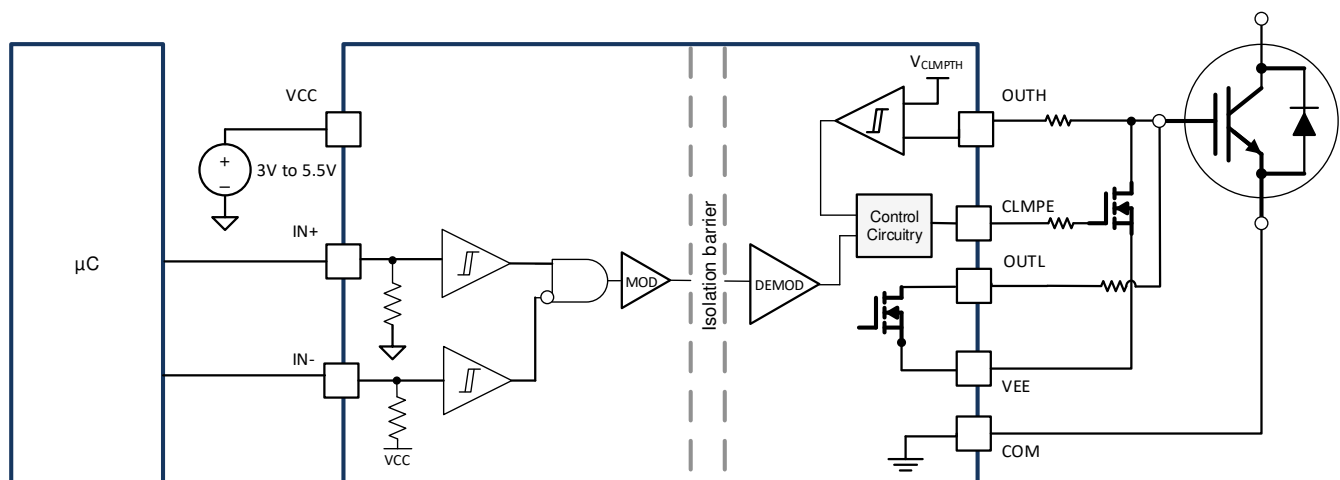


図 7-4. Active Miller Clamp

7.3.7 Overcurrent and Short Circuit Protection

The UCC21732-Q1 implements a fast overcurrent and short circuit protection feature to protect the SiC MOSFET or IGBT from catastrophic breakdown during fault. The OC pin of the device has a typical 0.7-V threshold with respect to COM, source or emitter of the power semiconductor. When the input is in floating condition, or the output is held in low state, the OC pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The OC pin is in high-impedance state when the output is in high state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in on state. The internal pulldown MOSFET helps to discharge the voltage of OC pin when the power semiconductor is turned off.

The overcurrent and short circuit protection feature can be used to SiC MOSFET module or IGBT module with SenseFET, traditional desaturation circuit and shunt resistor in series with the power loop for lower power applications. For SiC MOSFET module or IGBT module with SenseFET, the SenseFET integrated in the module can scale down the drain current or collector current. With an external high precision sense resistor, the drain current or collector current can be accurately measured. If the voltage of the sensed resistor higher than the overcurrent threshold V_{OCTH} is detected, the 2-Level turn-off is initiated. A fault will be reported to the input side \overline{FLT} pin to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the $\overline{RST/EN}$ pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

The overcurrent and short circuit protection feature can also be paired with desaturation circuit and shunt resistors. The DESAT threshold can be programmable in this case, which increases the versatility of the device. Detailed application diagrams of desaturation circuit and shunt resistor will be given in Overcurrent and Short Circuit Protection.

- High current and high di/dt during the overcurrent and short circuit fault can cause a voltage bounce on shunt resistor's parasitic inductance and board layout parasitic, which results in false trigger of OC pin. High precision, low ESL and small value resistor must be used in this approach.
- Shunt resistor approach is not recommended for high power applications and short circuit protection of the low power applications.

The detailed applications of the overcurrent and short circuit feature is discussed in the Application and Implementation section.

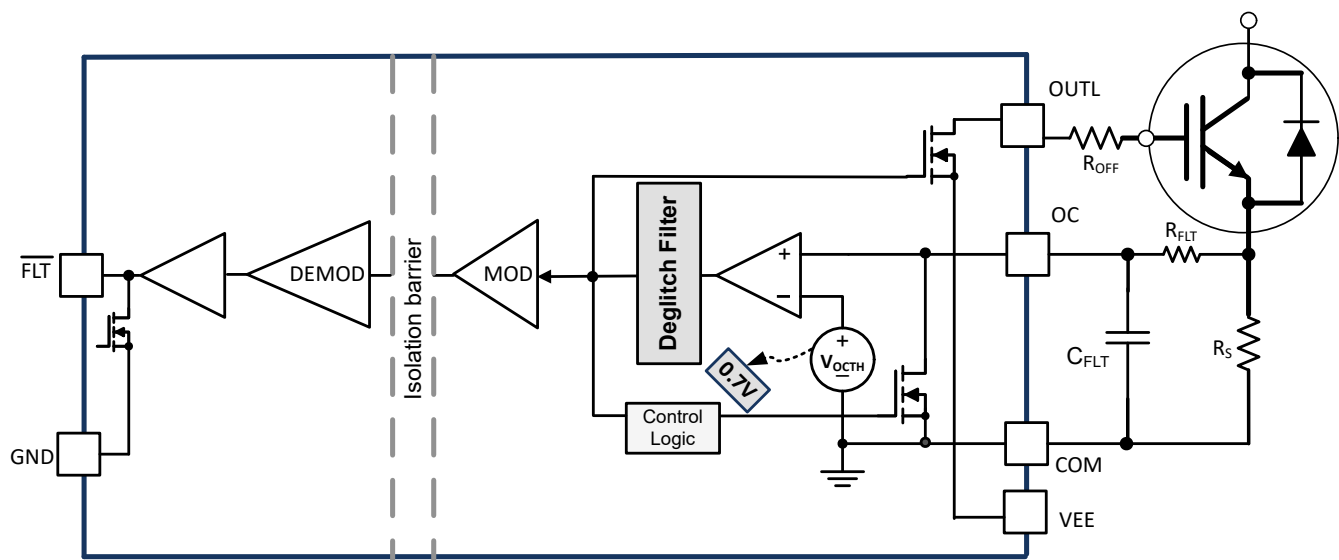


图 7-5. Overcurrent and Short Circuit Protection

7.3.8 2-Level Turn-Off

The UCC21732-Q1 initiates a fast 2-level turn-off when the overcurrent and short circuit protection is triggered. When the overcurrent and short circuit fault happens, the power semiconductor transits from the linear region to the saturation region very fast. The channel current is controlled by the gate voltage. By pulling down the gate voltage to a mid-voltage level V_{2LOFF} and stay for a fixed time t_{2LOFF} , the channel current can be limited to a much lower level, which significantly reduces the energy dissipation during the fault event. After t_{2LOFF} , the driver continues to pull down the gate voltage by the soft turn off current $ITL3$ until it reaches V_{EE} . With di/dt of the channel current is controlled by the gate voltage and decreasing in a soft manner, thus the overshoot of the power semiconductor is limited and prevents the overvoltage breakdown. The timing diagram of 2-level turn-off shows in 6-10.

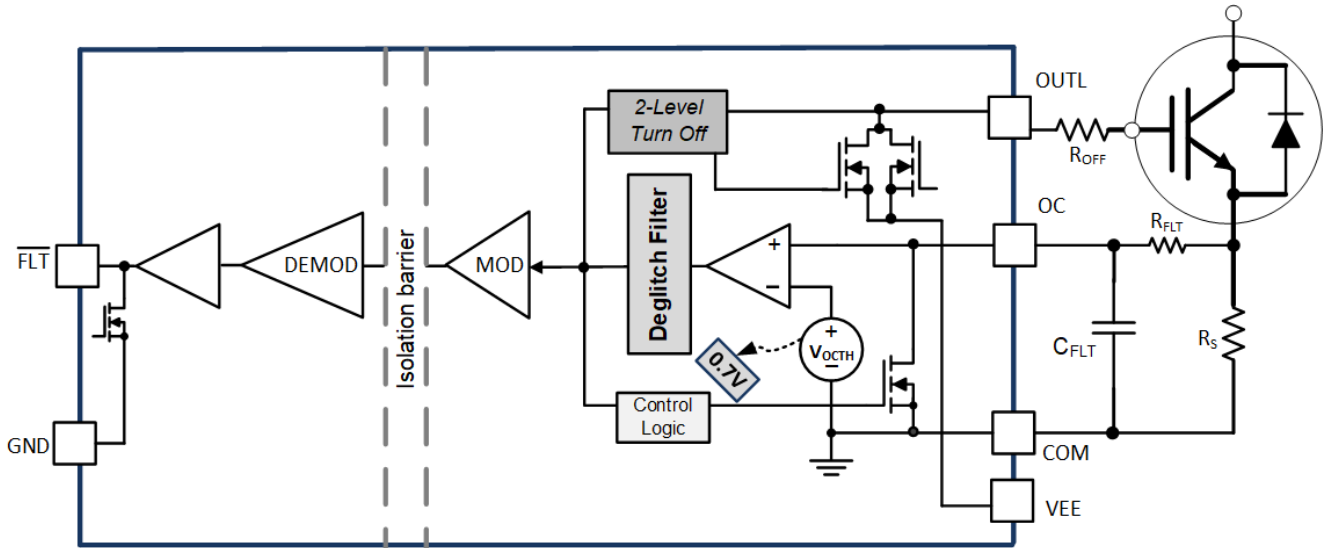


図 7-6. 2-Level Turn-Off

7.3.9 Fault (\overline{FLT} , Reset and Enable ($\overline{RST/EN}$)

The \overline{FLT} pin of the UCC21732-Q1 is open drain and can report a fault signal to the DSP/MCU when the overcurrent and short circuit fault is detected through OC pin. The \overline{FLT} pin is pulled down to GND, and is held in low state unless a reset signal is received from $\overline{RST/EN}$. The device has a fault mute time $t_{FLT MUTE}$, within which the device ignores any reset signal.

The $\overline{RST/EN}$ is pulled down internally. The device is disabled by default if the $\overline{RST/EN}$ pin is floating. The pin has two purposes:

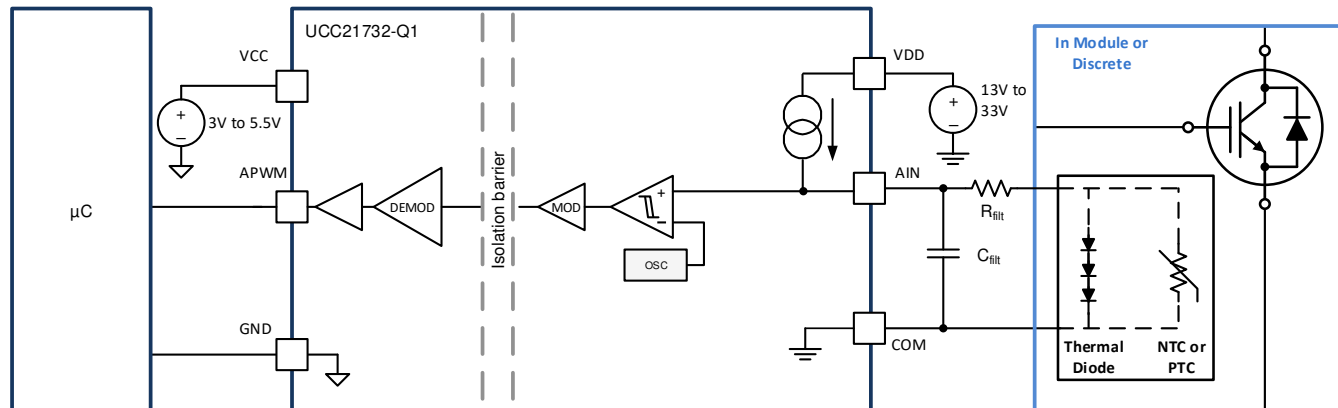
- Resets the overcurrent and short circuit signaled on \overline{FLT} pin. The $\overline{RST/EN}$ pin is active low, if the pin is set and held in low state for more than t_{RSTFIL} , the fault signal is reset and \overline{FLT} is reset back to the high impedance status at the rising edge of $\overline{RST/EN}$ pin.
- Enable and shutdown the device. If the $\overline{RST/EN}$ pin is pulled low, the driver is disabled and shut down by the regular turn off. The pin must be pulled up externally to enable the part, otherwise the device is disabled by default.

7.3.10 Isolated Analog to PWM Signal Function

The UCC21732-Q1 features an isolated analog to PWM signal function from AIN to APWM pin, which allows the isolated temperature sensing, high voltage dc bus voltage sensing, etc. An internal current source I_{AIN} in AIN pin is implemented in the device to bias an external thermal diode or temperature sensing resistor. The UCC21732-Q1 encodes the voltage signal V_{AIN} to a PWM signal, passing through the reinforced isolation barrier, and output to APWM pin on the input side. The PWM signal can either be transferred directly to DSP/MCU to calculate the duty cycle, or filtered by a simple RC filter as an analog signal. The AIN voltage input range is from 0.6 V to 4.5

V, and the corresponding duty cycle of the APWM output ranges from 88% to 10%. The duty cycle increases linearly from 10% to 88% while the AIN voltage decreases from 4.5 V to 0.6 V. This corresponds to the temperature coefficient of the negative temperature coefficient (NTC) resistor and thermal diode. When AIN is floating, the AIN voltage is 5 V and the APWM operates at 400 kHz with approximately 10% duty cycle. The accuracy of the duty cycle is $\pm 5\%$ across temperature without one time calibration. The accuracy can be improved to $\pm 2\%$ with calibration. The accuracy of the internal current source I_{AIN} is 3% across temperature.

The isolated analog to PWM signal feature can also support other analog signal sensing, such as the high voltage dc bus voltage, and so on. The internal current source I_{AIN} should be taken into account when designing the potential divider if sensing a high voltage.



7-7. Isolated Analog to PWM Signal

7.4 Device Functional Modes

表 7-1 lists the device function.

表 7-1. Function Table

INPUT							OUTPUT				
VCC	VDD	VEE	IN+	IN-	$\overline{\text{RST}}/\text{EN}$	AIN	RDY	FLT	OUTH/ OUTL	CLMPE	APWM
PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low	Low
PD	PU	PU	X	X	X	X	Low	HiZ	Low	High	Low
PU	PU	PU	X	X	Low	X	HiZ	HiZ	Low	High	Low
PU	Open	PU	X	X	X	X	Low	HiZ	HiZ	HiZ	HiZ
PU	PU	Open	X	X	X	X	Low	HiZ	Low	High	Low
PU	PU	PU	Low	X	High	X	HiZ	HiZ	Low	High	P*
PU	PU	PU	X	High	High	X	HiZ	HiZ	Low	High	P*
PU	PU	PU	High	High	High	X	HiZ	HiZ	Low	High	P*
PU	PU	PU	High	Low	High	X	HiZ	HiZ	High	HiZ	P*

PU: Power Up ($V_{CC} \geq 2.85 \text{ V}$, $V_{DD} \geq 13.1 \text{ V}$, $V_{EE} \leq 0 \text{ V}$); PD: Power Down ($V_{CC} \leq 2.35 \text{ V}$, $V_{DD} \leq 9.9 \text{ V}$); X: Irrelevant; P*: PWM Pulse; HiZ: High Impedance

8 Applications and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The UCC21732-Q1 device is very versatile because of the strong drive strength, wide range of output power supply, high isolation ratings, high CMTI and superior protection and sensing features. The 1.5-kVRMS working voltage and 12.8-kV_{PK} surge immunity can support up both SiC MOSFET and IGBT modules with DC bus voltage up to 2121V. The device can be used in both low power and high power applications such as the traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies and so on. The device can drive the high power SiC MOSFET module, IGBT module or paralleled discrete device directly without external buffer drive circuit based on NPN/PNP bipolar transistor in totem-pole structure, which allows the driver to have more control to the power semiconductor and saves the cost and space of the board design. The UCC21732-Q1 can also be used to drive very high power modules or paralleled modules with external buffer stage. The input side can support power supply and microcontroller signal from 3.3 V to 5 V, and the device level shifts the signal to output side through reinforced isolation barrier. The device has wide output power supply range from 13 V to 33 V and support wide range of negative power supply. This allows the driver to be used in SiC MOSFET applications, IGBT application and many others. The 12-V UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

The UCC21732-Q1 device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short circuit fault. The feature is preferable in a split source SiC MOSFET module or a split emitter IGBT module. For the modules with no integrated current mirror or paralleled discrete semiconductors, the traditional desaturation circuit can be modified to implement short circuit protection. The semiconductor is shutdown when the fault is detected and FLTb pin is pulled down to indicate the fault detection. The device is latched unless reset signal is received from the $\overline{\text{RST}}/\text{EN}$ pin.
- 2-level turn-off feature to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power good status can be monitored from the RDY pin.
- Analog signal sensing with isolated analog to PWM signal feature. This feature allows the device to sense the temperature of the semiconductor from the thermal diode or temperature sensing resistor, or dc bus voltage with resistor divider. A PWM signal is generated on the low voltage side with reinforced isolated from the high voltage side. The signal can be fed back to the microcontroller for the temperature monitoring, voltage monitoring and so on.
- The active miller clamp feature protects the power semiconductor from false turn on by driving an external MOSFET. This feature allows the flexibility of the board layout design and the pulldown strength of miller clamp FET.
- Enable and disable function through the RSTb/EN pin.
- Short circuit clamping
- Active pulldown

8.2 Typical Application

図 8-1 shows the typical application of a half bridge using two UCC21732-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications such as traction inverter in HEV/EV to convert the DC current of the electric vehicle's battery to the AC current to drive the electric motor in the propulsion system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.

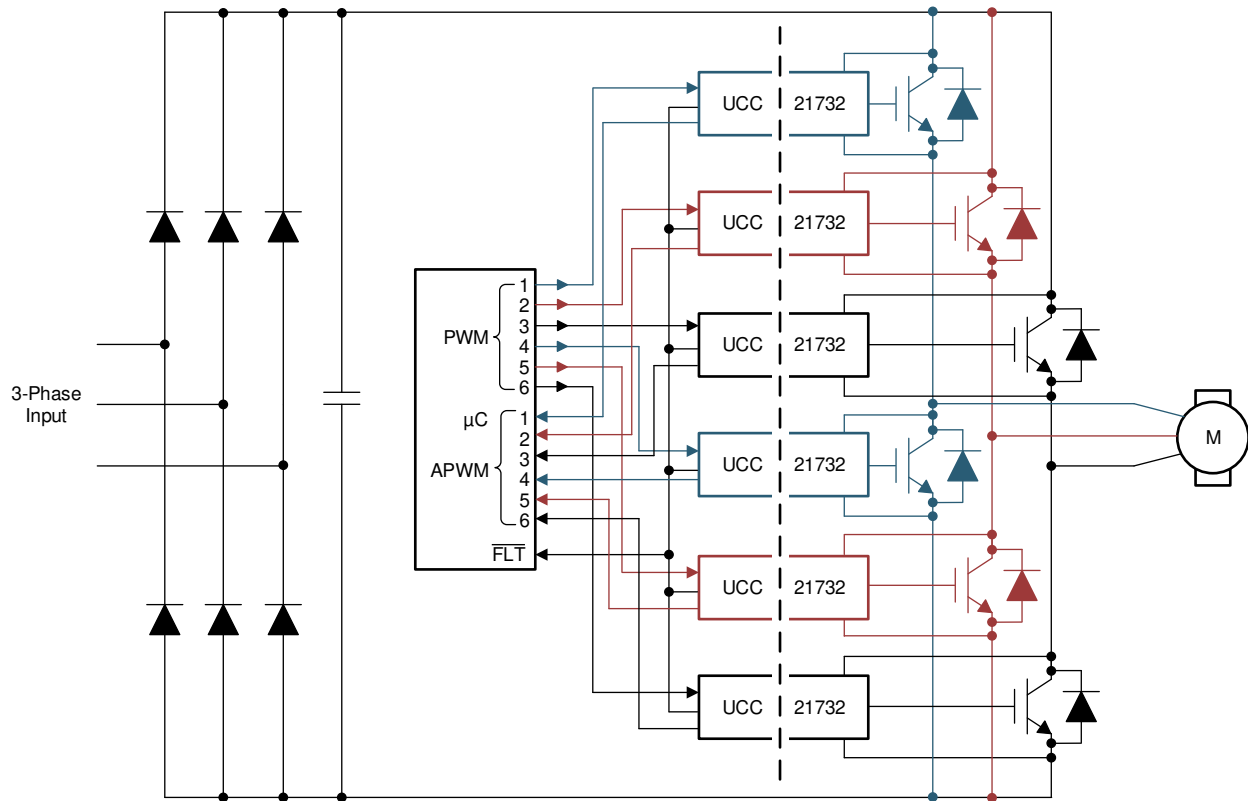


図 8-1. Typical Application Schematic

8.2.1 Design Requirements

The design of the power system for end equipment should consider some design requirements to ensure the reliable operation of UCC1732-Q1 through the load range. The design considerations include the peak source and sink current, power dissipation, overcurrent and short circuit protection, AIN-APWM function for analog signal sensing and so on.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are show in 表 8-1.

表 8-1. Design Parameters

PARAMETER	VALUE
Input Supply Voltage	5 V
IN-OUT Configuration	Non-inverting
Positive Output Voltage VDD	15 V
Negative Output Voltage VEE	-5 V
DC Bus Voltage	800 V
Peak Drain Current	300 A
Switching Frequency	50 kHz

表 8-1. Design Parameters (続き)

PARAMETER	VALUE
Switch Type	IGBT Module

8.2.2 Detailed Design Procedure

8.2.2.1 Input Filters for IN+, IN- and $\overline{\text{RST/EN}}$

In the applications of traction inverter or motor drive, the power semiconductors are in hard switching mode. With the strong drive strength of UCC21732-Q1, the dV/dt can be high, especially for SiC MOSFET. Noise can not only be coupled to the gate voltage due to the parasitic inductance, but also to the input side as the non-ideal PCB layout and coupled capacitance.

The UCC21732-Q1 features a 40-ns internal deglitch filter to IN+, IN- and $\overline{\text{RST/EN}}$ pin. Any signal less than 40 ns can be filtered out from the input pins. For noisy systems, external low-pass filter can be added externally to the input pins. Adding low-pass filters to IN+, IN- and $\overline{\text{RST/EN}}$ pins can effectively increase the noise immunity and increase the signal integrity. When not in use, the IN+, IN- and $\overline{\text{RST/EN}}$ pins should not be floating. IN- should be tied to GND if only IN+ is used for non-inverting input to output configuration. The purpose of the low-pass filter is to filter out the high frequency noise generated by the layout parasitics. While choosing the low-pass filter resistors and capacitors, both the noise immunity effect and delay time should be considered according to the system requirements.

8.2.2.2 PWM Interlock of IN+ and IN-

The UCC21732-Q1 features the PWM interlock for IN+ and IN- pins, which can be used to prevent the phase leg shoot through issue. As shown in 表 7-1, the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in 図 8-2, the PWM_T is the PWM signal to top side switch, the PWM_B is the PWM signal to bottom side switch. For the top side gate driver, the PWM_T signal is given to the IN+ pin, while the PWM_B signal is given to the IN- pin; for the bottom side gate driver, the PWM_B signal is given to the IN+ pin, while PWM_T signal is given to the IN- pin. When both PWM_T and PWM_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot through condition.

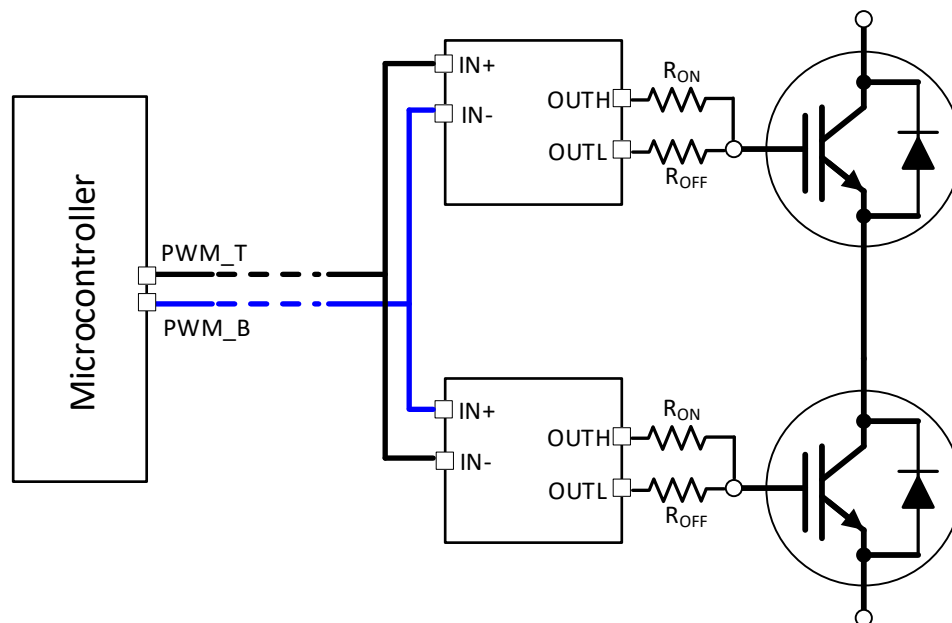


図 8-2. PWM Interlock for a Half Bridge

8.2.2.3 $\overline{\text{FLT}}$, RDY and $\overline{\text{RST/EN}}$ Pin Circuitry

Both $\overline{\text{FLT}}$ and RDY pin are open-drain output. The $\overline{\text{RST/EN}}$ pin has 50-k Ω internal pulldown resistor, so the driver is in OFF status if the $\overline{\text{RST/EN}}$ pin is not pulled up externally. A 5-k Ω resistor can be used as pullup resistor for the $\overline{\text{FLT}}$, RDY and $\overline{\text{RST/EN}}$ pins.

To improve the noise immunity due to the parasitic coupling and common mode noise, low-pass filters can be added between the $\overline{\text{FLT}}$, RDY and $\overline{\text{RST/EN}}$ pins and the microcontroller. A filter capacitor between 100 pF to 300 pF can be added.

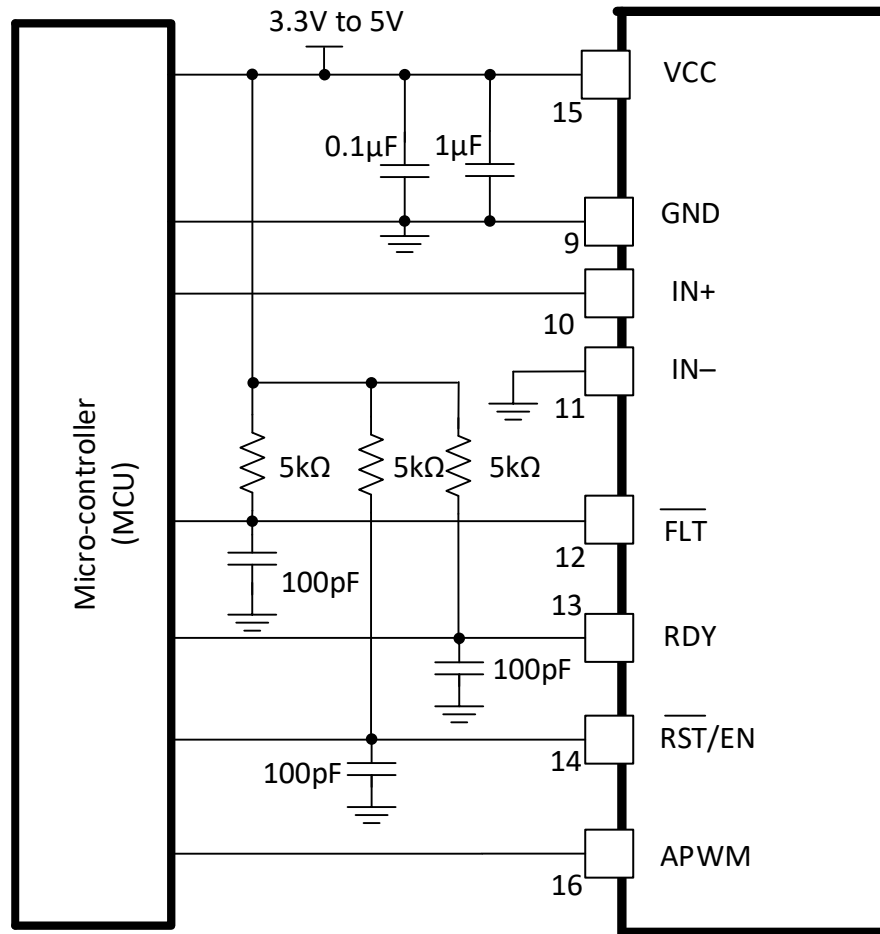


図 8-3. $\overline{\text{FLT}}$, RDY and $\overline{\text{RST/EN}}$ Pins Circuitry

8.2.2.4 $\overline{\text{RST/EN}}$ Pin Control

The $\overline{\text{RST/EN}}$ pin has two functions. It can be used to enable and shutdown the outputs of the driver, and reset the fault signaled on the $\overline{\text{FLT}}$ pin. $\overline{\text{RST/EN}}$ pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. With a 50-k Ω pulldown resistor existing, the driver is disabled by default.

When the driver is latched after overcurrent or short circuit fault is detected, the $\overline{\text{FLT}}$ pin and output are latched low and need to be reset by $\overline{\text{RST/EN}}$ pin. $\overline{\text{RST/EN}}$ pin is active low. The microcontroller needs to send a signal to $\overline{\text{RST/EN}}$ pin after the fault mute time t_{FLTMUTE} to reset the driver. This pin can also be used to automatically reset the driver. The continuous input signal IN+ or IN- can be applied to $\overline{\text{RST/EN}}$ pin, so the microcontroller does not need to generate another control signal to reset the driver. If non-inverting input IN+ is used, then IN+ can be tied to $\overline{\text{RST/EN}}$ pin. If inverting input IN- is used, then a NOT logic is needed between the inverting PWM signal from the microcontroller and the $\overline{\text{RST/EN}}$ pin. In this case, the driver can be reset in every switching cycle without an extra control signal from microcontroller to $\overline{\text{RST/EN}}$ pin.

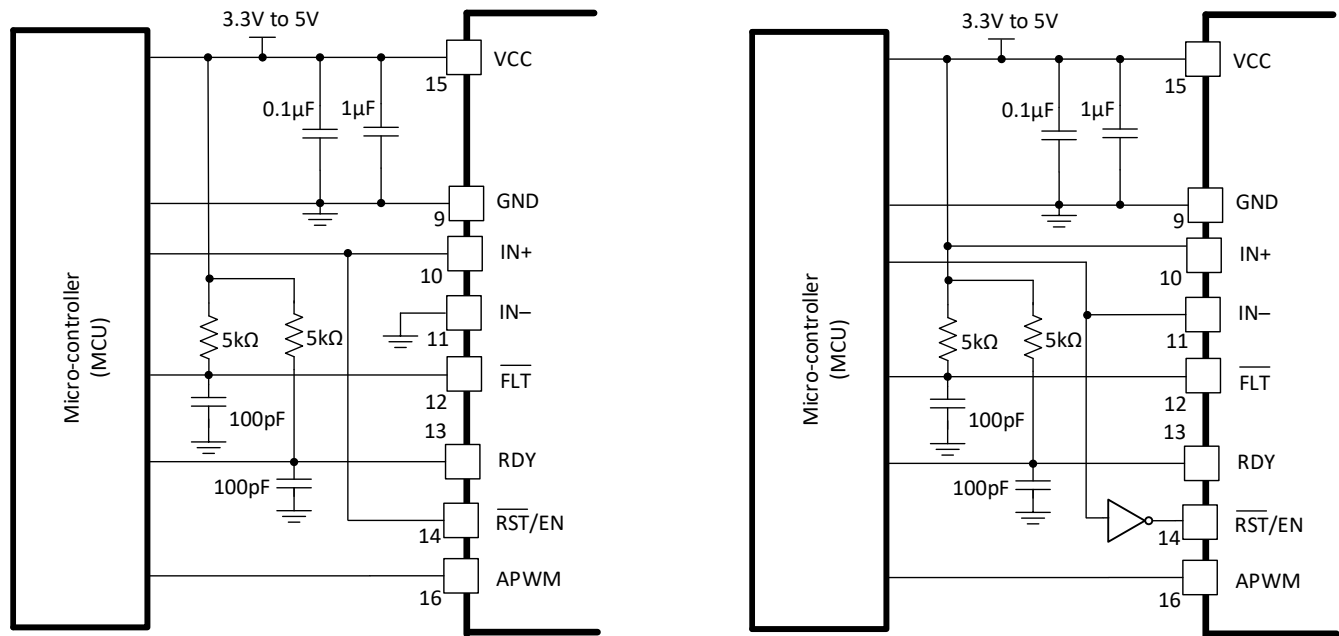


图 8-4. Automatic Reset Control

8.2.2.5 Turn-On and Turn-Off Gate Resistors

The UCC21732-Q1 features split outputs OUTH and OUTL, which enables the independent control of the turn on and turn off switching speed. The turn-on and turn-off resistance determine the peak source and sink current, which controls the switching speed in turn. Meanwhile, the power dissipation in the gate driver should be considered to ensure the device is in the thermal limit. At first, the peak source and sink current are calculated as:

$$I_{\text{source_pk}} = \min\left(10\text{A}, \frac{V_{\text{DD}} - V_{\text{EE}}}{R_{\text{OH_EFF}} + R_{\text{ON}} + R_{\text{G_Int}}}\right)$$

$$I_{\text{sink_pk}} = \min\left(10\text{A}, \frac{V_{\text{DD}} - V_{\text{EE}}}{R_{\text{OL}} + R_{\text{OFF}} + R_{\text{G_Int}}}\right)$$
(1)

Where

- $R_{\text{OH_EFF}}$ is the effective internal pull-up resistance of the hybrid pull-up structure, which is approximately $2 \times R_{\text{OL}}$, about 0.7Ω
- R_{OL} is the internal pull-down resistance, about 0.3Ω
- R_{ON} is the external turn-on gate resistance
- R_{OFF} is the external turn-off gate resistance
- $R_{\text{G_Int}}$ is the internal resistance of the SiC MOSFET or IGBT module

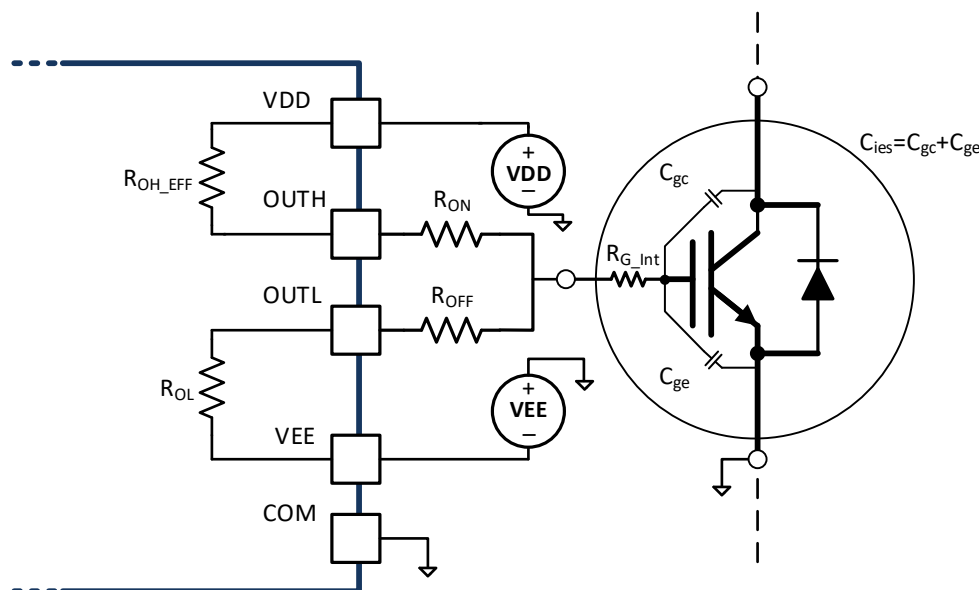


FIG 8-5. Output Model for Calculating Peak Gate Current

For example, for an IGBT module based system with the following parameters:

- $Q_g = 3300 \text{ nC}$
- $R_{G_Int} = 1.7 \Omega$
- $R_{ON}=R_{OFF}= 1 \Omega$

The peak source and sink current in this case are:

$$I_{\text{source_pk}} = \min(10\text{A}, \frac{V_{DD} - V_{EE}}{R_{OH_EFF} + R_{ON} + R_{G_Int}}) \approx 5.9\text{A}$$

$$I_{\text{sink_pk}} = \min(10\text{A}, \frac{V_{DD} - V_{EE}}{R_{OL} + R_{OFF} + R_{G_Int}}) \approx 6.7\text{A} \quad (2)$$

Thus by using 1-Ω external gate resistance, the peak source current is 5.9 A, the peak sink current is 6.7 A. The collector-to-emitter dV/dt during the turn on switching transient is dominated by the gate current at the miller plateau voltage. The hybrid pullup structure ensures the peak source current at the miller plateau voltage, unless the turn on gate resistor is too high. The faster the collector-to-emitter, V_{ce} , voltage rises to V_{DC} , the smaller the turn-on switching loss is. The dV/dt can be estimated as $Q_g/I_{\text{source_pk}}$. For the turn-off switching transient, the drain-to-source dV/dt is dominated by the load current, unless the turn-off gate resistor is too high. After V_{ce} reaches the dc bus voltage, the power semiconductor is in saturation mode and the channel current is controlled by V_{ge} . The peak sink current determines the dI/dt , which dominates the V_{ce} voltage overshoot accordingly. If using relatively large turn-off gate resistance, the V_{ce} overshoot can be limited. The overshoot can be estimated by:

$$\Delta V_{ce} = L_{\text{stray}} \cdot I_{\text{load}} / ((R_{OFF} + R_{OL} + R_{G_Int}) \cdot C_{ies} \cdot \ln(V_{\text{plat}} / V_{th})) \quad (3)$$

Where

- L_{stray} is the stray inductance in power switching loop, as shown in [FIG 8-6](#)
- I_{load} is the load current, which is the turn-off current of the power semiconductor
- C_{ies} is the input capacitance of the power semiconductor
- V_{plat} is the plateau voltage of the power semiconductor
- V_{th} is the threshold voltage of the power semiconductor

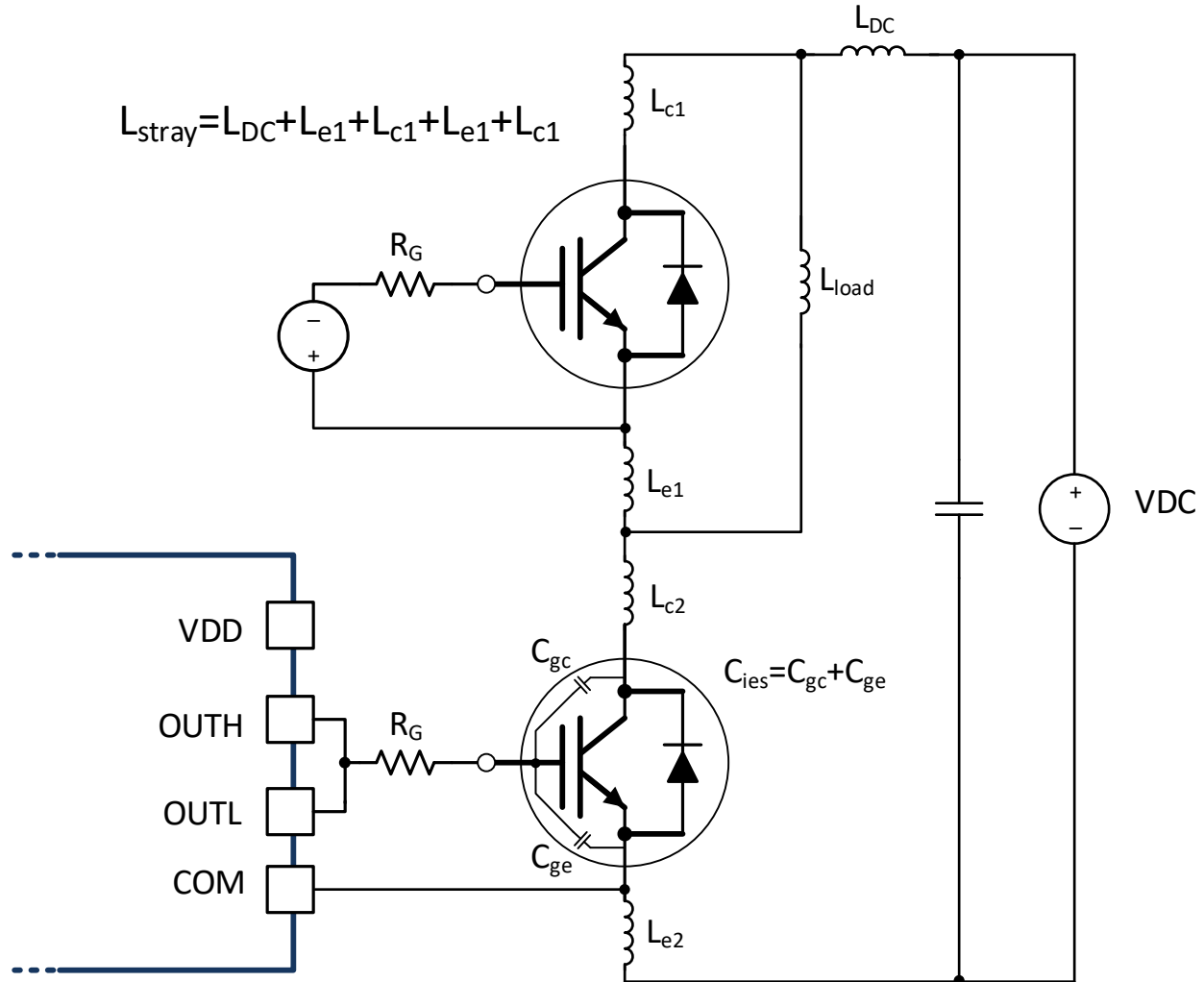


図 8-6. Stray Parasitic Inductance of IGBTs in a Half-Bridge Configuration

The power dissipation should be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as:

$$P_{DR} = P_Q + P_{SW} \quad (4)$$

P_Q is the quiescent power loss for the driver, which is $I_q \times (VDD - VEE) = 5 \text{ mA} \times 20 \text{ V} = 0.100 \text{ W}$. The quiescent power loss is the power consumed by the internal circuits such as the input stage, reference voltage, logic circuits, protection circuits when the driver is switching when the driver is biased with VDD and VEE, and also the charging and discharging current of the internal circuit when the driver is switching. The power dissipation when the driver is switching can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH_EFF}}{R_{OH_EFF} + R_{ON} + R_{G_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g \quad (5)$$

Where

- Q_g is the gate charge required at the operation point to fully charge the gate voltage from VEE to VDD
- f_{sw} is the switching frequency

In this example, the P_{SW} can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH_EFF}}{R_{OH_EFF} + R_{ON} + R_{G_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G_Int}} \right) \cdot (V_{DD} - V_{EE}) \cdot f_{sw} \cdot Q_g = 0.505W \quad (6)$$

Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.10W + 0.505W = 0.605W \quad (7)$$

When the board temperature is 125°C, the junction temperature can be estimated as:

$$T_j = T_b + \psi_{jb} \cdot P_{DR} \approx 150^\circ C \quad (8)$$

Therefore, for the application in this example, with 125°C board temperature, the maximum switching frequency is ~50 kHz to keep the gate driver in the thermal limit. By using a lower switching frequency, or increasing external gate resistance, the gate driver can be operated at a higher switching frequency.

8.2.2.6 External Active Miller Clamp

External active miller clamp feature allows the gate driver to stay at the low status when the gate voltage is detected below $V_{CLMP_{TH}}$. When the other switch of the phase leg turns on, the dV/dt can cause a current through the parasitic miller capacitance of the switch and sink in the gate driver. The sinking current causes a negative voltage drop on the turn off gate resistance, and bumps up the gate voltage to cause a false turn on. The external active miller clamp features allows flexibility of board layout and active miller clamp pulldown strength. Limited by the board layout, if the driver cannot be placed close enough to the switch, external active miller clamp MOSFET can be placed close to the switch and the MOSFET can be chosen according to the peak current needed. Caution must be exercised when the driver is placed far from the power semiconductor. Since the device has high peak sink and source current, the high dI/dt in the gate loop can cause a ground bounce on the board parasitics. The ground bounce can cause a positive voltage bump on CLMPE pin during the turn off transient, and results in the external active miller clamp MOSFET to turn on shortly and add extra drive strength to the sink current. To reduce the ground bounce, a 2-Ω resistance is recommended to the gate of the external active clamp MOSFET.

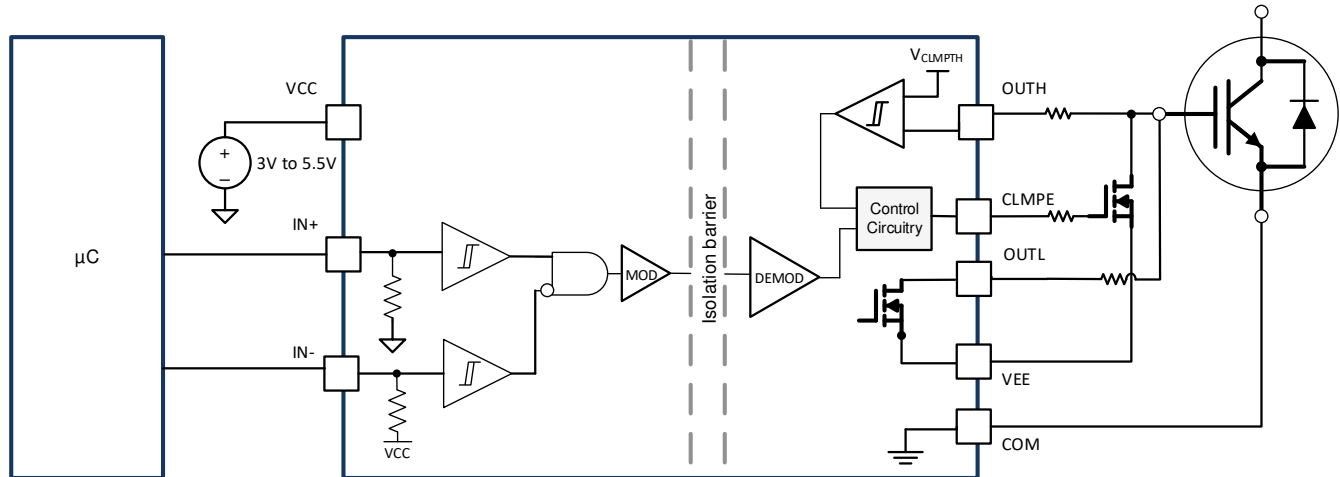
When the V_{OUTH} is detected to be lower than $V_{CLMP_{TH}}$ above VEE, the CLMPE pin outputs a 5-V voltage with respect to VEE, the external clamp FET is in linear region and the pulldown current is determined by the peak drain current, unless the on-resistance of the external clamp FET is large.

$$I_{CLMPE_PK} = \min(I_{D_PK}, \frac{V_{DS}}{R_{DS_ON}}) \quad (9)$$

Where

- I_{D_PK} is the peak drain current of the external clamp FET
- V_{DS} is the drain-to-source voltage of the clamp FET when the CLMPE is activated
- R_{DS_ON} is the on-resistance of the external clamp FET

The total delay time of the active miller clamp circuit from the gate voltage detection threshold $V_{CLMP_{TH}}$ can be calculated as $t_{DCLMPE} + t_{CLMPER}$. t_{CLMPER} depends on the parameter of the external active miller clamp MOSFET. As long as the total delay time is longer than the deadtime of high-side and low-side switches, the driver can effectively protect the switch from false turn on issue caused by miller effect.



8-7. External Active Miller Clamp Configuration

8.2.2.7 Overcurrent and Short Circuit Protection

Fast and reliable overcurrent and short circuit protection is important to protect the catastrophic break down of the SiC MOSFET and IGBT modules, and improve the system reliability. The UCC21732-Q1 features a state-of-art overcurrent and short circuit protection, which can be applied to both SiC MOSFET and IGBT modules with various detection circuits.

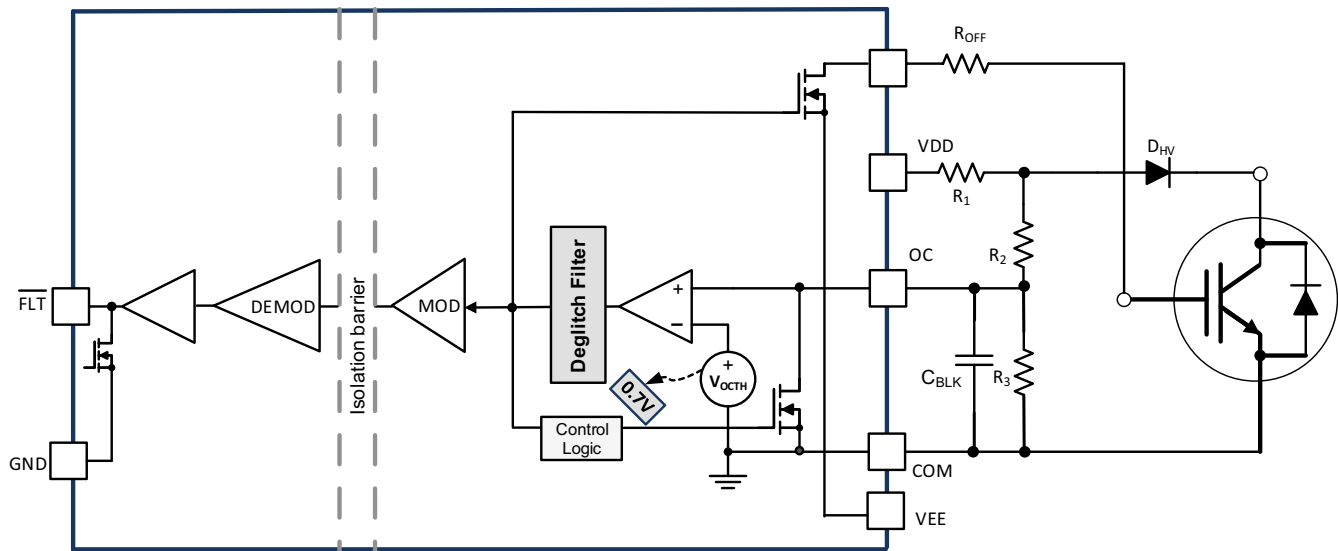
8.2.2.7.1 Protection Based on Power Modules with Integrated SenseFET

The overcurrent and short circuit protection function is suitable for the SiC MOSFET and IGBT modules with integrated SenseFET. The SenseFET scales down the main power loop current and outputs the current with a dedicated pin of the power module. With external high precision sensing resistor, the scaled down current can be measured and the main power loop current can be calculated. The value of the sensing resistor R_S sets the protection threshold of the main current. For example, with a ratio of $1:N = 1:50000$ of the integrated current mirror, by using the R_S as $20\ \Omega$, the threshold protection current is:

$$I_{OC_TH} = \frac{V_{OCTH}}{R_S} \cdot N = 1750A \quad (10)$$

The overcurrent and short circuit protection based on integrated SenseFET has high precision, as it is sensing the current directly. The accuracy of the method is related to two factors: the scaling down ratio of the main power loop current and the SenseFET, and the precision of the sensing resistor. Since the current is sensed from the SenseFET, which is isolated from the main power loop, and the current is scaled down significantly with much less di/dt , the sensing loop has good noise immunity. To further improve the noise immunity, a low-pass filter can be added. A 100-pF to 10-nF filter capacitor can be added. The delay time caused by the low-pass filter should also be considered for the protection circuitry design.

detection threshold voltage of the driver. A parallel schottky diode can be connected between OC and COM pins to prevent the negative voltage on the OC pin in noisy system. Since the desaturation circuit measures the V_{CE} of the IGBT or V_{DS} of the SiC MOSFET, not directly the current, the accuracy of the protection is not as high as the SenseFET based protection method. The current threshold cannot be accurately controlled in the protection.



8-9. Overcurrent and Short Circuit Protection Based on Desaturation Circuit

8.2.2.7.3 Protection Based on Shunt Resistor in Power Loop

In lower power applications, to simplify the circuit and reduce the cost, a shunt resistor can be used in series in the power loop and measure the current directly. Since the resistor is in series in the power loop, it directly measures the current and can have high accuracy by using a high precision resistor. The resistance needs to be small to reduce the power loss, and should have large enough voltage resolution for the protection. Since the sensing resistor is also in series in the gate driver loop, the voltage drop on the sensing resistor can cause the voltage drop on the gate voltage of the IGBT or SiC MOSFET modules. The parasitic inductance of the sensing resistor and the PCB trace of the sensing loop will also cause a noise voltage source during switching transient, which makes the gate voltage oscillate. Thus, this method is not recommended for high power application, or when di/dt is high. To use it in low power application, the shunt resistor loop should be designed to have the optimal voltage drop and minimum noise injection to the gate loop.

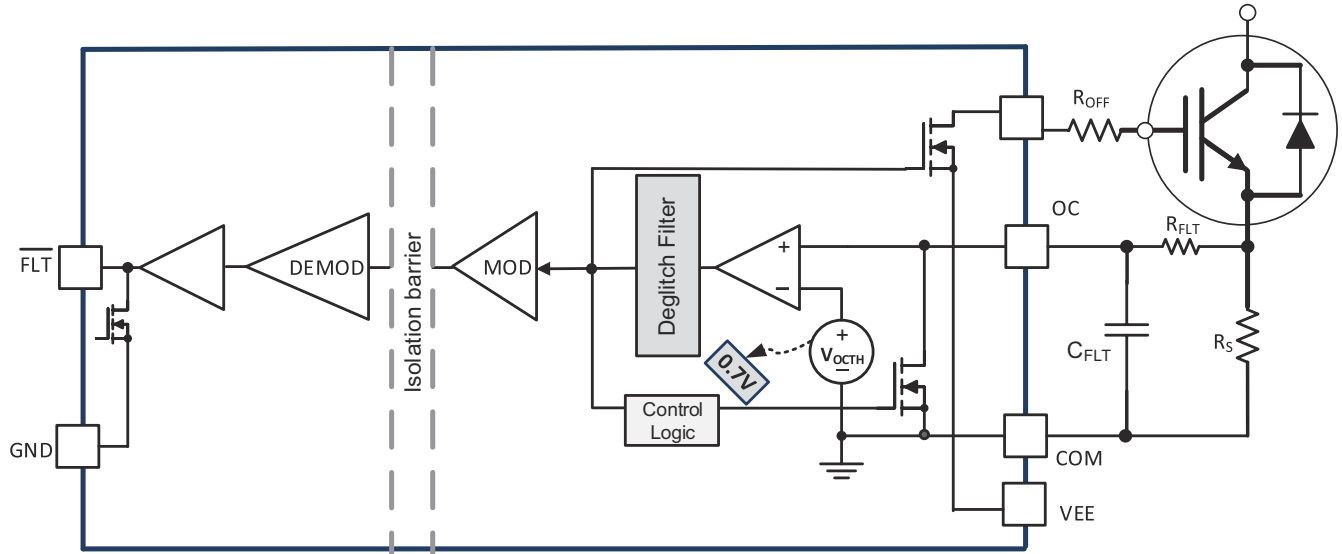


図 8-10. Overcurrent and Short Circuit Protection Based on Shunt Resistor

8.2.2.8 Isolated Analog Signal Sensing

The isolated analog signal sensing feature provides a simple isolated channel for the isolated temperature detection, voltage sensing and etc. One typical application of this function is the temperature monitor of the power semiconductor. Thermal diodes or temperature sensing resistors are integrated in the SiC MOSFET or IGBT module close to the dies to monitor the junction temperature. UCC21732-Q1 has an internal 200-μA current source with 3% accuracy across temperature, which can forward bias the thermal diodes or create a voltage drop on the temperature sensing resistors. The sensed voltage from the AIN pin is passed through the isolation barrier to the input side and transformed to a PWM signal. The duty cycle of the PWM changes linearly from 10% to 88% when the AIN voltage changes from 4.5 V to 0.6 V and can be represented using 式 13.

$$D_{APWM}(\%) = -20 * V_{AIN} + 100 \quad (13)$$

8.2.2.8.1 Isolated Temperature Sensing

A typical application circuit is shown in 図 8-11. To sense temperature, the AIN pin is connected to the thermal diode or thermistor which can be discrete or integrated within the power module. A low-pass filter is recommended for the AIN input. Since the temperature signal does not have a high bandwidth, the low-pass filter is mainly used for filtering the noise introduced by the switching of the power device, which does not require stringent control for propagation delay. The filter capacitance for C_{filt} can be chosen between 1 nF to 100 nF and the filter resistance R_{filt} between 1 Ω to 10 Ω according to the noise level.

The output of APWM is directly connected to the microcontroller to measure the duty cycle dependent on the voltage input at AIN, using 式 13.

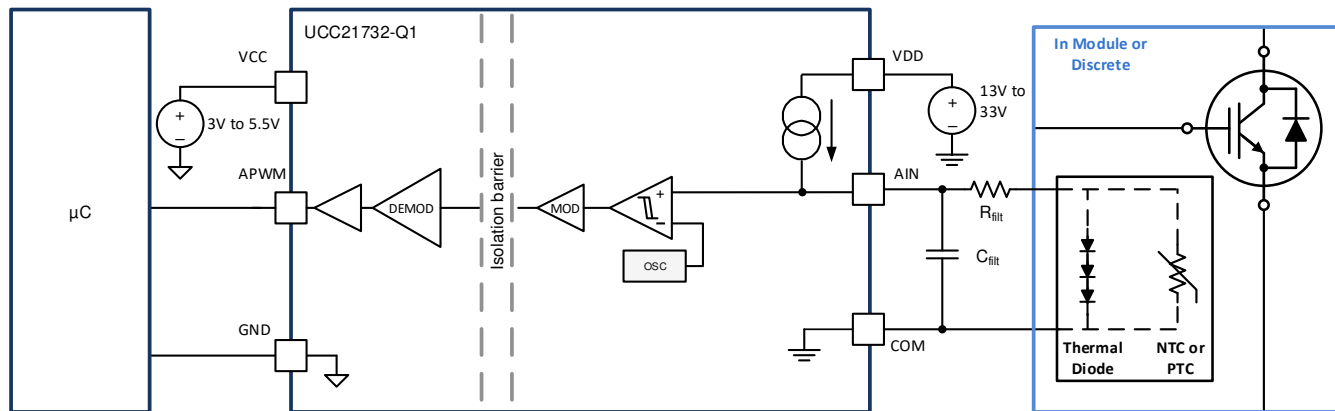


Figure 8-11. Thermal Diode or Thermistor Temperature Sensing Configuration

When a high-precision voltage supply for VCC is used on the primary side of UCC21732-Q1 the duty cycle output of APWM may also be filtered and the voltage measured using the microcontroller's ADC input pin, as shown in Figure 8-12. The frequency of APWM is 400 kHz, so the value for R_{filt_2} and C_{filt_2} should be such that the cutoff frequency is below 400 kHz. Temperature does not change rapidly, thus the rise time due to the RC constant of the filter is not under a strict requirement.

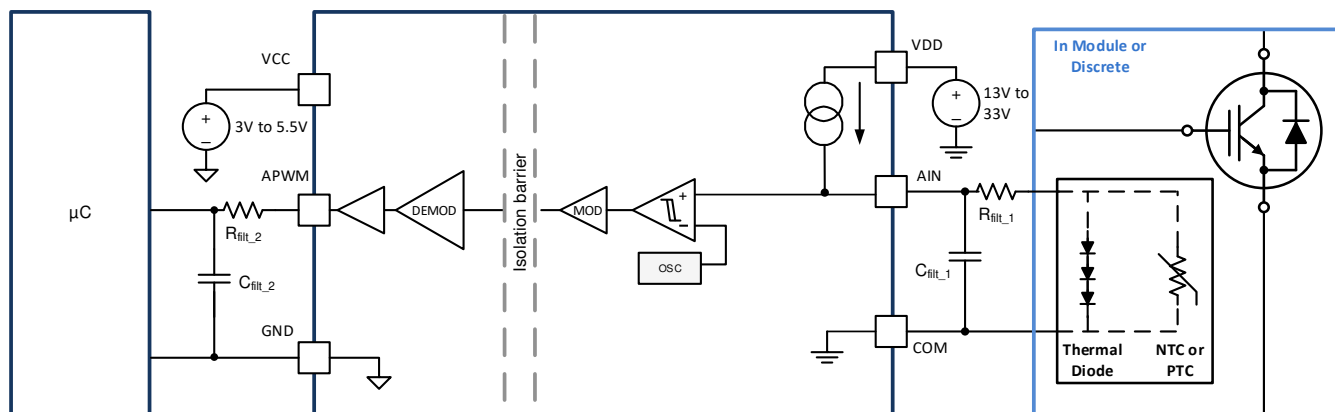


Figure 8-12. APWM Channel with Filtered Output

The example below shows the results using a 4.7-kΩ NTC, NTCS0805E3472FMT, in series with a 3-kΩ resistor and also the thermal diode using four diode-connected MMBT3904 NPN transistors. The sensed voltage of the 4 MMBT3904 thermal diodes connected in series ranges from about 2.5 V to 1.6 V from 25°C to 135°C, corresponding to 50% to 68% duty cycle. The sensed voltage of the NTC thermistor connected in series with the 3-kΩ resistor ranges from about 1.5 V to 0.6 V from 25°C to 135°C, corresponding to 70% to 88% duty cycle. The voltage at VAIN of both sensors and the corresponding measured duty cycle at APWM is shown in Figure 8-13.

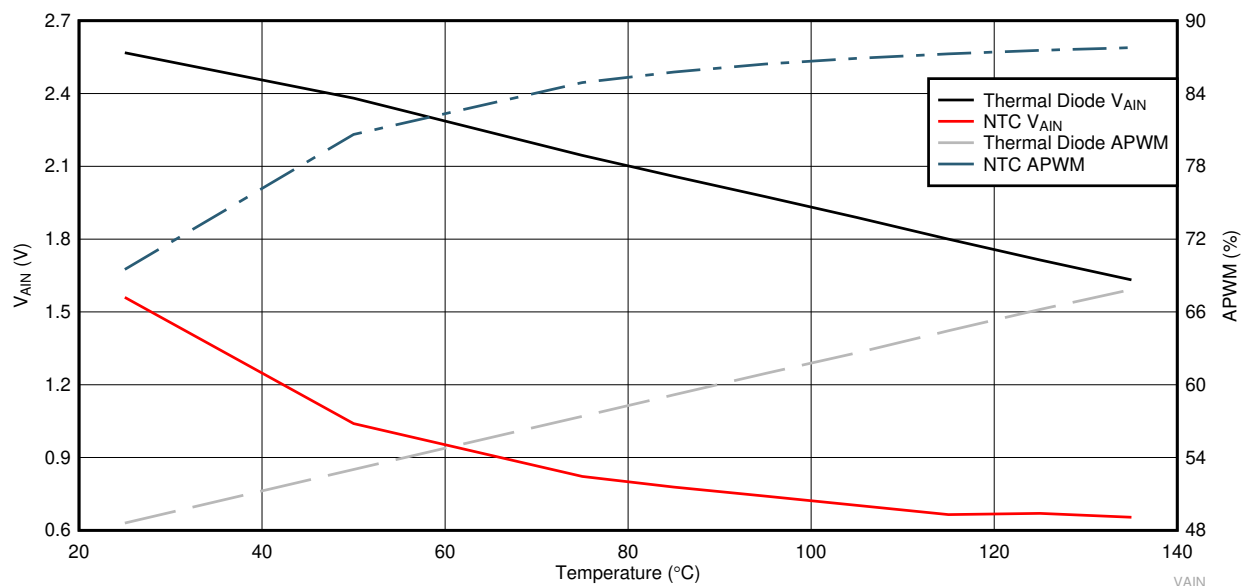


図 8-13. Thermal Diode and NTC V_{AIN} and Corresponding Duty Cycle at APWM

The duty cycle output has an accuracy of $\pm 3\%$ throughout temperature without any calibration, as shown in 図 8-14 but with single-point calibration at 25°C, the duty accuracy can be improved to $\pm 1\%$, as shown in 図 8-15.

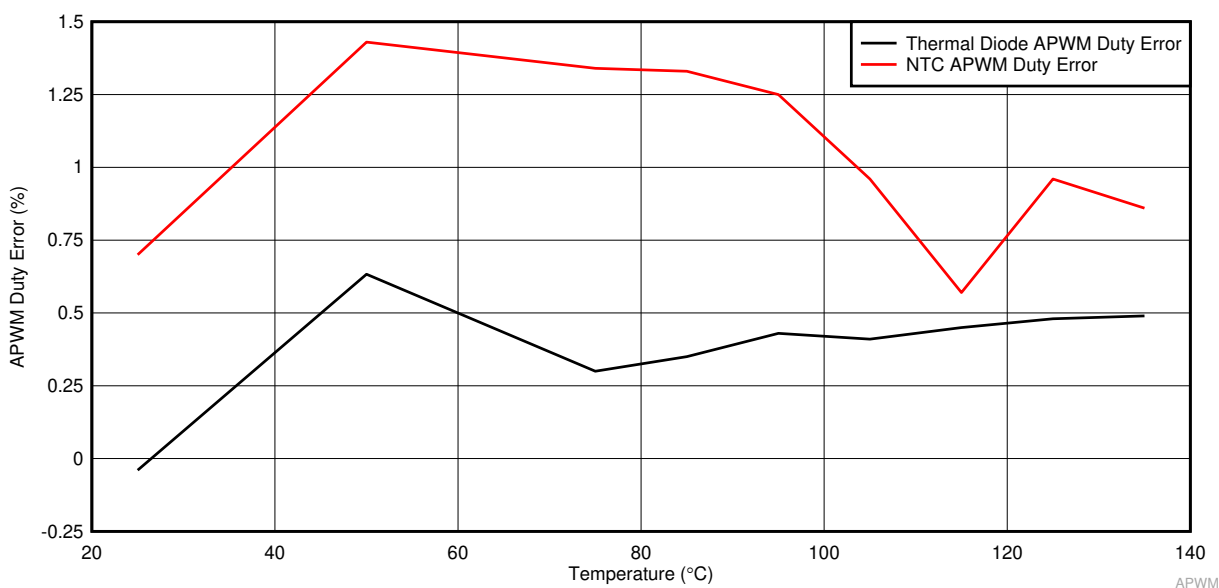


図 8-14. APWM Duty Error Without Calibration

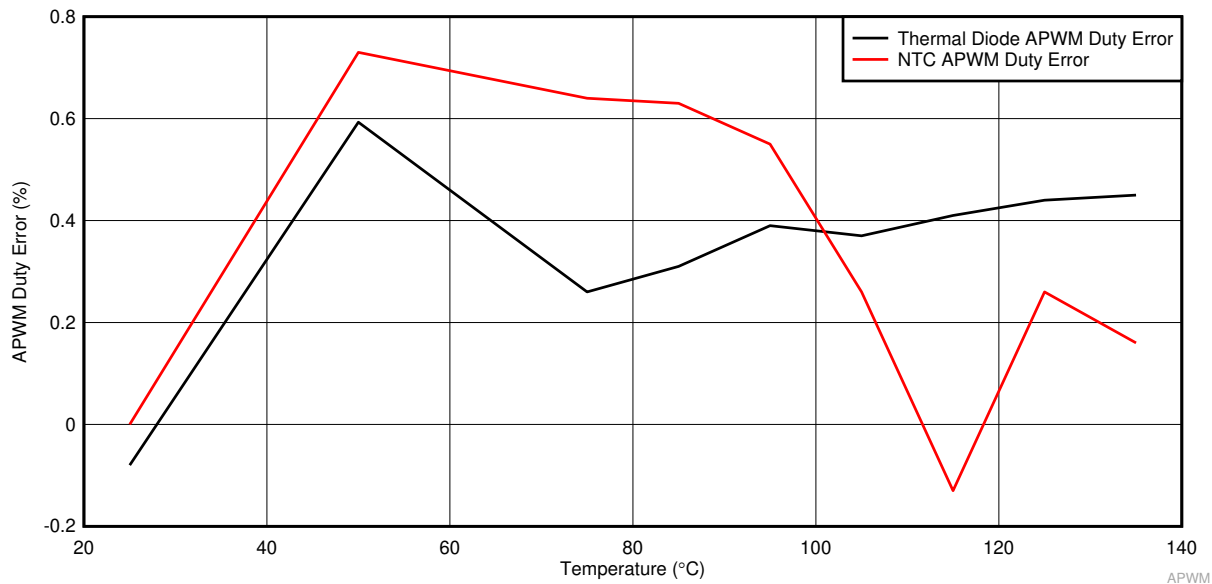


図 8-15. APWM Duty Error with Single-Point Calibration

8.2.2.8.2 Isolated DC Bus Voltage Sensing

The AIN to APWM channel may be used for other applications such as the DC-link voltage sensing, as shown in 図 8-16. The same filtering requirements as given above may be used in this case, as well. The number of attenuation resistors, R_{atten_1} through R_{atten_n} , is dependent on the voltage level and power rating of the resistor. The voltage is finally measured across R_{LV_DC} to monitor the stepped-down voltage of the HV DC-link which must fall within the voltage range of AIN from 0.6 V to 4.5 V. The driver should be referenced to the same point as the measurement reference, thus in the case shown below the UCC21732-Q1 is driving the lower IGBT in the half-bridge and the DC-link voltage measurement is referenced to COM. The internal current source I_{AIN} should be taken into account when designing the resistor divider. The AIN pin voltage is:

$$V_{AIN} = \frac{R_{LV_DC}}{R_{LV_DC} + \sum_{i=1}^n R_{atten_i}} \cdot V_{DC} + R_{LV_DC} \cdot I_{AIN} \quad (14)$$

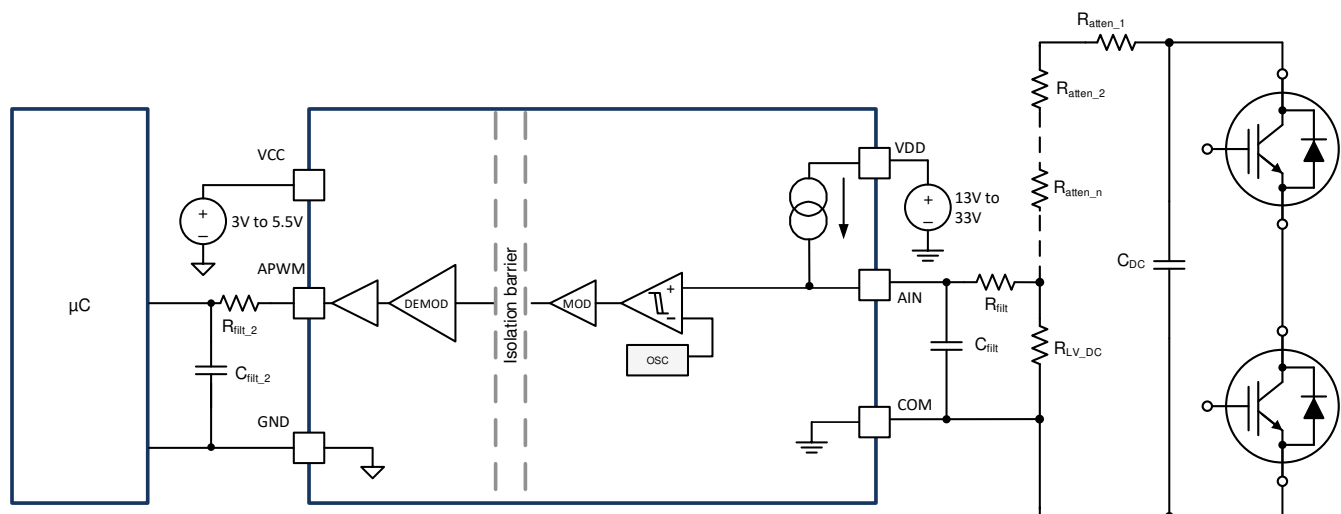


図 8-16. DC-Link Voltage Sensing Configuration

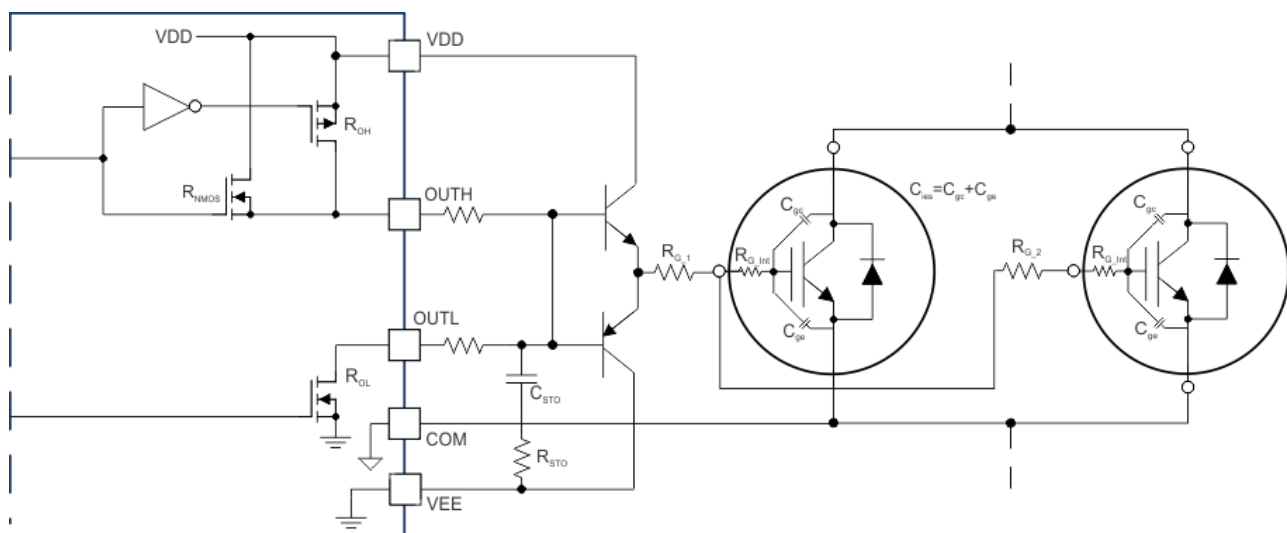
8.2.2.9 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the NPN/PNP buffer shown in 8-17) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for peak currents up to 15 A, the D44VH10/ D45VH10 pair is up to 20-A peak.

In the case of a overcurrent detection, the soft turn off (STO) is activated. External components must be added to implement STO instead of normal turn off speed when an external buffer is used. C_{STO} sets the timing for soft turn off and R_{STO} limits the inrush current to below the current rating of the internal FET (10A). R_{STO} should be at least $(VDD-VEE)/10$. The soft turn off timing is determined by the internal current source of 400 mA and the capacitor C_{STO} . C_{STO} is calculated using the following equation.

$$C_{STO} = \frac{I_{STO} \cdot t_{STO}}{VDD - VEE} \quad (15)$$

- I_{STO} is the the internal STO current source, 400 mA
- t_{STO} is the desired STO timing



8-17. Current Buffer for Increased Drive Strength

9 Power Supply Recommendations

During the turn on and turn off switching transient, the peak source and sink current is provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering the UCC21732-Q1 has ± 10 -A peak drive strength and can generate high dV/dt , a 10- μ F bypass cap is recommended between VDD and COM, VEE and COM. A 1- μ F bypass cap is recommended between VCC and GND due to less current comparing with output side power supplies. A 0.1- μ F decoupling cap is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD, and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

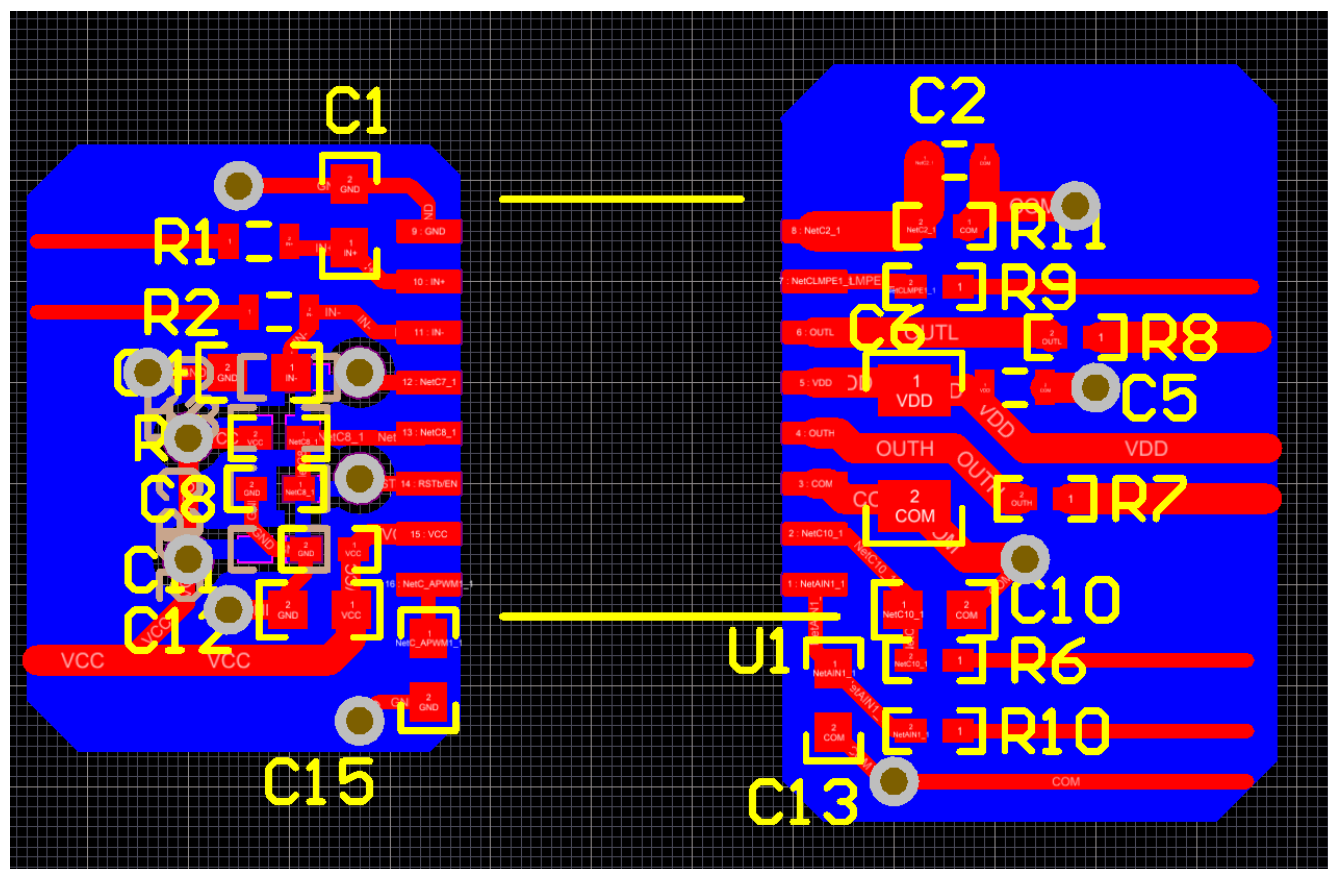
10 Layout

10.1 Layout Guidelines

Due to the strong drive strength of the UCC21732-Q1, careful considerations must be taken in PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high di/dt and voltage spike on the parasitic inductance of PCB traces.
- The driver COM pin should be connected to the Kelvin connection of SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow.
- If the gate driver is used for the low side switch which the COM pin connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high side switch, which the COM pin is connected to the switch node, ground plane is not recommended.
- If ground plane is not used on the output side, separate the return path of the OC and AIN ground loop from the gate loop ground which has large peak source and sink current.
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier.

10.2 Layout Example



☒ 10-1. Layout Example

11 Device and Documentation Support

11.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- [Isolation Glossary](#)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

11.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

11.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。






11.7 用語集

テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (September 2019) to Revision C (January 2024)	Page
• タイトルに車載用を追加.....	1
• AEC-Q100 認定の下に副項目を追加.....	1
• 「特長」に「安全関連認証」を追加.....	1
• Added what to do with unused pins to Pin Functions table.....	3
• Changed recommended value of decoupling capacitors in Pin Functions table.....	3
• Added recommended decoupling capacitor layout placement in Pin Functions table.	3
• Changed insulation voltage according to the latest standard.....	6
• Changed certification status in Safety-Related Certifications.....	7
• Changed max safety input values in Safety Limiting Values.....	7
• Deleted short circuit clamping MAX values in Electrical Characteristics.....	8
• Changed V_{AIN} MIN value to 0.6V in Electrical Characteristics.....	8
• Changed rise and fall times in Switching Characteristics to correct data sheet draft errors.....	10
• Changed thermal derating curves in Insulation Characteristics Curves to reflect device characteristics.....	11
• Changed to correct Functional Block Diagram to reflect device characteristics.....	24
• Changed  7-5	28
• Removed 150ns from deglitch filter block.....	29
• Added function state showing gate driver turning on and changed RDY condition when VCC is PD in Function Table.	31
• Changed  8-8	40
• Changed  8-9	41
• Changed  8-10	42
• Deleted tie dot in  8-17	47

Changes from Revision A (April 2019) to Revision B (September 2019)	Page
• マーケティング ステータスを「事前情報」から「量産データ」に変更。.....	1

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC21732QDWQ1	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-40 to 125	UCC21732Q
UCC21732QDWRQ1	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21732Q
UCC21732QDWRQ1.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21732Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC21732-Q1 :

- Catalog : [UCC21732](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





DW0016B

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

NOTES:

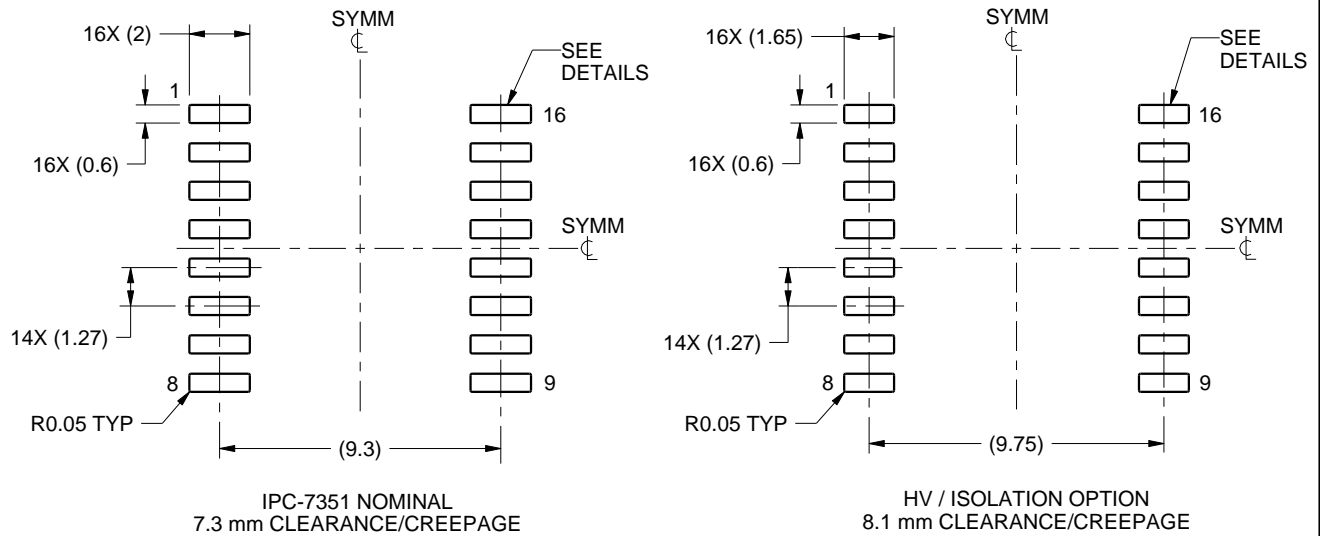
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

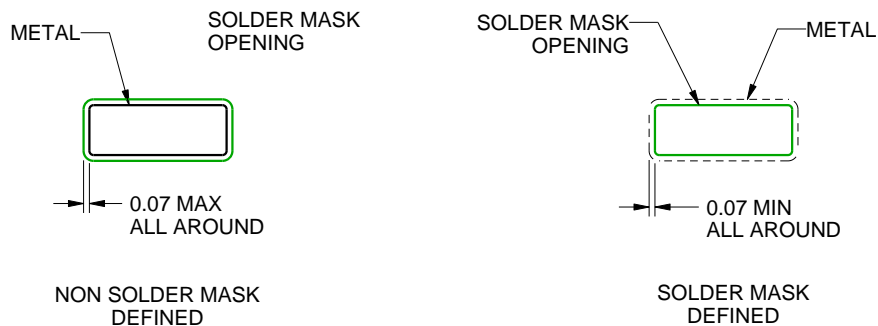
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

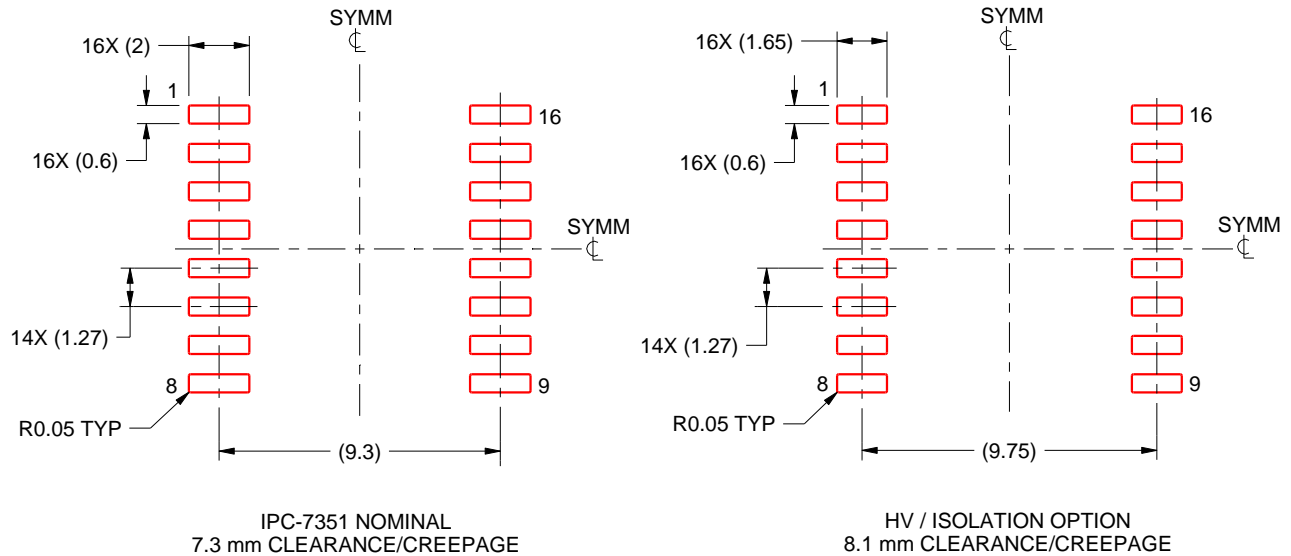
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含みいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](https://www.ti.com) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月