

# UCC23113 5A、5A、フォトカプラ互換シングル・チャンネル機能絶縁型ゲート・ドライバ、UVLO 搭載

## 1 特長

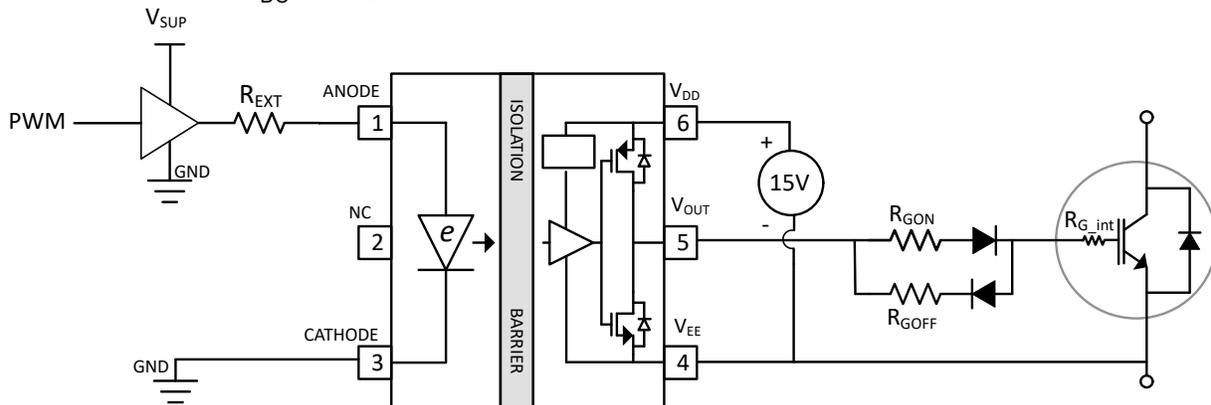
- フォトカプラ互換入力付き 1.5kV<sub>DC</sub> シングル・チャンネル絶縁型ゲート・ドライバ
- 光絶縁型ゲート・ドライバに対して、ピン互換でドロップイン・アップグレード可能
- ソース 5A、シンク 5A のピーク出力電流
- 最大 30V の出力ドライバ電源電圧
- 12V VDD 低電圧ロックアウト
- レール・ツー・レール出力
- 伝搬遅延時間：105ns 以下
- 部品間遅延ばらつき：25ns 以下
- パルス幅歪み：35ns 以下
- 同相過渡耐性 (CMTI)：100kV/μs 以上
- インターロック対応の入力段で 5V の逆極性電圧を処理可能
- 沿面距離と空間距離が 8.5mm を超える、ストレッチ SO-6 パッケージ
- 動作時の接合部温度、T<sub>J</sub>：-40°C ~ +150°C

## 2 アプリケーション

- 産業用モータ制御ドライブ
- ソーラー・インバータ
- 産業用電源、UPS
- 誘導加熱

## 3 概要

UCC23113 は、IGBT、MOSFET、SiC OSFET 用のフォトカプラ互換、シングル・チャンネル、絶縁型ゲート・ドライバです。ソース 5A、シンク 5A のピーク電流を出力でき、1.5kV<sub>DC</sub> の機能絶縁を備えています。



代表的なアプリケーション回路図

す。電源電圧範囲が 30V と高いため、バイポーラ電源を使用して IGBT および SiC パワー FET を効果的に駆動できます。UCC23113 は、ローサイドとハイサイドの両方のパワー FET を駆動できます。

主な機能と特性は、標準的なフォトカプラ・ベースのゲート・ドライバに比べて性能と信頼性を大幅に向上させると同時に、回路設計とレイアウト設計の両方でピン互換性を維持しています。特に、高い同相過渡耐性 (CMTI)、低伝搬遅延、小さなパルス幅歪みは、性能の大きな特長です。厳密なプロセス制御により、部品間スキューも小さくなっています。入力段はダイオード・エミュレーション (e-diode) であり、フォトカプラ・ゲート・ドライバで使われている従来型 LED に比べて、長期的な信頼性と優れた経時特性を実現します。本デバイスは、沿面距離と空間距離がどちらも 8.5mm を超え、材料グループ I (比較トラッキング指数 (CTI) > 600V) のモールド・コンパウンドを使用した、ストレッチ SO6 パッケージで供給されます。

UCC23113 は高性能で信頼性が高いため、あらゆる種類のモータ駆動、ソーラー・インバータ、産業用電源、電化製品に最適です。高い温度で動作するため、従来のフォトカプラでは対応できなかったアプリケーションで活用する機会が広がります。

### 製品情報

部品番号	パッケージ <sup>(1)</sup>	UVLO レベル
UCC23113CDWYR	ストレッチ SO-6	12V

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
August 2023	*	Initial Release

## 5 Pin Configuration and Function

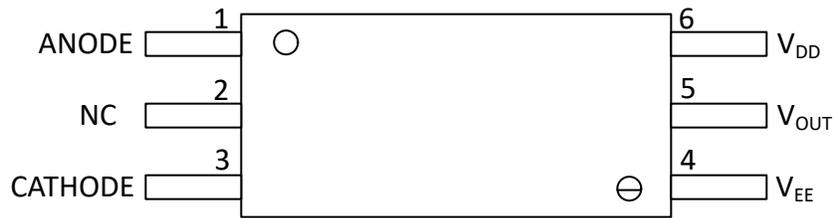


图 5-1. UCC23113 DWY Package SOIC-6 Top View

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
ANODE	1	I	Anode
CATHODE	3	I	Cathode
NC	2	-	No Connection
V <sub>DD</sub>	6	P	Positive output supply rail
V <sub>EE</sub>	4	P	Negative output supply rail
V <sub>OUT</sub>	5	O	Gate-drive output

(1) P = Power, G = Ground, I = Input, O = Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Average Input Current	$I_{F(AVG)}$	-	25	mA
Peak Transient Input Current	$I_{F(TRAN)} < 1\mu s \text{ pulse, } 300\text{pps}$		1	A
Reverse Input Voltage	$V_{R(MAX)}$		6	V
Output supply voltage	$V_{DD} - V_{EE}$	-0.3	36	V
Output DC Steady State Voltage	$V_{OUT(DC)}$	VEE-0.5	VDD+0.5	V
Output Transient Voltage	$V_{OUT(TRAN)}$	VEE-5	VDD+5	V
Junction temperature	$T_J$ <sup>(2)</sup>	-40	150	°C
Storage temperature	$T_{stg}$	-65	150	°C
Input-to-output operating voltage	$ V_{IO} $		1500	$V_{DC}$

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) To maintain the recommended operating conditions for  $T_J$ , see [セクション 6.4](#).

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Output Supply Voltage( $V_{DD} - V_{EE}$ ) - 12V UVLO	13		30	V
$I_F$ (ON)	Input Diode Forward Current (Diode "ON")	7		16	mA
$V_F$ (OFF)	Anode voltage - Cathode voltage (Diode "OFF")	-5		0.8	V
$T_J$	Junction temperature	-40		150	°C
$T_A$	Ambient temperature	-40		125	°C
$ V_{IO} $	Input-to-output operating voltage			1500	$V_{DC}$

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC23113		UNIT
		DWY (SOIC-6)		
		6 PINS		
$R_{qJA}$	Junction-to-ambient thermal resistance	138		°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	79.2		°C/W
$R_{qJB}$	Junction-to-board thermal resistance	76.4		°C/W
$Y_{JT}$	Junction-to-top characterization parameter	44.9		°C/W

## 6.4 Thermal Information (continued)

THERMAL METRIC <sup>(1)</sup>		UCC23113	UNIT
		DWY (SOIC-6)	
		6 PINS	
Y <sub>JB</sub>	Junction-to-board characterization parameter	72.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub>	Maximum power dissipation on input and output <sup>(1)</sup>	V <sub>DD</sub> - V <sub>EE</sub> = 20 V, I <sub>F</sub> = 10mA, 10-kHz, 50% duty cycle, square wave, 180-nF load, T <sub>A</sub> = 25°C			750	mW
P <sub>D1</sub>	Maximum input power dissipation <sup>(2)</sup>				10	mW
P <sub>D2</sub>	Maximum output power dissipation				740	mW

- (1) Derate at 6 mW/°C beyond 25°C ambient temperature  
 (2) Recommended maximum P<sub>D1</sub> = 40mW. Absolute maximum P<sub>D1</sub> = 55mW

## 6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	>8.5	mm
CPG	External Creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	>8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material Group	According to IEC 60664-1	I	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(2)</sup>		0.5	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(2)</sup>		>10 <sup>9</sup>	Ω

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
- (2) All pins on each side of the barrier tied together creating a two-pin device.

## 6.7 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD}-V_{EE} = 15\text{V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT</b>						
$I_{FLH}$	Input Forward Threshold Current Low to High	$V_{DD} - V_{EE} = 15\text{V}$	1.5	2.8	4	mA
$V_F$	Input Forward Voltage	$I_F = 10\text{ mA}$	1.8	2.1	2.4	V
$\Delta V_F/\Delta T$	Temp Coefficient of Input Forward Voltage	$I_F = 10\text{ mA}$		1	1.35	mV/°C
$V_R$	Input Reverse Breakdown Voltage	$I_R = 10\text{ }\mu\text{A}$	6			V
$C_{IN}$	Input Capacitance	$F = 0.5\text{ MHz}$		15		pF
<b>OUTPUT</b>						
$I_{OH}$	Output Peak Source Current	$I_F = 10\text{ mA}$ , $V_{DD} = 15\text{V}$ , $C_{LOAD} = 0.18\text{ }\mu\text{F}$ , $C_{VDD} = 10\text{ }\mu\text{F}$ , pulse width $< 10\text{ }\mu\text{s}$		5		A
$I_{OL}$	Output Peak Sink Current	$V_F = 0\text{ V}$ , $V_{DD} = 15\text{V}$ , $C_{LOAD} = 0.18\text{ }\mu\text{F}$ , $C_{VDD} = 10\text{ }\mu\text{F}$ , pulse width $< 10\text{ }\mu\text{s}$		5		A
$V_{OH}$	High Level Output Voltage	$I_F = 10\text{ mA}$ , $I_O = -20\text{ mA}$	VDD-0.07	VDD-0.18	VDD-0.36	V
		$I_F = 10\text{ mA}$ , $I_O = 0\text{ mA}$	VDD			V
$V_{OL}$	Low Level Output Voltage	$V_F = 0\text{ V}$ , $I_O = 20\text{ mA}$			25	mV
$I_{DD\_H}$	Output Supply Current (Diode On)	$I_F = 10\text{ mA}$ , $I_O = 0\text{ mA}$			2.2	mA
$I_{DD\_L}$	Output Supply Current (Diode Off)	$V_F = 0\text{ V}$ , $I_O = 0\text{ mA}$			2	mA
<b>UNDER VOLTAGE LOCKOUT</b>						
UVLOR	Under Voltage Lockout $V_{DD}$ rising (12V UVLO)	$I_F = 10\text{ mA}$	11	12.5	13.5	V
UVLOF	Under Voltage Lockout $V_{DD}$ falling (12V UVLO)	$I_F = 10\text{ mA}$	10	11.5	12.5	V
UVLOHYS	UVLO Hysteresis (12V UVLO)	$I_F = 10\text{ mA}$		1.0		V

## 6.8 Switching Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at  $T_A = 25^\circ\text{C}$ ,  $V_{DD}-V_{EE} = 15\text{V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output-signal Rise Time	$C_g = 1\text{ nF}$ $F_{SW} = 20\text{ kHz}$ , (50% Duty Cycle) $V_{DD} = 15\text{V}$			28	ns
$t_f$	Output-signal Fall Time				25	ns
$t_{PLH}$	Propagation Delay, Low to High			70	105	ns
$t_{PHL}$	Propagation Delay, High to Low			70	105	ns
$t_{PWD}$	Pulse Width Distortion $ t_{PHL} - t_{PLH} $				35	ns
$t_{sk(pp)}$	Part-to-Part Skew in Propagation Delay Between any Two Parts <sup>(1)</sup>	$C_g = \text{open}$ $F_{SW} = 20\text{ kHz}$ , (50% Duty Cycle) $V_{DD} = 15\text{V}$ , $I_F = 10\text{ mA}$			25	ns
$t_{UVLO\_rec}$	UVLO Recovery Delay	$V_{DD}$ rising from 0V to 15V		20	30	$\mu\text{s}$
CMT <sub>H</sub>	Common-mode Transient Immunity (Output High)	$I_F = 10\text{ mA}$ , $V_{CM} = 1500\text{ V}$ , $V_{DD} = 30\text{V}$ , $T_A = 25^\circ\text{C}$	100			V/ns
CMT <sub>L</sub>	Common-mode Transient Immunity (Output Low)	$V_F = 0\text{ V}$ , $V_{CM} = 1500\text{ V}$ , $V_{DD} = 30\text{V}$ , $T_A = 25^\circ\text{C}$	100			V/ns

(1)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads ensured by characterization.

## 6.9 Typical Characteristics

$V_{DD} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{DD}$  to  $V_{EE}$ ,  $C_{LOAD} = 1\text{ nF}$  for timing tests and  $180\text{ nF}$  for  $I_{OH}$  and  $I_{OL}$  tests,  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ , (unless otherwise noted)

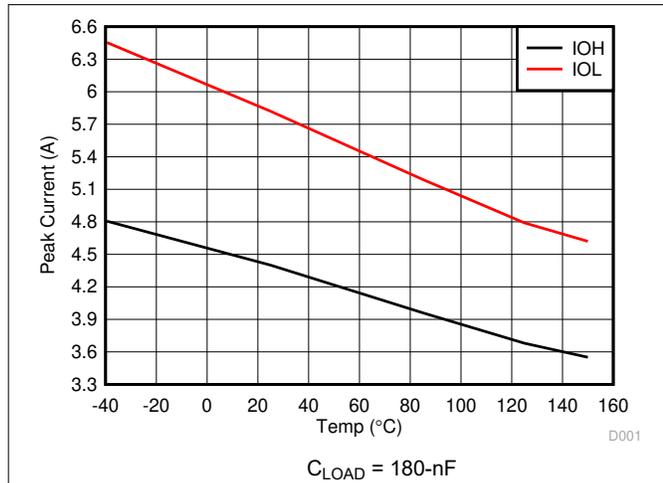


Figure 6-1. Output Drive Currents vs Temperature

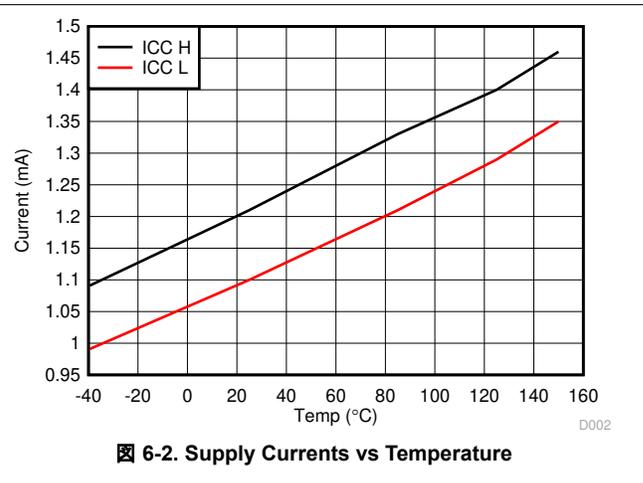


Figure 6-2. Supply Currents vs Temperature

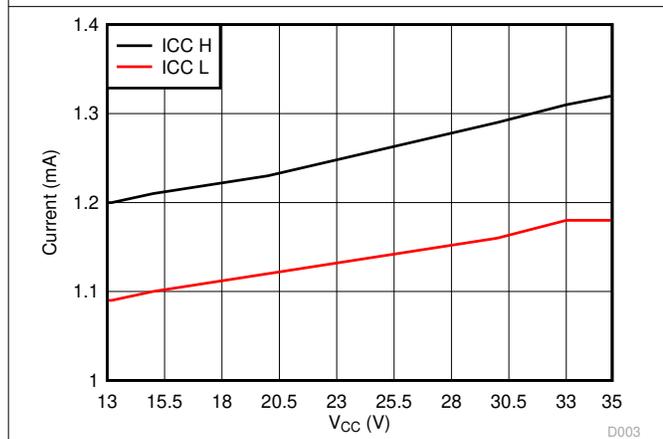


Figure 6-3. Supply Current vs Supply Voltage

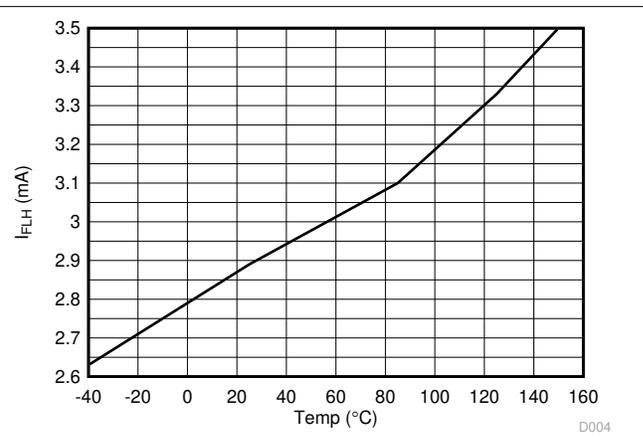


Figure 6-4. Forward Threshold Current vs Temperature

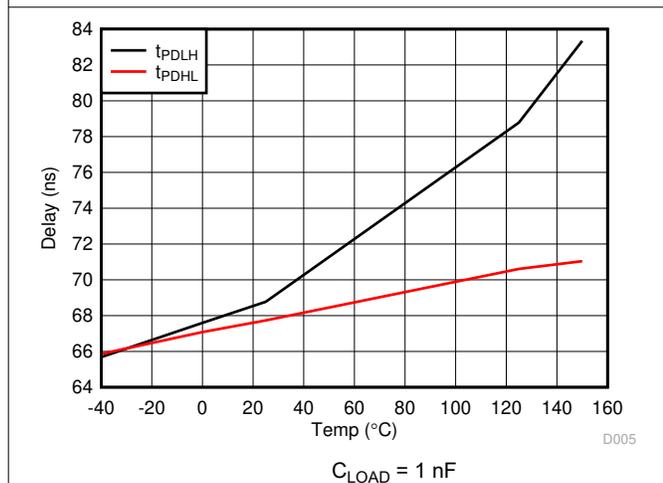


Figure 6-5. Propagation Delay vs Temperature

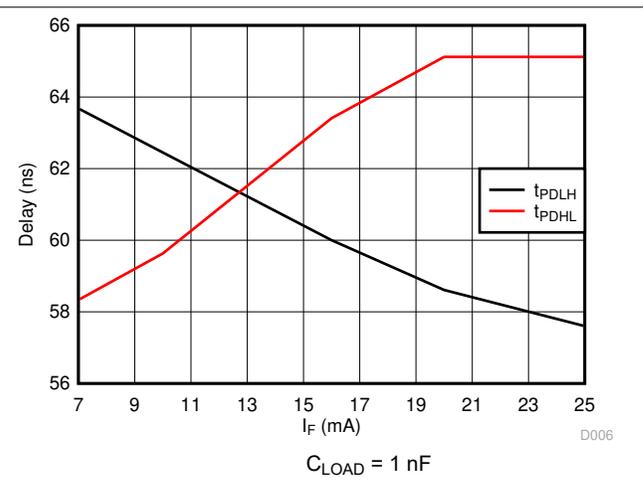


Figure 6-6. Propagation Delay vs Forward Current

### 6.9 Typical Characteristics (continued)

$V_{DD} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{DD}$  to  $V_{EE}$ ,  $C_{LOAD} = 1\text{ nF}$  for timing tests and  $180\text{ nF}$  for  $I_{OH}$  and  $I_{OL}$  tests,  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ , (unless otherwise noted)

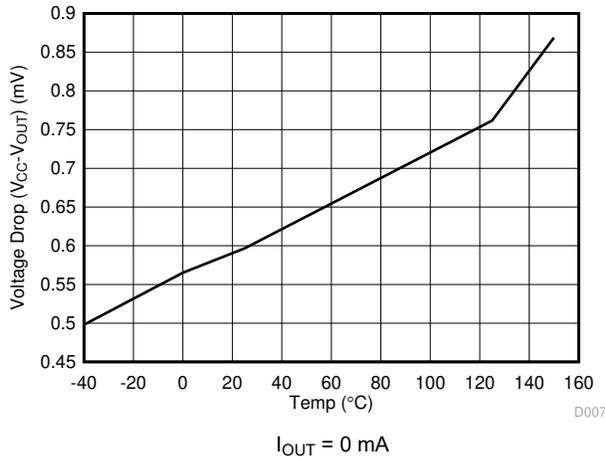


图 6-7.  $V_{OH}$  (No Load) vs Temperature

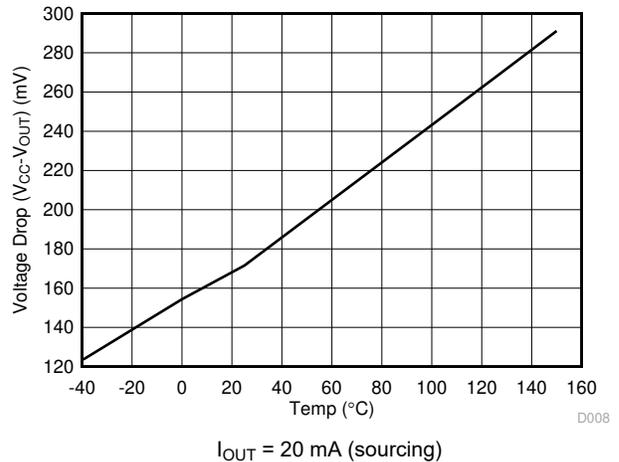


图 6-8.  $V_{OH}$  (20mA Load) vs Temperature

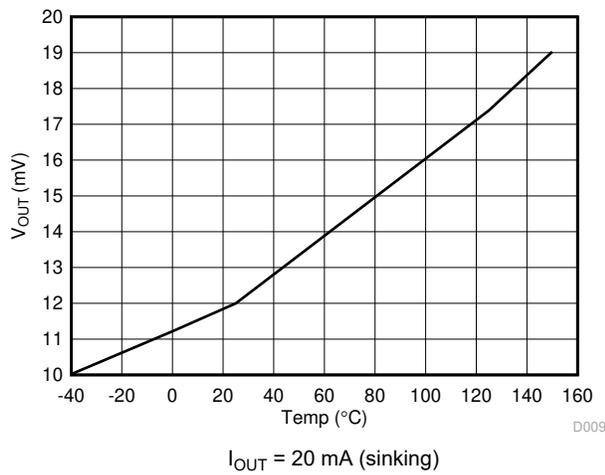


图 6-9.  $V_{OL}$  vs Temperature

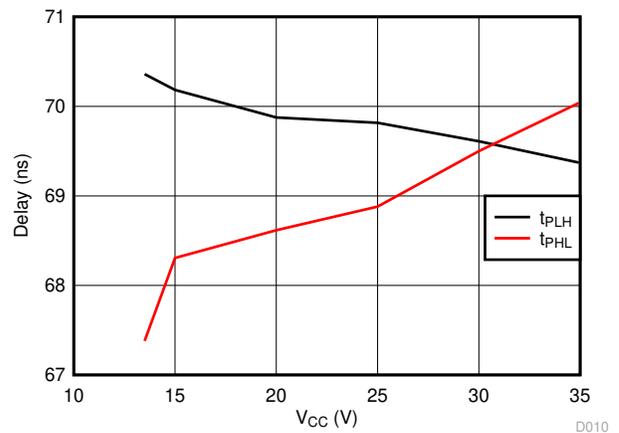


图 6-10. Propagation Delay vs Supply Voltage

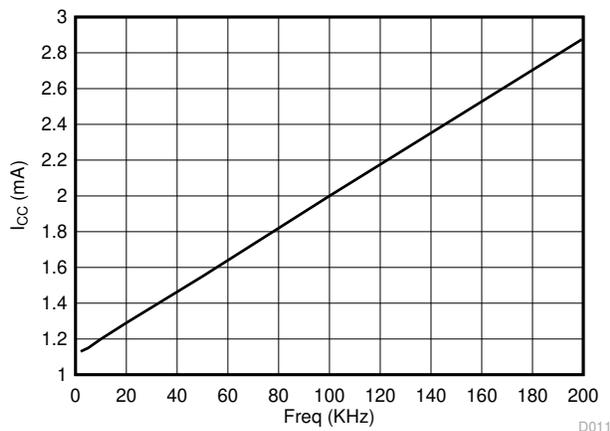


图 6-11. Supply Current vs Frequency

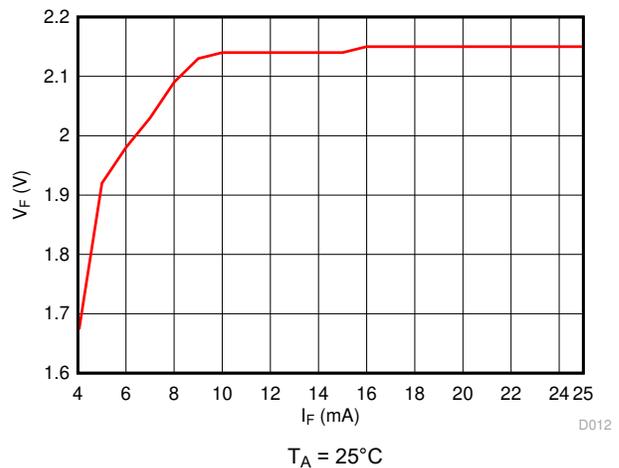
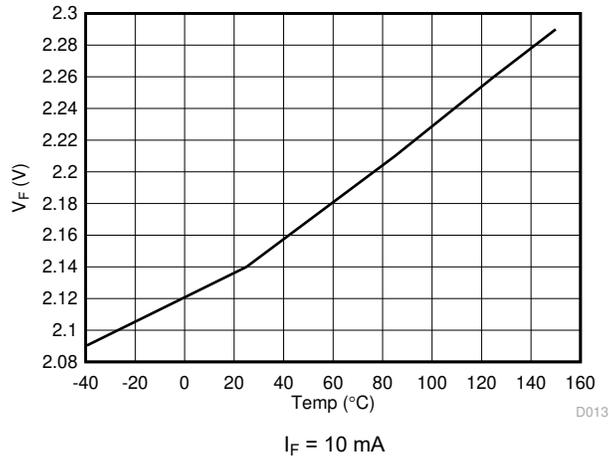


图 6-12. Forward Current vs Forward Voltage Drop

### 6.9 Typical Characteristics (continued)

$V_{DD} = 15\text{ V}$ ,  $1\text{-}\mu\text{F}$  capacitor from  $V_{DD}$  to  $V_{EE}$ ,  $C_{LOAD} = 1\text{ nF}$  for timing tests and  $180\text{ nF}$  for  $I_{OH}$  and  $I_{OL}$  tests,  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ , (unless otherwise noted)



**6-13. Forward Voltage Drop vs Temperature**

## 7 Parameter Measurement Information

### 7.1 Propagation Delay, Rise Time and Fall Time

Figure 7-1 shows the propagation delay from the input forward current  $I_F$  to  $V_{OUT}$ . This figure also shows the circuit used to measure the rise ( $t_r$ ) and fall ( $t_f$ ) times and the propagation delays  $t_{PD,LH}$  and  $t_{PD,HL}$ .

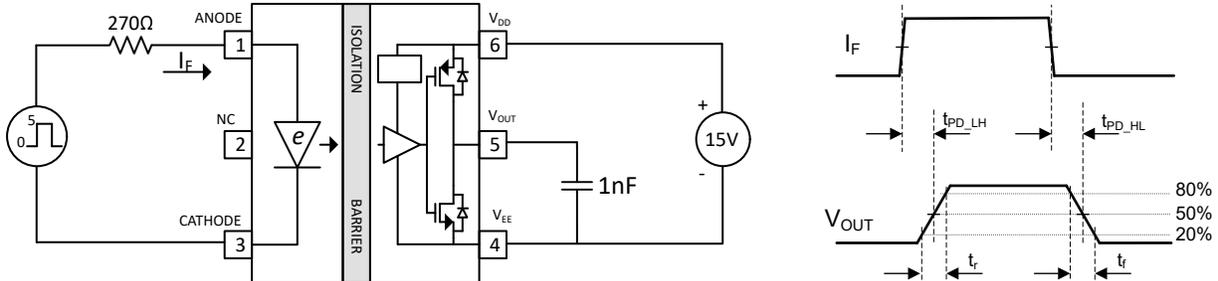


Figure 7-1.  $I_F$  to  $V_{OUT}$  Propagation Delay, Rise Time and Fall Time

### 7.2 $I_{OH}$ and $I_{OL}$ testing

Figure 7-2 shows the circuit used to measure the output drive currents  $I_{OH}$  and  $I_{OL}$ . A load capacitance of 180nF is used at the output. The peak  $dv/dt$  of the capacitor voltage is measured in order to determine the peak source and sink currents of the gate driver.

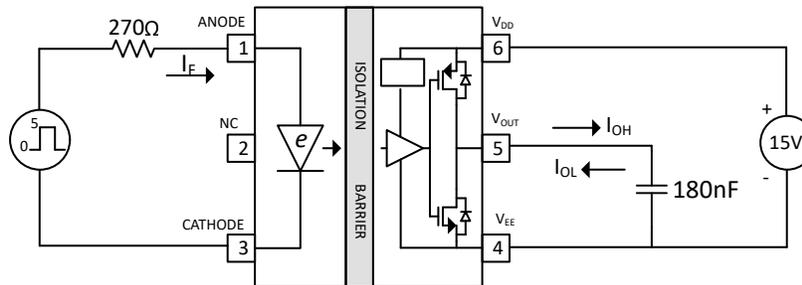


Figure 7-2.  $I_{OH}$  and  $I_{OL}$

### 7.3 CMTI Testing

Figure 7-3 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1500V. The test is performed with  $I_F = 10\text{mA}$  ( $V_{OUT} = \text{High}$ ) and  $I_F = 0\text{mA}$  ( $V_{OUT} = \text{LOW}$ ). The diagram also shows the fail criteria for both cases. During the application on the CMTI pulse with  $I_F = 10\text{mA}$ , if  $V_{OUT}$  drops from  $V_{DD}$  to  $\frac{1}{2}V_{DD}$  it is considered as a failure. With  $I_F = 0\text{mA}$ , if  $V_{OUT}$  rises above 1V, it is considered as a failure.

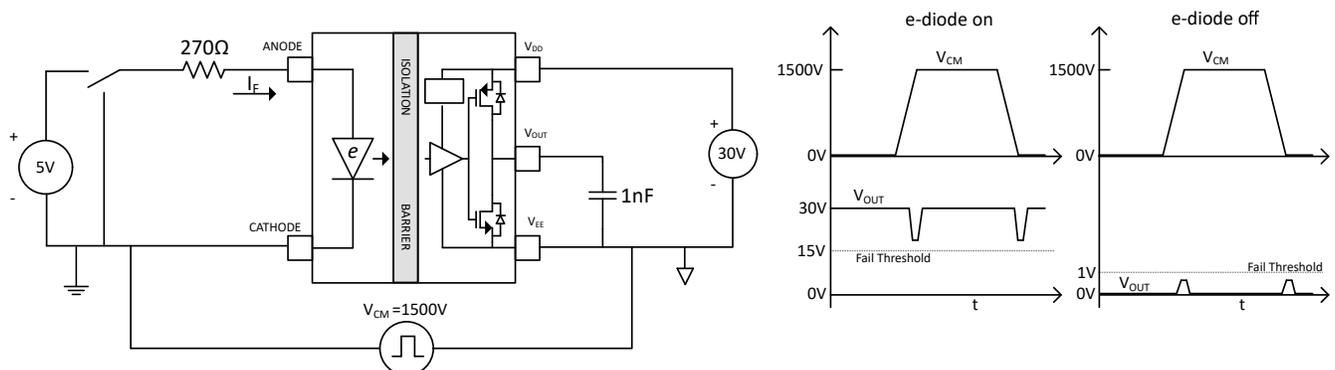


Figure 7-3. CMTI Test Circuit for UCC23113

## 8 Detailed Description

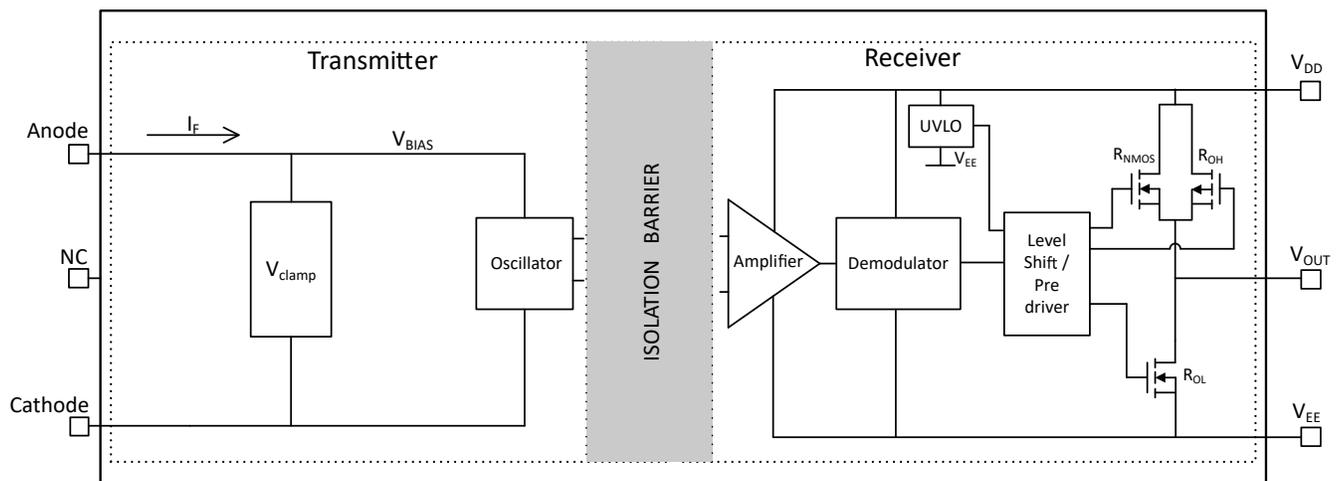
### 8.1 Overview

The UCC23113 is a single channel isolated gate driver, with an opto-compatible input stage, that can drive IGBTs, MOSFETs and SiC FETs. It has 5-A peak output current capability with max output driver supply voltage of 30 V. The inputs and the outputs are galvanically isolated. UCC23113 is offered in an industry standard 6 pin (SO6) package with >8.5 mm creepage and clearance. It has a working voltage of 1.5-kV<sub>DC</sub>. It is pin-to-pin compatible with standard opto isolated gate drivers. While standard opto isolated gate drivers use an LED as the input stage, UCC23113 uses an emulated diode (or "e-diode") as the input stage which does not use light emission to transmit signals across the isolation barrier. The input stage is isolated from the driver stage by dual, series HV SiO<sub>2</sub> capacitors in full differential configuration that offers best-in-class common mode transient immunity of > 100 kV/us. The e-diode input stage along with the isolation technology gives UCC23113 several performance advantages over standard opto isolated gate drivers. They are as follows:

1. Since the e-diode does not use light emission for its operation, the reliability and aging characteristics of UCC23113 are naturally superior to those of standard opto isolated gate drivers.
2. Higher ambient operating temperature range of 125°C, compared to only 105°C for most opto isolated gate drivers
3. The e-diode forward voltage drop has less part-to-part variation and smaller variation across temperature. Hence, the operating point of the input stage is more stable and predictable across different parts and operating temperature.
4. Higher common mode transient immunity than opto isolated gate drivers
5. Smaller propagation delay than opto isolated gate drivers
6. Due to superior process controls achievable in UCC23113 isolation compared to opto isolation, there is less part-to-part skew in the prop delay, making the system design simpler and more robust
7. Smaller pulse width distortion than opto isolated gate drivers

The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see [Fig 8-1](#)). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC23113 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. [Fig 8-2](#) shows conceptual detail of how the OOK scheme works.

### 8.2 Functional Block Diagram



**Fig 8-1. Conceptual Block Diagram of a Isolated Gate Driver with an Opto Emulated Input Stage (SOIC-6 package)**

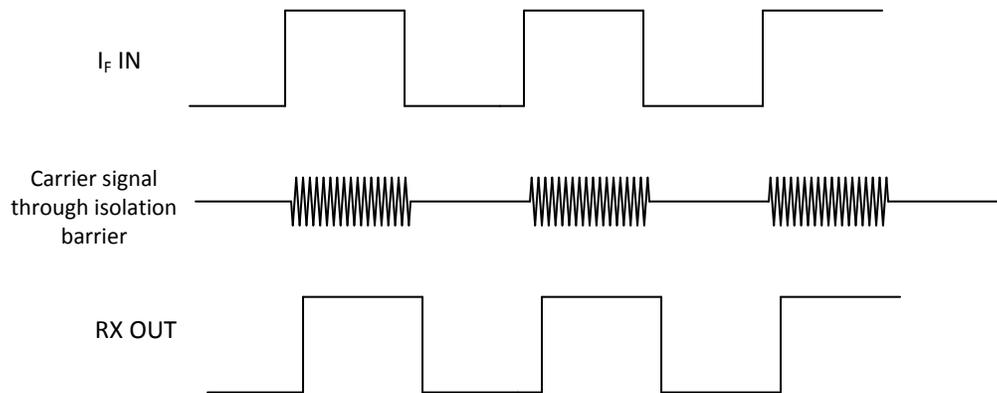


図 8-2. On-Off Keying (OOK) Based Modulation Scheme

## 8.3 Feature Description

### 8.3.1 Power Supply

Since the input stage is an emulated diode, no power supply is needed at the input.

The output supply,  $V_{DD}$ , supports a voltage range from 13 V to 30 V. For operation with bipolar supplies, the power device is turned off with a negative voltage on the gate with respect to the emitter or source. This configuration prevents the power device from unintentionally turning on because of current induced from the Miller effect. The typical values of the  $V_{DD}$  and  $V_{EE}$  output supplies for bipolar operation are 15 V and -8 V with respect to GND for IGBTs, and 20 V and -5 V for SiC MOSFETs.

For operation with unipolar supply, the  $V_{DD}$  supply is connected to 15 V with respect to GND for IGBTs, and 20 V for SiC MOSFETs. The  $V_{EE}$  supply is connected to 0 V.

### 8.3.2 Input Stage

The input stage of UCC23113 is simply the e-diode and therefore has an Anode (Pin 1) and a Cathode (Pin 3). Pin 2 has no internal connection and can be left open or connected to ground. The input stage does not have a power and ground pin. When the e-diode is forward biased by applying a positive voltage to the Anode with respect to the Cathode, a forward current  $I_F$  flows into the e-diode. The forward voltage drop across the e-diode is 2.1 V (typ). An external resistor should be used to limit the forward current. The recommended range for the forward current is 7 mA to 16 mA. When  $I_F$  exceeds the threshold current  $I_{FLH}$  (2.8 mA typ) a high frequency signal is transmitted across the isolation barrier through the high voltage  $\text{SiO}_2$  capacitors. The HF signal is detected by the receiver and  $V_{OUT}$  is driven high. See [セクション 9.2.2.1](#) for information on selecting the input resistor. The dynamic impedance of the e-diode is very small ( $<1.0 \Omega$ ) and the temperature coefficient of the e-diode forward voltage drop is  $<1.35 \text{ mV}/^\circ\text{C}$ . This leads to excellent stability of the forward current  $I_F$  across all operating conditions. If the Anode voltage drops below  $V_{F\_HL}$  (0.8 V), or reverse biased, the gate driver output is driven low. The reverse breakdown voltage of the e-diode is  $>6 \text{ V}$ . So for normal operation, a reverse bias of up to 5 V is allowed. The large reverse breakdown voltage of the e-diode enables UCC23113 to be operated in interlock architecture (see example in [図 8-3](#)) where  $V_{SUP}$  can be as high as 5 V. The system designer has the flexibility to choose a 3.3 V or 5.0 V PWM signal source to drive the input stage of UCC23113 using an appropriate input resistor. The example shows two gate drivers driving a set of IGBTs. The inputs of the gate drivers are connected as shown and driven by two buffers that are controlled by the MCU. Interlock architecture prevents both the e-diodes from being "ON" at the same time, preventing shoot through in the IGBTs. It also ensures that if both PWM signals are erroneously stuck high (or low) simultaneously, both gate driver outputs are driven low.

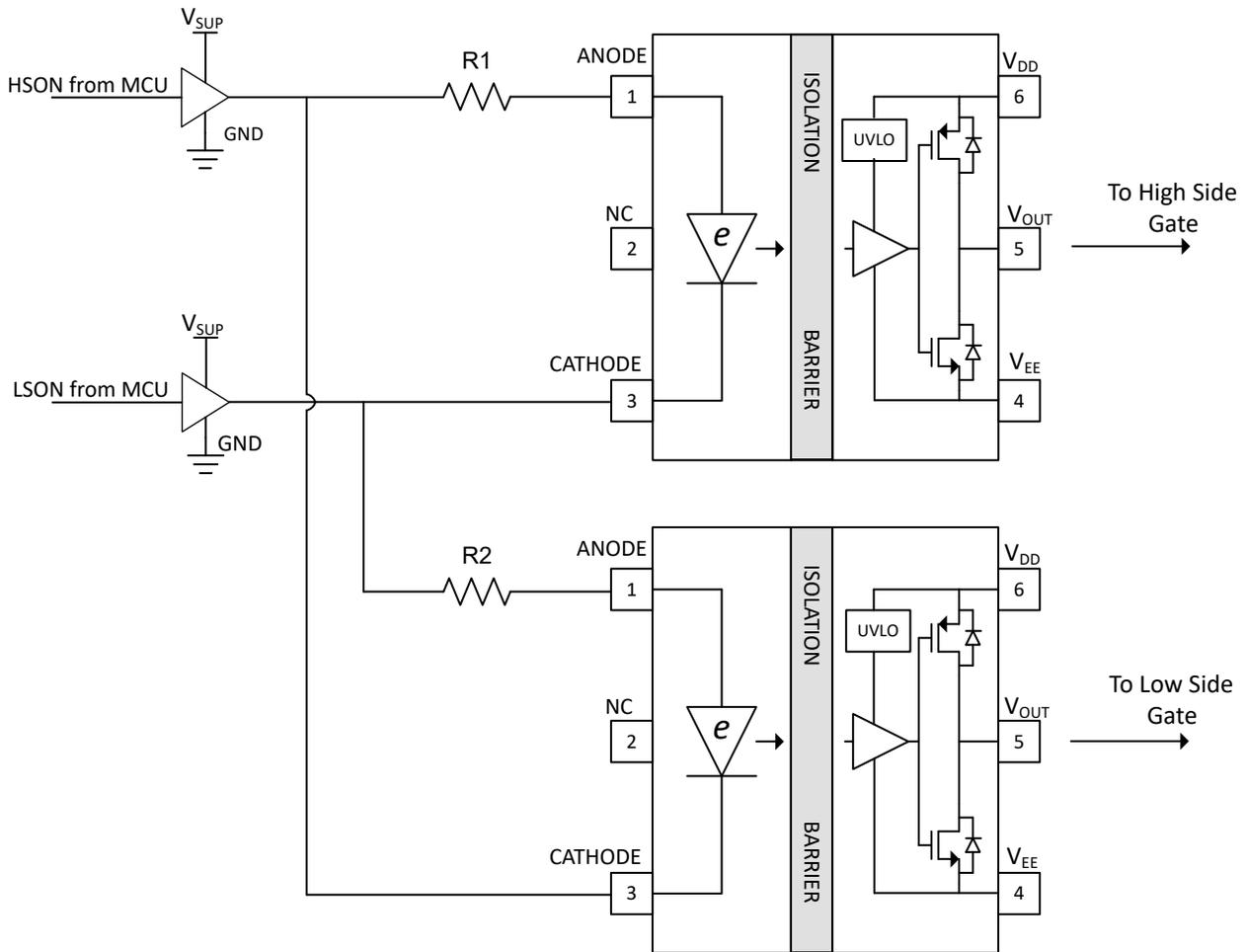


图 8-3. Interlock

### 8.3.3 Output Stage

The output stages of the UCC23113 family feature a pullup structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turnon transition (when the power-switch drain or collector voltage experiences  $dV/dt$ ). The output stage pullup structure features a P-channel MOSFET and an additional pull-up N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turnon. Fast turnon is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET ( $R_{NMOS}$ ) is approximately  $5.1 \Omega$  when activated.

表 8-1. UCC23113 On-Resistance

$R_{NMOS}$	$R_{OH}$	$R_{OL}$	UNIT
5.1	9.5	0.40	$\Omega$

The  $R_{OH}$  parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device because the pullup N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC23113 pullup stage during this brief turnon phase is much lower than what is represented by the  $R_{OH}$  parameter, yielding a faster turn on. The turnon-phase output resistance is the parallel combination  $R_{OH} \parallel R_{NMOS}$ .

The pulldown structure in the UCC23113 is simply composed of an N-channel MOSFET. The output voltage swing between  $V_{DD}$  and  $V_{EE}$  provides rail-to-rail operation because of the MOS-out stage which delivers very low dropout.

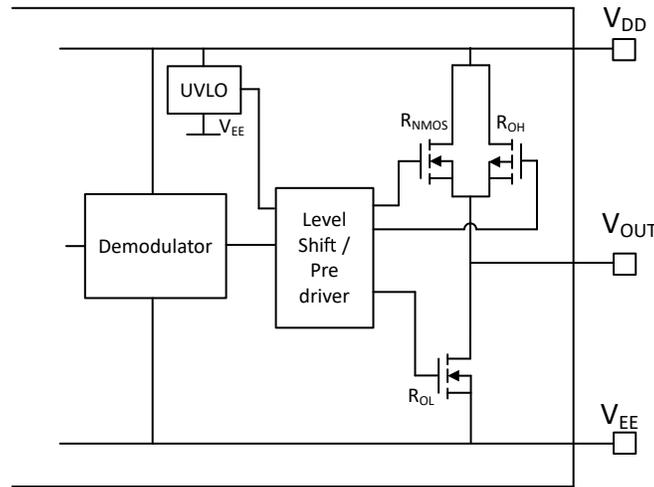


图 8-4. Output Stage

### 8.3.4 Protection Features

#### 8.3.4.1 Undervoltage Lockout (UVLO)

UVLO function is implemented for  $V_{DD}$  and  $V_{EE}$  pins to prevent an under-driven condition on IGBTs and MOSFETs. When  $V_{DD}$  is lower than  $UVLO_R$  at device start-up or lower than  $UVLO_F$  after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input forward current as shown in 表 8-2. The  $V_{DD}$  UVLO protection has a hysteresis feature ( $UVLO_{hys}$ ). This hysteresis prevents chatter when the power supply produces ground noise which allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly.

When  $V_{DD}$  drops below  $UVLO_F$ , a delay,  $t_{UVLO\_rec}$  occurs on the output when the supply voltage rises above  $UVLO_R$  again.

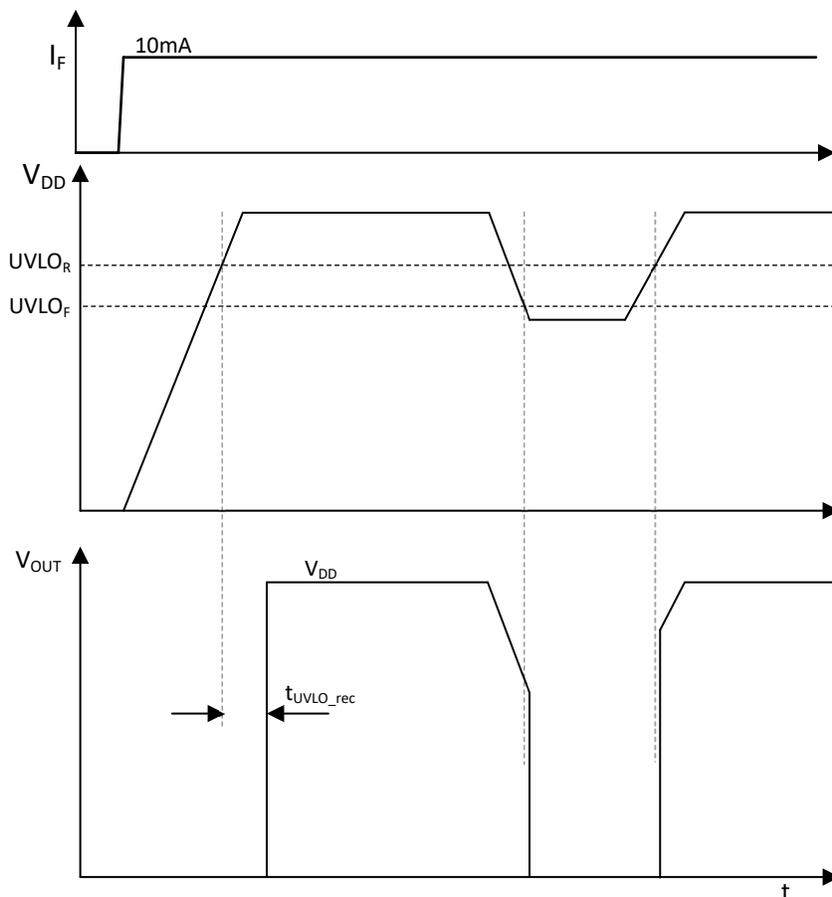


图 8-5. UVLO Functionality

### 8.3.4.2 Active Pulldown

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the  $V_{DD}$  supply. This feature prevents false IGBT and MOSFET turn-on by clamping  $V_{OUT}$  pin to approximately 2 V.

When the output stage of the driver is in an unbiased condition ( $V_{DD}$  floating), the driver outputs (see 图 8-4) are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS and NMOS are held off while the lower NMOS gate is tied to the driver output through an internal 500-k $\Omega$  resistor. In this configuration, the lower NMOS device effectively clamps the output ( $V_{OUT}$ ) to less than 2 V.

### 8.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the output pin  $V_{OUT}$  slightly higher than the  $V_{DD}$  voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the  $V_{DD}$  pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10  $\mu$ s and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

### 8.4 Device Functional Modes

表 8-2 和 表 8-3 list the functional modes for UCC23113.

**表 8-2. Function Table for UCC23113 with  $V_{DD}$  Rising**

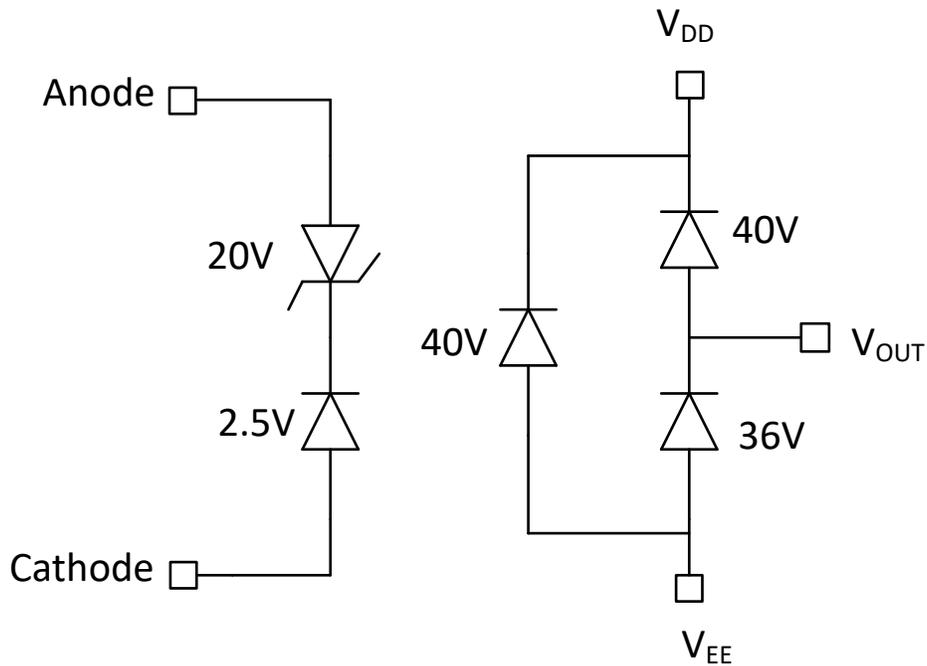
e-diode	$V_{DD}$	$V_{OUT}$
OFF ( $I_F < I_{FLH}$ )	0 V - 30 V	Low
ON ( $I_F > I_{FLH}$ )	0 V - $UVLO_R$	Low
ON ( $I_F > I_{FLH}$ )	$UVLO_R$ - 30 V	High

**表 8-3. Function Table for UCC23113 with  $V_{DD}$  Falling**

e-diode	$V_{DD}$	$V_{OUT}$
OFF ( $I_F < I_{FLH}$ )	0 V - 30 V	Low
ON ( $I_F > I_{FLH}$ )	$UVLO_F$ - 0 V	Low
ON ( $I_F > I_{FLH}$ )	30 V - $UVLO_F$	High

#### 8.4.1 ESD Structure

图 8-6 shows the multiple diodes involved in the ESD protection components of the UCC23113 device. This provides pictorial representation of the absolute maximum rating for the device.



**图 8-6. ESD Structure**

## 9 Application and Implementation

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### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 9.1 Application Information

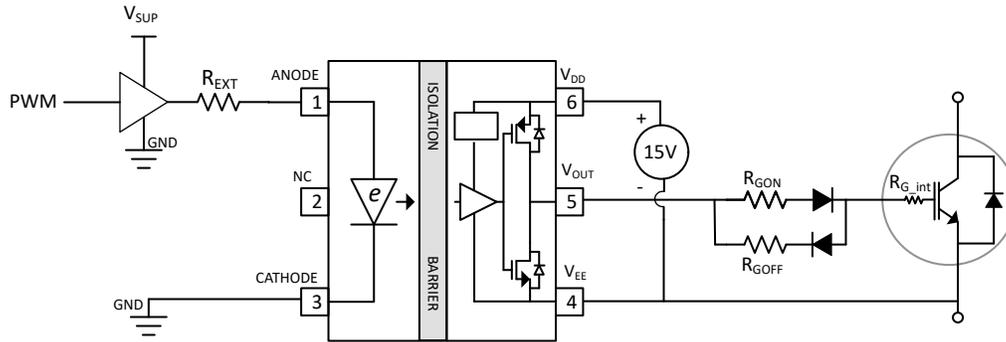
The UCC23113 is a single channel, isolated gate driver with opto-compatible input for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. It is intended for use in applications such as motor control, industrial inverters, and switched-mode power supplies. It differs from standard opto isolated gate drivers as it does not have an LED input stage. Instead of an LED, it has an emulated diode (e-diode). To turn the e-diode "ON", a forward current in the range of 7 mA to 16 mA should be driven into the Anode. This will drive the gate driver output High and turn on the power FET. Typically, MCUs are not capable of providing the required forward current. Hence a buffer has to be used between the MCU and the input stage of UCC23113. Typical buffer power supplies are either 5 V or 3.3 V. A resistor is needed between the buffer and the input stage of the UCC23113 to limit the current. It is simple, but important to choose the right value of resistance. The resistor tolerance, buffer supply voltage tolerance and output impedance of the buffer, have to be considered in the resistor selection. This will ensure that the e-diode forward current stays within the recommended range of 7 mA to 16 mA. Detailed design recommendations are given in the [セクション 9.1](#). The current driven input stage offers excellent noise immunity that is need in high power motor drive systems, especially in cases where the MCU cannot be located close to the isolated gate driver. UCC23113 offers best in class CMTI performance of >100 kV/ $\mu$ s at 1500 V common-mode voltages.

The e-diode is capable of 25 mA continuous in the forward direction. The forward voltage drop of the e-diode has a very tight part to part variation (1.8 V min to 2.4 V max). The temperature coefficient of the forward drop is <1.35 mV/ $^{\circ}$ C. The dynamic impedance of the e-diode in the forward biased region is  $\sim$ 1  $\Omega$ . All of these factors contribute in excellent stability of the e-diode forward current. To turn the e-diode "OFF", the Anode - Cathode voltage should be <0.8 V, or  $I_F$  should be < $I_{FLH}$ . The e-diode can also be reverse biased up to 5 V (6 V abs max) in order to turn it off and bring the gate driver output low. The large reverse breakdown voltage of the input stage provides system designers with the feature to use interlocking circuit and gain protection against shoot-through when driving a half-bridge power stage.

The output power supply for UCC23113 can be as high as 30 V (36 V abs max). The output power supply can be configured externally as a single isolated supply up to 30 V or isolated bipolar supply such that  $V_{DD}-V_{EE}$  does not exceed 30 V, or it can be bootstrapped (with external diode and capacitor) if the system uses a single power supply with respect to the power ground. Typical quiescent power supply current from  $V_{DD}$  is 1.2 mA (max 2.2 mA).

## 9.2 Typical Application

The circuit in [图 9-1](#), shows a typical application for driving IGBTs.



**图 9-1. Typical Application Circuit for UCC23113 to Drive IGBT**

### 9.2.1 Design Requirements

[表 9-1](#) lists the recommended conditions to observe the input and output of the UCC23113 gate driver.

**表 9-1. UCC23113 Design Requirements**

PARAMETER	VALUE	UNIT
$V_{DD}$	15	V
$I_F$	10	mA
Switching frequency	8	kHz



$$I_{OH} = \min \left[ 5A, \frac{V_{DD} - V_{GDF}}{R_{NMOS} \parallel [R_{OH} + R_{GON} + R_{GFET_{INT}}]} \right] \quad (2)$$

where

- $R_{GON}$  is the external turnon resistance.
- $R_{GFET_{Int}}$  is the power transistor internal gate resistance, found in the power transistor data sheet. Assume 0  $\Omega$  for this example.
- $I_{OH}$  is the peak source current which is the minimum value between 5 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance.
- $V_{GDF}$  is the forward voltage drop for each of the diodes in series with  $R_{GON}$  and  $R_{GOFF}$ . The diode drop for this example is 0.7 V.

In this example, the peak source current is approximately 1.7 A as calculated in [式 3](#).

$$I_{OH} = \min \left[ 5A, \frac{15 - 0.7}{5.1\Omega \parallel [9.5\Omega + 5\Omega + 0\Omega]} \right] = 1.72A \quad (3)$$

Similarly, use [式 4](#) to calculate the peak sink current.

$$I_{OL} = \min \left[ 5A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{GOFF} + R_{GFET_{INT}}} \right] \quad (4)$$

where

- $R_{GOFF}$  is the external turnoff resistance.
- $I_{OL}$  is the peak sink current which is the minimum value between 5 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak sink current is the minimum of 5 A and [式 5](#).

$$I_{OL} = \min \left[ 5A, \frac{15 - 0.7}{0.4\Omega + 10\Omega + 0\Omega} \right] = 1.38A \quad (5)$$

The diodes shown in series with each,  $R_{GON}$  and  $R_{GOFF}$ , in [图 9-1](#) ensure the gate drive current flows through the intended path, respectively, during turn-on and turn-off. Note that the diode forward drop reduces the voltage level at the gate of the power switch. To achieve rail-to-rail gate voltage levels, add a resistor from the  $V_{OUT}$  pin to the power switch gate, with a resistance value approximately 20 times higher than  $R_{GON}$  and  $R_{GOFF}$ . For the examples described in this section, a good choice is 100  $\Omega$  to 200  $\Omega$ .

### 注

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance ( $C_{ISS}$ ) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

#### 9.2.2.3 Estimate Gate-Driver Power Loss

The total loss,  $P_G$ , in the gate-driver subsystem includes the power losses ( $P_{GD}$ ) of the UCC23113 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The  $P_{GD}$  value is the key power loss which determines the thermal safety-related limits of the UCC23113 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss,  $P_{GDQ}$ , which includes power dissipated in the input stage ( $P_{GDQ_{IN}}$ ) as well as the quiescent power dissipated in the output stage ( $P_{GDQ_{OUT}}$ ) when operating with a certain

switching frequency under no load.  $P_{GDQ\_IN}$  is determined by  $I_F$  and  $V_F$  and is given by 式 6. The  $P_{GDQ\_OUT}$  parameter is measured on the bench with no load connected to  $V_{OUT}$  pin at a given  $V_{DD}$ , switching frequency, and ambient temperature. In this example,  $V_{DD}$  is 15 V. The current on the power supply, with PWM switching at 10 kHz, is measured to be  $I_{DD} = 1.33$  mA. Therefore, use 式 7 to calculate  $P_{GDQ\_OUT}$ .

$$P_{GDQ\_IN} = \frac{1}{2} \times V_F \times I_F \quad (6)$$

$$P_{GDQ\_OUT} = V_{DD} \times I_{DD} \quad (7)$$

The total quiescent power (without any load capacitance) dissipated in the gate driver is given by the sum of 式 6 and 式 7 as shown in 式 8.

$$P_{GDQ} = P_{GDQ\_IN} + P_{GDQ\_OUT} = 10\text{mW} + 20\text{mW} = 30\text{mW} \quad (8)$$

The second component is the switching operation loss,  $P_{GDSW}$ , with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use 式 9 to calculate the total dynamic loss from load switching,  $P_{GSW}$ .

$$P_{GSW} = V_{DD} \times Q_G \times f_{SW} \quad (9)$$

where

- $Q_G$  is the gate charge of the power transistor at  $V_{DD}$ .

So, for this example application the total dynamic loss from load switching is approximately 18 mW as calculated in 式 10.

$$P_{GSW} = 15\text{V} \times 120\text{nC} \times 10\text{kHz} = 18\text{mW} \quad (10)$$

$Q_G$  represents the total gate charge of the power transistor switching 520 V at 50 A, and is subject to change with different testing conditions. The UCC23113 gate-driver loss on the output stage,  $P_{GDO}$ , is part of  $P_{GSW}$ .  $P_{GDO}$  is equal to  $P_{GSW}$  if the external gate-driver resistance and power-transistor internal resistance are 0  $\Omega$ , and all the gate driver-loss will be dissipated inside the UCC23113. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 5 A/5 A, however, it will be non-linear if the source/sink current is saturated. Therefore,  $P_{GDO}$  is different in these two scenarios.

#### Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2} \left[ \frac{R_{OH} || R_{NMOS}}{R_{OH} || R_{NMOS} + R_{GON} + R_{GFET\_int}} + \frac{R_{OL}}{R_{OL} + R_{GOFF} + R_{GFET\_int}} \right] \quad (11)$$

In this design example, all the predicted source and sink currents are less than 5 A and 5 A, therefore, use 式 12 to estimate the UCC23113 gate-driver loss.

$$P_{GDO} = \frac{18\text{mW}}{2} \left[ \frac{9.5\Omega || 5.1\Omega}{9.5\Omega || 5.1\Omega + 5.1\Omega + 0\Omega} + \frac{0.4\Omega}{0.4\Omega + 10\Omega + 0\Omega} \right] \quad (12)$$

#### Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = f_{sw} \times \left[ \int_0^{T_{Rsys}} 5\text{A} \times (V_{DD} - V_{OUT}(t)) dt + \int_0^{T_{Rsys}} 5\text{A} \times V_{OUT}(t) dt \right] \quad (13)$$

where

- $V_{OUT(t)}$  is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (5 A at turnon and 5 A at turnoff) charging or discharging a load capacitor. Then, the  $V_{OUT(t)}$  waveform will be linear and the  $T_{R\_Sys}$  and  $T_{F\_Sys}$  can be easily predicted.

For some scenarios, if only one of the pullup or pulldown circuits is saturated and another one is not, the  $P_{GDO}$  is a combination of case 1 and case 2, and the equations can be easily identified for the pullup and pulldown based on this discussion.

Use 式 14 to calculate the total gate-driver loss dissipated in the UCC23113 gate driver,  $P_{GD}$ .

$$P_{GD} = P_{GDQ} + P_{GDO} = 30\text{mW} + 3.9\text{mW} = 33.9\text{mW} \quad (14)$$

#### 9.2.2.4 Estimating Junction Temperature

Use 式 15 to estimate the junction temperature ( $T_J$ ) of UCC23113.

$$T_J = T_C + \Psi_{JT} \times P_{GD} \quad (15)$$

where

- $T_C$  is the UCC23113 case-top temperature measured with a thermocouple or some other instrument.
- $\Psi_{JT}$  is the junction-to-top characterization parameter from the table.

Using the junction-to-top characterization parameter ( $\Psi_{JT}$ ) instead of the junction-to-case thermal resistance ( $R_{\theta JC}$ ) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The  $R_{\theta JC}$  resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of  $R_{\theta JC}$  will inaccurately estimate the true junction temperature. The  $\Psi_{JT}$  parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

#### 9.2.2.5 Selecting $V_{DD}$ Capacitor

Bypass capacitors for  $V_{DD}$  is essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances. A 50-V, 10- $\mu\text{F}$  MLCC and a 50-V, 0.22- $\mu\text{F}$  MLCC are selected for the  $C_{VDD}$  capacitor. If the bias power supply output is located a relatively long distance from the  $V_{DD}$  pin, a tantalum or electrolytic capacitor with a value greater than 10  $\mu\text{F}$  should be used in parallel with  $C_{VDD}$ .

#### 注

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1- $\mu\text{F}$  X7R capacitor is measured to be only 500 nF when a DC bias of 15  $V_{DC}$  is applied.

## 10 Power Supply Recommendations

The recommended input supply voltage ( $V_{DD}$ ) for the UCC23113 device is from 13 V to 30 V. The lower limit of the range of output bias-supply voltage ( $V_{DD}$ ) is determined by the internal UVLO protection feature of the device.  $V_{DD}$  voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low for more than 20  $\mu$ s by the UVLO protection feature. The higher limit of the  $V_{DD}$  range depends on the maximum gate voltage of the power device that is driven by the UCC23113 device, and should not exceed the recommended maximum  $V_{DD}$  of 30 V. A local bypass capacitor should be placed between the  $V_{DD}$  and  $V_{EE}$  pins, with a value of 220 nF to 10  $\mu$ F for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary side with the help of a transformer driver such as Texas Instruments' [SN6501](#) or [SN6505A](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501 Transformer Driver for Isolated Power Supplies data sheet](#) and [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies data sheet](#).

## 11 Layout

### 11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC23113. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the  $V_{DD}$  and  $V_{EE}$  pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the  $V_{EE}$  pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC23113 if the driving voltage is high, the load is heavy, or the switching frequency is high. Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance ( $\theta_{JB}$ ).
  - Increasing the PCB copper connecting to the  $V_{DD}$  and  $V_{EE}$  pins is recommended, with priority on maximizing the connection to  $V_{EE}$ . However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the  $V_{DD}$  and  $V_{EE}$  pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.



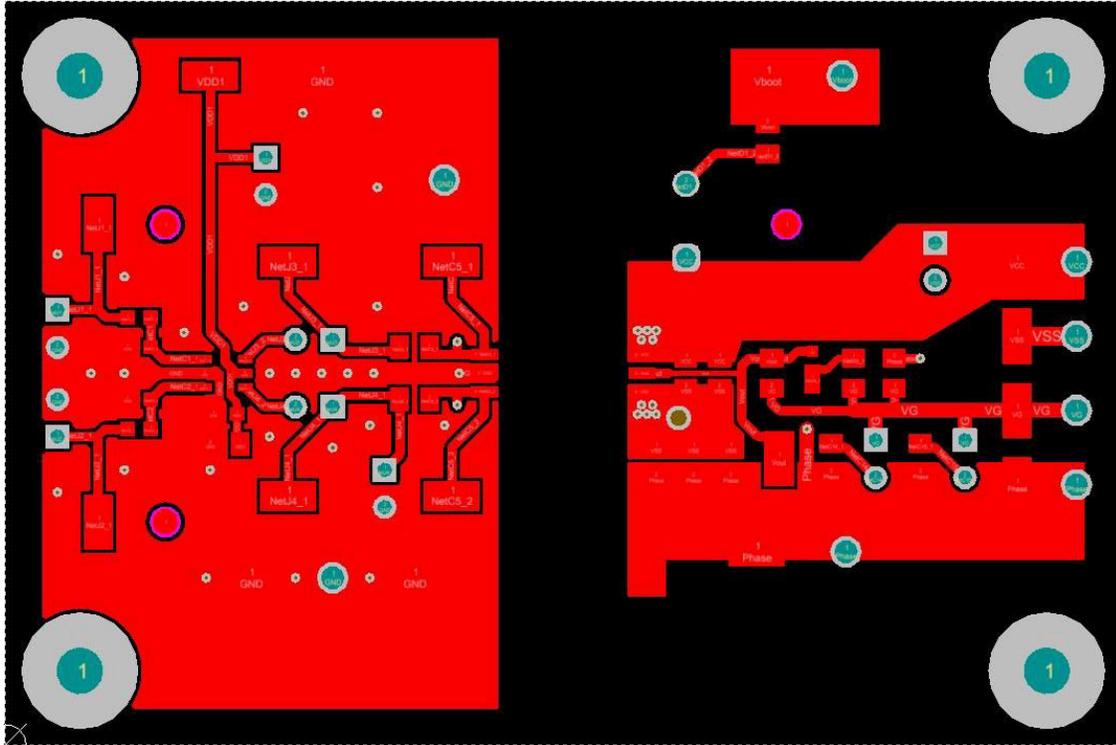


图 11-2. Top-Layer Traces and Copper

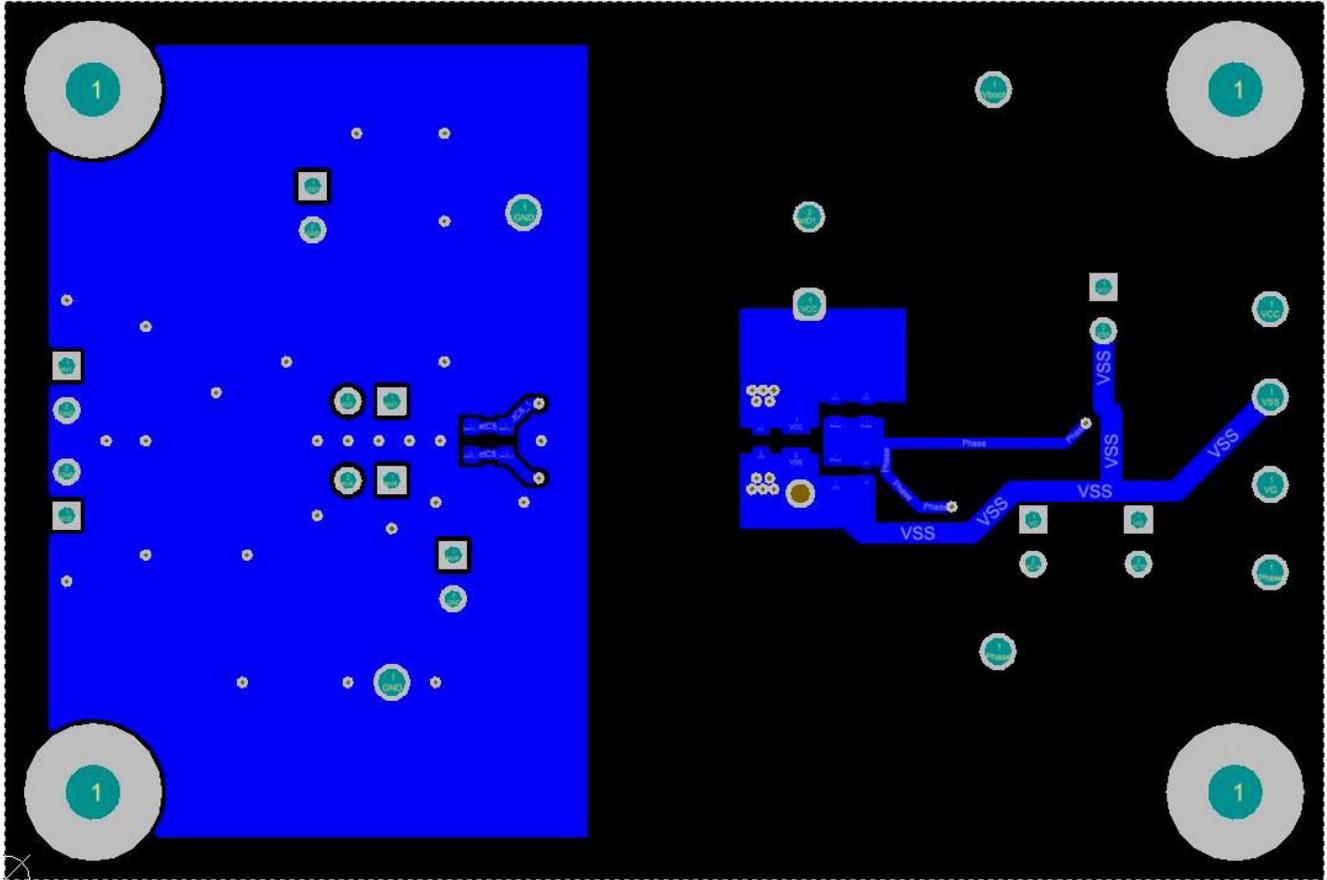
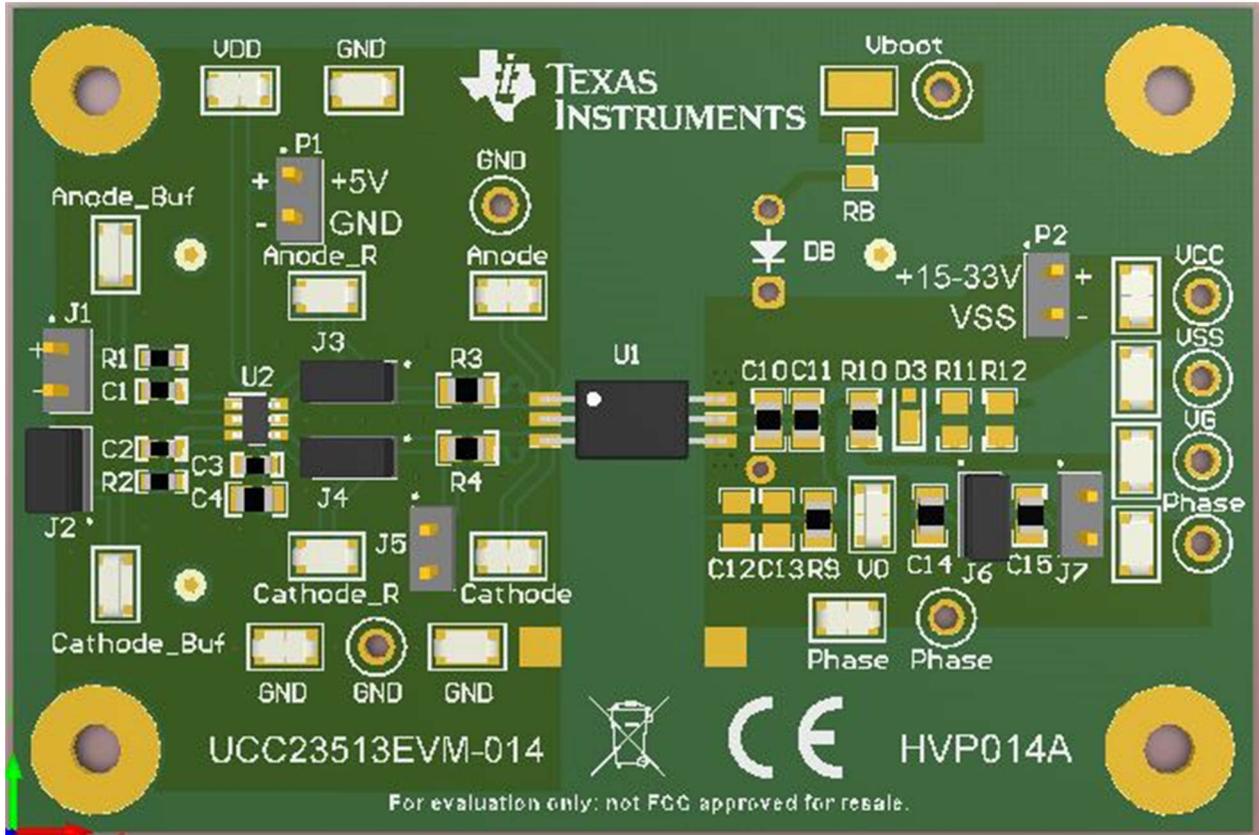


图 11-3. Bottom-Layer Traces and Copper (Flipped)

图 11-4 shows the 3D layout of the top view of the PCB.



11-4. 3-D PCB View

### 11.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 サード・パーティ製品に関する免責事項

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#### 12.1.2 Development Support

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation see the following:

- [Digital Isolator Design Guide](#)
- [Isolation Glossary](#)
- [SN6501 Transformer Driver for Isolated Power Supplies](#)
- [SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies](#)

#### 12.3 ドキュメントの更新通知を受け取る方法

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#### 12.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

#### 12.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">UCC23113DWYR</a>	Active	Production	SOIC (DWY)   6	850   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC23113
UCC23113DWYR.A	Active	Production	SOIC (DWY)   6	850   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC23113

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

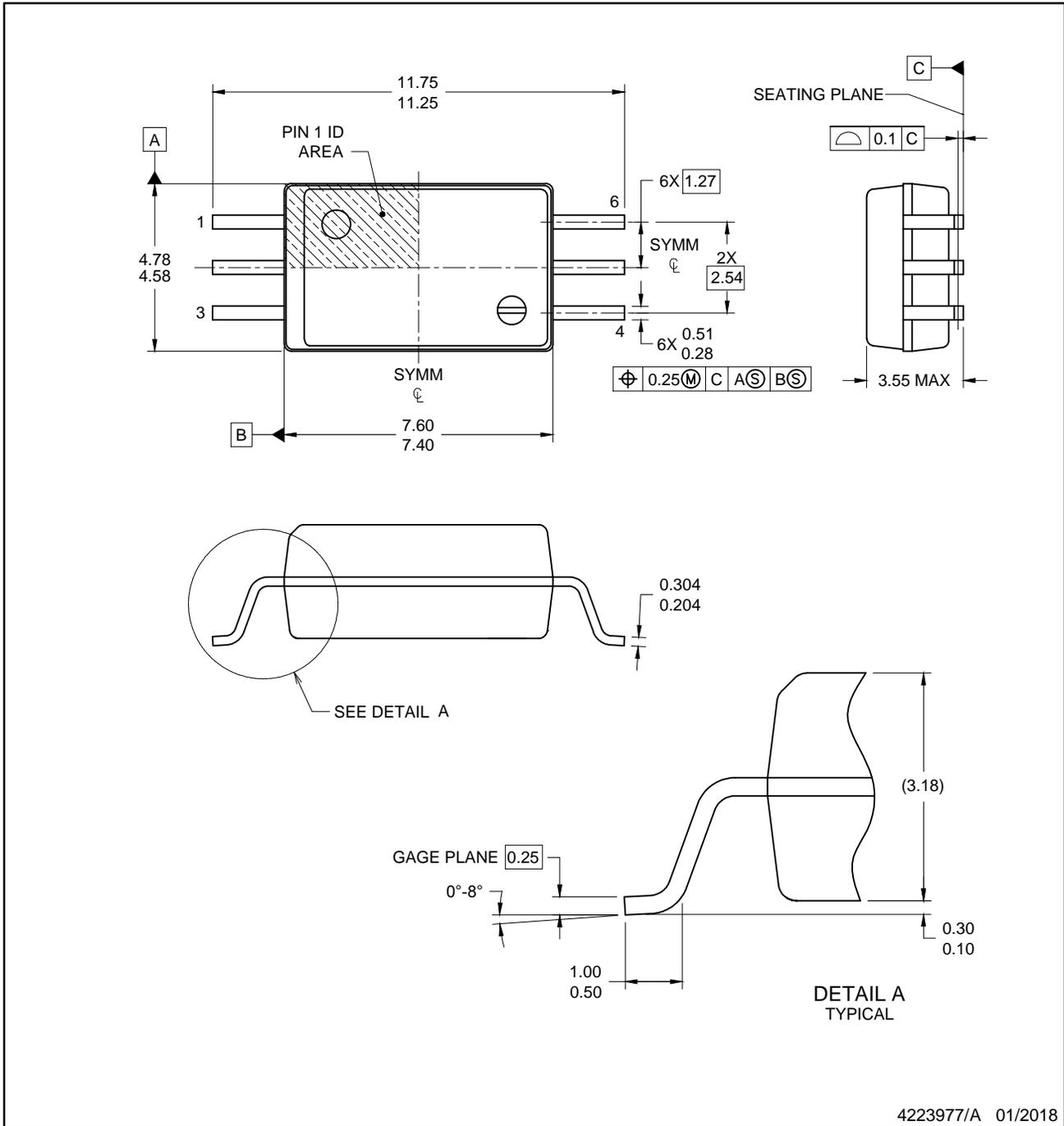
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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NOTES:

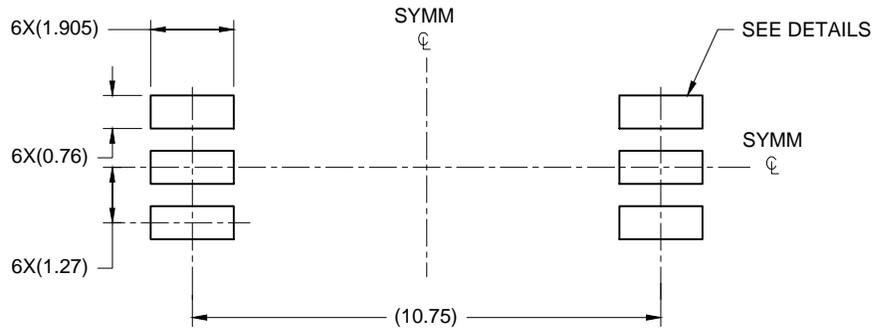
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.70 per side.

# EXAMPLE BOARD LAYOUT

SOIC - 3.55 mm max height

DWY0006A

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4223977/A 01/2018

NOTES: (continued)

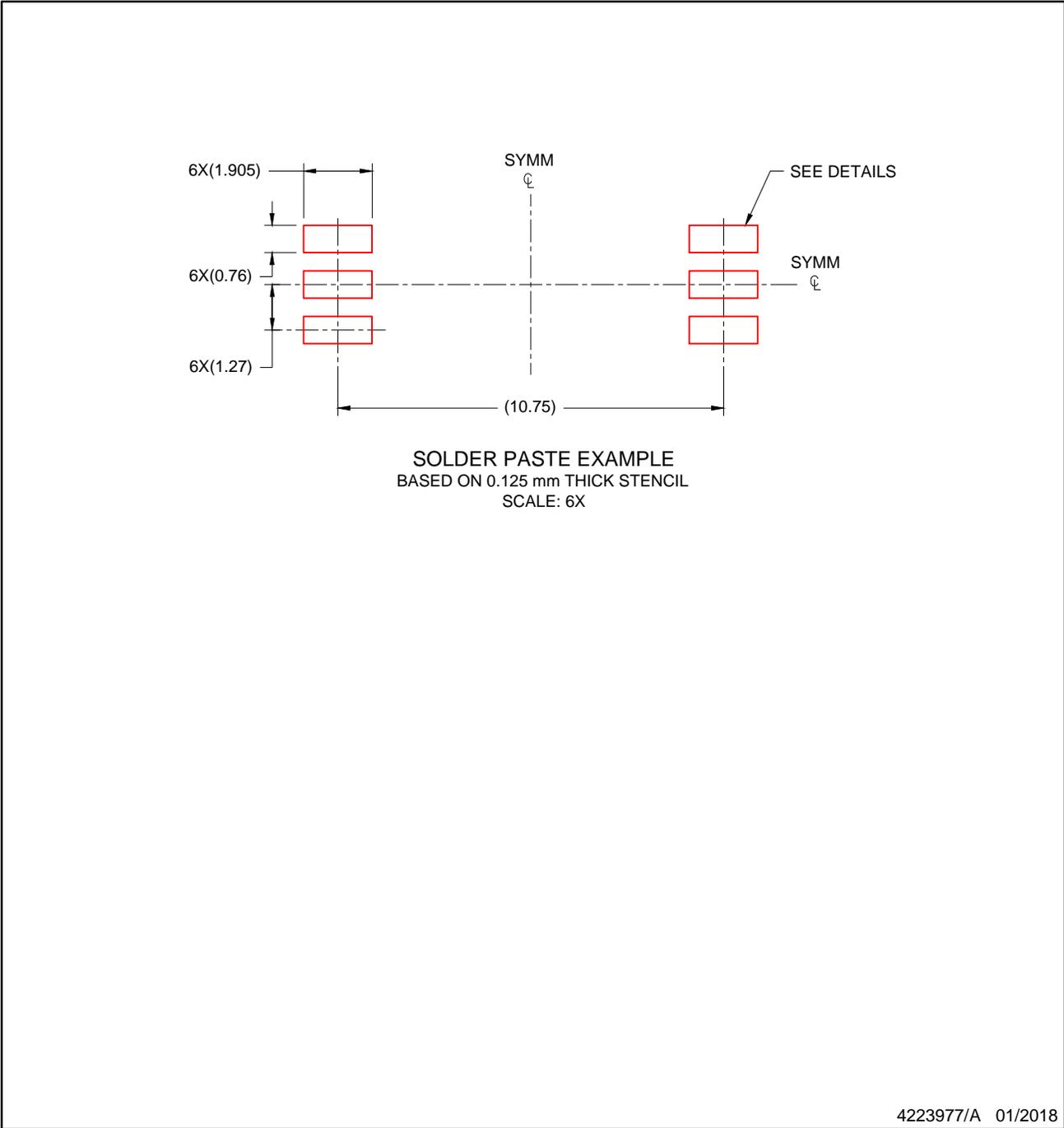
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

SOIC - 3.55 mm max height

DWY0006A

SOIC



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NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.

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