VCA824 超広帯域幅、ゲイン可変範囲 40dB 以上、V/V リニア可変ゲイン・アンプ

1 特長

- 小信号帯域幅：710MHz (G = 2V/V)
- $4V_{PP}$ 帯域幅：320MHz (G = 10V/V)
- ゲイン・フラットネス：0.1dB (135MHz まで)
- スルーレート：2500V/µs
- ゲイン可変範囲：40dB 以上
- 高いゲイン精度：20dB ±0.3dB
- 大きな出力電流：±90mA

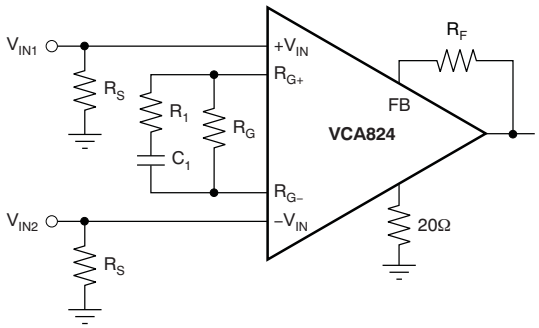
2 アプリケーション

- 差動ライン・レシーバ
- 差動イコライザ
- パルス振幅補償
- 可変アッテネータ
- 電圧で調整可能なアクティブ・フィルタ

3 概要

VCA824 は、DC 結合、広帯域、V/V リニア、連続可変、電圧制御ゲイン・アンプです。このデバイスは、ゲイン抵抗 (R_G) と帰還抵抗 (R_F) で設定した公称最大値からゲインを 40dB 下げることができる高インピーダンス・ゲイン制御入力を備えており、差動入力からシングルエンドへの変換を行います。

差動イコライザ



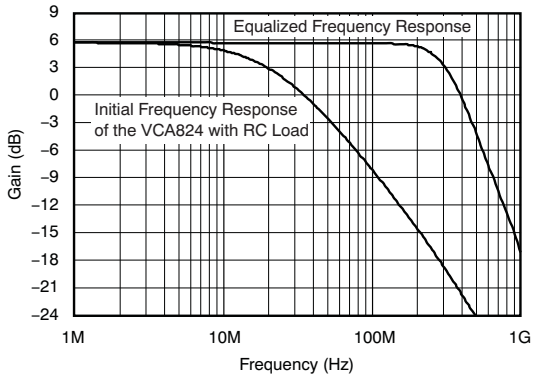
VCA824 の内部アーキテクチャは、2 つの入力バッファと、マルチプライヤ・コアと統合した出力電流帰還アンプ段とで構成されており、外部バッファを必要としない完全な可変ゲイン・アンプ (VGA) システムを実現できます。最大ゲインは 2 つの抵抗で外部から設定できるため、設計の柔軟性を高めることができます。最大ゲインは 2V/V～40V/V の範囲内で設定できます。±5V 電源で動作させた場合、VCA824 のゲイン制御電圧が 1V から -1V まで変化するにつれて、ゲイン (V/V) は線形的に変化します。たとえば、最大ゲインが 10V/V の場合、VCA824 のゲインはゲイン制御範囲の入力が 1V のとき 10V/V、-1V のとき 0.1V/V です。VCA824 はゲインの線形性が非常に優れています。最大ゲインが 20dB であり、かつゲイン制御入力電圧が 0V～1V の範囲で変化する場合、ゲインの偏差は ±0.3dB 以下 (25℃での最大値) です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
VCA824	SOIC (14)	8.65mm×3.91mm
	VSSOP (10)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

RC 負荷の差動イコライゼーション



目次

4 改訂履歴

Revision D (January 2016) から **Revision E** に変更 **Page**

- Changed *Output Voltage Swing* parameter R_L = 100 Ω specifications ... 6
- Changed *Output Current* parameter specifications ... 6

Revision C (December 2008) から **Revision D** に変更 **Page**

- 「*ピン構成および機能* 」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Deleted Thermal Characteristics rows from *Electrical Characteristics* ... 5

Revision B (August 2008) から **Revision C** に変更 **Page**

- Revised second paragraph in the *Wideband Variable Gain Amplifier Operation* section describing pin 9 ... 28

Revision A (December 2007) から **Revision B** に変更 **Page**

- Changed storage temperature range rating in Absolute Maximum Ratings table from – 40 ° C to 125 ° C to – 65 ° C to 125 ° C ... 4

2007年**11**月発行のものから更新 **Page**

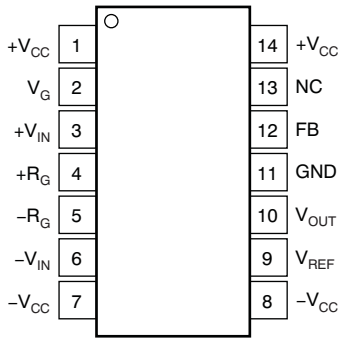
- Added typical value for output impedance ... 6
- Changed wording of explanation for X2Y capacitor usage at end of paragraph ... 28

5 Device Comparison Table

SINGLES	DUALS	GAIN ADJUST RANGE (dB)	INPUT NOISE (nV/√Hz)	SIGNAL BANDWIDTH (MHz)
VCA810	—	80	2.4	35
—	VCA2612	45	1.25	80
—	VCA2613	45	1	80
—	VCA2615	52	0.8	50
—	VCA2617	48	4.1	50
VCA820	—	40	8.2	150
VCA821	—	40	6.0	420
VCA822	—	40	8.2	150
VCA824	—	40	6.0	420

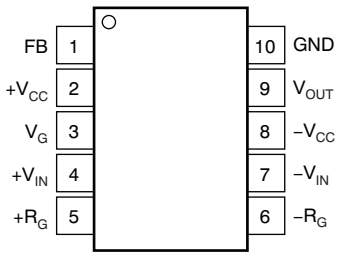
6 Pin Configuration and Functions

D Package
14-Pin SOIC
Top View



NC = No Connection

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	VSSOP		
V_{CC}	1,14	2	P	Positive supply voltage
V_G	2	3	I	Gain control voltage
$+V_{IN}$	3	4	I	noninverting input
$+R_G$	4	5	I	Gain set resistor noninverting input
$–R_G$	5	6	I	Gain set resistor inverting input
$–V_{IN}$	6	7	I	Inverting input
$–V_{CC}$	7,8	8	P	Negative supply voltage
V_{REF}	9	—	I	Output reference voltage (Non- Inverting input of output buffer)
V_{OUT}	10	9	O	Output voltage
GND	11	10	P	Ground
FB	12	1	I	Feedback resistor (inverting input of output buffer)
NC	13	—	—	Not connected

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply		±6.5	V
Internal power dissipation		See *Thermal Information*	
Input voltage		$\pm V_S$	V
Junction temperature (T_J)		260	°C
Junction temperature (T_J), continuous operation		140	°C
Storage temperature	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating voltage	7	10	12	V
Operating temperature	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		VCA824		UNIT
		D (SOIC)	DGS (VSSOP)	
		14 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.3	173.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.8	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.9	94.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.8	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.6	92.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: V_S = ±5 V

At A_{VMAX} = 10 V/V, V_G = 1V, R_F = 402 Ω, R_G = 80 Ω, and R_L = 100 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE								
Small-Signal Bandwidth		A_{VMAX} = 2 V/V, V_G = 1 V , V_O = 500 mV_{PP}		C		710		MHz
		A_{VMAX} = 10 V/V, V_G = 1 V, V_O = 500 mV_{PP}				420		
		A_{VMAX} = 40 V/V, V_G = 1 V, V_O = 500 mV_{PP}				170		
Large-Signal Bandwidth		A_{VMAX} = 10 V/V, V_G = 1 V, V_O = 4 V_{PP}		C		320		MHz
Gain Control Bandwidth		V_O = 200 mV_{PP}, T_A= 25°C	T_A= 25°C	B	240	330		MHz
			T_A = 0°C to 70°C		235			
			T_A = –40°C to 85°C		235			
Bandwidth for 0.1-dB Flatness		A_{VMAX} = 10 V/V, V_G = 1 V, V_O = 2 V_{PP}		C		135		MHz
Slew Rate		A_{VMAX} = 10 V/V, V_G = 1 V, V_O = 4 V Step	T_A= 25°C	B	1800	2500		V/µs
			T_A= 0°C to 70°		1700			
			T_A = –40°C to 85°C		1700			
Rise-and-Fall Time		A_{VMAX} = 10 V/V, V_G = 1 V, V_O = 4 V Step	T_A = 25°C	B		1.5	1.8	ns
			T_A = 0°C to 70°C				1.9	
			T_A = –40°C to 85°C				1.9	
Settling Time to 0.01%		A_{VMAX} = 10 V/V, V_G = 1 V, V_O = 4 V Step		C		11		ns
Harmonic Distortion	2nd-Harmonic	V_O = 2 V_{PP}, f = 20 MHz	T_A = 25°C	B	–64	-66		dBc
			T_A = 0°C to 70°C		–64			
			T_A = –40°C to 85°C		–64			
	3rd-Harmonic	V_O = 2 V_{PP}, f = 20 MHz	T_A = 25°C	B	–61	–63		dBc
			T_A = 0°C to 70°C		–61			
			T_A = –40°C to 85°C		–61			
Input Voltage Noise		f > 100 kHz		C		6		nV/√Hz
Input Current Noise		f > 100 kHz		C		2.6		pA/√Hz
GAIN CONTROL								
Gain Error		A_{VMAX} = 10 V/V, V_G = 1 V	T_A = 25°C	A		±0.1	±0.4	dB
			T_A = 0°C to 70°C				±0.5	
			T_A = –40°C to 85°C				±0.6	
Gain Deviation		A_{VMAX} = 10 V/V, 0 < V_G < 1	T_A = 25°C	A		±0.05	±0.3	dB
			T_A = 0°C to 70°C				±0.34	
			T_A = –40°C to 85°C				±0.37	
Gain Deviation		A_{VMAX} = 10 V/V, -0.8 < V_G < 1	T_A = 25°C	A		±1.06	±1.9	dB
			T_A = 0°C to 70°C				±2.1	
			T_A = –40°C to 85°C				±2.2	
Gain at V_G = –0.9V		Relative to max gain	T_A = 25°C	A		–26	–24	dB
			T_A = 0°C to 70°C				–24	
			T_A = –40°C to 85°C				–23	
Gain Control Bias Current		T_A = 25°C		A		22	30	µA
		T_A = 0°C to 70°C					35	
		T_A = –40°C to 85°C					37	
Average Gain Control Bias Current Drift		T_A = 0°C to 70°C		B			±100	nA/°C
		T_A = –40°C to 85°C					±100	
Gain Control Input Impedance		T_A = 25°C		C		1.5 || 0.6		MΩ || pF
DC PERFORMANCE								
Input Offset Voltage		A_{VMAX} = 10 V/V, V_{CM} = 0 V, V_G = 1 V	T_A = 25°C	A		±4	±17	mV
			T_A = 0°C to 70°				±17.8	
			T_A = –40°C to 85°C				±19	
Average Input Offset Voltage Drift		A_{VMAX} = 10 V/V, V_{CM} = 0 V, V_G = 1 V	T_A = 0°C to 70°C	B			±30	µV/°C
			T_A = –40°C to 85°C				±30	
Input Bias Current		A_{VMAX} = 10 V/V, V_{CM} = 0V, V_G = 1 V	T_A = 25°C	A		19	25	µA
			T_A = 0°C to 70°C				29	
			T_A = –40°C to 85°C				31	

(1) Test levels: (A) 100% tested at 25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

Electrical Characteristics: V_S = ±5 V (continued)

At A_{VMAX} = 10 V/V, V_G = 1V, R_F = 402 Ω, R_G = 80 Ω, and R_L = 100 Ω, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
Average Input Bias Current Drift		A_{VMAX} = 10 V/V, V_{CM} = 0 V, V_G = 1 V	T_A = 0°C to 70°C	B			±90	nA/°C
			T_A = –40°C to 85°				±90	
Input Offset Current		A_{VMAX} = 10 V/V, V_{CM} = 0 V, V_G = 1 V	T_A = 25°C	A		±0.5	±2.5	µA
			T_A = 0°C to 70°C				±3.2	
			T_A = –40°C to 85°C				±3.5	
Average Input Offset Current Drift		A_{VMAX} = 10 V/V, V_{CM} = 0 V, V_G = 1 V	T_A = 0°C to 70°C	B			±16	nA/°C
			T_A = –40°C to 85°C				±16	
Max Current Through Gain Resistance		T_A = 25°C		B		±2.6	±2.55	mA
		T_A = 0°C to 70°C					±2.55	
		T_A = –40°C to 85°C					±2.5	
INPUT								
Most Positive Common-Mode Input Voltage		R_L = 100 Ω	T_A = 25°C	A	1.6	1.6		V
			T_A = 0°C to 70°C		1.6			
			T_A = –40°C to 85°C		1.6			
Most Negative Common-Mode Input Voltage		R_L = 100 Ω	T_A = 25°C	A		–2.1	–2.1	V
			T_A = 0°C to 70°C				–2.1	
			T_A = –40°C to 85°C				–2.1	
Common-Mode Rejection Ratio		V_{CM} = ±0.5 V	T_A = 25°C	A		80	65	dB
			T_A = 0°C to 70°C				60	
			T_A = –40°C to 85°C				60	
Input Impedance	Differential			C		1 || 1		MΩ || pF
	Common-Mode			C		1 || 2		MΩ || pF
OUTPUT								
Output Voltage Swing		R_L = 1 kΩ	T_A = 25°C	A	±3.6	±3.9		V
			T_A = 0°C to 70°C		±3.4			
			T_A = –40°C to 85°C		±3.3			
		R_L = 100 Ω	T_A = 25°C	A	3.5	3.6		V
						–3.3	–3.2	
			T_A = 0°C to 70°C		3.3		–3	
			T_A = –40°C to 85°C		3.2		–2.9	
Output Current		V_O = 0V, R_L = 10 Ω	Source, T_A = 25°C	A	60	90		mA
			Sink, T_A = 25°C			–55	–50	
			T_A = 0°C to 70°C		50		–42	
			T_A = –40°C to 85°C		45		–38	
Output Impedance		A_{VMAX} = 10 V/V, f > 100 kHz		C		0.01		Ω
POWER SUPPLY								
Specified Operating Voltage				C		±5		V
Minimum Operating Voltage		T_A = 25°C		B	±4			V
		T_A = 0°C to 70°C			±4			
		T_A = –40°C to 85°C			±4			
Maximum Operating Voltage		T_A = 25°C		A			±6	V
		T_A = 0°C to 70°C					±6	
		T_A = –40°C to 85°C					±6	
Maximum Quiescent Current		V_G = 0 V	T_A = 25°C	A		36.5	37.5	mA
			T_A = 0°C to 70°C				38	
			T_A = –40°C to 85°C				38.5	
Minimum Quiescent Current		V_G = 0 V	T_A = 25°C	A		36.5	35	mA
			T_A = 0°C to 70°C				34.5	
			T_A = –40°C to 85°C				34	
Power-Supply Rejection Ratio (-PSRR)		V_G = 1 V	T_A = 25°C	A	–61	-68		dB
			T_A = 0°C to 70°C		–59			
			T_A = –40°C to 85°C		–58			

7.6 Typical Characteristics: V_S = ±5 V, A_{VMAX} = 2 V/V

At T_A = 25°C, R_L = 100 Ω, R_F = 453 Ω, R_G = 453 Ω, V_G = 1 V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and 14-Pin SOIC package, unless otherwise noted.

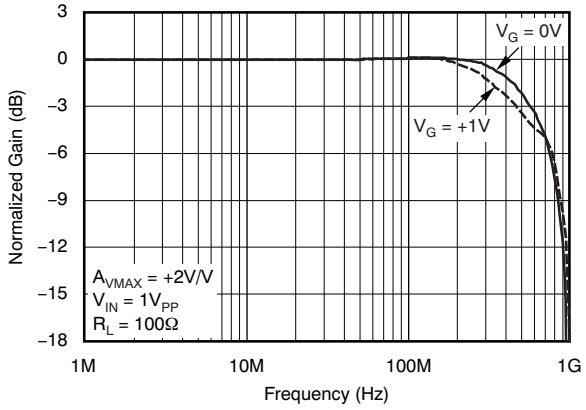


Figure 1. Small-Signal Frequency Response

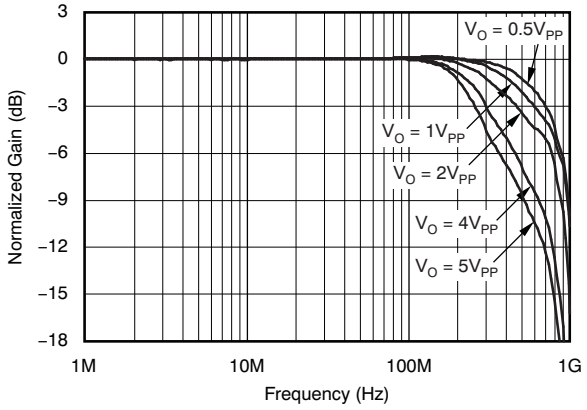


Figure 2. Large-Signal Frequency Response

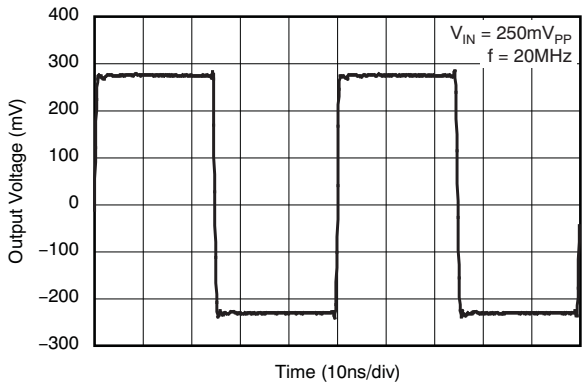


Figure 3. Small-Signal Pulse Response

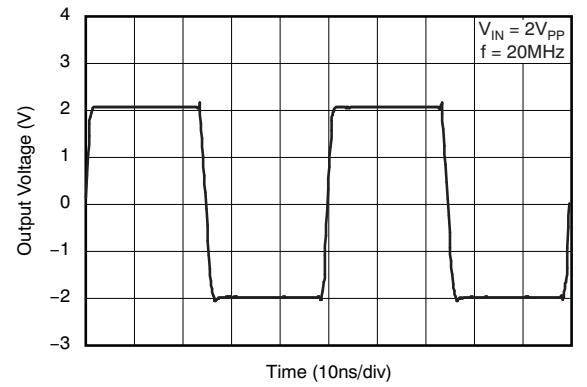


Figure 4. Large-Signal Pulse Response

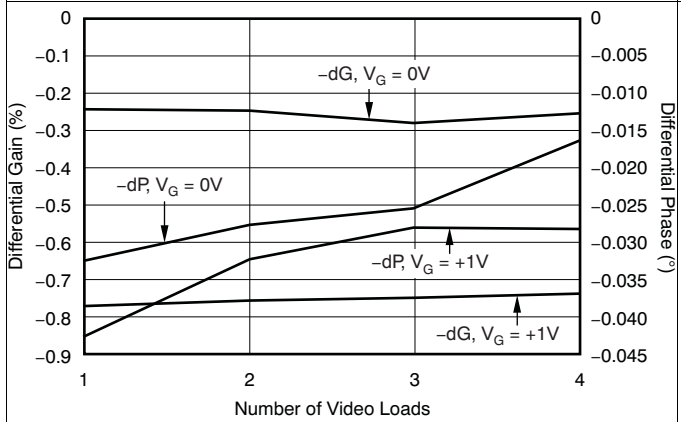


Figure 5. Composite Video dG/dP

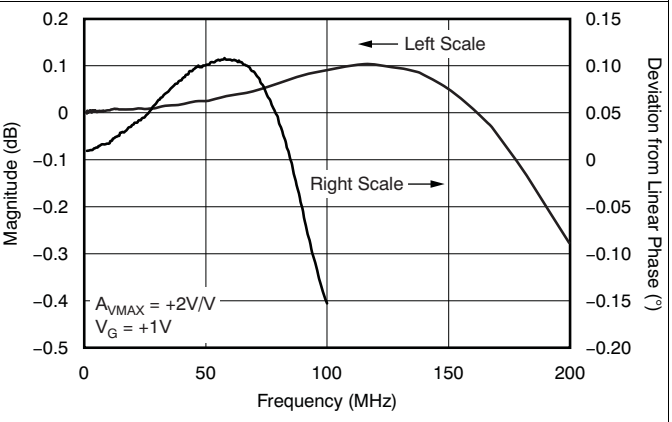


Figure 6. Gain Flatness, Deviation From Linear Phase

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 2 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 453 Ω, R_G = 453 Ω, V_G = 1 V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and 14-Pin SOIC package, unless otherwise noted.

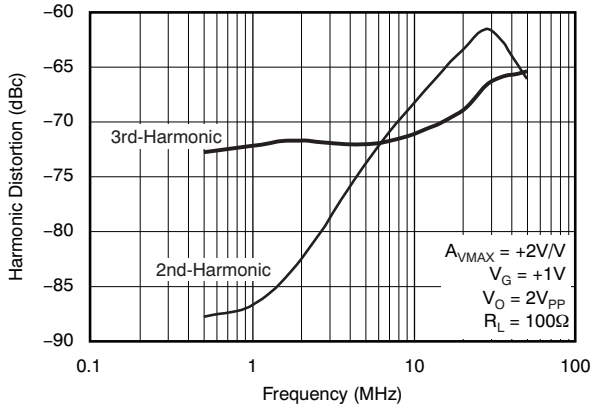


Figure 7. Harmoneic Distortion vs Frequency

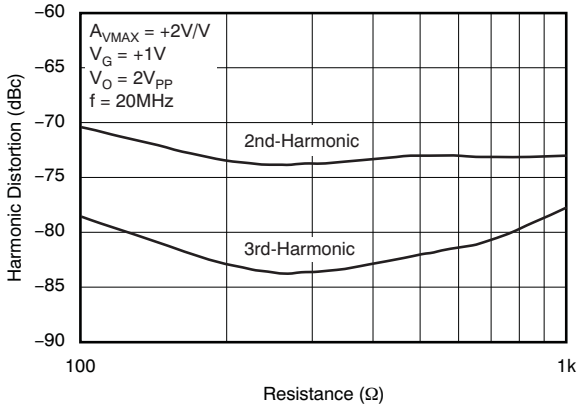


Figure 8. Harmonic Distortion vs Load Resistance

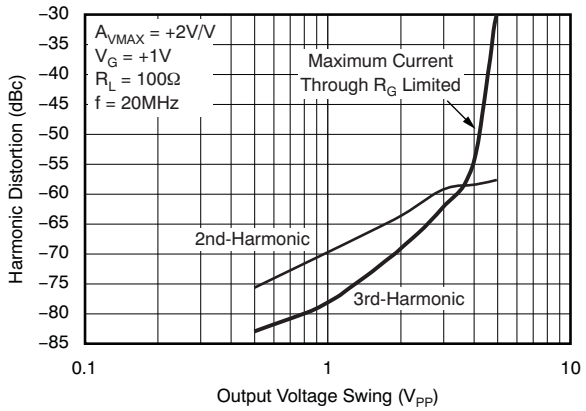


Figure 9. Harmonic Distortion vs Output Voltage

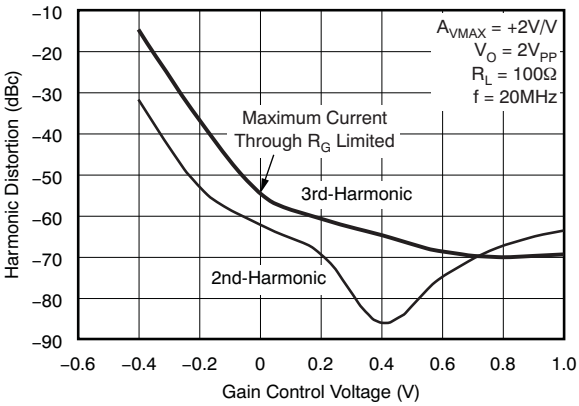


Figure 10. Harmonic Distortion vs Gain Control Voltage

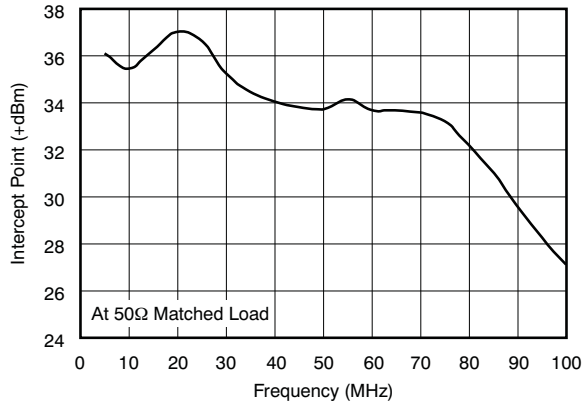


Figure 11. Two-Tone, 3rd-Order Intermodulation Intercept

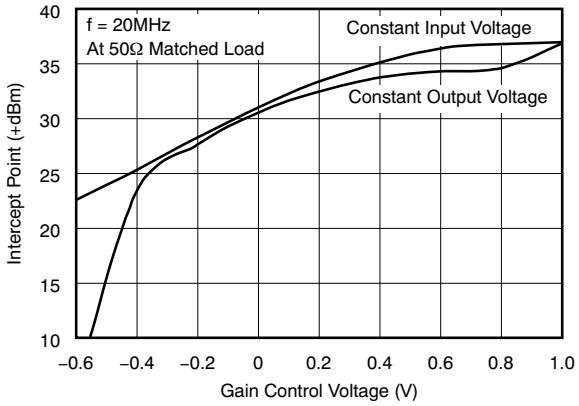


Figure 12. Two-Tone, 3rd-Order Intermodulation Intercept vs Gain Control Voltage

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 2 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 453 Ω, R_G = 453 Ω, V_G = 1 V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and 14-Pin SOIC package, unless otherwise noted.

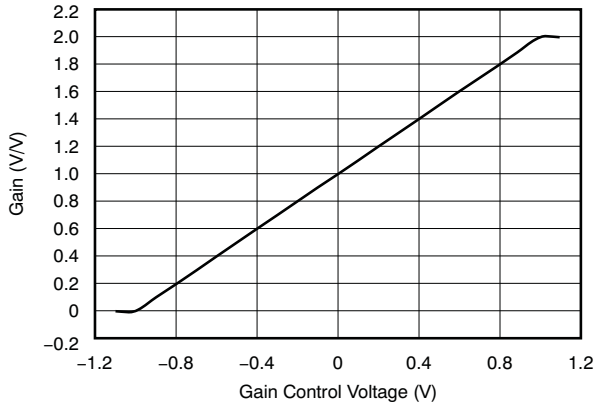


Figure 13. Gain vs Gain Control Voltage

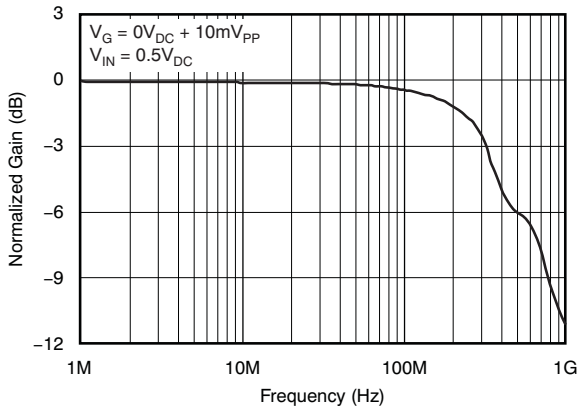


Figure 14. Gain Control Frequency Response

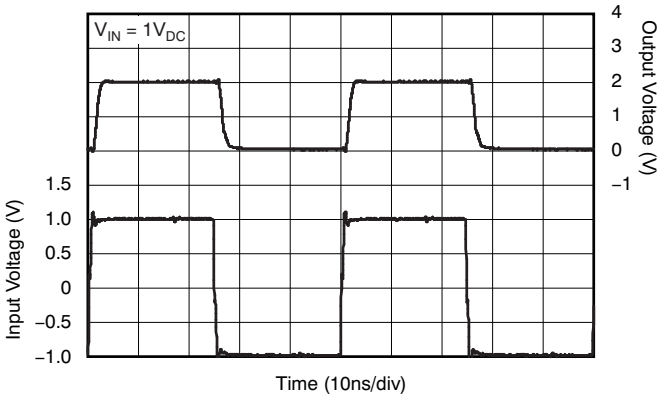


Figure 15. Gain Control Pulse Response

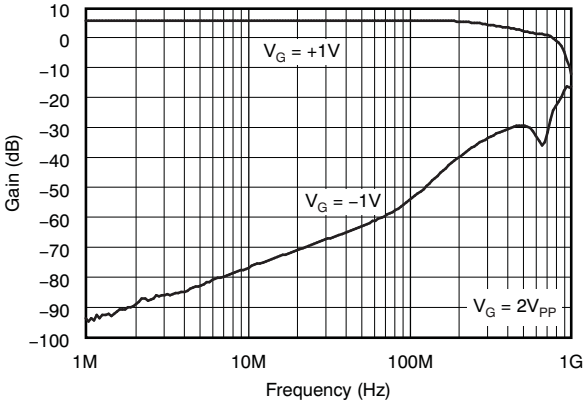


Figure 16. Fully-Attenuated Response

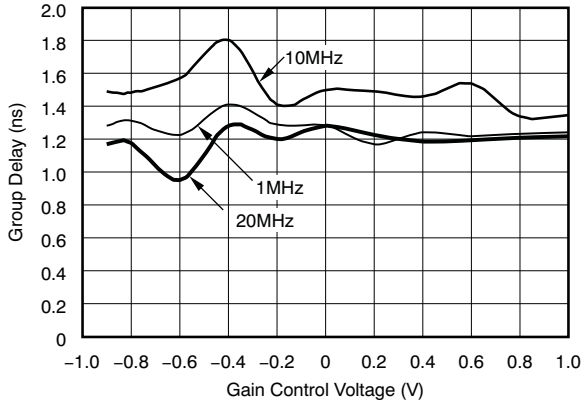


Figure 17. Group Delay vs Gain Control Voltage

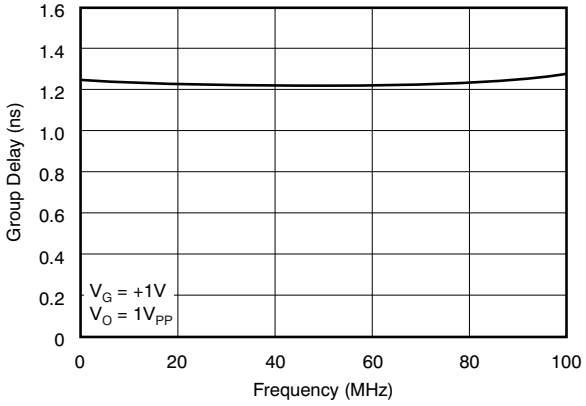


Figure 18. Group Delay vs Frequency

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 2 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 453 Ω, R_G = 453 Ω, V_G = 1 V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and 14-Pin SOIC package, unless otherwise noted.

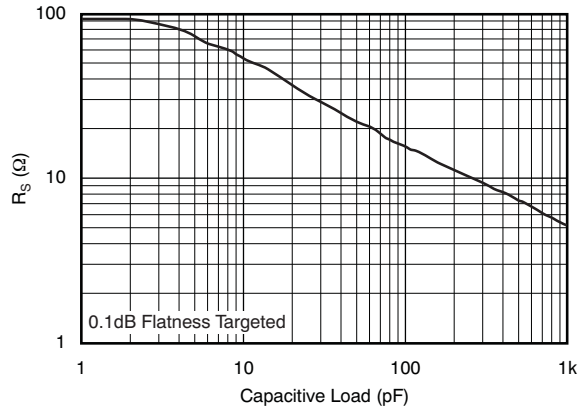


Figure 19. Recommended R_S vs Capacitive Load

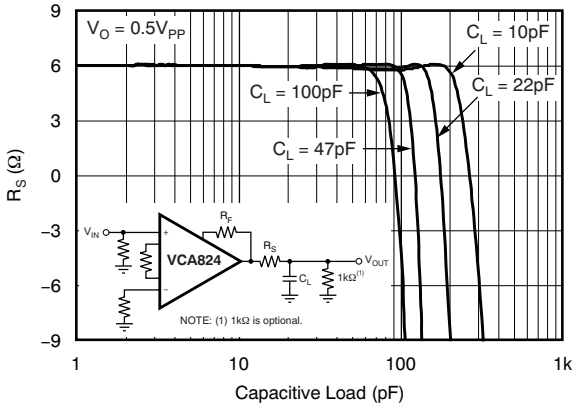


Figure 20. Frequency Response vs Capacitive Load

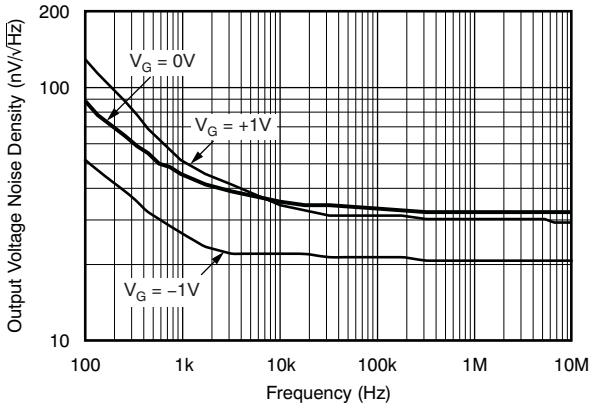


Figure 21. Output Voltage Density

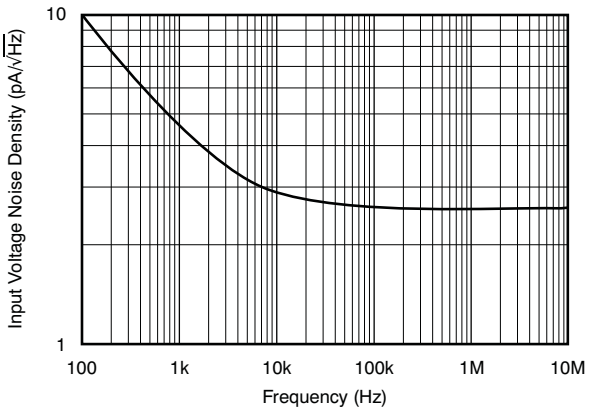


Figure 22. Input Current Noise Density

7.7 Typical Characteristics: V_S = ±5 V, A_{VMAX} = 10 V/V

At T_A = 25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 80 Ω, V_G = 1 V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

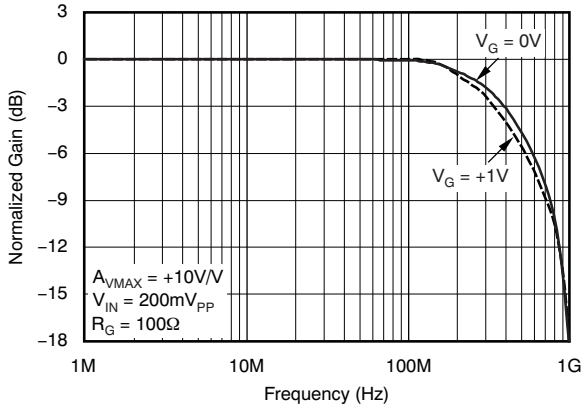


Figure 23. Small-Signal Frequency Response

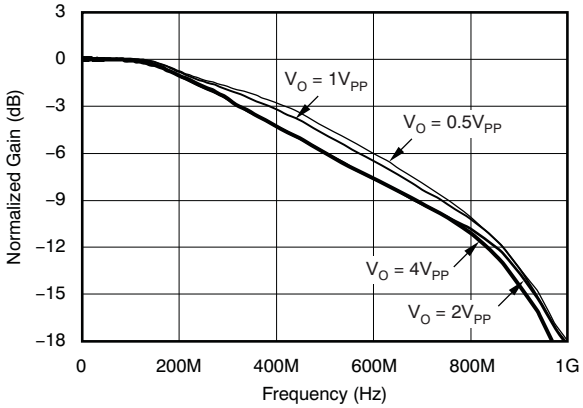


Figure 24. Large-Signal Frequency Response

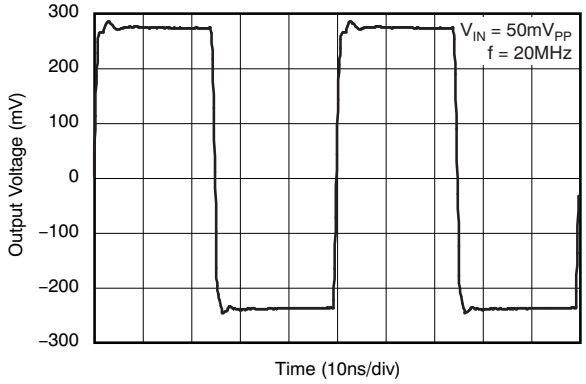


Figure 25. Small-Signal Pulse Response

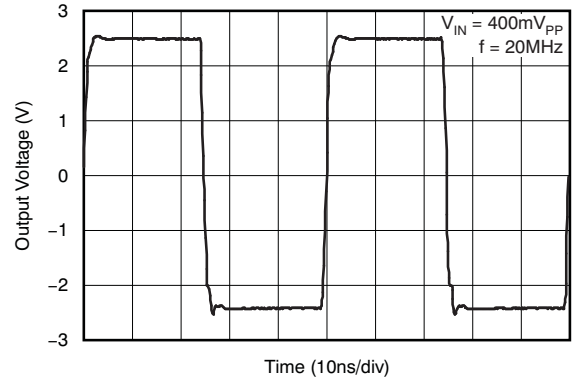


Figure 26. Large-Signal Pulse Response

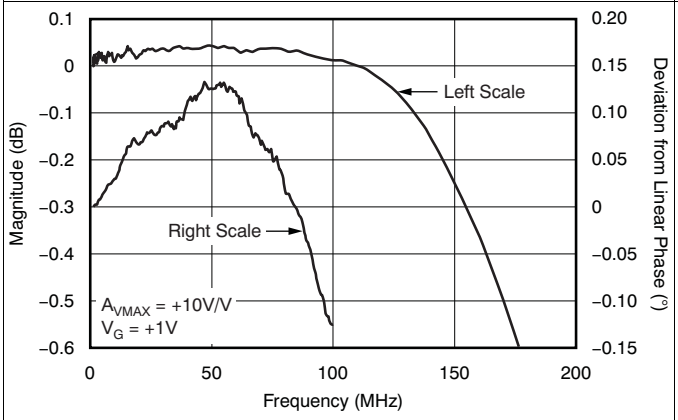


Figure 27. Gain Flatness, Deviation from Linear Phase

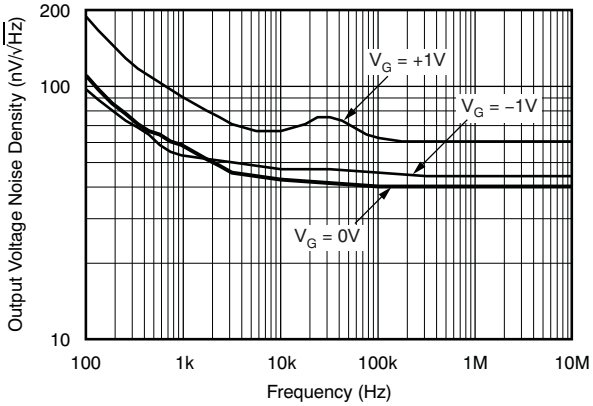


Figure 28. Output Voltage Noise Density

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 10 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 80 Ω, V_G = 1 V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

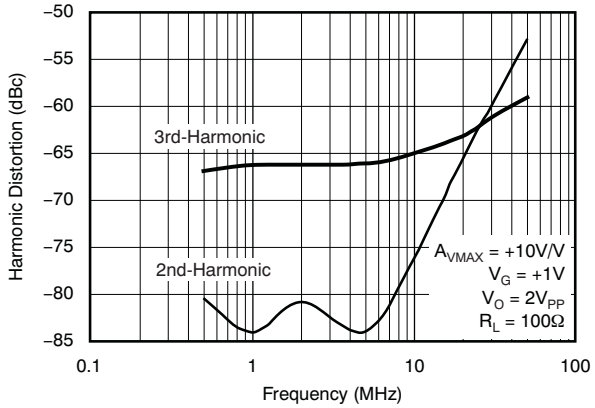


Figure 29. Harmonic Distortion vs Frequency

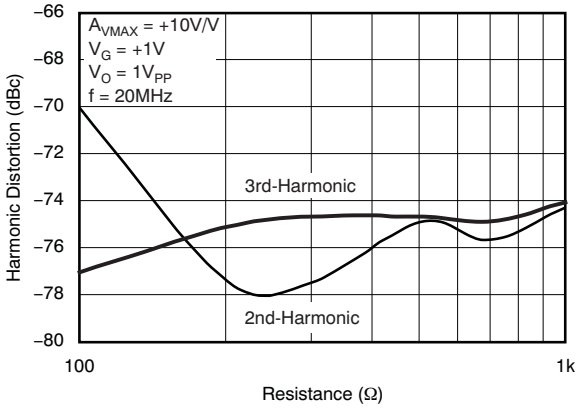


Figure 30. Harmonic Distortion vs Load Resistance

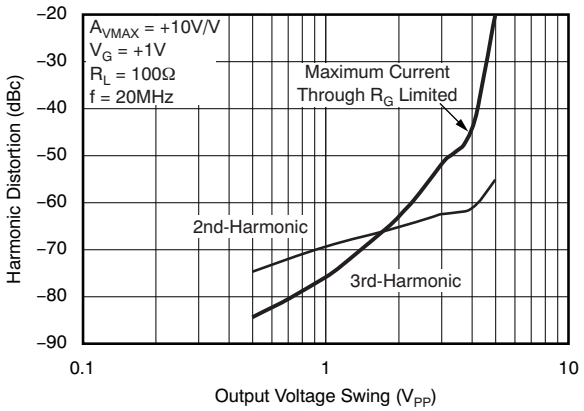


Figure 31. Harmonic Distortion vs Output Voltage

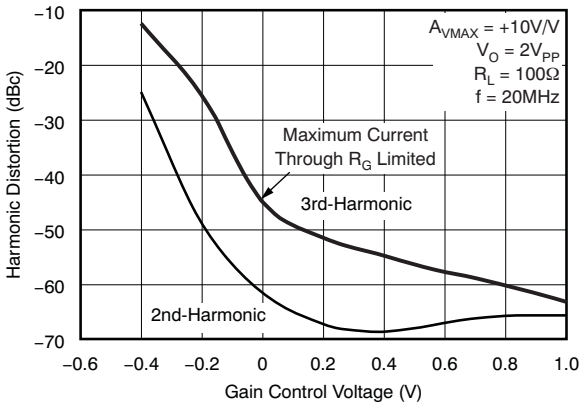


Figure 32. Harmonic Distortion vs Gain Control Voltage

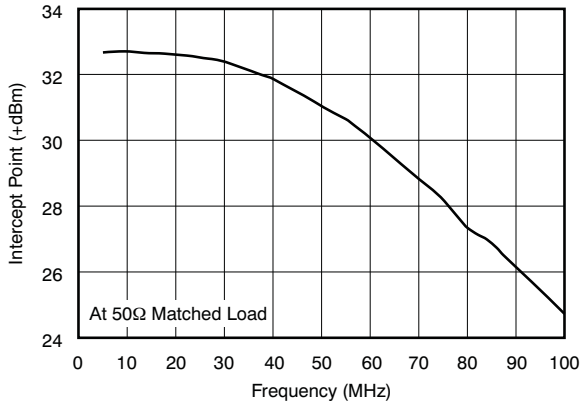


Figure 33. Two-Tone, 3rd-Order Intermodulation Intercept

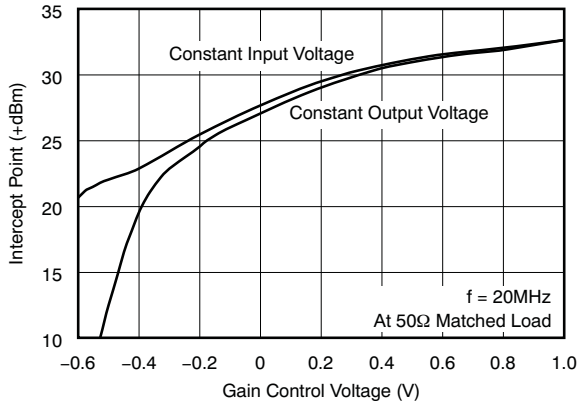


Figure 34. Two-Tone, 3rd-Order Intermodulation Intercept vs Gain Control Voltage

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 10 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 80 Ω, V_G = 1 V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

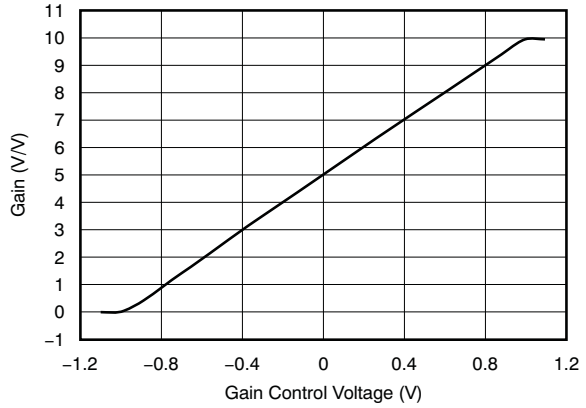


Figure 35. Gain vs Gain Control Voltage

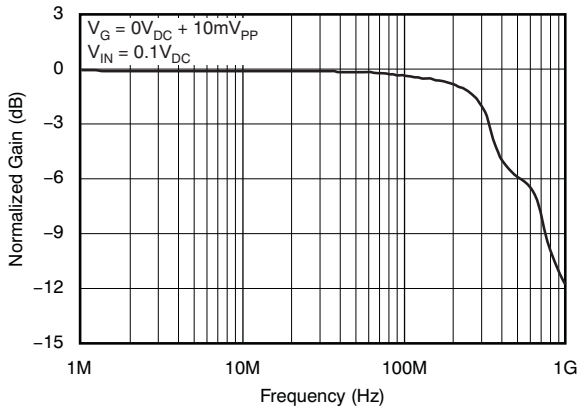


Figure 36. Gain Control Frequency Response

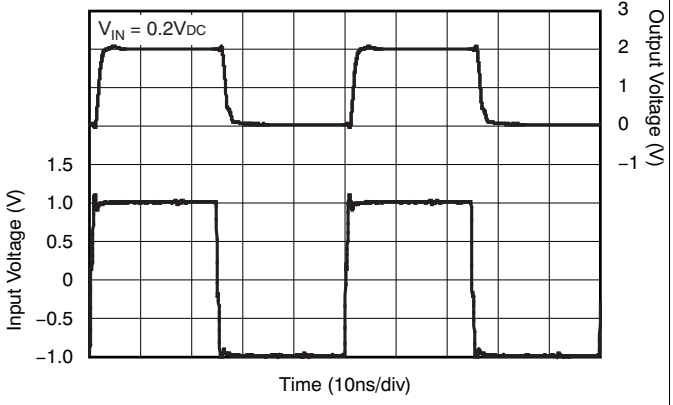


Figure 37. Gain Control Pulse Response

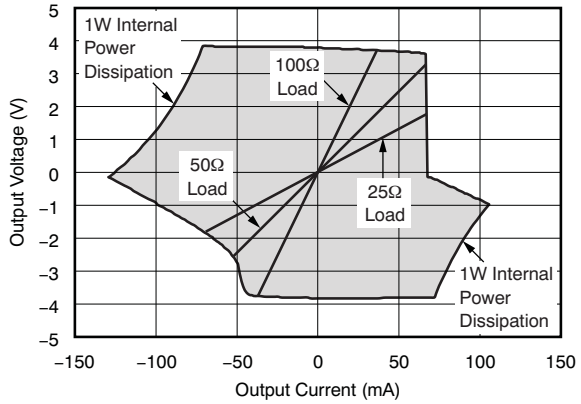


Figure 38. Output Voltage and Current Limitations

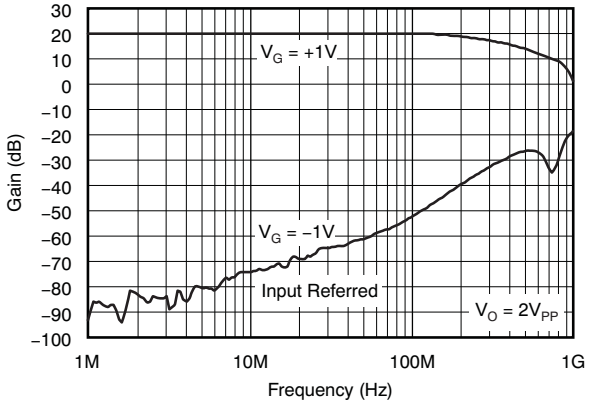


Figure 39. Fully-Attenuated Response

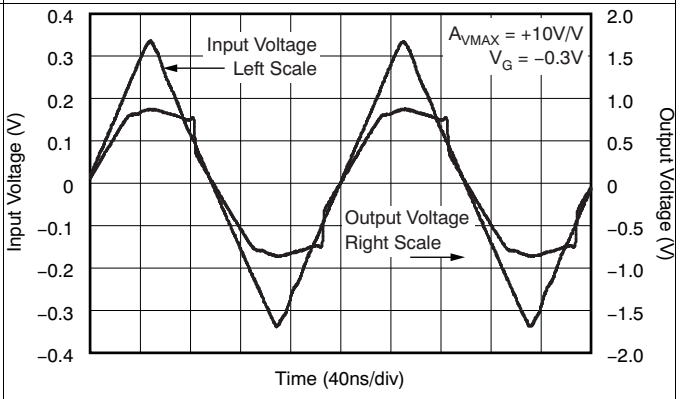


Figure 40. I_{RG} Limited Overdrive Recovery

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 10 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 80 Ω, V_G = 1 V, and V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, unless otherwise noted.

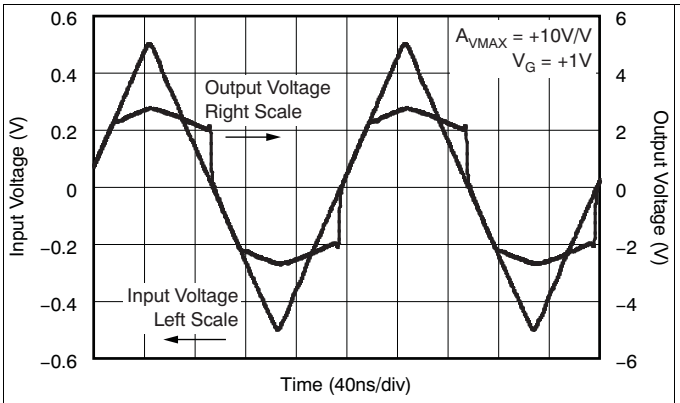


Figure 41. Output Limited Overdrive Recovery

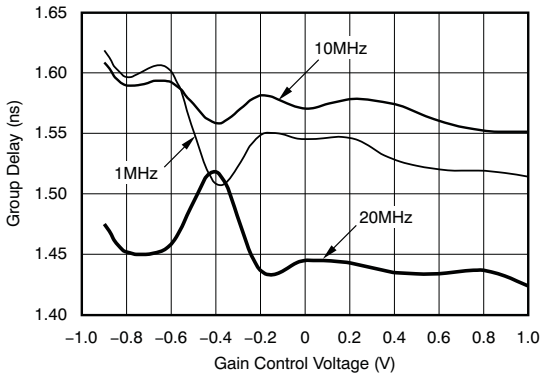


Figure 42. Group Delay vs Gain Control Voltage

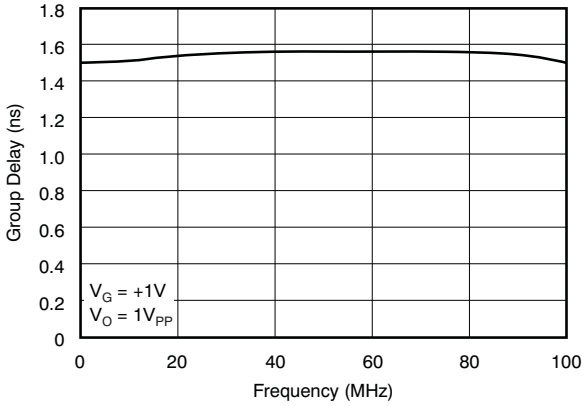


Figure 43. Group Delay vs Frequency

7.8 Typical Characteristics: V_S = ±5 V, A_{VMAX} = 40 V/V

At T_A = 25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 18 Ω, V_G = 1 V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

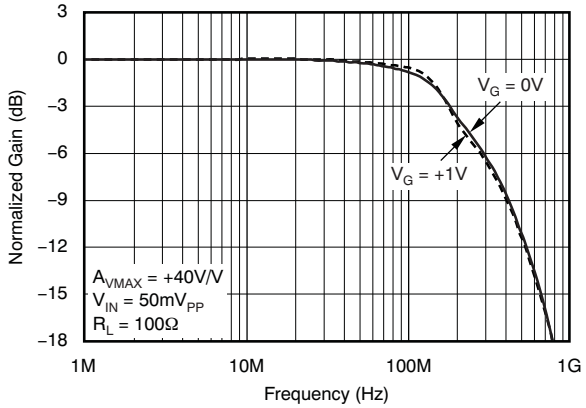


Figure 44. Small-Signal Frequency Response

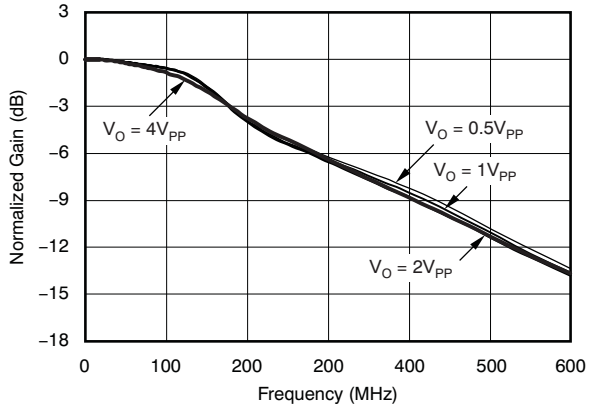


Figure 45. Large-Signal Frequency Response

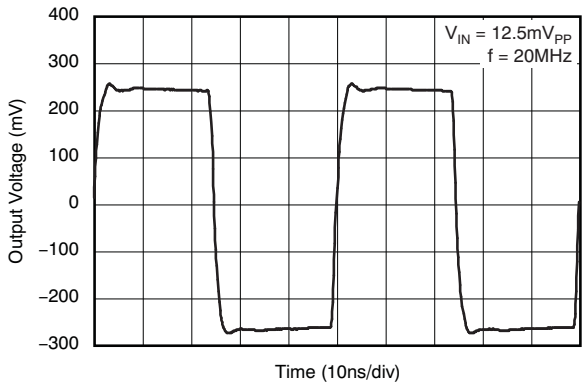


Figure 46. Small-Signal Pulse Response

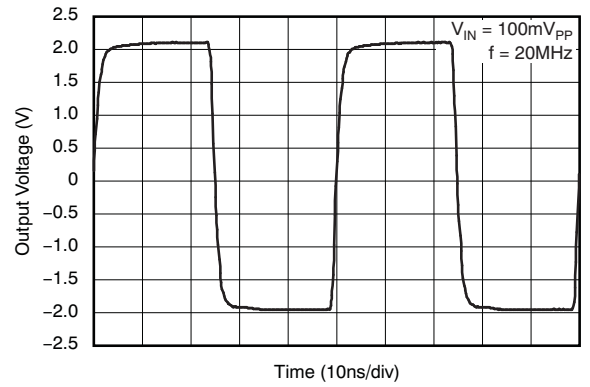


Figure 47. Large-Signal Pulse Response

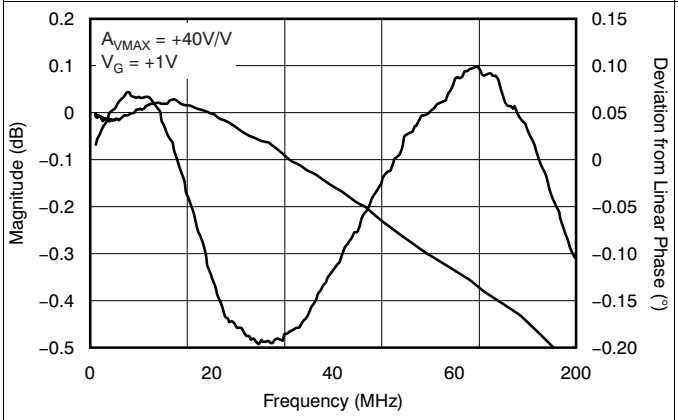


Figure 48. Gain Flatness, Deviation from Linear Phase

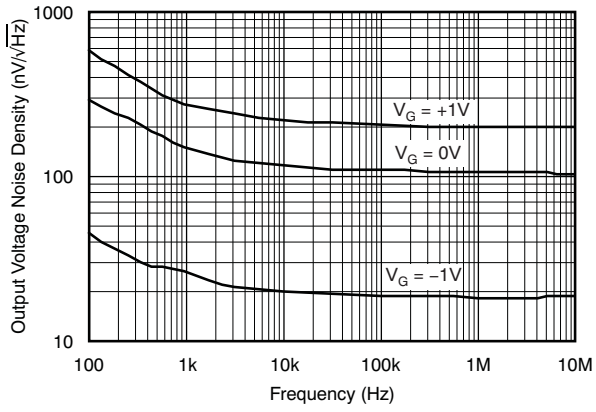


Figure 49. Output Voltage Noise Density

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 40 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 18 Ω, V_G = 1 V, V_{IN} = single-ended input on $+V_{IN}$ with $-V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

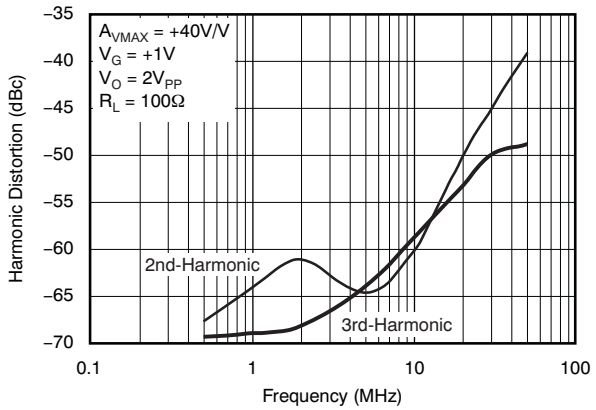


Figure 50. Harmonic Distortion vs Frequency

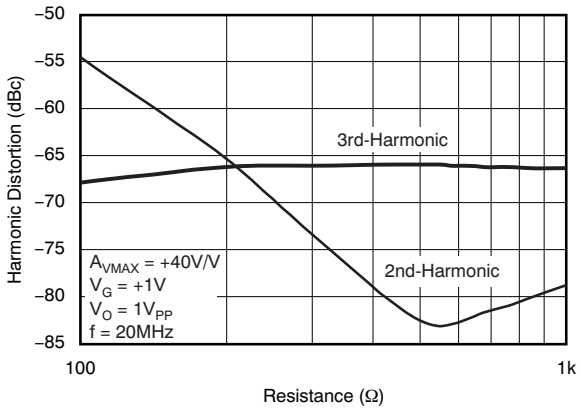


Figure 51. Harmonic Distortion vs Load Resistance

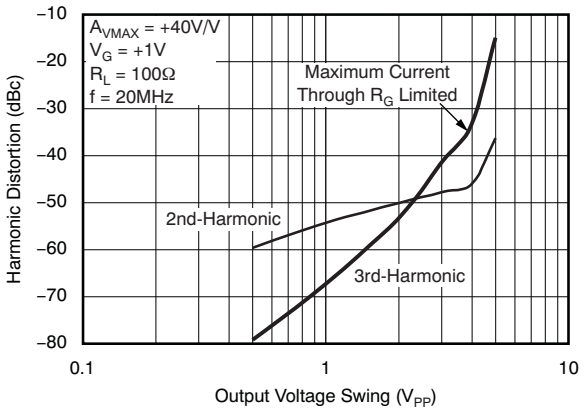


Figure 52. Harmonic Distortion vs Output Voltage

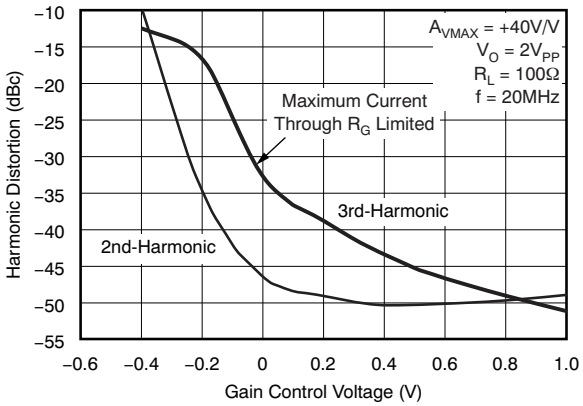


Figure 53. Harmonic Distortion vs Gain Control Voltage

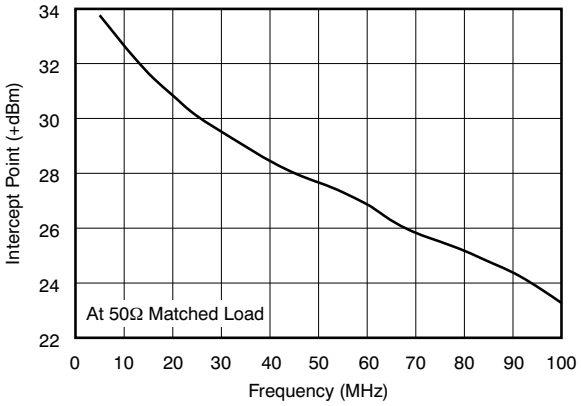


Figure 54. Two-Tone, 3rd-Order Intermodulation Intercept

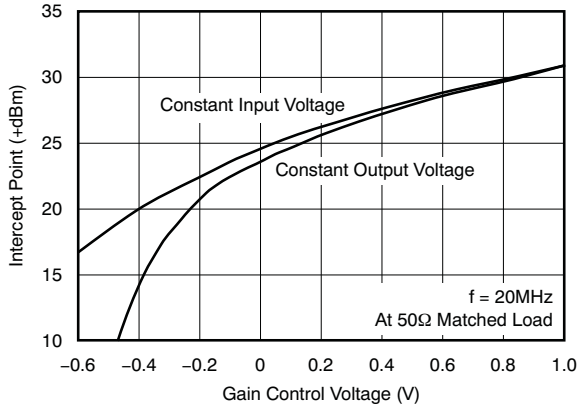


Figure 55. Two-Tone, 3rd-Order Intermodulation Intercept vs Gain Control Voltage

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 40 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 18 Ω, V_G = 1 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

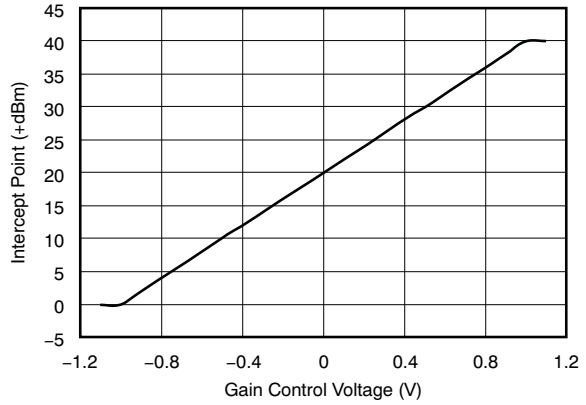


Figure 56. Gain vs Gain Control Voltage

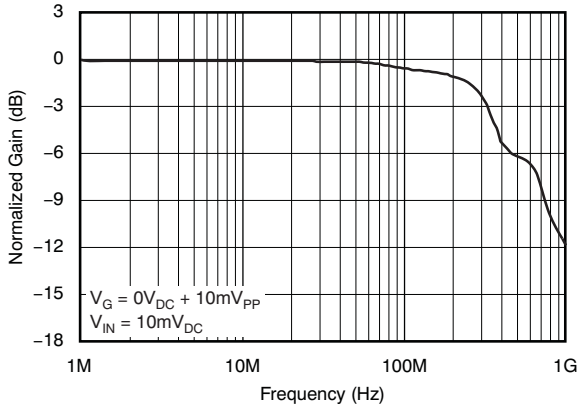


Figure 57. Gain Control Frequency Response

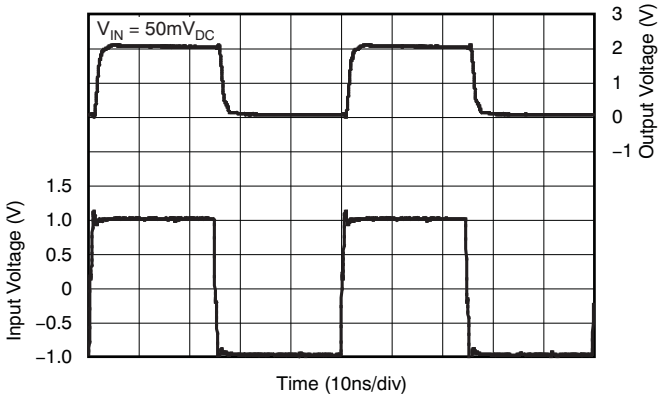


Figure 58. Gain Control Pulse Response

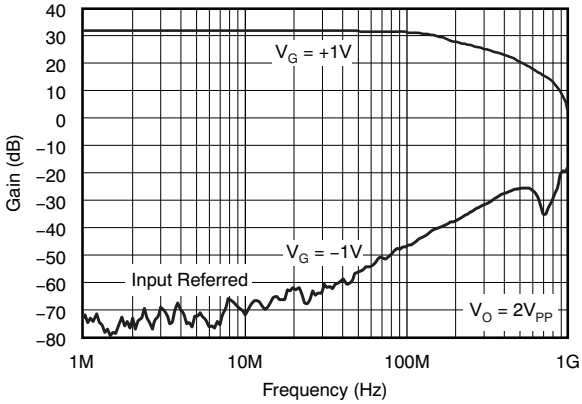


Figure 59. Fully Attenuated Response

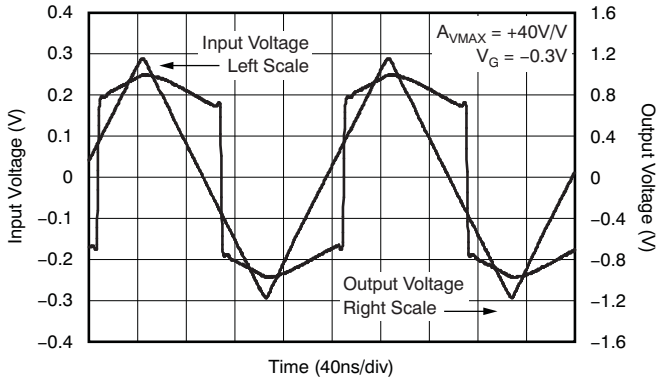


Figure 60. I_{RG} Limited Overdrive Recovery

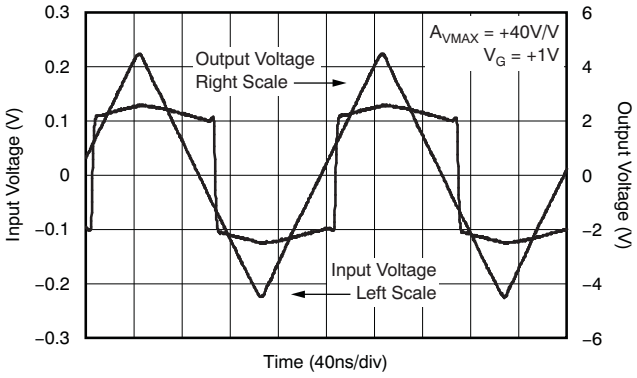


Figure 61. Output Limited Overdrive Recovery

Typical Characteristics: V_S = ±5 V, A_{VMAX} = 40 V/V (continued)

At T_A = 25°C, R_L = 100 Ω, R_F = 402 Ω, R_G = 18 Ω, V_G = 1 V, V_{IN} = single-ended input on $+V_{IN}$ with $–V_{IN}$ at ground, and SO-14 package, unless otherwise noted.

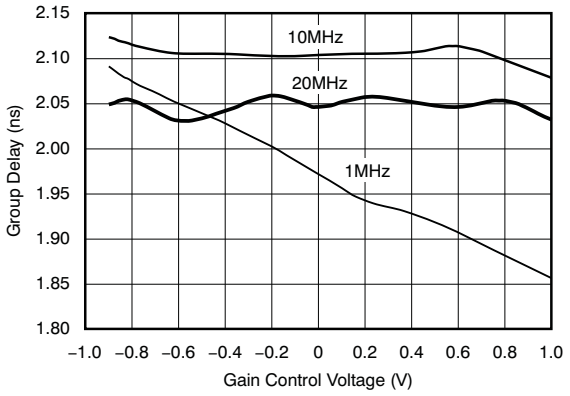


Figure 62. Group Delay vs Gain Control Voltage

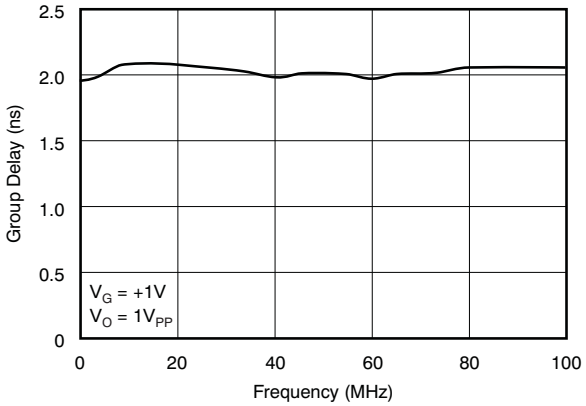


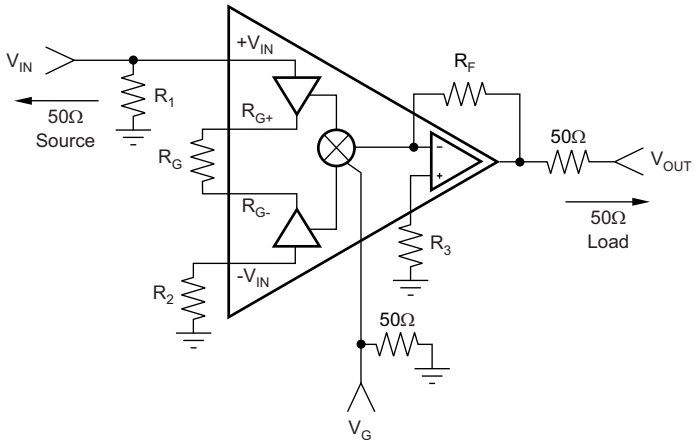
Figure 63. Group Delay vs Frequency

8 Detailed Description

8.1 Overview

The VCA824 is a voltage controlled variable gain amplifier with differential inputs and a single ended output. The maximum gain is set by external resistors while the gain range is controlled by an external analog voltage. The maximum gain is designed for gains of 2 V/V up to 100 V/V and the analog control allows a gain range of over 40 dB. The VCA824 Input consists of two buffers, which together create a fully symmetrical, high impedance differential input with a typical common mode rejection of 80 dB. The gain set resistor is connected between the two input buffer output pins, so that the input impedance is independent of the gain settings. The bipolar inputs have a input voltage range of 1.6 and –2.1 V on ±5 V supplies. The amplifier maximum gain is set by external resistors, but the internal gain control circuit is controlled by a continuously variable, analog voltage. The gain control is a multiplier stage which is linear in V/V. The gain control input pin operates over a voltage range of –1 V to 1 V. The VCA824 contains a high-speed, high-current output buffer. The output stage can typically swing ±3.9 V and source/sink ±90 mA. The VCA824 can be operated over a voltage range of ±3.5 V to ±6 V.

8.2 Functional Block Diagram



8.3 Feature Description

The VCA824 can be operated with both single ended or differential input signals. The inputs present consistently high impedance across all gain configurations. By using an analog control signal the amplifier gain is continuously variable for smooth, glitch free gain changes. With a large signal bandwidth of 320 Mhz and a slew rate of 2500 V/us the VCA824 offers linear performance over a wide range of signal amplitudes and gain settings. The low impedance/high current output buffer can drive loads ranging from low impedance transmission lines to high-impedance, switched-capacitor analog-to-digital converters. By using closely matched internal components, the VCA824 offers gain accuracy of ±0.3 dB.

8.4 Device Functional Modes

The VCA824 functions as a differential input, single maximum gain of operation-ended output variable gain amplifier. This functional mode is enabled by applying power to the amplifier supply pins and is disabled by turning the power off. The gain is continuously variable through the analog gain control input. While the gain range is fixed, the maximum gain is set by two external components, Rf and Rg, as shown in the Functional Block Diagram. The maximum gain is equal to 2x (Rf / Rg). This gain is achieved with a 1-V voltage on the gain adjust pin VG. As the voltage decreases on the VG pin, the gain decreases in a linear in dB fashion with over 40 dB of gain range from 1-V to –1-V control voltage. As with most other differential input amplifiers, inputs can be applied to either one or both of the amplifier inputs. The amplifier gain is controlled through the gain control pin.

8.4.1 Maximum Gain Of Operation

This section describes the use of the VCA824 in a fixed-gain application in which the V_G control pin is set at V_G = 1 V. The tradeoffs described here are with bandwidth, gain, and output voltage range.

Device Functional Modes (continued)

In the case of an application that does not make use of the V_{GAIN}, but requires some other characteristic of the VCA824, the R_G resistor must be set such that the maximum current flowing through the resistance I_{RG} is less than ±2.6 mA typical, or 5.2 mA_{PP} as defined in *Electrical Characteristics: V_S = ±5 V*, and must follow Equation 1.

$$I_{RG} = \frac{V_{OUT}}{A_{VMAX} \times R_G} \quad (1)$$

As Equation 1 illustrates, once the output dynamic range and maximum gain are defined, the gain resistor is set. This gain setting in turn affects the bandwidth, because in order to achieve the gain (and with a set gain element), the feedback element of the output stage amplifier is set as well. Keeping in mind that the output amplifier of the VCA824 is a current-feedback amplifier, the larger the feedback element, the lower the bandwidth because the feedback resistor is the compensation element.

Limiting the discussion to the input voltage only and ignoring the output voltage and gain, Equation 2 illustrates the tradeoff between the input voltage and the current flowing through the gain resistor.

8.4.2 Output Current And Voltage

The VCA824 provides output voltage and current capabilities that are unsurpassed in a low-cost monolithic VCA. Under no-load conditions at 25°C, the output voltage typically swings closer than 1 V to either supply rails; the 25°C swing limit is within 1.2 V of either rails. Into a 15-Ω load (the minimum tested load), the VCA824 device is tested to deliver more than ±160 mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or *V-I product*, that is more relevant to circuit operation (See Figure 38). The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the VCA824 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1-W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the VCA824 can drive ±2.5 V into 25-Ω or ±3.5 V into 50-Ω without exceeding the output capabilities or the 1-W dissipation limit. A 100-Ω load line (the standard test circuit load) shows the full ±3.9-V output swing capability, as shown in *Typical Characteristics*.

The minimum specified output voltage and current overtemperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers shown in *Electrical Characteristic*. As the output transistors deliver power, the respective junction temperatures increase, thereby increasing the available output voltage swing and output current.

In steady-state operation, the available output voltage and current are always greater than the temperature shown in the overtemperature specifications because the output stage junction temperatures are higher than the specified operating ambient.

8.4.3 Input Voltage Dynamic Range

The VCA824 has a input dynamic range limited to 1.6 V and –2.1 V. Increasing the input voltage dynamic range can be done by using an attenuator network on the input. If the VCA824 is trying to regulate the amplitude at the output, such as in an AGC application, the input voltage dynamic range is directly proportional to Equation 2.

$$V_{IN(PP)} = R_G \times I_{RG(PP)} \quad (2)$$

As such, for unity-gain or under-attenuated conditions, the input voltage must be limited to the CMIR of ±1.6 V (3.2 V_{PP}) and the current (I_{RG}) must flow through the gain resistor, ±2.6 mA (5.2 mA_{PP}). This configuration sets a minimum value for R_E such that the gain resistor must be greater than Equation 3.

$$R_{GMIN} = \frac{3.2V_{PP}}{5.2mA_{PP}} = 615.4\Omega \quad (3)$$

Values lower than 615.4 Ω are gain elements that result in reduced input range, as the dynamic input range is limited by the current flowing through the gain resistor R_G (I_{RG}). If the I_{RG} current limits the performance of the circuit, the input stage of the VCA824 goes into overdrive, resulting in limited output voltage range. Such I_{RG}-limited overdrive conditions are shown in Figure 40 for the gain of 10V/V and Figure 60 for the gain of 40 V/V.

Device Functional Modes (continued)

8.4.4 Output Voltage Dynamic Range

With its large output current capability and its wide output voltage swing of ±3.9 V typical on 100-Ω load, it is easy to forget other types of limitations that the VCA824 can encounter. For these limitations, careful analysis must be done to avoid input stage limitation: either voltage or I_{RG} current. Note that if control pin V_G varies, the gain limitation may affect other aspects of the circuit.

8.4.5 Bandwidth

The output stage of the VCA824 is a wideband current-feedback amplifier. As such, the feedback resistance is the compensation of the last stage. Reducing the feedback element and maintaining the gain constant limits the useful range of I_{RG}, and therefore, reduces the gain adjust range. For a given gain, reducing the gain element limits the maximum achievable output voltage swing.

8.4.6 Offset Adjustment

As a result of the internal architecture used on the VCA824, the output offset voltage originates from the output stage and from the input stage and multiplier core. Figure 67 shows how to compensate both sources of the output offset voltage. Use this procedure to compensate the output offset voltage: starting with the output stage compensation, set V_G = –1 V to eliminate all offset contribution of the input stage and multiplier core. Adjust the output stage offset compensation potentiometer. Finally, set V_G = 1 V to the maximum gain and adjust the input stage and multiplier core potentiometer. This procedure effectively eliminates all offset contribution at the maximum gain. Because adjusting the gain modifies the contribution of the input stage and the multiplier core, some residual output offset voltage remains.

8.4.7 Noise

The VCA824 offers 6 nV/$\sqrt{\text{Hz}}$ input-referred voltage noise density at a gain of 10 V/V and 2.6-pA/$\sqrt{\text{Hz}}$ input-referred current noise density. The input-referred voltage noise density considers that all noise terms (except the input current noise but including the thermal noise of both the feedback resistor and the gain resistor) are expressed as one term.

This model is formulated in Equation 4 and Figure 68.

$$e_O = A_{VMAX} \times \sqrt{2 \times (R_S \times i_n)^2 + e_n^2 + 2 \times 4kTR_S} \quad (4)$$

A more complete model is shown in Figure 69. For additional information on this model and the actual modeled noise terms, please contact the High-Speed Product Application Support team at www.ti.com.

8.4.8 Input and ESD Protection

The VCA824 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings*.

All pins on the VCA824 are internally protected from ESD by means of a pair of back-to-back reverse-biased diodes to either power supply, as shown in Figure 64. These diodes begin to conduct when the pin voltage exceeds either power supply by about 0.7 V. This situation can occur with loss of the amplifier power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30 mA without destruction. To ensure long-term reliability, however, diode current should be externally limited to 10 mA whenever possible.

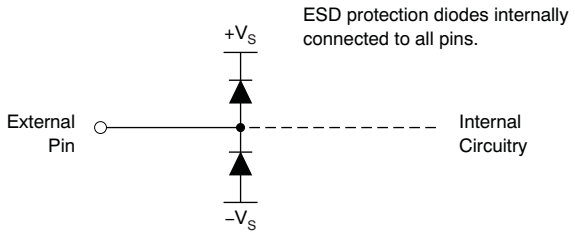


Figure 64. Internal ESD Protection

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Difference Amplifier

Because both inputs of the VCA824 are high-impedance, a difference amplifier can be implemented without any major problem. Figure 65 shows this implementation. This circuit provides excellent common-mode rejection ratio (CMRR) as long as the input is within the CMRR range of –2.1 V to 1.6 V. Note that this circuit does not make use of the gain control pin, V_G. Also, it is recommended to choose R_S such that the pole formed by R_S and the parasitic input capacitance does not limit the bandwidth of the circuit. Figure 66 shows the common-mode rejection ratio for this circuit implemented in a gain of 10 V/V for V_G = 1 V. Note that because the gain control voltage is fixed and is normally set to 1V, the feedback element can be reduced in order to increase the bandwidth. When reducing the feedback element, make sure that the VCA824 is not limited by common-mode input voltage, the current flowing through R_G, or any other limitation described in this data sheet.

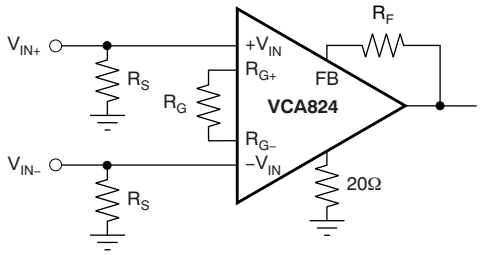


Figure 65. Difference Amplifier

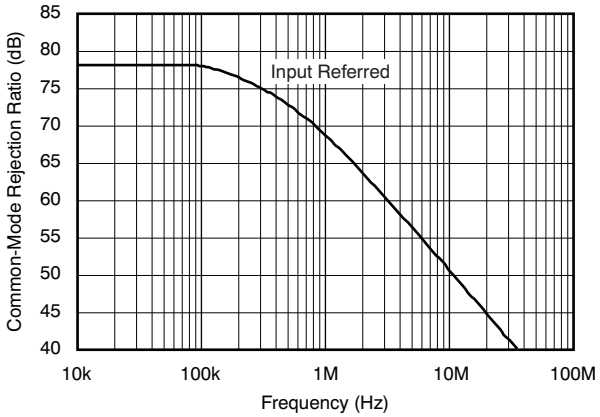


Figure 66. Common-Mode Rejection Ratio

Application Information (continued)

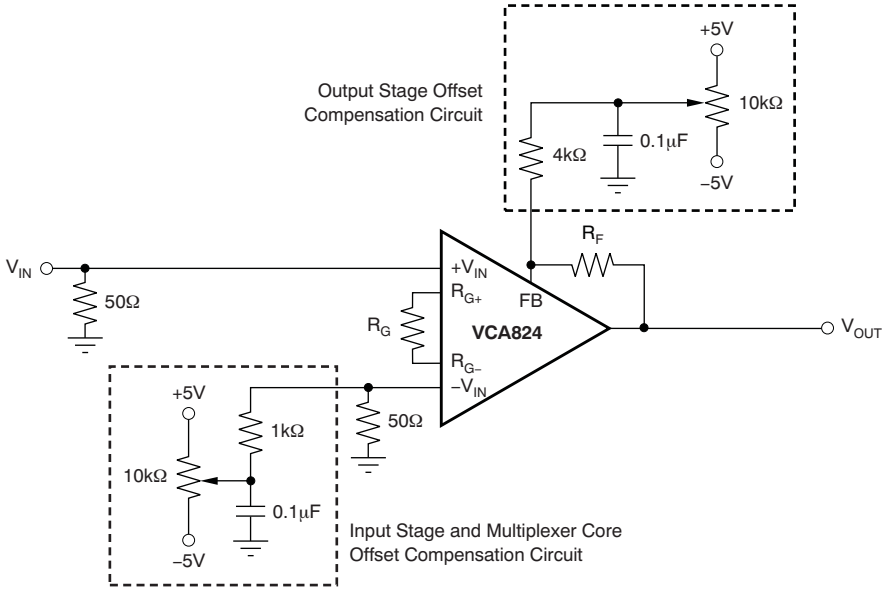


Figure 67. Adjusting the Input and Output Voltage Sources

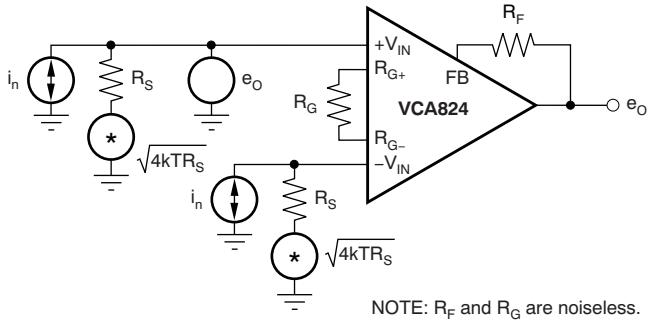


Figure 68. Simple Noise Model

Application Information (continued)

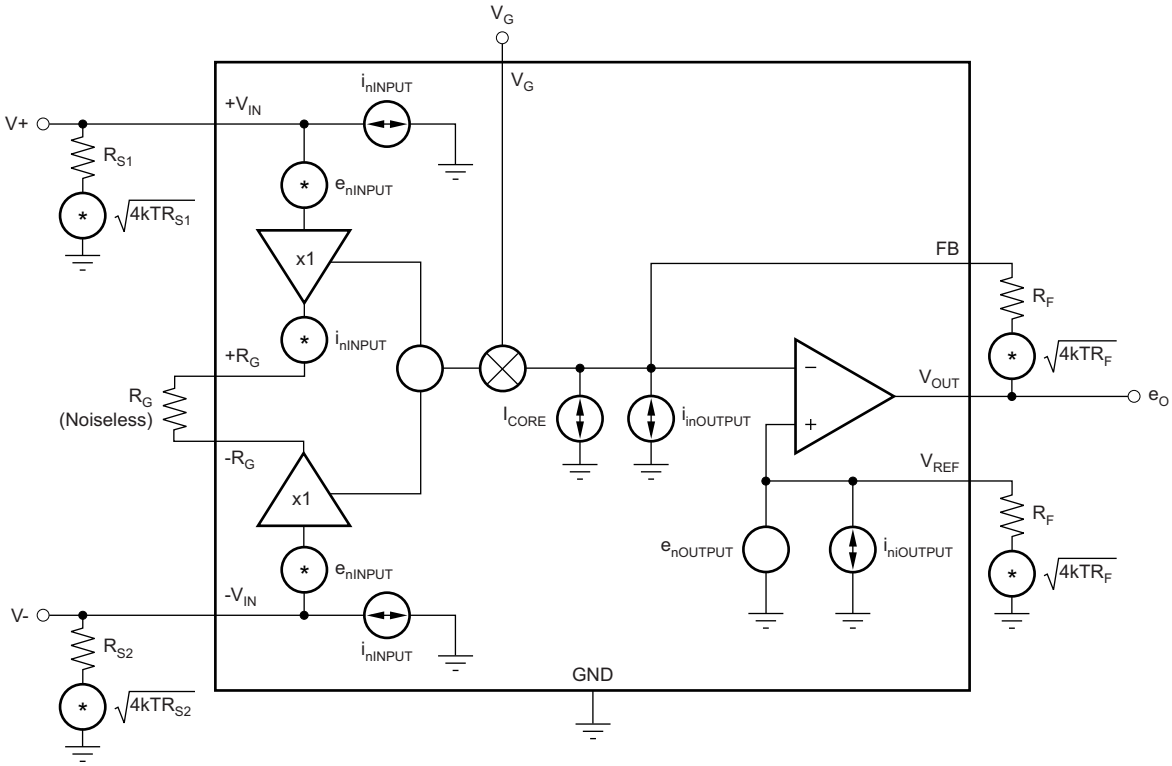


Figure 69. Full Noise Model

Application Information (continued)

9.1.2 Differential Equalizer

If the application requires frequency shaping (the transition from one gain to another), the VCA824 can be used advantageously because its architecture allows the application to isolate the input from the gain setting elements. Figure 70 shows an implementation of such a configuration. The transfer function is shown in Equation 5.

$$G = 2 \times \frac{R_F}{R_G} \times \frac{1 + sR_GC_1}{1 + sR_1C_1} \quad (5)$$

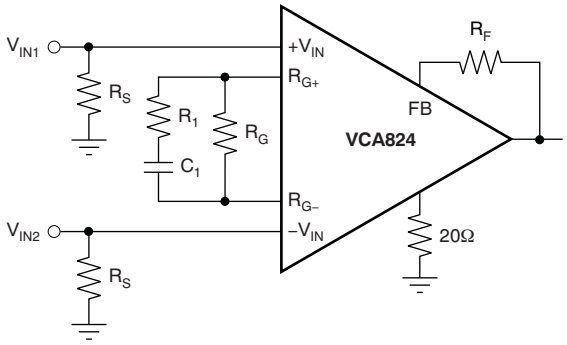


Figure 70. Differential Equalizer

This transfer function has one pole, P_1 (located at R_GC_1), and one zero, Z_1 (located at R_1C_1). When equalizing an RC load, R_L and C_L, compensate the pole added by the load located at R_LC_L with the zero Z_1. Knowing R_L, C_L, and R_G allows the user to select C_1 as a first step and then calculate R_1. Using R_L = 75-Ω, C_L = 100pF and wanting the VCA824 to operate at a gain of 2 V/V, which gives $R_F = R_G$ = 453-kΩ, allows the user to select C_1 = 15.5 pF to ensure a positive value for the resistor R_1. With all these values known, to achieve greater than 300 MHz bandwidth, R_1 can be calculated to be 20-Ω. Figure 71 shows the frequency response for both the initial, unequalized frequency response and the resulting equalized frequency response.

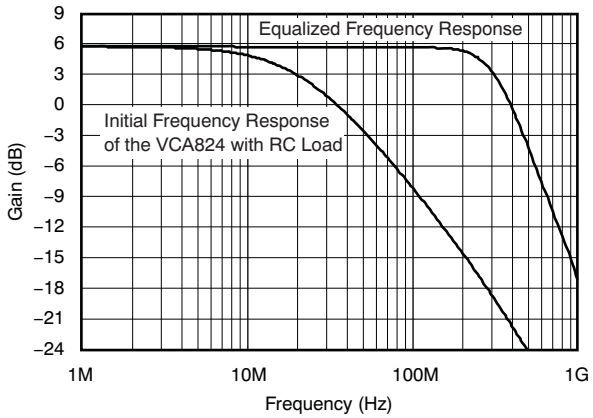


Figure 71. Differential Equalization of an RC Load

9.1.3 Differential Cable Equalizer

A differential cable equalizer can easily be implemented using the VCA824. An example of a cable equalization for 100 feet of Belden Cable 1694F is illustrated in Figure 73, with Figure 72 showing the result for this implementation. This implementation has a maximum error of 0.2 dB from DC to 70 MHz.

Application Information (continued)

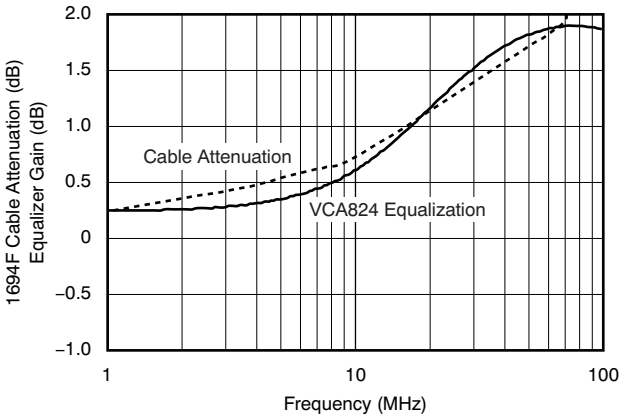


Figure 72. Cable Attenuation vs Equalizer Gain

Note that this implementation shows the cable attenuation side-by-side with the equalization in the same plot. For a given frequency, the equalization function realized with the VCA824 matches the cable attenuation. The circuit in Figure 73 is a driver circuit. To implement a receiver circuit, the signal is received differentially between the $+V_{IN}$ and $–V_{IN}$ inputs.

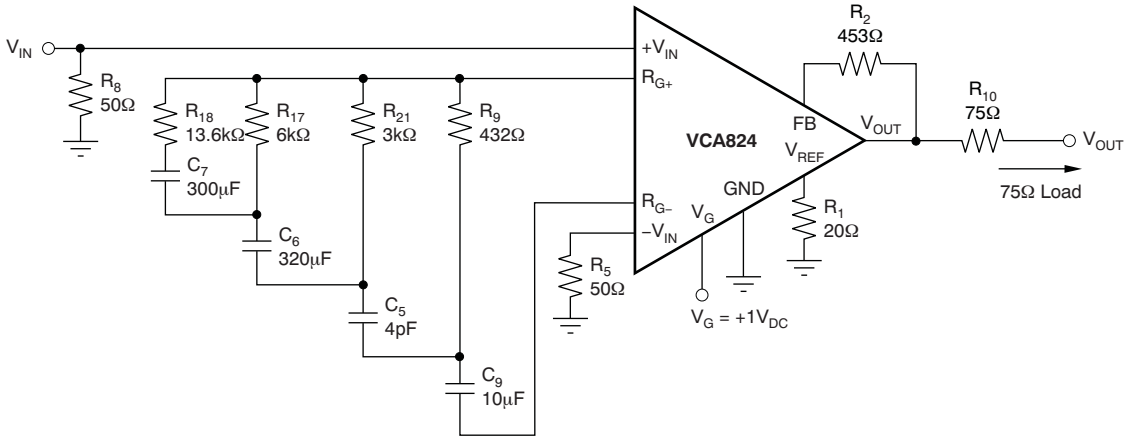


Figure 73. Differential Cable Equalizer

9.1.4 Voltage-Controlled Lowpass Filter [application sub]

In the circuit of Figure 74, the VCA824 serves as the variable-gain element of a voltage-controlled low-pass filter. This section discusses how this implementation expands the circuit voltage swing capability over that normally achieved with the equivalent multiplier implementation. The circuit control voltage, V_G, is calculated as according to the simplified relationship described in Equation 6.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1} \times \frac{1}{1 + s\frac{R_2 C}{G}} \tag{6}$$

Application Information (continued)

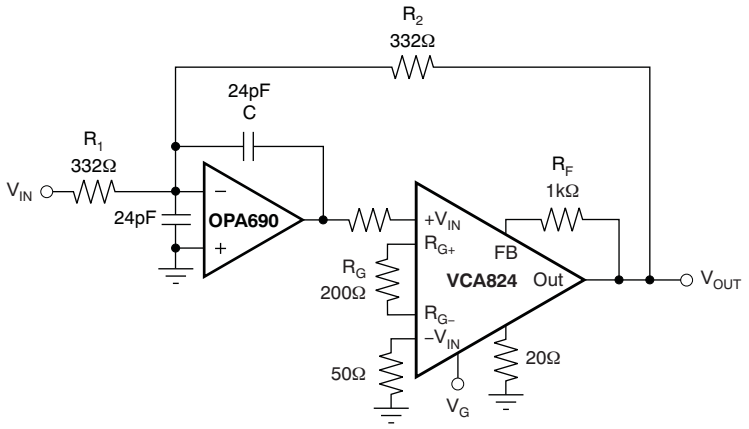


Figure 74. Voltage-Control Low-Pass Filter

The response control results from amplification of the feedback voltage applied to R_2. First, consider the case where the VCA824 produces G = 1V/V. Then this circuit performs as if the amplifier were replaced by a short circuit. Visually replacing the amplifier by a short leaves a simple voltage-feedback amplifier with a feedback resistor bypassed by a capacitor. Replacing this gain with a variable gain, G, the pole can be written as shown in Equation 7.

$$f_8 = \frac{G}{2\pi R_2 C} \tag{7}$$

Because the VCA824 is most linear in the midrange, the median of the adjustable pole should be set at V_G = 0V (see Figure 13, Figure 33, Figure 54, and Equation 8). Selecting $R_1 = R_2 = 332\Omega$, and targeting a median frequency of 10MHz, the capacitance (C) is 24pF. Because the OPA690 was selected for the circuit of Figure 74, and in order to limit peaking in the OPA690 frequency response, a capacitor equal to C was added on the inverting mode to ground. This architecture has the effect of setting the high-frequency noise gain of the OPA690 to 2V/V, ensuring stability and providing flat frequency response.

$$-0.8V \le V_G \le 0.8V \tag{8}$$

Once the median frequency is set, the maximum and minimum frequencies can be determined by using V_G = –0.8 V and V_G = 0.8 V in the gain equation of Equation 9. Note that this is a first-order analysis and does not take into consideration the open-loop gain limitation of the OPA690.

$$G = 2 \times \frac{R_F}{R_G} \times \frac{V_G + 1}{2} \tag{9}$$

With the components shown, the circuit provides a linear variation of the low-pass cutoff from 2MHz to 20MHz, using $-1V \le V_G \le 1V$.

9.1.5 Wideband Variable Gain Amplifier Operation

The VCA824 provides an exceptional combination of high output power capability with a wideband, greater than 40dB gain adjust range, linear in V/V variable gain amplifier. The VCA824 input stage places the transconductance element between two input buffers, using the output currents as the forward signal. As the differential input voltage rises, a signal current is generated through the gain element. This current is then mirrored and gained by a factor of two before reaching the multiplier. The other input of the multiplier is the voltage gain control pin, V_G. Depending on the voltage present on V_G, up to two times the gain current is provided to the transimpedance output stage. The transimpedance output stage is a current-feedback amplifier providing high output current capability and high slew rate, 2500 V/μs. This exceptional full-power performance comes at the price of relatively high quiescent current (36.5 mA), but low input voltage noise for this type of architecture (6 nV/$\sqrt{\text{Hz}}$).

Application Information (continued)

Figure 75 shows the dc-coupled, gain of 10 V/V, dual power-supply circuit used as the basis of *Electrical Characteristics- V_S = ± 5 V* *Electrical Characteristics: V_S = ±5 V* and *Typical Characteristics*. For test purposes, the input impedance is set to 50-Ω with a resistor to ground and the output impedance is set to 50-Ω with a series output resistor. Voltage swings reported in *Electrical Characteristics- VS = ± 5 V* are taken directly at the input and output pins, while output power (dBm) is at the matched 50-Ω load. For the circuit in Figure 75, the total effective load is 100-Ω ‖ 1-kΩ. Note that for the 14-pin, SOIC package, there is a voltage reference pin, V_{REF} (pin 9). For the 14-pin SOIC package, this pin must be connected to ground through a 20-Ω resistor to avoid possible oscillations of the output stage. In the 10-pin, MSOP package, this pin is internally connected and does not require such precaution. An X2Y® capacitor has been used for power-supply bypassing. The combination of low inductance, high resonance frequency, and integration of three capacitors in one package (two capacitors to ground and one across the supplies) enables the VCA824 to achieve the low second-harmonic distortion reported in *Electrical Characteristics- VS = ± 5 V*.

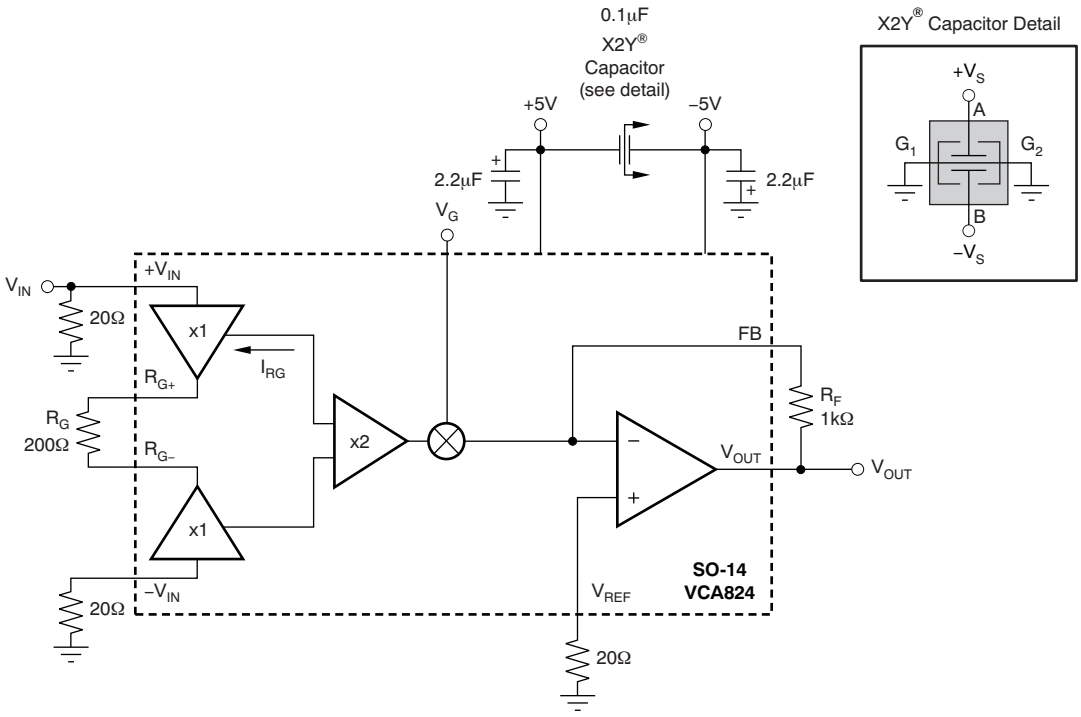


Figure 75. DC-Coupled, A_{VMAX} = 10 V/V, Bipolar Supply Specification and Test Circuit

9.2 Typical Application

A four-quadrant multiplier can easily be implemented using the VCA824. By placing a resistor between FB and V_{IN}, the transfer function depends upon both V_{IN} and V_G, as shown in Equation 10.

$$V_{OUT} = \frac{R_F}{R_G} \times V_G \times V_{IN} + \left(\frac{R_F}{R_G} - \frac{R_F}{R_1} \right) \times V_{IN} \tag{10}$$

Setting R_1 to equal R_G, the term that depends only on V_{IN} drops out of the equation, leaving only the term that depends on both V_G and V_{IN}. V_{OUT} then follows Equation 11.

$$V_{OUT} = \frac{R_F}{R_G} \times V_{IN} \times V_G \tag{11}$$

Typical Application (continued)

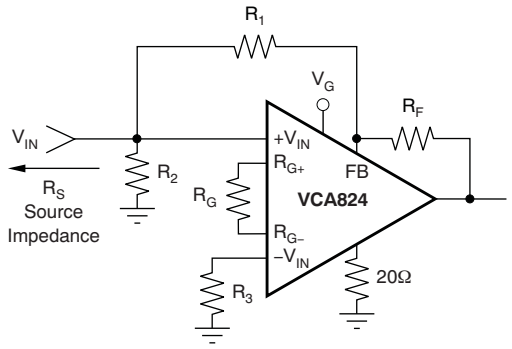


Figure 76. Four-Quadrant Multiplier Circuit

Figure 77 illustrates the behavior of this circuit. Keeping the input amplitude of a 1-MHz signal constant and varying the V_G voltage (100 kHz, 2 V_{PP}) gives the modulated output voltage shown in Figure 77.

9.2.1 Design Requirements

A multiplier requires two inputs, one for the X input and one for the Y input. The output of the multiplier circuit is in the form of Vout = aVin1 × bVin2 : where a and b are real numbers and should not be negative. For four quadrant operation both positive and negative inputs must be supported on the X and Y inputs.

A four-quadrant multiplier can easily be implemented using the VCA824. By placing a resistor between FB and VIN, the transfer function depends upon both VIN and V_G, as shown in Equation 10

9.2.2 Detailed Design Procedure

Setting R1 to equal RG, the term that depends only on VIN drops out of the equation, leaving only the term that depends on both VG and VIN. VOUT then follows Equation 11.

The behavior of this circuit is illustrated in Figure 77. Keeping the input amplitude of a 1MHz signal constant and varying the VG voltage (100 kHz, 2 VPP) gives the modulated output voltage shown in Figure 77.

9.2.3 Application Curve

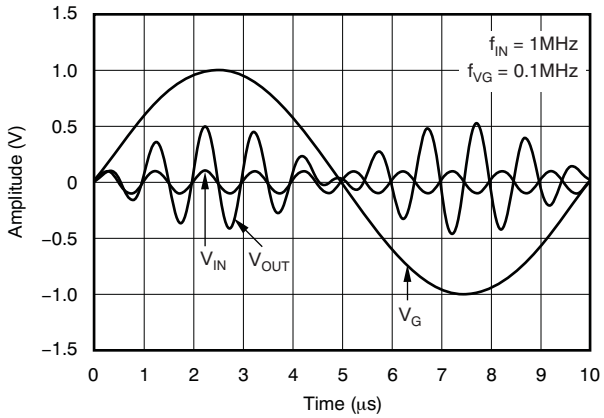


Figure 77. Modulated Output Signal of the 4-Quadrant Multiplexer Circuit

10 Power Supply Recommendations

High-speed amplifiers require low inductance power supply traces and low ESR bypass capacitors. When possible both power and ground planes should be used in the printed circuit board design and the power plane should be adjacent to the ground plane in the board stack-up. The power supply voltage should be centered on the desired amplifier output voltage, so for ground referenced output signals, split supplies are required. The power supply voltage should be from 7-V to 12-V.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the VCA824 requires careful attention to printed circuit board (PCB) layout parasitics and external component types. Recommendations to optimize performance include:

a. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. This recommendation includes the ground pin (pin 2). Parasitic capacitance on the output can cause instability: on both the inverting input and the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board. Place a small series resistance (greater than 25-Ω) with the input pin connected to ground to help decouple package parasitics.

b. **Minimize the distance** (less than 0.25") from the power-supply pins to high-frequency 0.1-μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2-μF to 6.8-μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c. **Careful selection and placement** of external components preserve the high-frequency performance of the VCA824. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin is the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as inverting or noninverting input termination resistors, should also be placed close to the package.

d. **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils, or 1.27 mm to 2.54 mm) should be used, preferably with ground and power planes opened up around them.

e. **Socketing a high-speed part like the VCA824 device is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the VCA824 device onto the board.

11.1.1 Thermal Considerations

The VCA824 does not require heatsinking or airflow in most applications. The maximum desired junction temperature sets the maximum allowed internal power dissipation as described in this section. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by Equation 12:

$$T_J = T_A + P_D \times \theta_{JA} \quad (12)$$

Layout Guidelines (continued)

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, however, it is at a maximum when the output is fixed at a voltage equal to one-half of either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S{}^2/(4 \times R_L)$, where R_L is the resistive load.

Note that it is the power in the output stage and not in the load that determines internal power dissipation. As a worst-case example, compute the maximum T_J using a VCA824ID (SO-14 package) in the circuit of Figure 75 operating at maximum gain and at the maximum specified ambient temperature of 85°C.

$$P_D = 10V(38.5mA) + 5^2/(4 \times 100\Omega) = 447.5mW \quad (13)$$

$$\text{Maximum } T_J = +85°C + (0.449W \times 80°C/W) = 120.8°C \quad (14)$$

This maximum operating junction temperature is well below most system level targets. Most applications should be lower because an absolute worst-case output stage power was assumed in this calculation of $V_{CC}/2$, which is beyond the output voltage range for the VCA824.

11.2 Layout Example

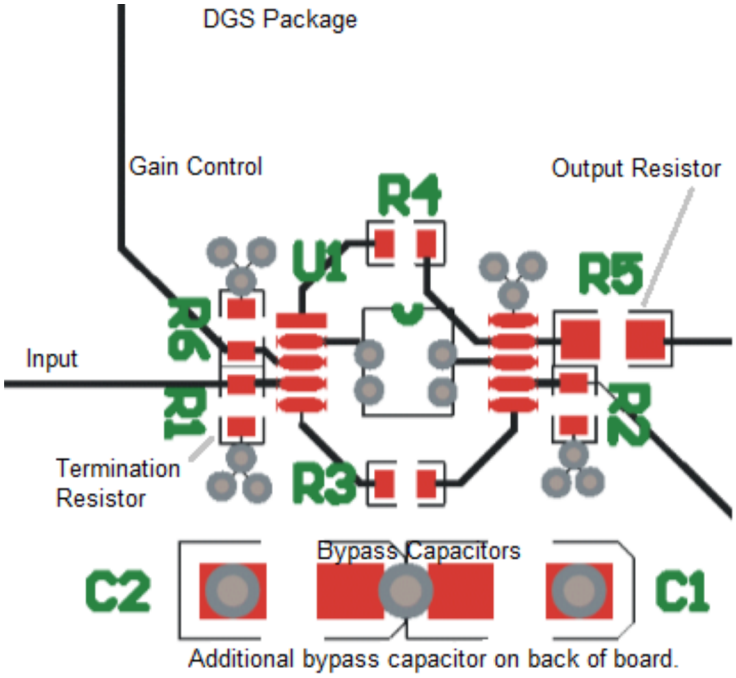


Figure 78. Layout Recommendation

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 デモ用基板

2 種類のパッケージの VCA824 を使用した回路性能の初期評価に便利なように、2 種類のプリント基板 (PCB) を提供しています。どちらの基板も部品なしの PCB として、ユーザー・ガイドとともに無償で提供しています。表 1 に、これらの基板の要約情報を示します。

表 1. EVM 注文情報

製品名	パッケージ	基板の型番	文書の請求番号
VCA824ID	SO-14	DEM-VCA-SO-1B	SBOU050
VCA824IDGS	MSOP-10	DEM-VCA-MSOP-1A	SBOU051

このデモ用基板は、テキサス・インスツルメンツの Web サイト (www.ti.com) の VCA824 製品フォルダで請求できます。

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

E2E is a trademark of Texas Instruments.
X2Y is a registered trademark of X2Y Attenuators LLC.
All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
VCA824ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA824ID
VCA824ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCA824ID
VCA824IDGST	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BOT
VCA824IDGST.A	Active	Production	VSSOP (DGS) | 10	250 | SMALL T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BOT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

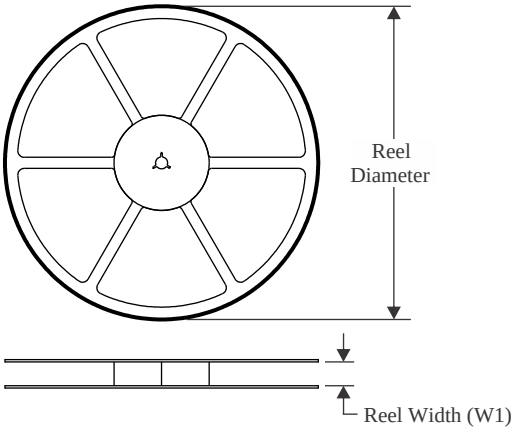
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

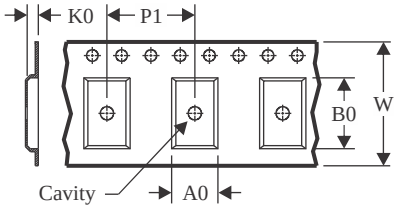
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

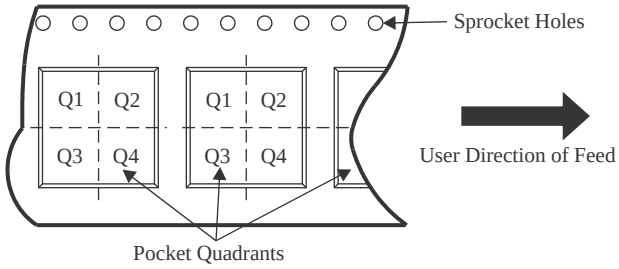


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

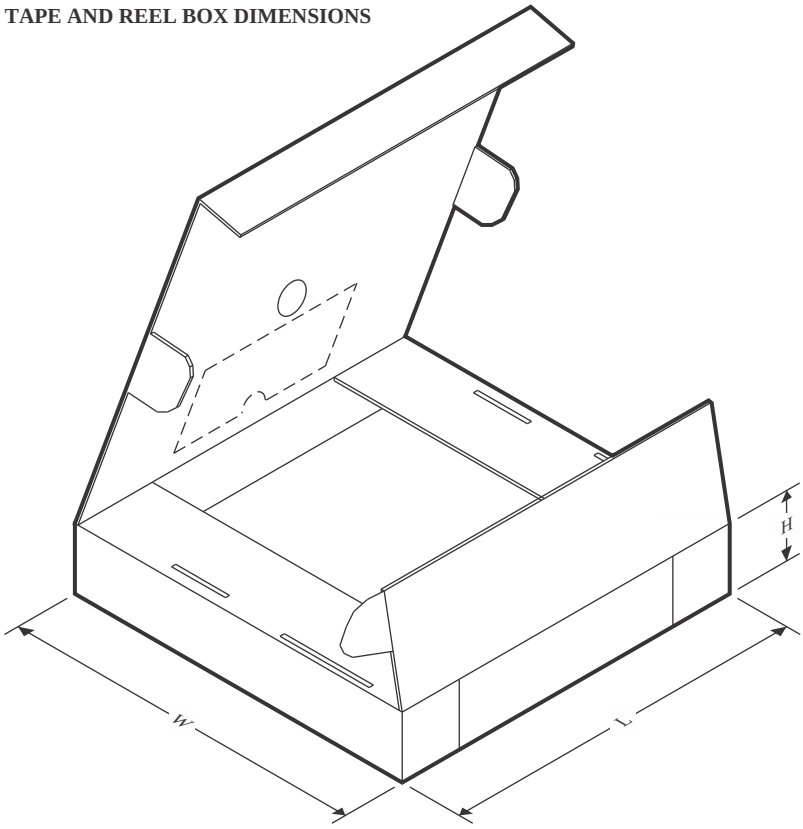
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VCA824IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

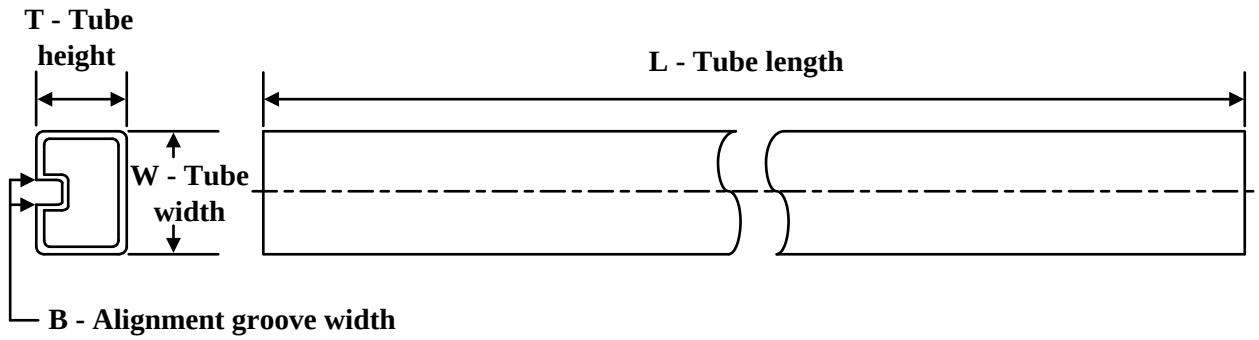
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VCA824IDGST	VSSOP	DGS	10	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

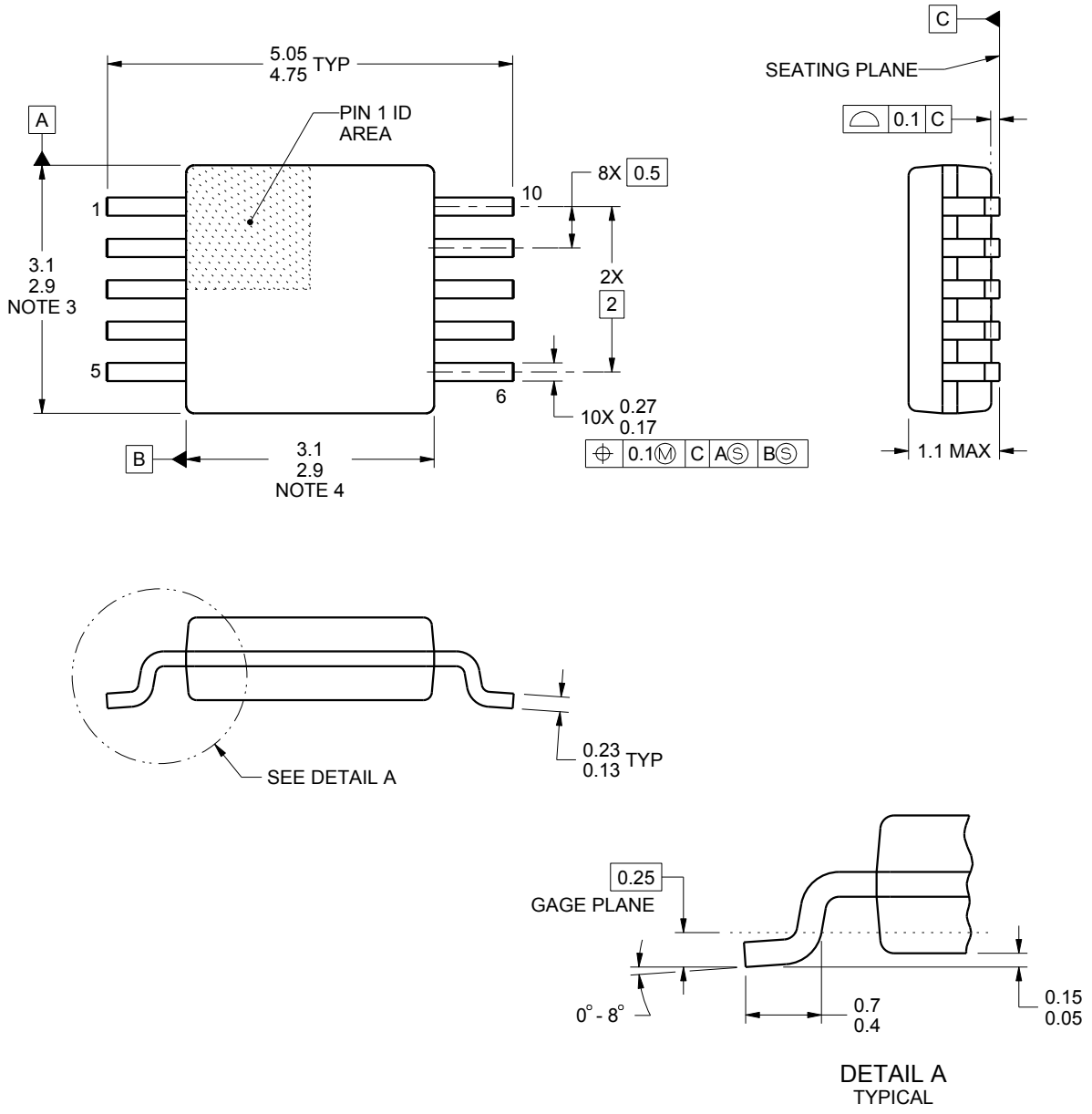
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
VCA824ID	D	SOIC	14	50	506.6	8	3940	4.32
VCA824ID.A	D	SOIC	14	50	506.6	8	3940	4.32

PACKAGE OUTLINE

DGS0010A

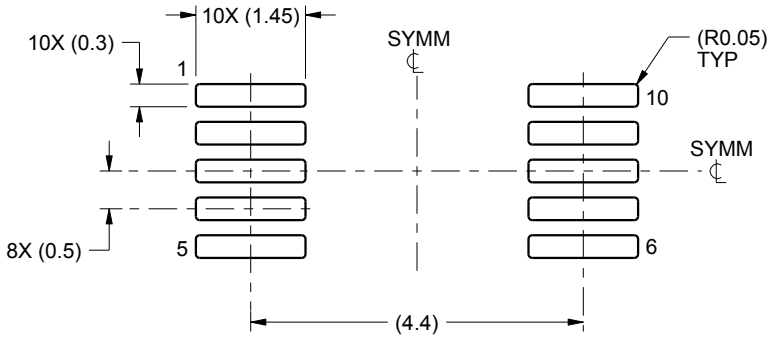
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

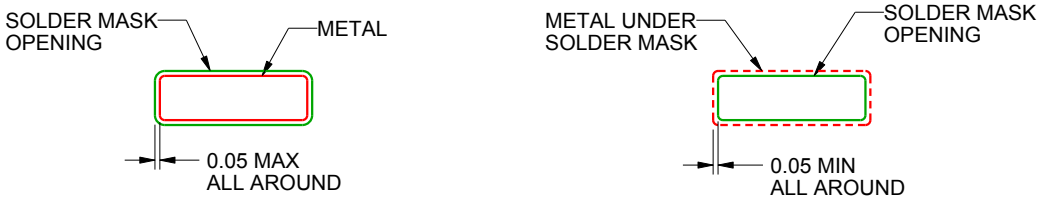


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

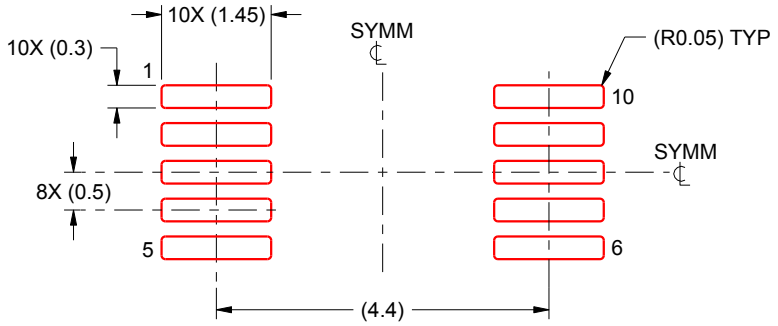


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

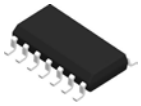


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

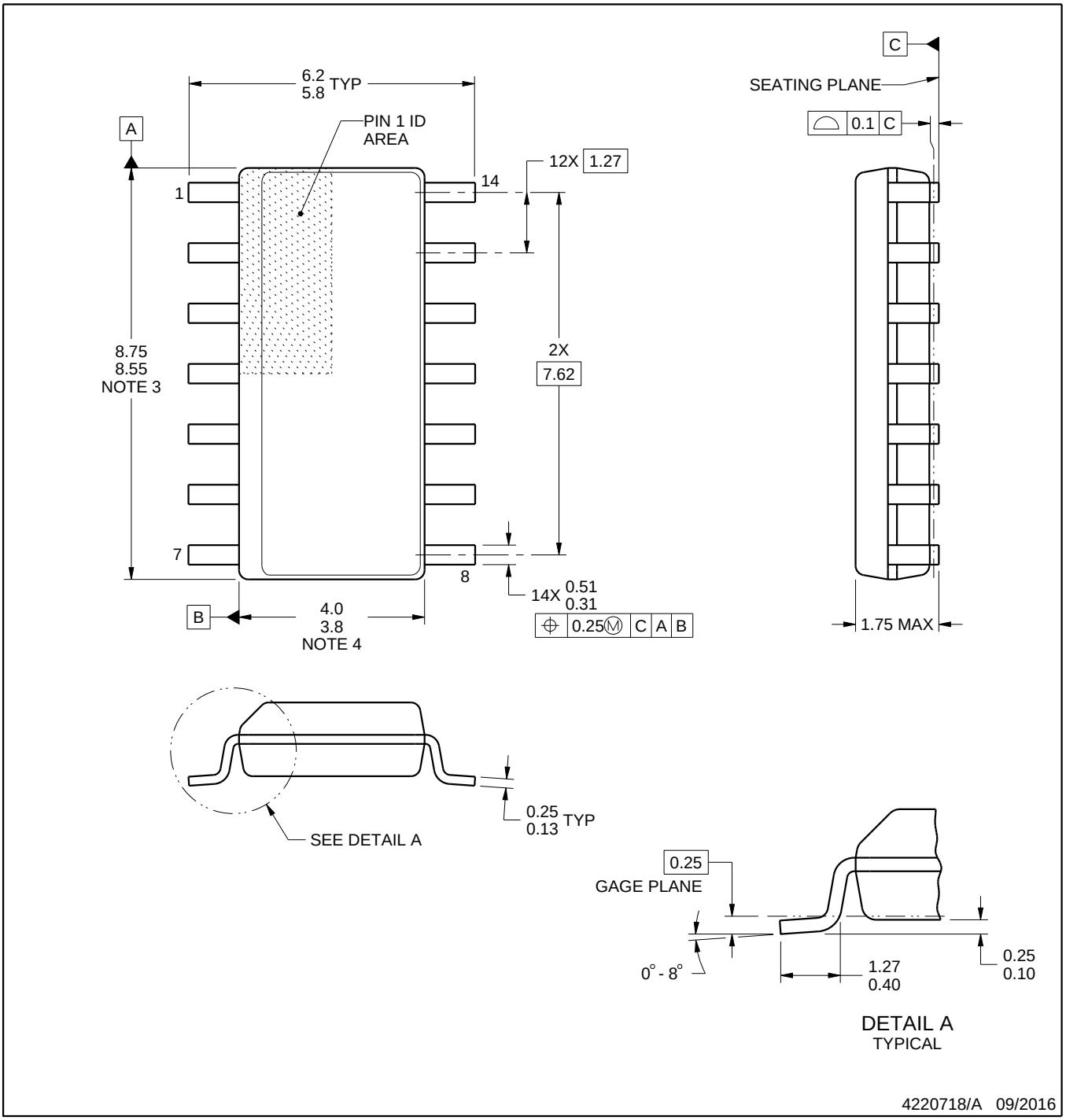


PACKAGE OUTLINE

D0014A

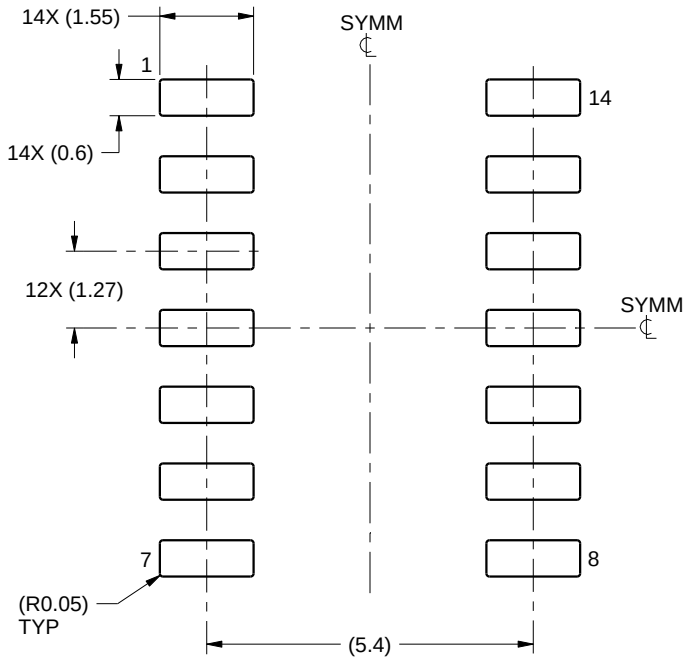
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

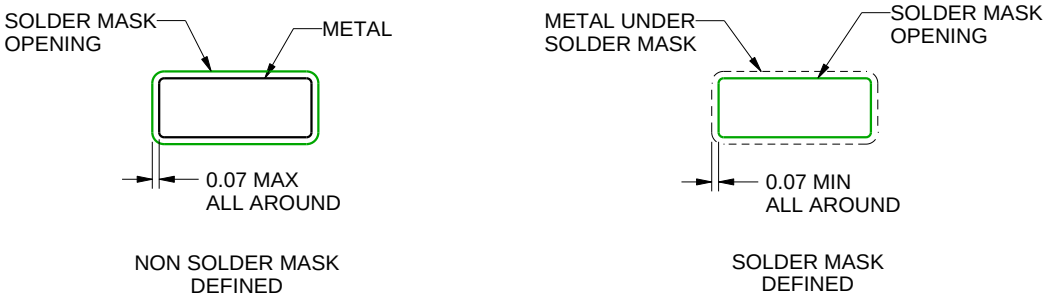


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

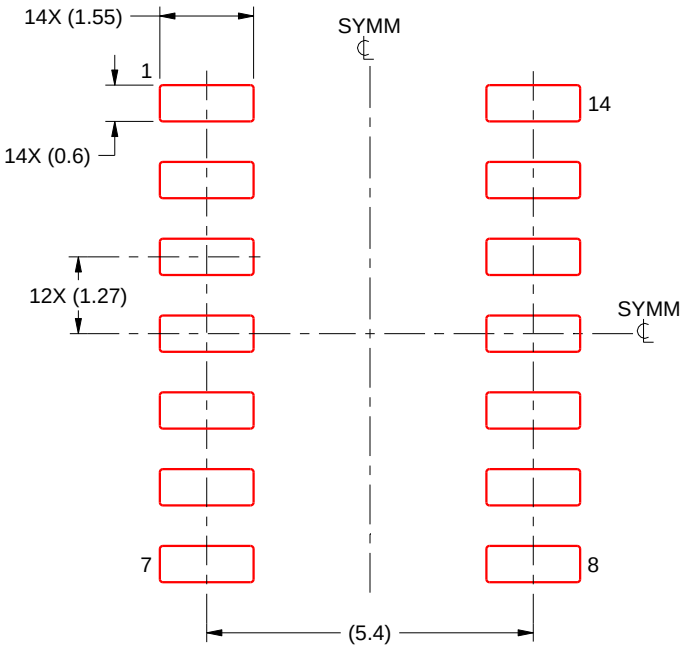
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

最終更新日：2025 年 10 月