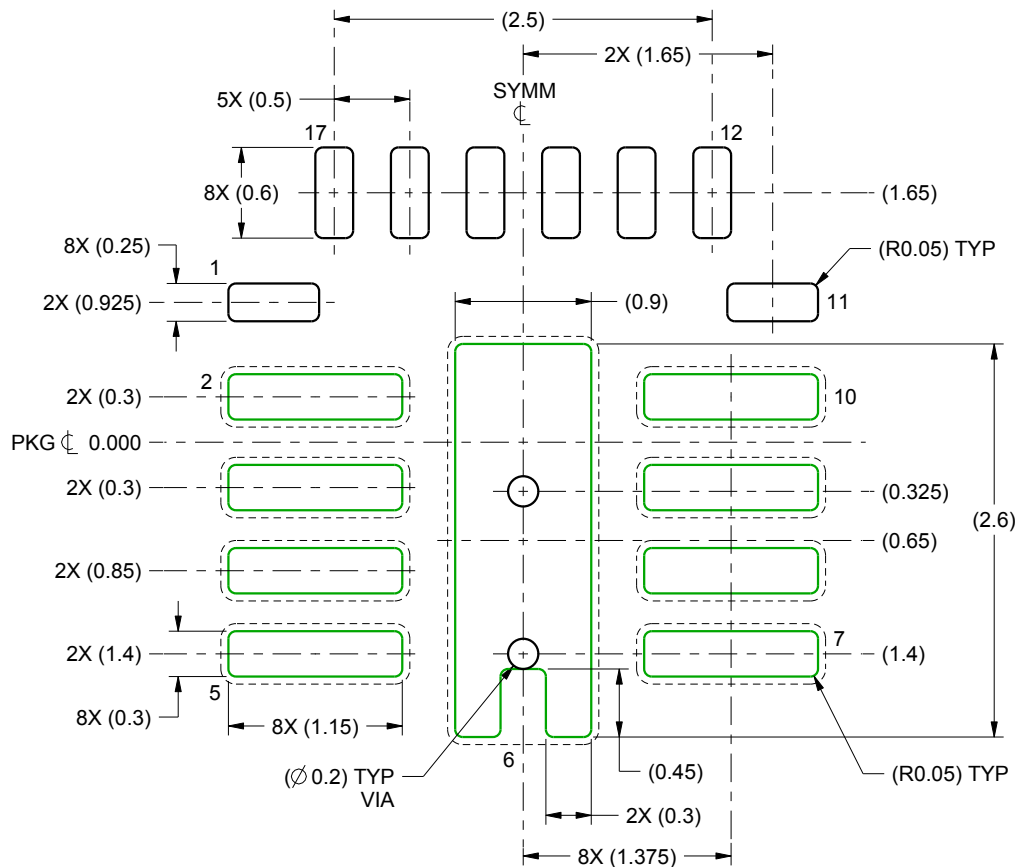


EXAMPLE BOARD LAYOUT

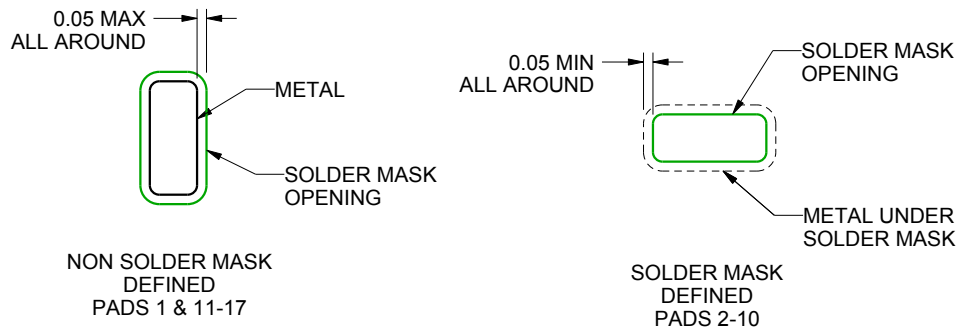
RNV0017A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222776/B 05/2016

NOTES: (continued)

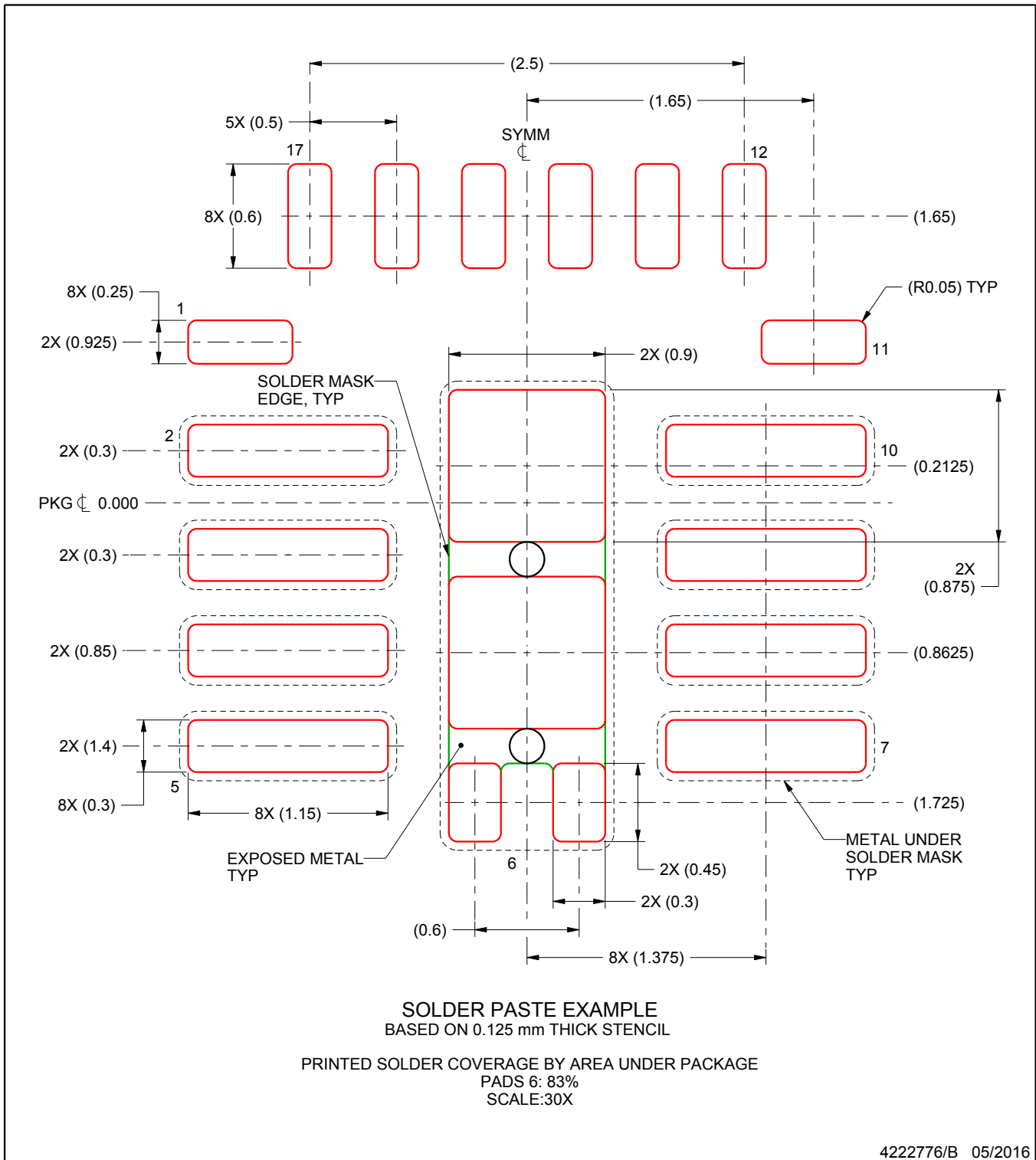
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RNV0017A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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