More Power in Less Space: A Thermal Enhancement Solution for Thin Packages

Mary Helmick, Larry Nye, and Edgar Zuniga
Advanced System Logic – Semiconductor Group

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More Power in Less Space: A Thermal Enhancement Solution for Thin Packages

Abstract: Integrated circuit packaging technology can no longer be treated as a secondary consideration to circuit design. The packaging system is an integral part of the device function, composed of sophisticated materials and complex assembly processes that balances many diverse factors, dramatically impacting the device performance. Often, package design must now be done concurrent with circuit design, understanding the limitations of each on the other.

Recent advances in wafer fabrication technology have forced IC package designers to provide packaging solutions for higher power in smaller spaces. Traditionally, shrinking the size of plastic packages restricts the device performance due to thermal constraints.

Using the equivalent 8- and 16-bit functions as the board space benchmark, a package was needed to accommodate 32- and 36-bit logic devices. The resulting package size presented thermal management problems that had to be addressed with some revolutionary approaches. Additional design goals were the equivalent package reliability to existing packages and the ability to produce the package at an acceptable cost for the target market.

A cross-functional team was structured to include resources from package design, chip design, package assembly, reliability and device testing. Design for Manufacturability concepts were used to meet six sigma process capability on all aspects of the packaging system. The resulting design was a thermally enhanced thin quad flat package (TQFP TEP) that can dissipate 2.4 watts of power in a 256-mm^2 board area, assuming 25°C ambient temperature and 150°C maximum junction temperature.

TRENDS toward higher device functionality in smaller space have driven the development of space-efficient packages. Integrated circuit (IC) devices have evolved from low-pin-count, coarse-pitch, through-hole packages to high-pin count, fine-pitch, surface-mount packages. This evolution has placed new thermal management demands on IC packaging technology.

As plastic packages shrink in area and thickness, thermal impedances increase, limiting the power and frequency at which devices can operate. To take advantage of the increasing capability of IC devices, solutions must be found for smaller packages that can dissipate high power. A traditional option for thermal management is to add external heat sinks to conventional plastic packages, but emerging applications (e.g., laptop and notebook PCs) have placed additional clearance constraints, preventing this approach.

Customer requirements for this package design were: meet existing package reliability levels, 2.4 W power dissipation, footprint smaller than the equivalent function in multiple packages and manufacturable at acceptable cost. A design team was structured to include chip designers, assembly process engineers, package design engineers and key component suppliers to facilitate the development process.

Design Criteria

A new package was required for a family of 32- and 36-bit bus interface logic components. Several constraints were placed on the design of the package: the package must have 100- and 120-pin configurations; the board area must be no larger than that required for the equivalent function in 8- or 16-bit versions; the package must dissipate 2.4 watts without an external heat sink; and the manufacturing cost must be competitive in the marketplace.

Design Approach

Considering the design constraints, two form factors were analyzed; a dual in-line design and a quad design. Device architecture preferred the in-line design, but considering available die bonding and leadframe manufacturing capabilities, an in-line design that met the board space constraint would require a lead pitch of 0.3 mm. Research throughout the marketplace indicated that by 1993, 0.4-mm pitch

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was acceptable, but 0.3-mm pitch was not compatible with current board mount capabilities. The 0.4-mm outer lead pitch quad design was chosen.

Two approaches to thermal enhancement were considered (*Figure 1*) a cavity-type lidded plastic package and an exposed heat slug plastic package. Two heat slug options were evaluated; a heat slug attached to a conventional die pad and direct die attach to a heat slug. All designs were evaluated in chip-up and chip-down configurations.

Thermal models and analytical data showed that both design approaches can dissipate the required power. For each design, the chip-down configuration maximizes the heat transfer from the package, especially with forced convection. In this configuration, the customer has the option to use an external heat sink if the application demands (*Table I*).

The cavity design had addi-

Table I. Modeled Power Dissipation of Various Package Configurations.

Maximum Power Dissipation, Watts — assuming 25°C ambient & 150°C maximum junction temperature			
Package Configuration	**0 ft/min Airflow**	**250 ft/min Airflow**	**500 ft/min Airflow**
Cavity Style Chip Up	2.31	4.24	5.98
Chip Down	2.25	3.77	5.04
Heat Slug Style Chip Up	2.40	4.45	6.35
Chip Down	2.38	4.19	5.81

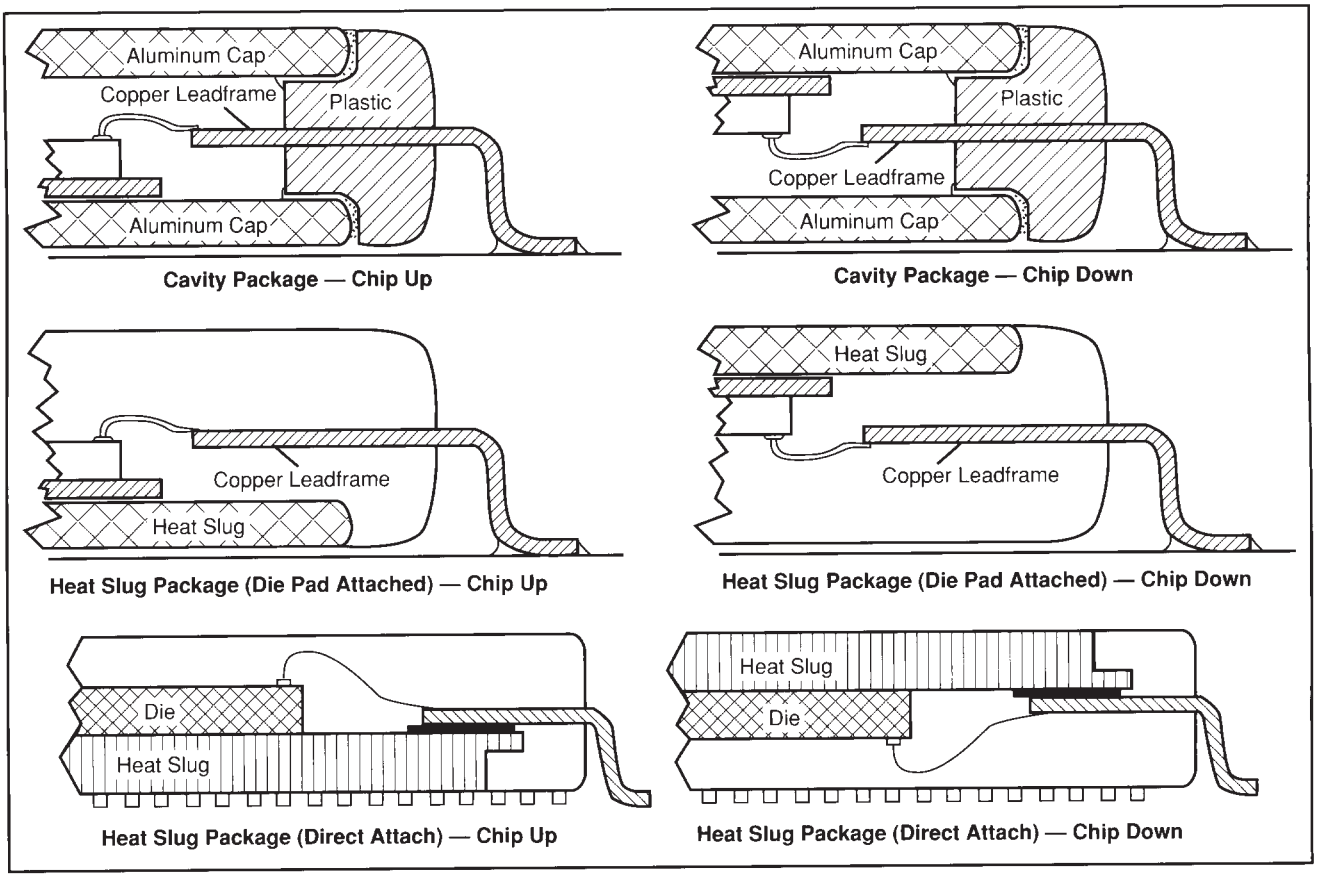


Figure 1. Package Configurations Considered.

tional process complexity and possible reliability problems due to moisture ingress, thermal mismatch and bond wire movement. The heat slug design used conventional processes and equipment. The heat slug design in the chip-down configuration was chosen based on its ability to meet the design criteria, compatibility with existing processes, potential for improved reliability performance and more cost-effective manufacturing flow. The package was designed to meet the emerging JEDEC standard for 1.4-mm thick thin quad flat packages (MO-136) (*Figure 2*).

Material Selection

Thermal constraints drove the use of a copper leadframe and a copper heat slug (*Figure 3*). Based on positive past results with fine-pitch packages, a palladium preplated leadframe was selected. The heat slug was directly attached to the leadframe due to the 1.4-mm thickness of the package. This design, as opposed to a slug attached to the die pad or a drop in heat spreader, gives a more direct heat path to the outside of the package and simplifies the assembly process. The heat slug is attached to the leadframe using a two-sided adhesive film. A polyimide film was chosen due to its stability at elevated processing temperatures and its low moisture absorption. The adhesive film also provides electrical isolation between the heat slug and the lead fingers.

The heat slug required a surface treatment to inhibit corrosion since it was exposed to air. A proprietary surface treatment was selected based on its superior adhesion performance with molding compounds. Shear tests were

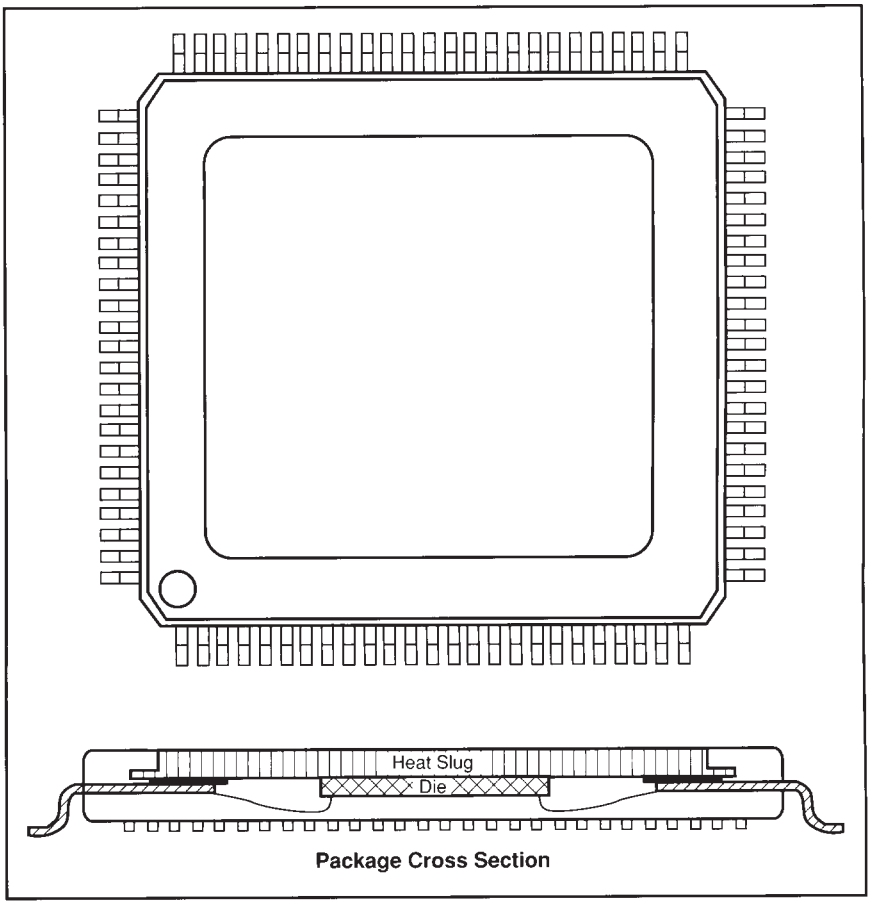


Figure 2. Package Outline Drawing — 100 TQFP TEP.

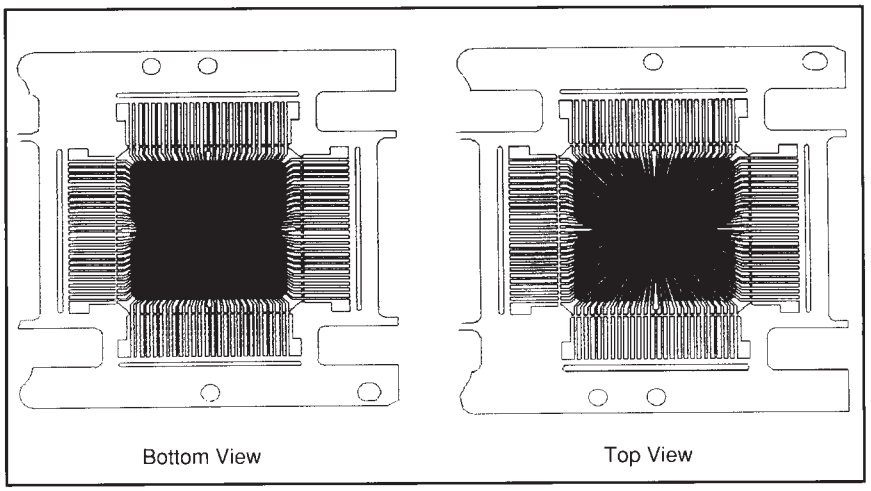


Figure 3. Leadframe with Attached Heat Slug.

run to compare the adhesion of various mold compounds to copper treated with this proprietary process and standard leadframe materials by shearing "buttons" of mold compound off of material samples (*Figure 4*). The "buttons" of compound are molded to the heat slugs or conventional die-attach pads and subjected to the normal post-mold cure process before being sheared from the slugs. The shear force required to remove the "button" from the sample provides a relative adhesion value for different compounds and leadframe or heat slug materials (*Table II*).

Finite element analysis was used to determine the von Mises stress levels in the silicon chip, at the mold compound/chip surface interface and at the die attach/heat slug interface using different size and shape heat slugs (*Figure 5*). Heat slugs with troughs were considered in an attempt to deflect the point of maximum stress away from the ball bond area. For example, in Cases 1 and 3 (Figure 5), while the stress at the ball bond was reduced from 7 K psi to 5.9 K psi with the addition of a trough, stresses at the die attach/heat slug interface increased from 62 K psi to 70 K psi. The die attach/heat slug interface is the weakest "link" in the package, therefore the trough design was not chosen. Heat slug thickness and shape was optimized by balancing thermal and stress responses to meet the design guidelines.

Mold compound candidates were evaluated for wire sweep and autoclave performance and gold wire was chosen to minimize wire sweep in this package. Silicone die coating was evaluated for enhanced die corrosion resistance, but test results showed that this extra processing step was not required to obtain the desired package reliability.

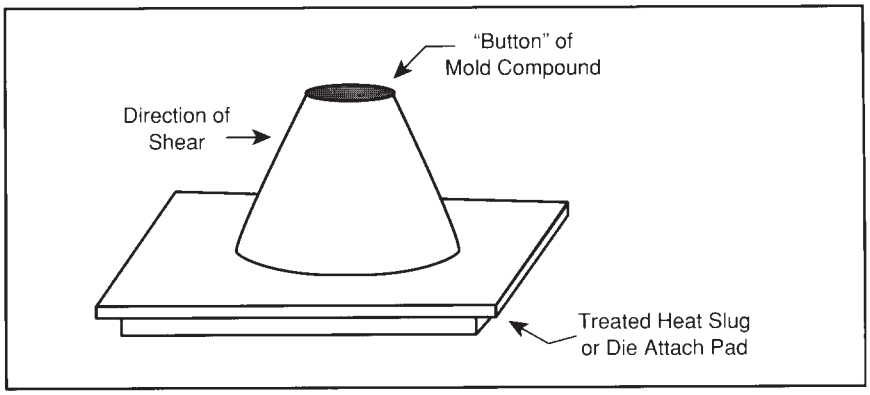


Figure 4. "Button" Shear Test Setup.

Table II. Average Shear Force Normalized for Button Area (psi).

Mold Compound	Cu - Ni Plate	Cu - Pd Plate	Cu - Proprietary Surface Finish
A	0	31	1017
B	182	130	1286

Design Features

The heat slug was designed to maximize the exposed surface area for heat flux and to accommodate the largest possible chip. The heat slug was designed with a flange on the top surface. This flange provides both a locking mechanism with the mold compound and a longer surface interface between the compound and the slug. If moisture penetrates along the slug-mold compound interface, this moisture would have a longer path to reach the die surface. The slug shape also allows for easy orientation in automated assembly processes (*Figure 6*).

The leadframe design employs a preplated palladium finish. The slug is attached to the leadframe using a two-sided adhesive film applied at high temperature. The film is cut in a "window-frame" configuration, providing support for all lead fingers. The package assembly operation starts with an assembled leadframe, which is processed using the same equipment and flows as conventional plastic packages.

The chip-down configuration of this package maximizes the thermal performance. The leadframe design allows the package to be processed conventionally (chip-up) through the molding operation (*Figure 7*). The package orientation is changed before lead form, but this change is transparent to the manufacturing process.

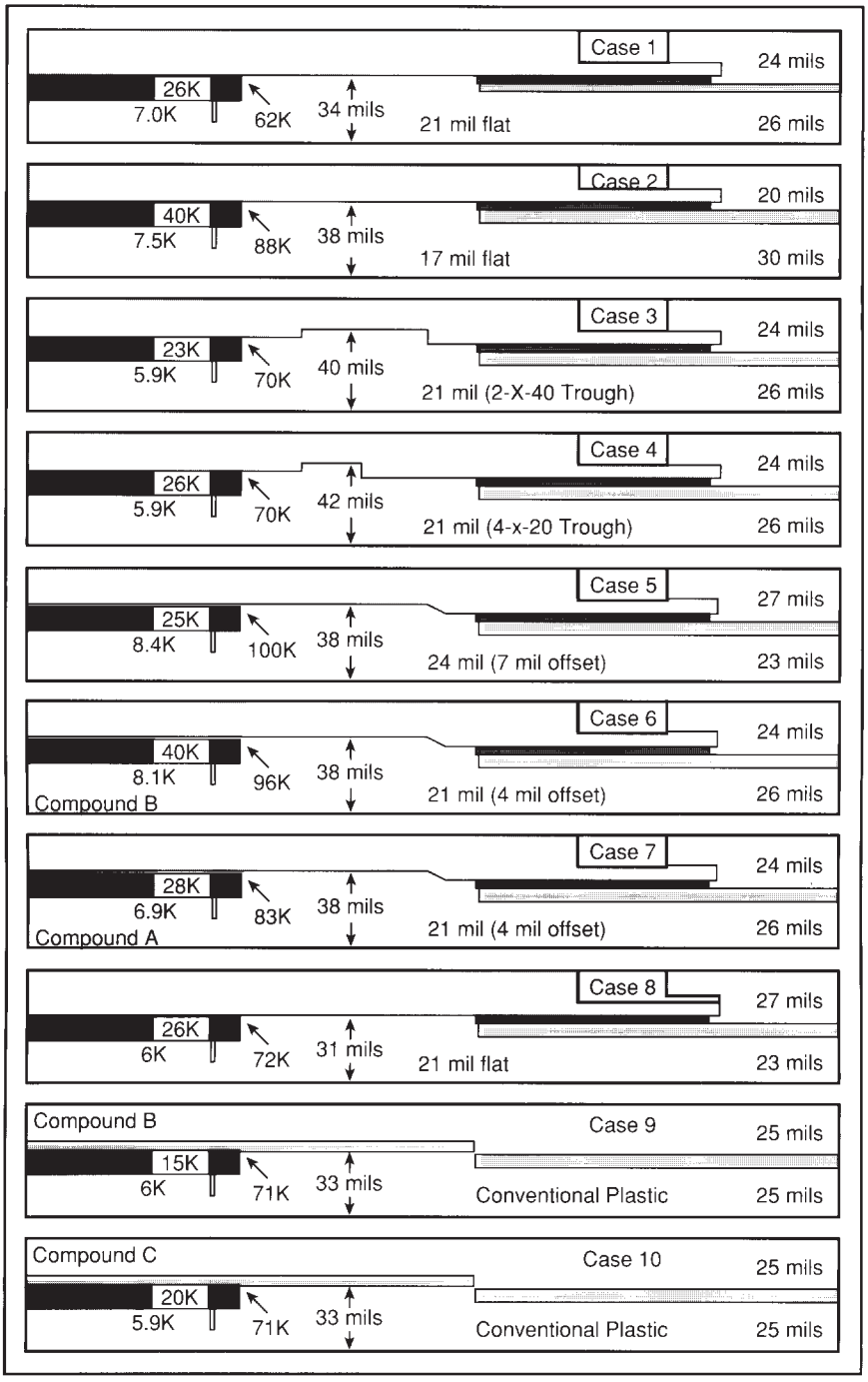


Figure 5. 100/120 Pin TQFP Heat Slug Stress Analysis Comparison of Critical Stress Sites Von Mises Stress (PSI).

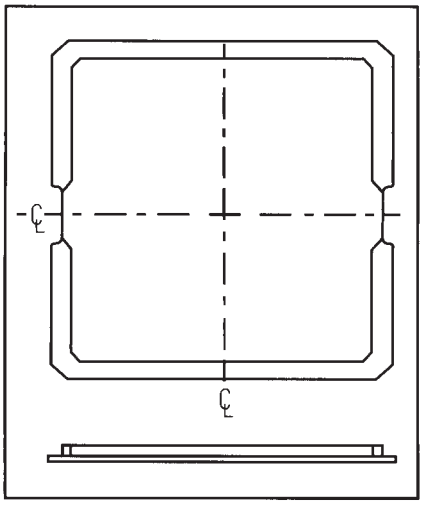


Figure 6. Heat Slug.

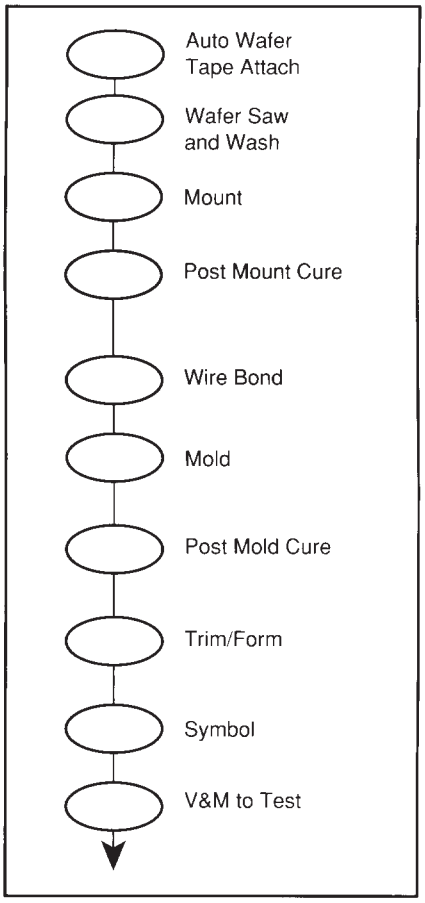


Figure 7. Assembly Process Flow.

Thermal Performance

Both model and analytical data shows that the heat slug package can meet the design constraint of dissipating 2.4 W in either the chip-up or chip-down configurations. The chip-down style was chosen due to its thermal efficiency when airflow is present in the system. When considering if the required heat could be dissipated using a thin package, different thicknesses of heat slugs were modeled. The results showed that a heat slug as thin as 0.015" could be used without sacrificing the desired performance (*Table III*).

Actual power dissipation of all packages is dependent on the thermal impedance of the package, the system ambient temperature, the maximum allowable junction temperature and the available airflow. The TQFP TEP package dissipates between 1 and 5 watts, depending on the system conditions. (See *Figure 8* and *Figure 9*.)

The slug provides a spreading effect for the heat generated by the chip. Since the chip is attached directly to the heat slug, the die attach material is the only thermal resistance interface between the chip and the slug. This interface is relatively short, typically 0.001" and the heat is easily drawn away from the chip. Conventional plastic packages receive some heat spreading effects from the die attach pad, but the heat still has to pass through a layer of plastic molding compound before reaching the ambient air. Compared to the conventional plastic package of the same outline, the heat slug package thermal impedance is 30% lower (*Figure 10*).

Assembly Process Development

Design for manufacturability concepts were used to meet six sigma process capability in every assem-

Table III. Maximum Power Dissipation of 1.4mm Heat Slug Package (Watts) — Thermal Model Data. (Assumes 25°C Ambient Temperature and 150°C Maximum Junction Temperature.)

	0 ft/min airflow	250 ft/min airflow	500 ft/min airflow
0.021" Thick Slug	2.56	3.32	4.37
0.015" Thick Slug	2.49	3.21	4.18

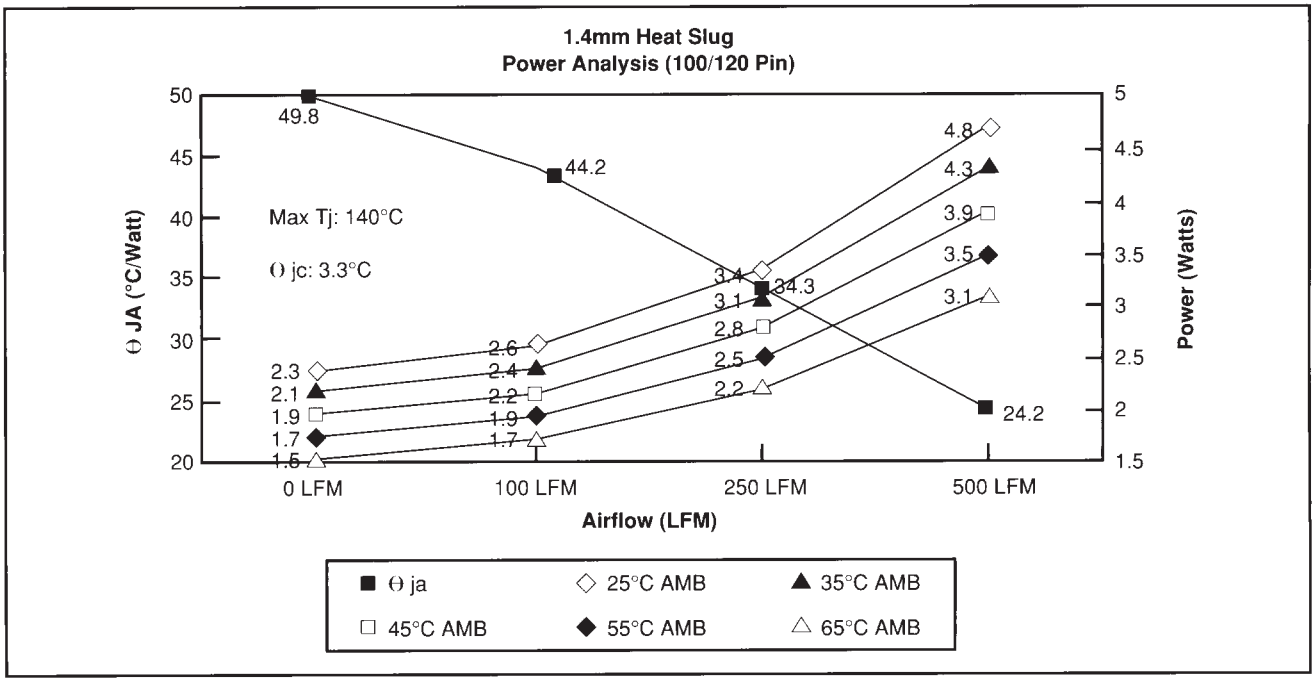


Figure 8. Power Dissipation at Scheduled Ambient Temperatures.

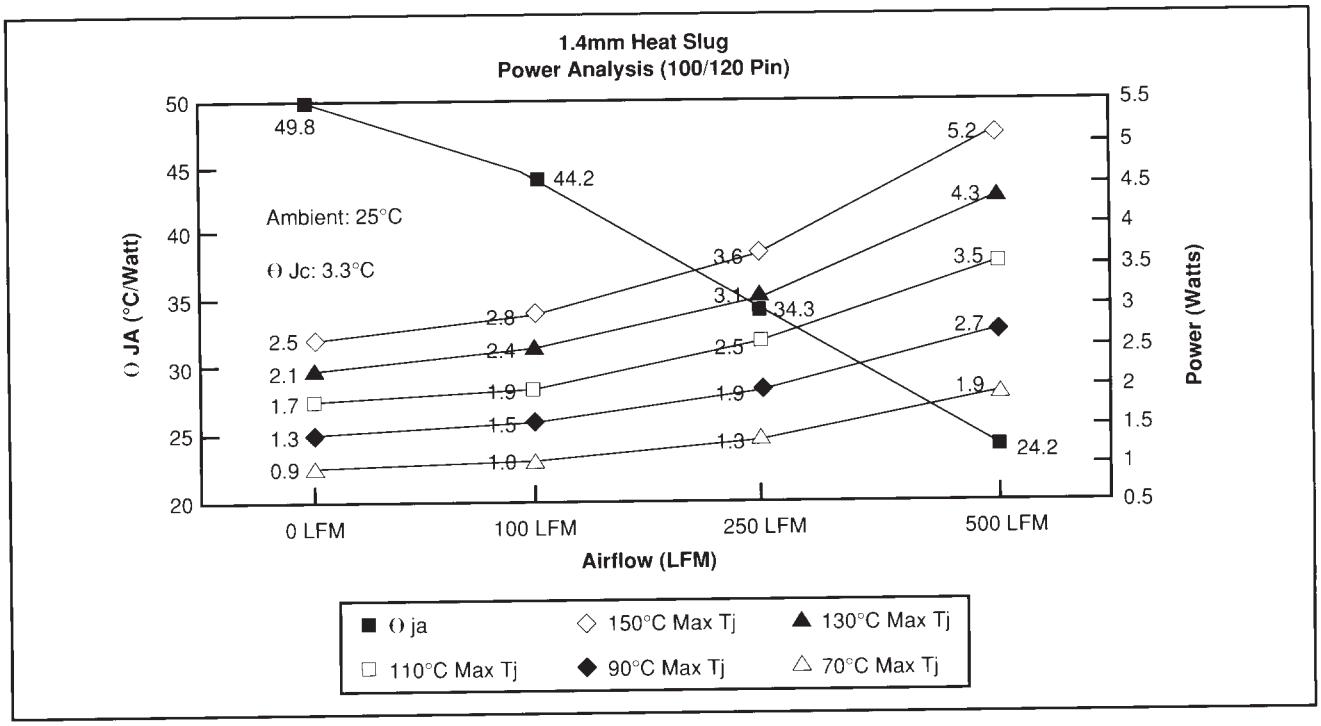


Figure 9. Power Dissipation at Selected Maximum Junction Temperatures.

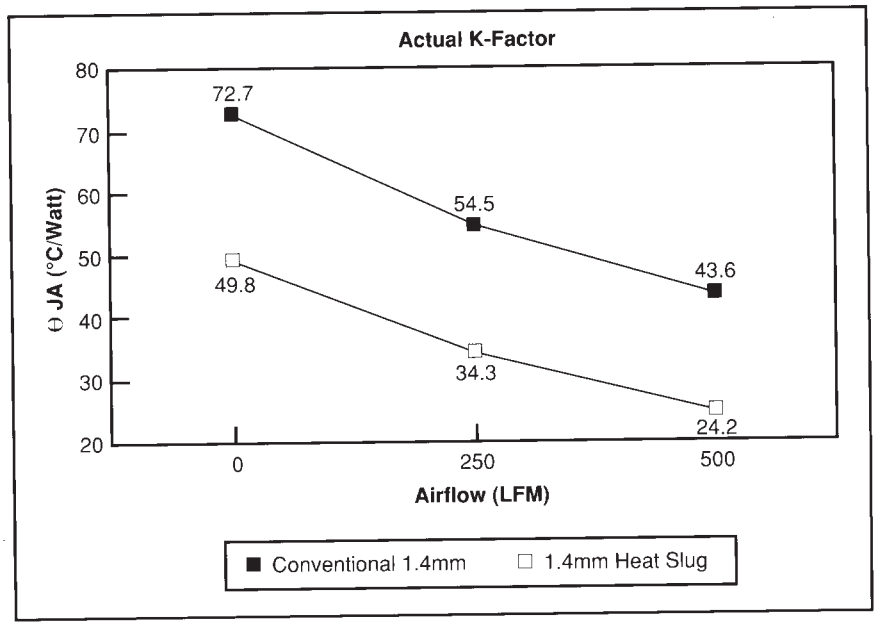


Figure 10. Thermal Impedance of Conventional vs. Heat Slug Packages.

bly process operation. Stress reduction and good thermal dissipation required a low stress die attach material with minimum voiding, thick bond line (>0.001") and excellent adhesion characteristics. Several die attach materials, dispensing needles and parameters were evaluated to find the best combination. The evaluation efforts combined with the improved adhesion characteristics of the heat slug surface treatment yielded a substantial improvement in die shear strength compared with conventional Pd plated leadframes, as *Table IV* shows.

Optimum epoxy application parameters and customized dispenser needles designs allowed us to meet 100% epoxy coverage, less than 10% epoxy voiding and a minimum bond line thickness of 0.001" (*Figure 11*).

Table IV. Average Die Shear Force in Kg.

Die Pad Coating	Die Shear Force	Die Shear Standard Deviation
Pd Plated Die Pad	13.0	2.7
Heat Slug with Surface Treatment	41.2	8.6

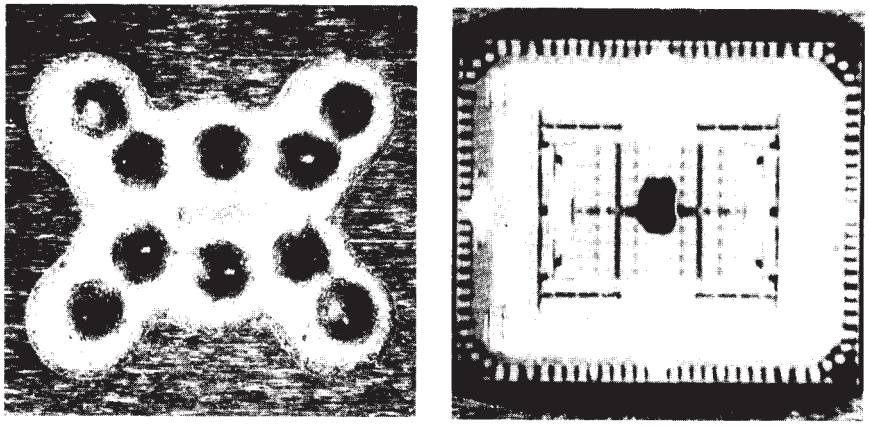


Figure 11. Epoxy Dispensing Pattern.

The heat slug leadframe subassembly required substantial wire bond process development. Heater block design was critical due to the presence of adhesive film in the bonding areas. The fine pitch leadframe fingers and the chip bonding pads required a new capillary design and utilization of advanced wire looping techniques (*Figure 12*).

Mold compounds were evaluated for wire sweep, voiding and moldability (*Table V*). The high-adhesion properties of the mold compound candidates required a unique mold die design, to assist in mold release. Both bond process and mold process optimization were used to minimize wire deflection during the encapsulation process (*Figure 13*).

Devices are symbolized using a proprietary laser process. Ultra precise dam bar removal tooling was required due to the 0.4-mm outer lead pitch. A "cam form" process was used to form leads, preventing damage to the pre-plated 5-mil-thick leads. Optical lead inspection was employed to confirm outgoing coplanarity and lead true position.

Package Reliability

One of the design constraints for developing a thin thermally-enhanced package was that its reliability meet the current reliability level of conventional plastic packages. The heat slug package was tested using the same qualification requirements for all plastic packages. All electrical tests were preconditioned using 168 hours exposure at 85°C/60%RH followed by two reflow operations. *Table VI*

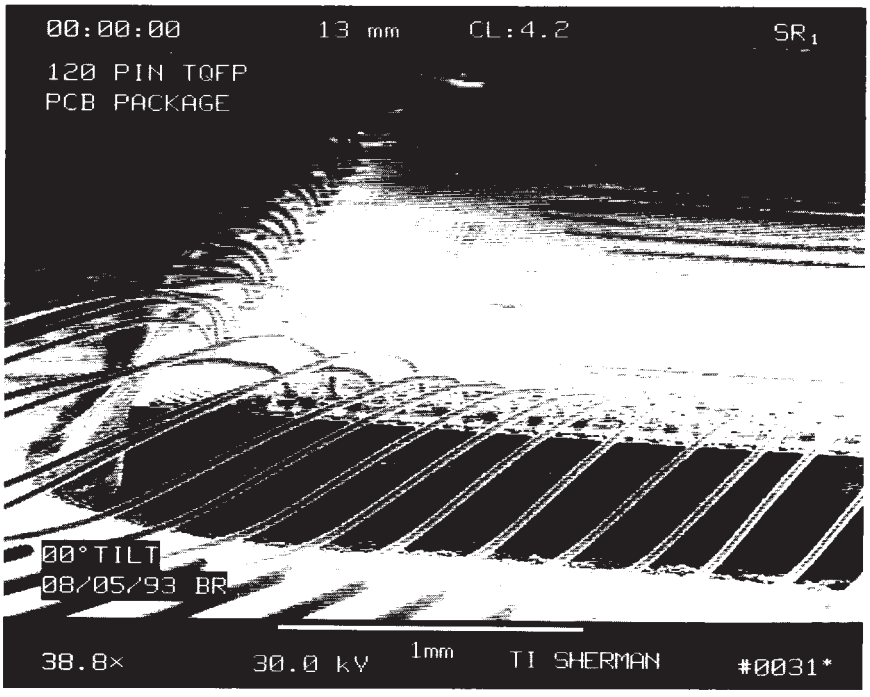


Figure 12. Wire Looping — 120 TQFP.

Table V. Mold Compound Evaluations — Wire Sweep. (*Wire Sweep % Deflection for Various Mold Compounds on 100 Pin TQFP Packages.)

Mold Compound	Compound A	Compound C	Compound D	Compound B	Compound B	Compound E	Compound F
Package Thickness (mm)	1.57	1.9	1.4	1.9	1.4	1.9	1.9
Average (%)	7.02	4.50	5.50	2.89	5.33	4.56	6.94
STD DEV (%)	1.86	1.81	1.37	1.16	1.01	1.07	1.19

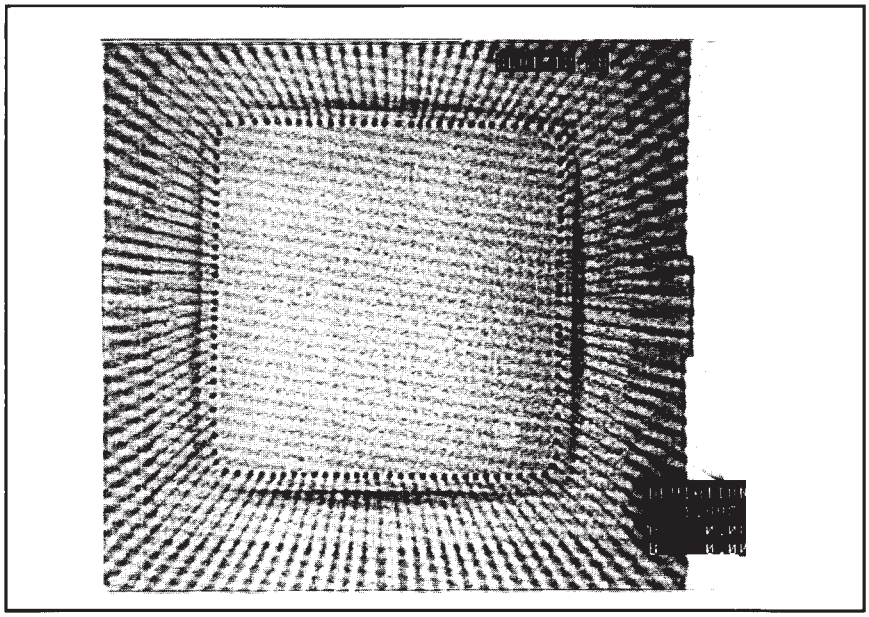


Figure 13. Molded Wires.

describes the results of this reliability qualification testing.

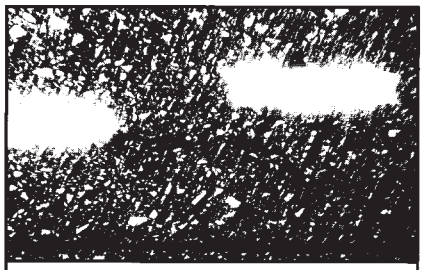
The moisture sensitivity tests were performed per the proposed IPC-SM-786A Level 1 and Level 2 conditions, 168 hours of 85 °C/85 %RH and 168 hours of 85 °C/60 %RH, respectively. The heat slug package passed both Level 1 and Level 2 moisture sensitivity tests, showing no degradation in delamination nor internal cracking after stressing. This is superior performance to a conventional plastic TQFP package. The photos in *Figure 14* show a typical crack in a TQFP package after Level 1 testing and the heat slug package after identical stress conditions (Figure 14).

Level 1 conditions equate to an unlimited exposure time at factory floor conditions of 30°C/ 60%RH and no special "dry" packaging. The Level 2 conditions equate to an exposure time of one year at 30°C/60%RH, providing the devices are protected during shipping and storage using a "dry" packaging scheme. This package provides an excellent opportunity to eliminate the need for desiccated packaging and special handling in a customer's factory.

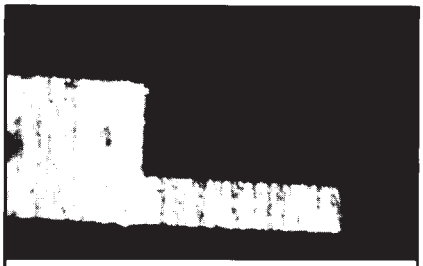
Conclusions

A thermally-enhanced plastic IC package has been developed by a cross-functional team from engineering and manufacturing to meet the constraints of space and power required by the customer. The package was developed with a primary goal of efficiency of manufacturing and compatibility with current plastic package assembly equipment and processes.

The TQFP TEP uses a leadframe subassembly, with a heat slug attached by two-sided adhesive film. This leadframe is processed through conventional assembly processes and equipment, with a change of orientation after the mold process. The proprietary surface treatment of the copper heat slug provides a tenfold improvement in mold compound adhesion and a threefold improvement in die attach adhesion compared to conventional leadframe surface finishes. The slug also provides stability to the thin package, preventing warpage. This package represents a substantial step forward in the quest for plastic IC



Typical Crack in TQFP Package Resulting from "Popcorn Effect"



TQFP TEP Package with No Cracks

Figure 14. Cross Sections of TQFP Packages After 168 Hours 85°C/85%RH.

packages that can meet the ever-increasing power and board space requirements of the electronics industry.

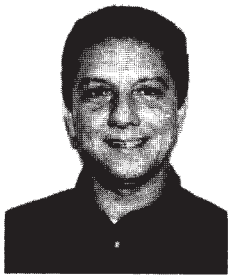
Acknowledgments

The authors would like to express their sincere appreciation to the following people, without whose contributions the development of this package would not have been possible: Bobby O'Donley, Mario Magaña, John Tellkamp, Pedro Cabezas, Mike Pomeroy, John Wiley, Rich Brook, Ray Purdom,

Table VI. 120 Pin TQFP TEP Environmental Test Data.

Test	Duration	Result	Comments
150°C HTRB	300 Hours	0/116	
85°C/85%RH THB	1000 Hours	0/116	
150°C Storage Life	1000 Hours	0/45	
–65°C/150°C Temperature Cycle	1000 Cycles	0/116	
–65°C/150°C Thermal Shock	1000 Cycles	0/116	
121°C/2 ATM Autoclave	240 Hours	0/76	Used Ceramic Substrate
Solderability	8 Hours Steam Age	0/22	Used Ceramic Plate Test
Lead Fatigue		0/22	
Lead Pull	To Destruction	0/22	
Lead Finish Adhesion		0/15	
Salt Atmosphere	24 Hours	0/22	
X-Ray	Top Only	0/5	
Physical Dimension		0/5	
Flammability	A	0/5	
	B	0/5	
	Condition	**Electrical**	**Cracks**
Moisture Sensitivity	168 Hours 85°C/85%RH	0/10	0/10
	168 Hours 85°C/60%RH	0/10	0/10

Terrill Sallee, Jim Fielding, Tomas Luna, Brenda Gogue, Steve Groothius, Dick Shaw, Jim Sisco, Jay Alexander, Archie Sutton, Herb Wyman and others who may have been omitted.

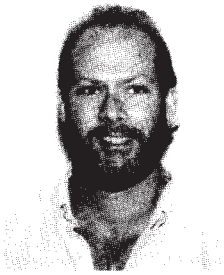


Edgar R. Zuniga

Edgar Zuniga has been involved with the development of new packages since 1989, first as part of the group that developed the 48- and 56-pin SSOP packages. For the last two years he has served as the team leader in the development of the 100- and 120-pin TQFP TEP packages. Before this, Edgar spent two years as engineering section head manager for the assembly operations in the Flexible Assembly Module in Sherman (FAM) and one year as assembly process engineer.

He joined TI in 1975 at the TI plant in El Salvador as a process engineer in the assembly operation. He transferred to Sherman in 1986.

Edgar received a B. S. in electrical engineering in 1977 from the Catholic University, San Salvador, El Salvador, and an M. S. in engineering science from the University of Texas at Dallas in 1993.



Larry Nye

Larry Nye is currently a member of the package development team within the Advanced System Logic Organization. Since 1983, Larry has been heavily involved in die attach and bonding process development activities including programs such as palladium bonding process development, copper wire bonding, low temperature bonding, hermetic chip, bonds over active circuits (BOAC), rapid cure process (RCP), and others.

Besides his development responsibilities, Larry serves as the ASL representative on the Worldwide Mount Commodity Team, the Worldwide Gold Wire Commodity Team and the Worldwide Bond Process Standardization Team. Additional responsibilities include thermal and stress modeling activities along with material characterization and qualification. He joined TI in 1983.

Larry has presented papers twice at the international electronic packaging conference on thermal analysis of semiconductor packages. He has written other papers on palladium bonding and thermal modeling of semiconductor packages. In addition, Larry has served as a co-author on papers dealing with thermal modeling, experimental design, semiconductor package design, and bonds over active circuits (BOAC). He currently has two patents pending in the U.S. patent office.

Mary Helmick

Mary Helmick is part of the package development group for the Advanced System Logic Department in Sherman. Mary joined TI in 1990 as part of the 48- and 56-pin SSOP package development team in the ASL Test/Finish area (formerly FAM). Since 1991 she has been part of ASL packaging engineering, working on the 100/120 pin Heat Slug Package Development Team.

She received her bachelor of science in mechanical engineering from Purdue University in 1986 and her master's degree in computer integrated design and manufacturing from George Washington University in 1989. ❑