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TNETA1570

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HyperSAR

Networking Business Unit

4atm@msg.ti.com

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Agenda

- Main Features
- Interfaces
- Architecture
- Applications
- Summary

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Design Objectives

- **Architecture provides for legacy LAN to asynchronous transfer mode (ATM) translation**
- **High performance (>200 Mbit/s) to support more LAN ports**
- **Direct interface to local switching fabric capability**
- **Efficient buffer chaining and data structures tailored for internetworking products**

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Main Features

FEATURE	BENEFIT
• Supports 200 Mbit/s throughput full-duplex	• Can support a greater number of legacy LAN ports • Provides cut-through capability
• Early segmentation feature • Integrated 32-/64-bit PCI interface	• Easily interfaced to 32- or 64-bit buses
• Easy access to AAL5 trailer information • Supports buffer scatter/gather (transmit/receive buffer chaining)	• Makes it easier to support frame relay over ATM • Makes more efficient use of memory

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Main Features (cont.)

FEATURE	BENEFIT
• Segmentation/reassembly of AAL5 packets	• Full support in hardware for AAL5 processing
• Supports a transparent AAL	• Can be used to support other AALs or for proprietary control
• High-priority transmit mechanism	• Hardware-oriented method to support CBR traffic
• Supports full range of VPIs (12 bits) and 30,720 VCIs	• Can be used for NNI (network-to-network interface) applications
• NNI/UNI option for handling VPIs	• VPI bits masked by 1570 in UNI mode to reduce software overhead

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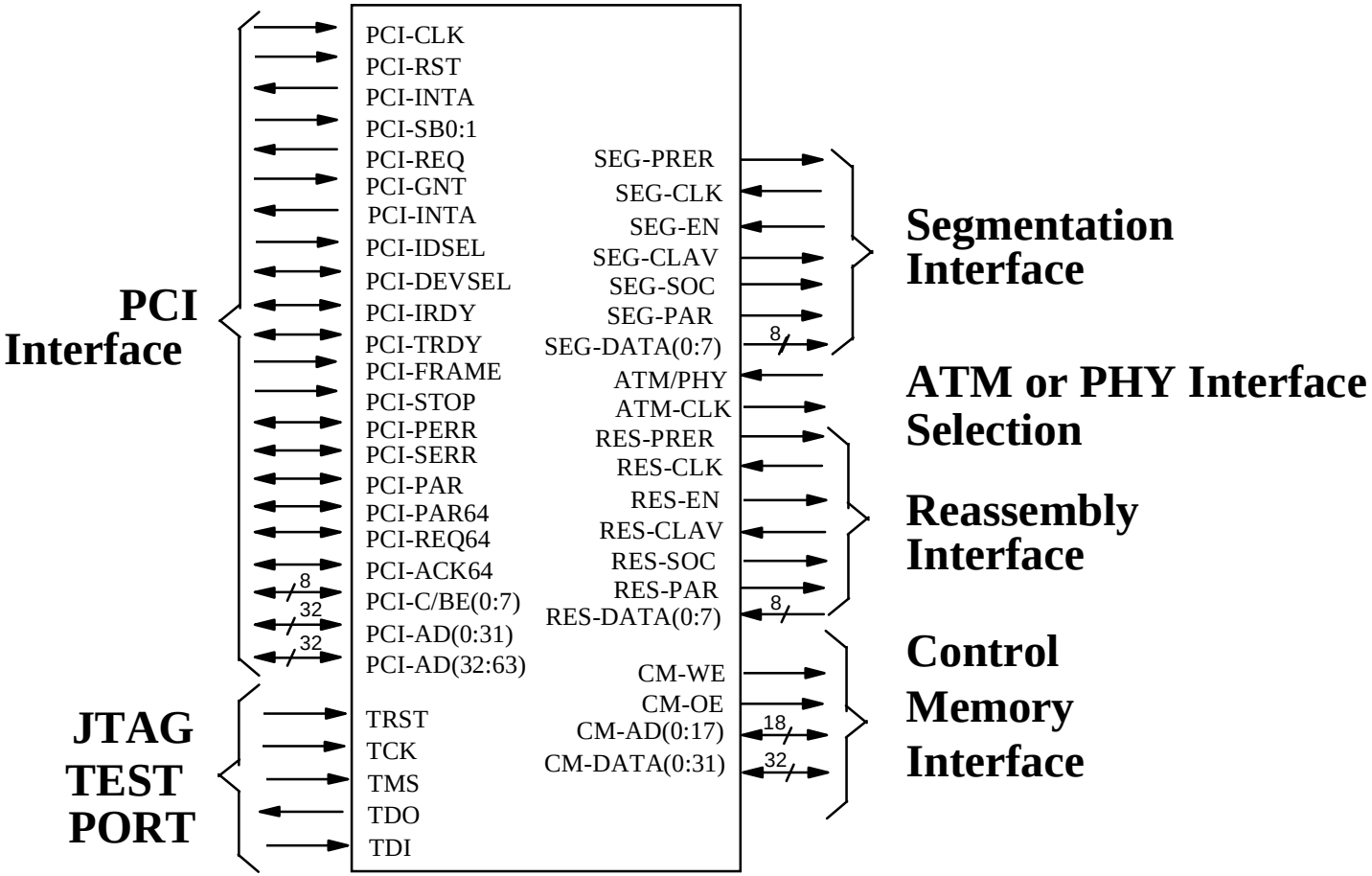
Main Features (cont.)

FEATURE	BENEFIT
• Simultaneous segmentation of up to 1,023 packets	• Can support 1,023 transmit channels at any one time
• Reassembly of 30,720 packets	• Can support 30,720 receive channels at any one time
• Implements optional reassembly time-out for incoming packets	• Allows early release of memory buffers and terminates a channel that has died
• MIB counters for: - IETF; RFC1695 - ATM Forum; UNI 3.1 ILMI	• Provides all the real-time MIB counters on chip to support management functions

Main Features (cont.)

FEATURE	BENEFIT
• UTOPIA Level 1, configurable for physical layer (PHY) or ATM device	• For local switching fabrics, saves cost of PHY devices and provides higher performance
• Calculates and checks HEC byte	• Allows the TNETA1570 to interface directly to switch core when nonATM traffic is coming into the part
• Provides internal loopback for transmit receive	• Provides system diagnostic capability
• Supports JTAG boundary scan interface	• Allows board-level testing

TNETA1570 HyperSAR Interfaces



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PCI Host Interface

FEATURE	BENEFIT
• PCI revision 2.0 compliant host interface	• Complies to industry standards
• Supports single cycle data transfers in burst mode	• Utilizes PCI capabilities for performance
• Operates as a 32-bit PCI slave device for accesses to configuration space, internal registers and control memory	• Ease of use

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PCI Host Interface (cont.)

FEATURE	BENEFIT
• Operates as a bus master device for accesses to data structures in host memory	• Provides high performance throughput for data transfer
• Performs 32- or 64-bit data transfers to/from host memory	• Can interface to 64-bit systems
• In 32-bit PCI mode, upper 32 bits are in quiet mode	• Reduces system noise (ease of use)
• All configuration registers implemented in internal registers	• No external memory required for configuration of device

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Control Memory Interface

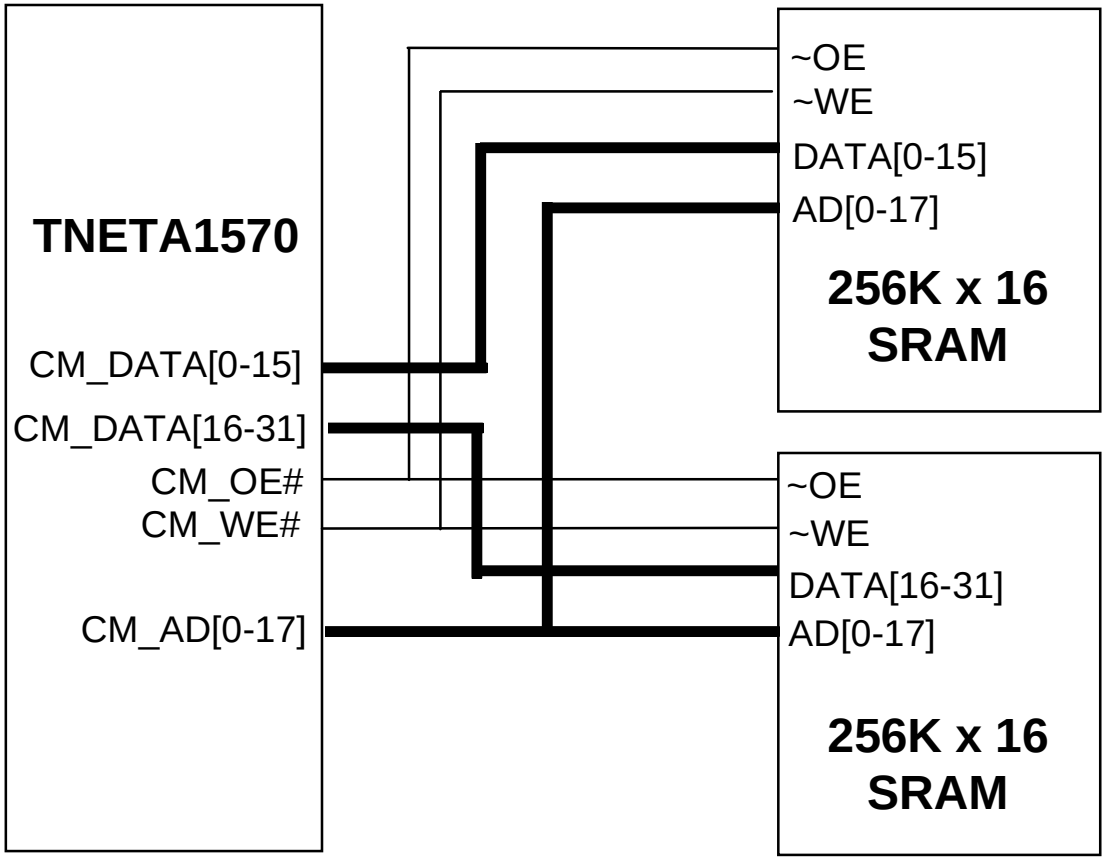
FEATURE

- **Control memory interface provides a glueless interface to local SRAM (15 ns)**
- **Choice of two control memory maps via the configuration register:**
  - **Normal control memory map (32K-256K x 32 SRAM)**
  - **Small control memory map (16K x 32 SRAM)**

BENEFIT

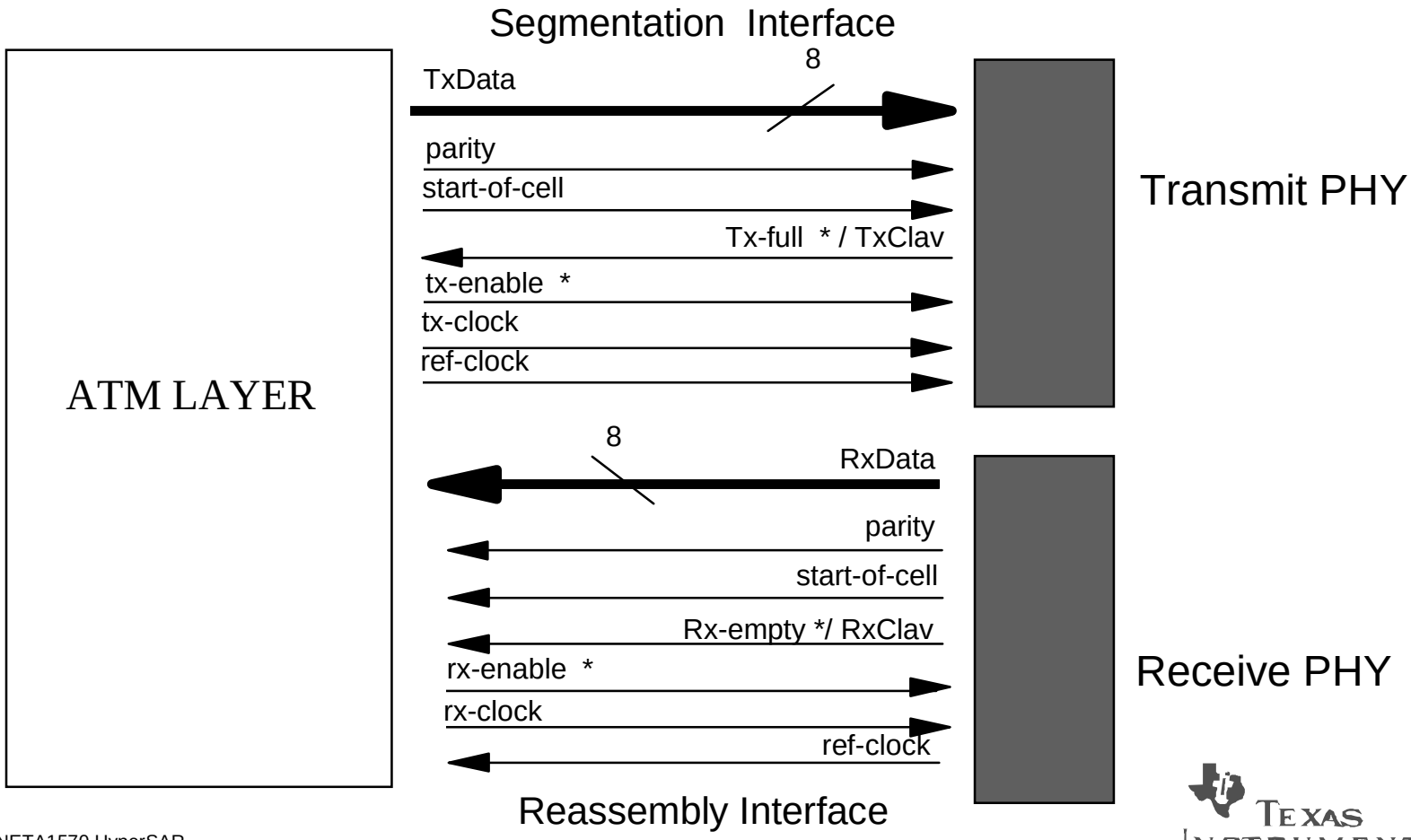
- **No external logic required (saves cost)**
- **Provides the flexibility to scale system features and save cost:**
  - **Allows control memory to handle maximum size of all the data structures**
  - **Restricts the size of data structures to reduce memory requirements**

Control Memory Interface Block Diagram

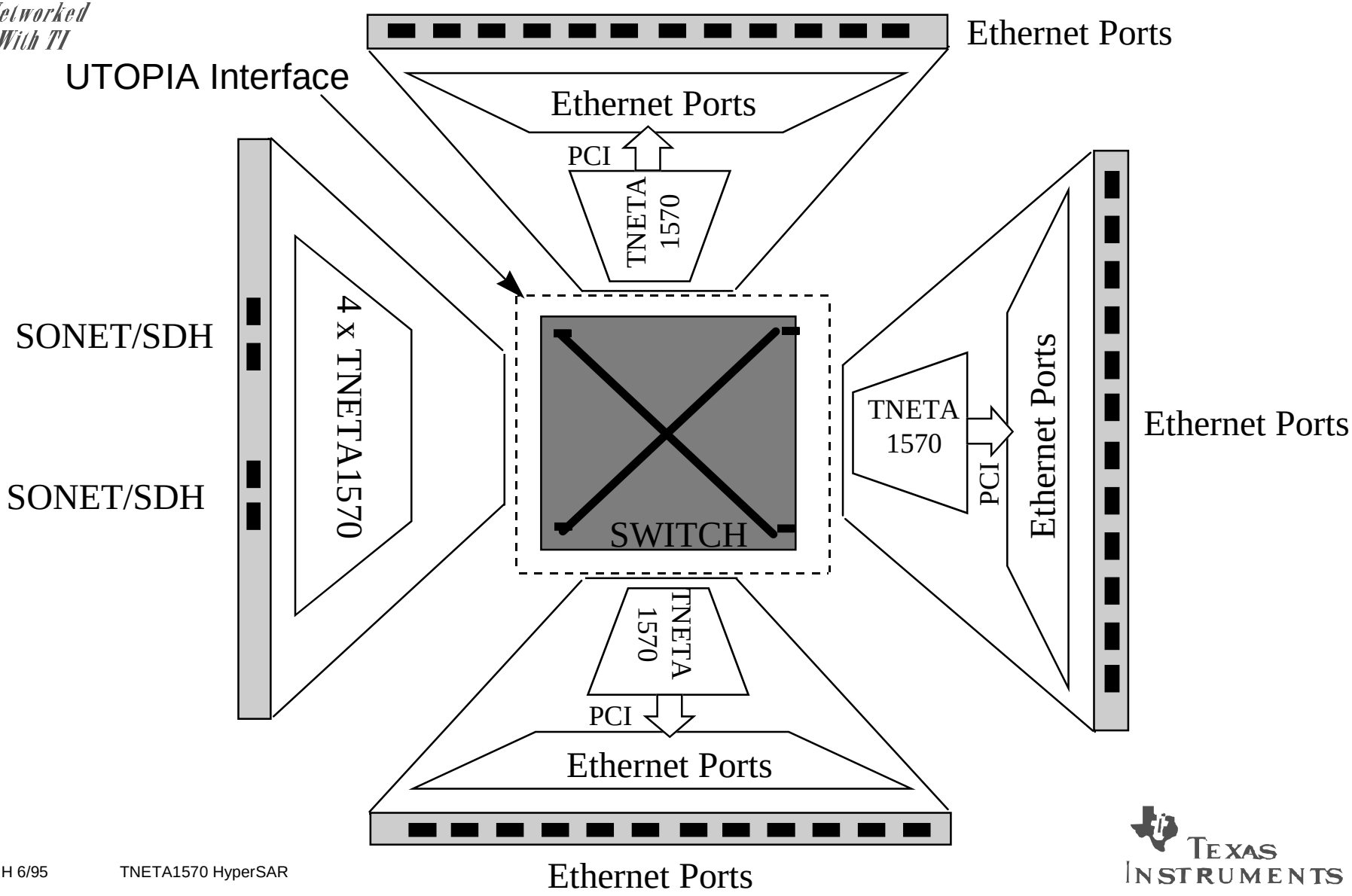


ATM/PHY UTOPIA Interface Definition

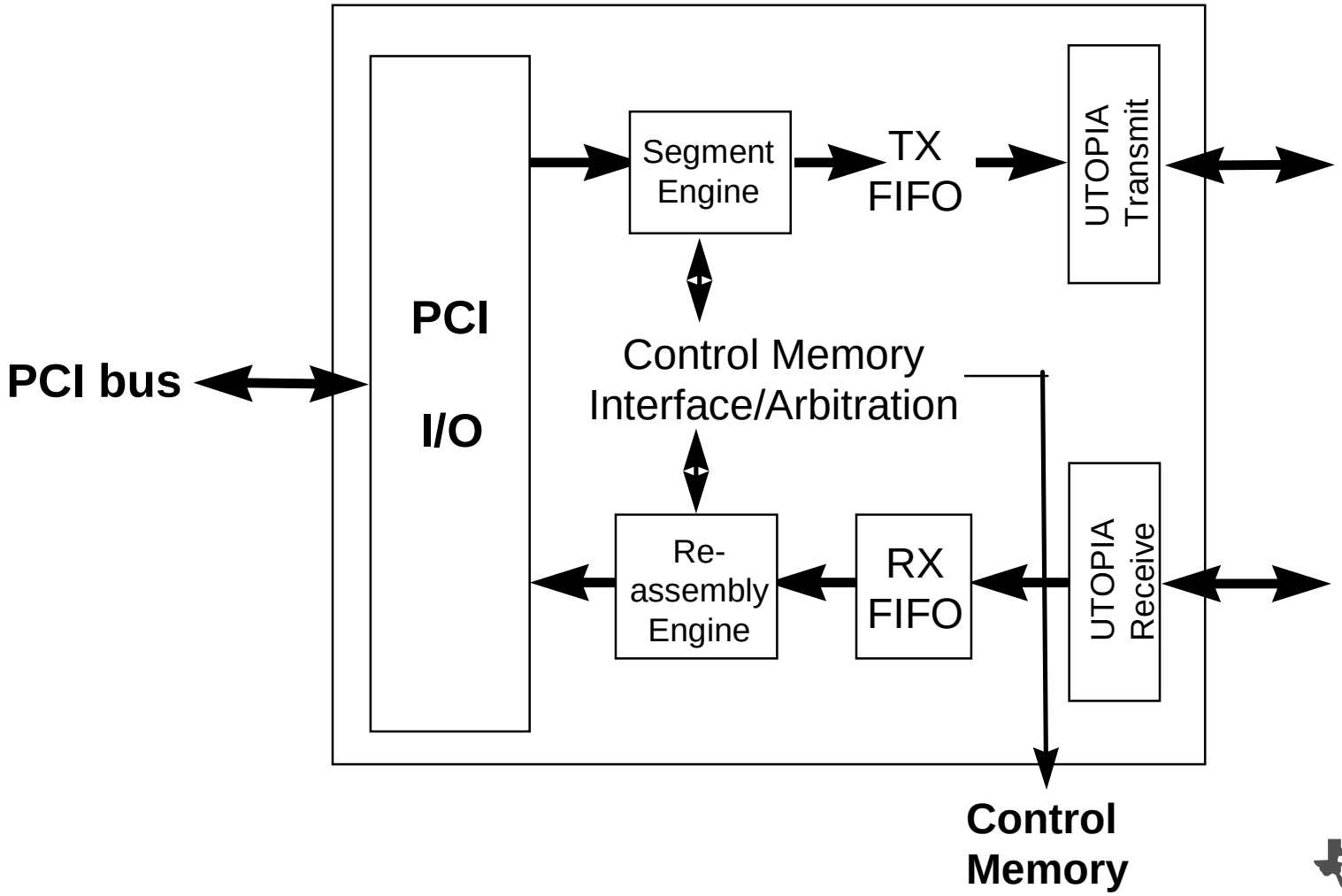
- **Single pin to select between ATM/PHY modes.**



Interfacing to Local Switching Fabric



TNETA1570 Simplified Block Diagram



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TNETA1570 HyperSAR Block Diagram

FEATURE	BENEFIT
• Independent transmit and receive channels	• Provides full duplex operation and reduces internal thrashing of device
• Segmentation based on buffers, not packets: – Allows early segmentation (cut-through capability)	• Reduces latency (programmable buffer size 1 byte - 64 Kbytes)
• Control memory only used to store DMA state information	• Improves performance by reducing accesses across PCI bus
• Cells transferred directly from internal FIFOs to host memory and vice versa	• Improves performance by passing data directly to host

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TNETA1570 Tools

- **32-/64-bit PCI evaluation module**
  - **Uses TNETA1570 and TNETA1500 SONET devices**
  - **Capability to exercise high-priority segmentation scheme**
- **Windows-based software utility**
  - **Transmits and receive ATM data**
  - **Monitors incoming traffic**
  - **Tries different configurations**
  - **Tests error and alarm conditions**
- **Software drivers (third-party software)**
  - **Provides turnkey solution of internetworking applications**
  - **Can work with any CPU**
  - **Improves time-to-market**
- **Application note (1570/1500 interface)**

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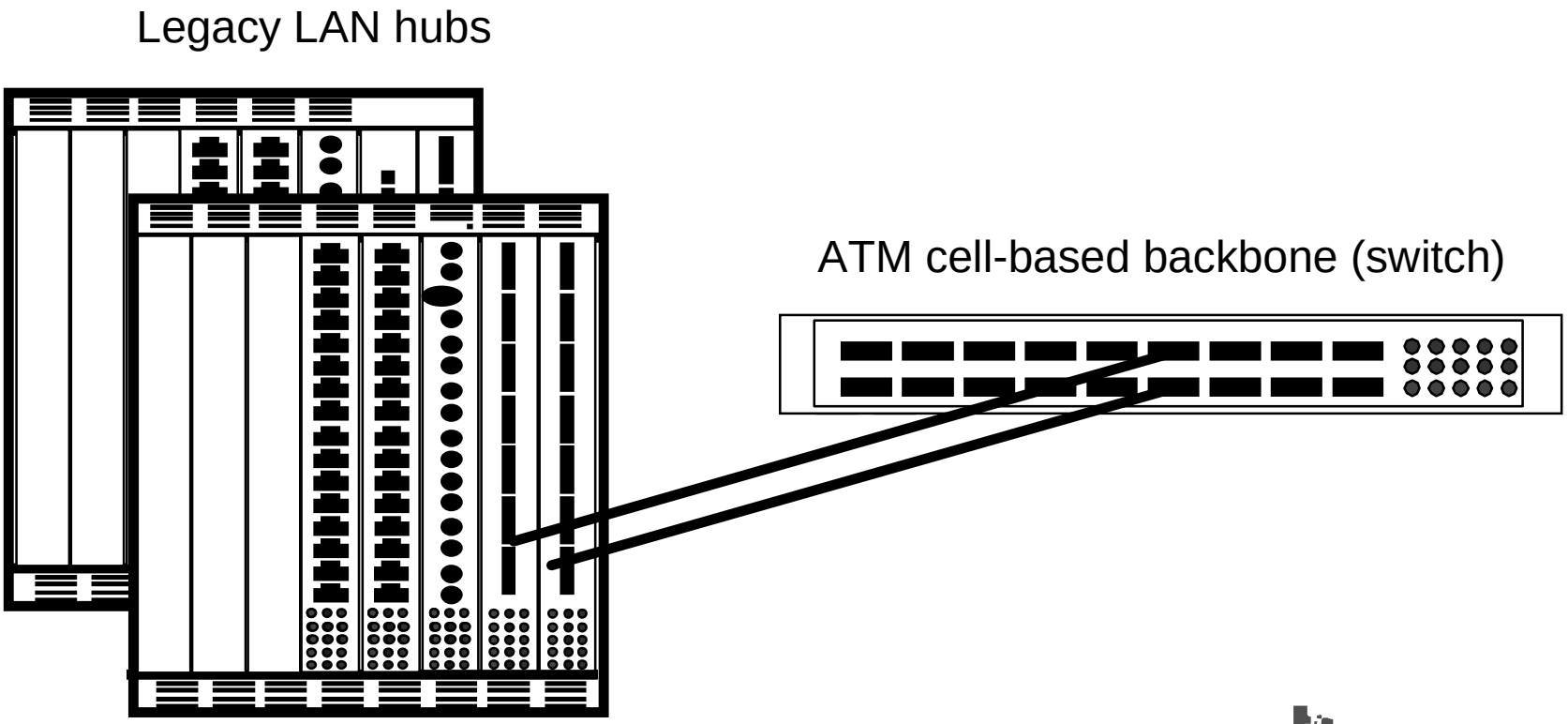
Applications

ATM Backbone

To connect to backbone switch, each HUB requires an ATM interface card.



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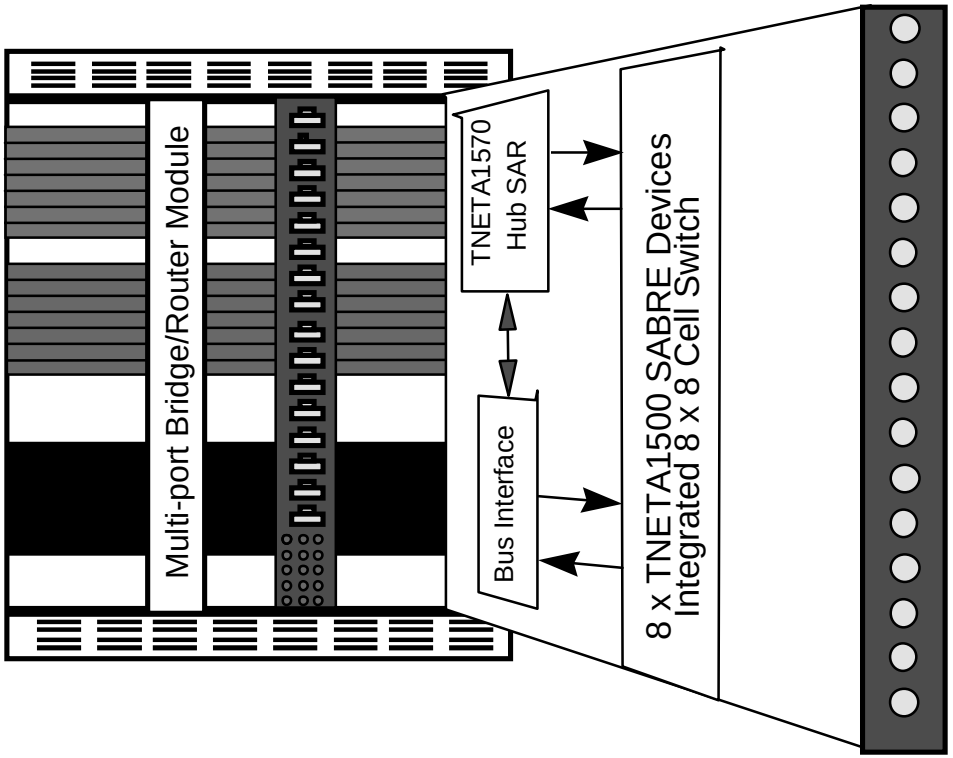
Enterprise Hub
With Legacy LAN-based Backplane

- **Legacy LAN hub with ATM interface card**
- **Allows connection to backbone switch**
- **Provides interfaces for high-performance users**



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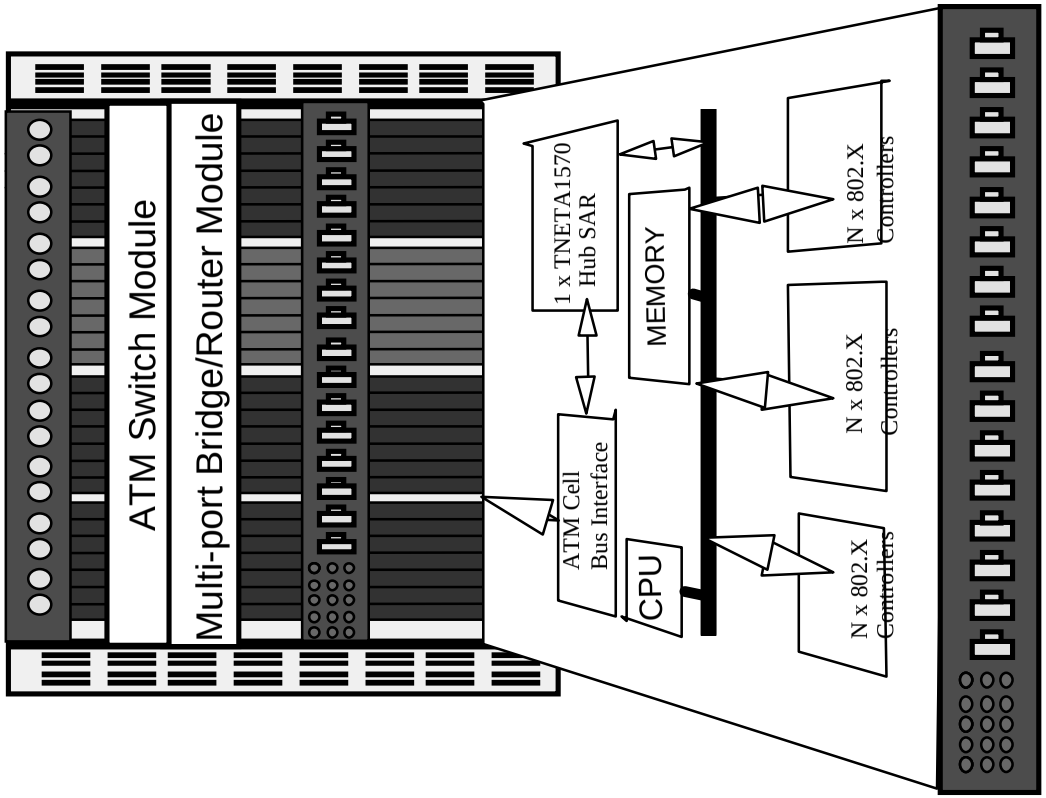
ATM Cell-based Backplane

- More ATM backplanes are added.
- LAN backplanes move directly to interface cards.
- Hub can support switched virtual networks.



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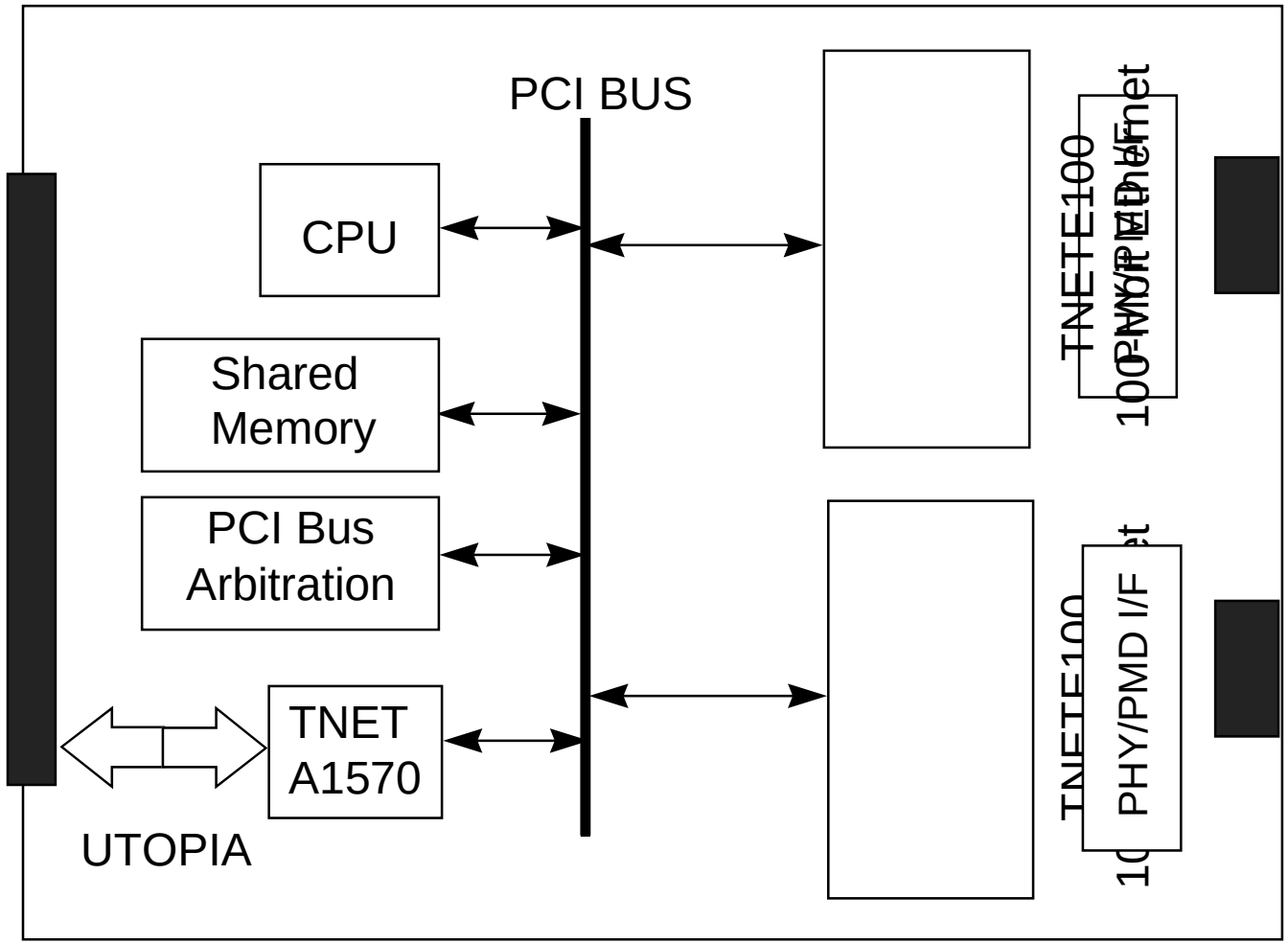
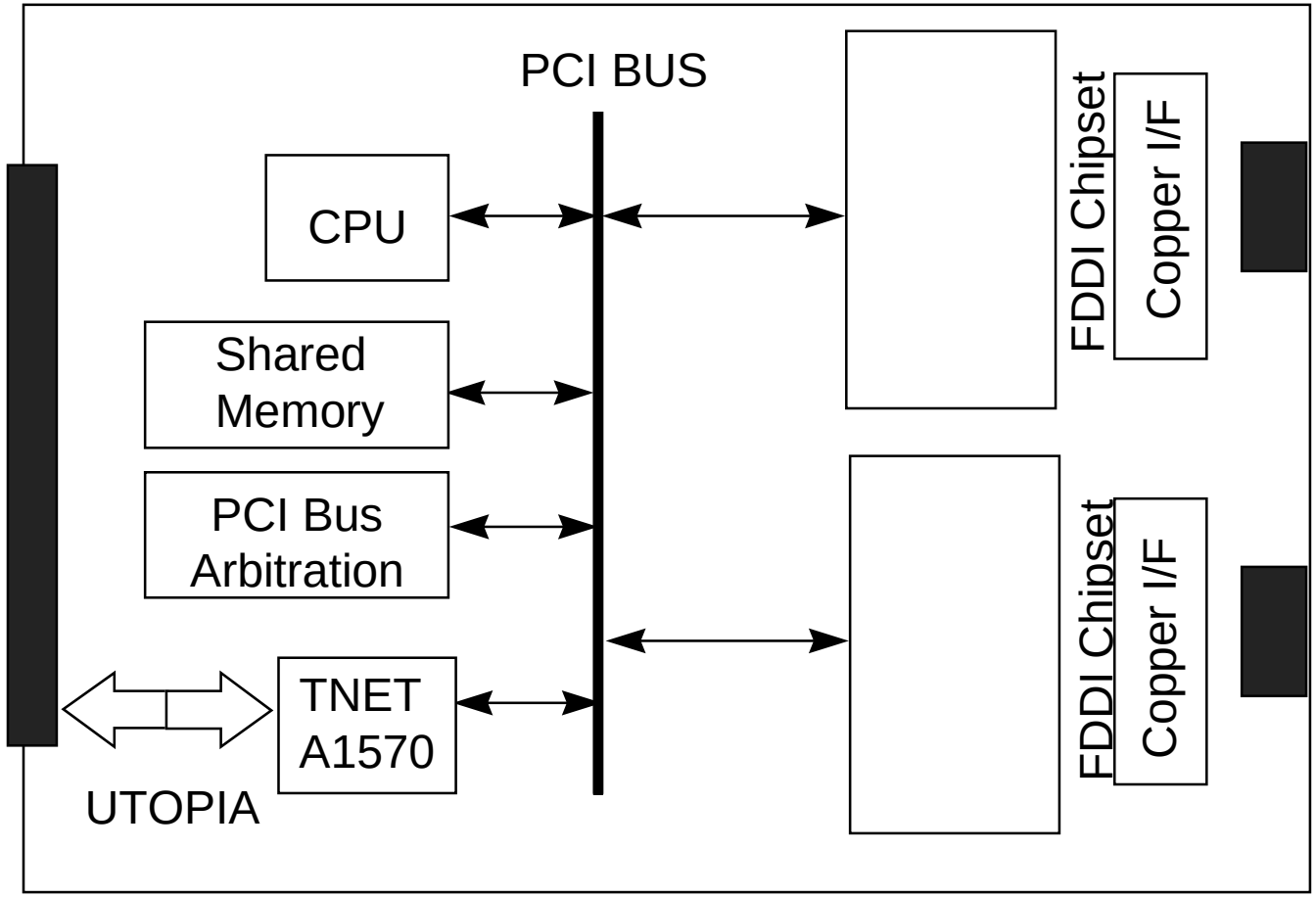
100Mbit/s Ethernet Interface Card



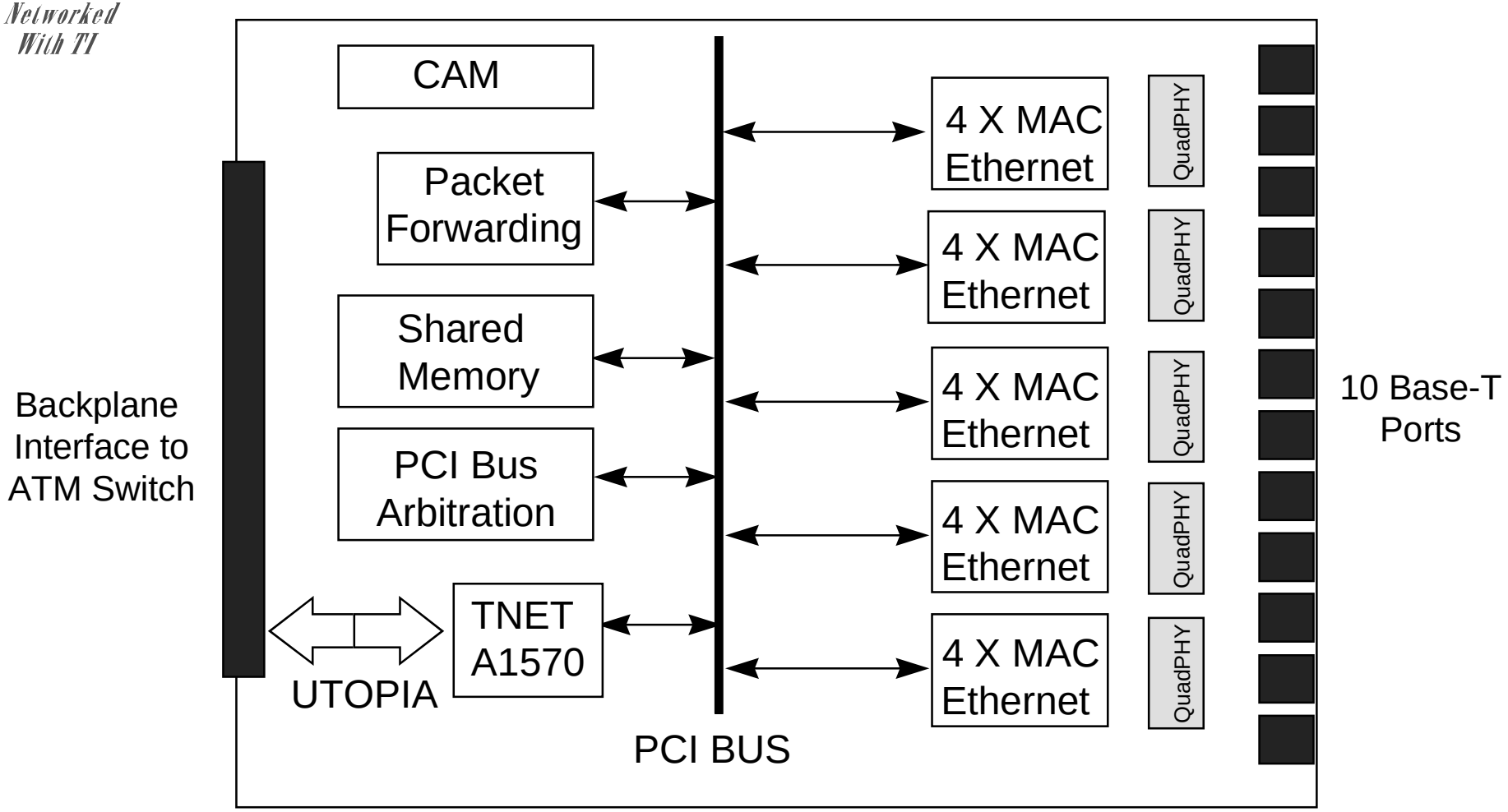
Backplane Interface to ATM Switch

FDDI Interface Card

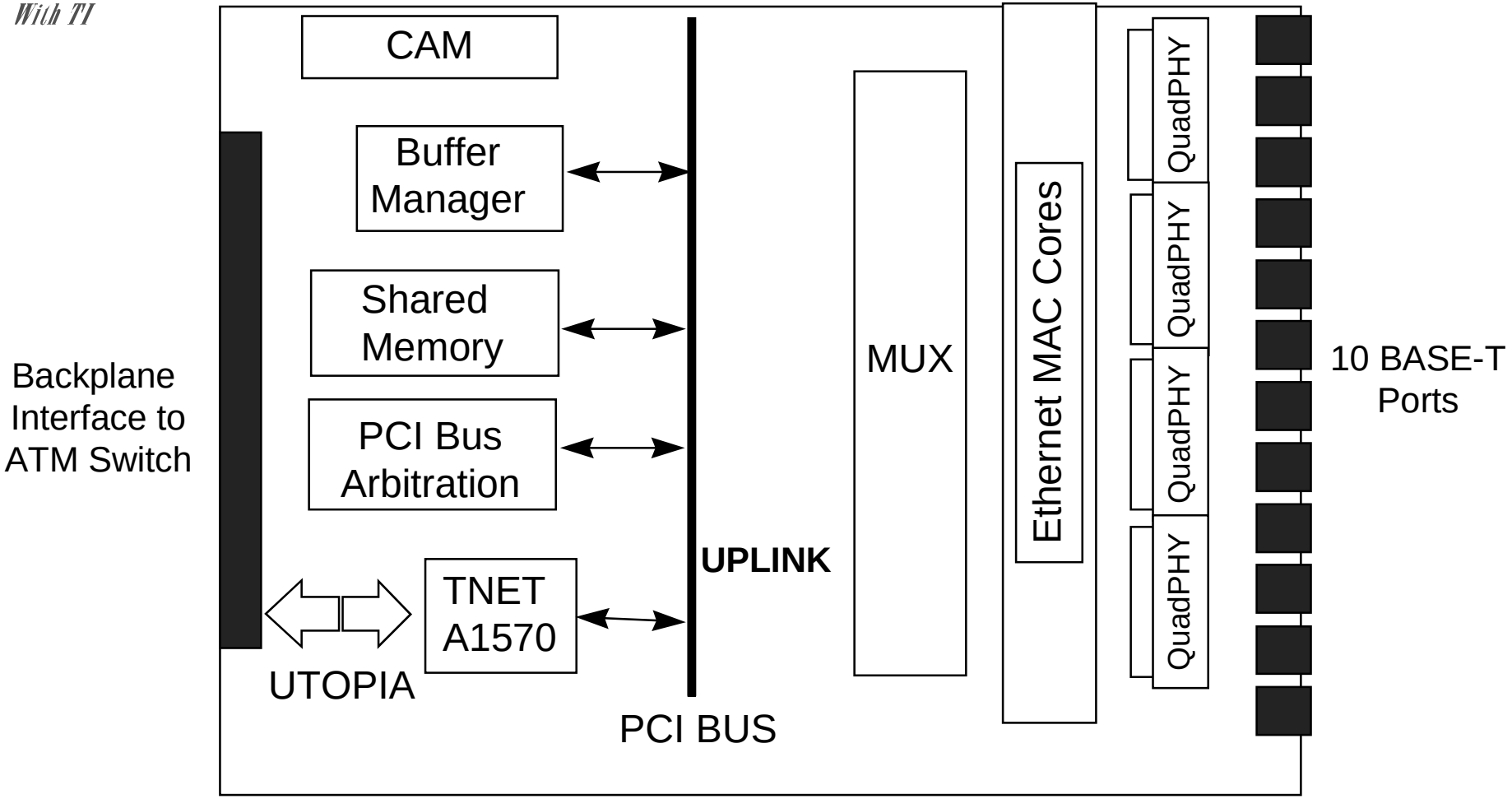


Backplane Interface to ATM Switch

Switched/Dedicated Ethernet



Switched/Dedicated Ethernet



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Summary

- **HyperSAR provides the highest performance solution for legacy LAN to ATM translation**
- **Samples available now**
- **Evaluation board and software available now**
- **S/W drivers for embedded systems also available (via third party) to reduce time-to-market**
- **Future proof (will provide upgrade to support ABR flow control)**