

Contents of MSP430F41x2 Code Examples (slac288.zip) - asm (CCS), .s43 (IAR), and .c (CCS & IAR)

Link to zip file: <http://www.ti.com/lit/zip/slac288>

Applicable Devices: MSP430F4132, MSP430F4152

Consult readme.txt included in the zip file for disclaimer and coding style guidelines

Contents:

- [Assembly Code Examples \(.asm, CCS compatible\)](#)
- [Assembly Code Examples \(.s43, IAR compatible\)](#)
- [C Code Examples \(.c, IAR & CCS compatible\)](#)

| .asm code examples – CCS | |
|---------------------------------|---|
| File name | Description |
| msp430x41x2_1.asm | Toggle P5.1 in software |
| msp430x41x2_1_vlo.asm | Software Toggle P5.1, MCLK = VLO/8 |
| msp430x41x2_lpm3_vlo.asm | Basic Clock, LPM3 Using WDT ISR, VLO ACLK |
| msp430x41x2_clks.asm | FLL+, Output 32kHz XTAL + Internal DCO |
| msp430x41x2_fll_01.asm | FLL+, Runs Internal DCO at 2.5MHz |
| msp430x41x2_fll_02.asm | FLL+, Runs Internal DCO at 8MHz |
| msp430x41x2_LFxtal_nmi.asm | LFXT1 Oscillator Fault Detection |
| msp430x41x2_P1_01.asm | Software Poll P1.4, Set P5.1 if P1.4 = 1 |
| msp430x41x2_P1_02.asm | Software Port Interrupt on P1.4 from LPM4 |
| msp430x41x2_bt_01.asm | Basic Timer, Toggle P5.1 Inside ISR, DCO SMCLK |
| msp430x41x2_bt_02.asm | Basic Timer, Toggle P5.1 Inside ISR, 32kHz ACLK |
| msp430x41x2_wdt_01.asm | WDT, Toggle P5.1, Interval Overflow ISR, DCO SMCLK |
| msp430x41x2_wdt_02.asm | WDT, Toggle P5.1, Interval Overflow ISR, 32kHz ACLK |
| msp430x41x2_wdt_04.asm | WDT+ Failsafe Clock, DCO SMCLK |
| msp430x41x2_wdt_06.asm | WDT+ Failsafe Clock, 32kHz ACLK |
| msp430x41x2_ta_01.asm | Timer_A, Toggle P5.1, CCR0 Cont. Mode ISR, DCO SMCLK |
| msp430x41x2_ta_02.asm | Timer_A, Toggle P5.1, CCR0 Up Mode ISR, DCO SMCLK |
| msp430x41x2_ta_03.asm | Timer_A, Toggle P5.1, Overflow ISR, DCO SMCLK |
| msp430x41x2_ta_04.asm | Timer_A, Toggle P5.1, Overflow ISR, 32kHz ACLK |
| msp430x41x2_ta_05.asm | Timer_A, Toggle P5.1, CCR0 Up Mode ISR, 32kHz ACLK |
| msp430x41x2_ta_16.asm | Timer_A, Timer_A, PWM TA1-2 Up Mode, DCO SMCLK |
| msp430x41x2_ta_17.asm | Timer_A, PWM TA1-2, Up Mode, 32kHz ACLK |
| msp430x41x2_svs_01.asm | SVS, POR @ 2.5V Vcc |
| msp430x41x2_svs_03.asm | SVS, Toggle port 5.1 on Vcc < 2.8V |
| msp430x41x2_compA_01.asm | Comparator A, Poll input CA0, result in P5.1 |
| msp430x41x2_compA_02.asm | Comparator A, Poll input CA0, CA exchange, result in P5.1 |
| msp430x41x2_compA_04.asm | Comparator A, Poll input CA0, result in P5.1 |
| msp430x41x2_compA_05.asm | Comparator A, Poll input CA0, interrupt triggered |
| msp430x41x2_adc10_01.asm | ADC10, Sample A0, AVcc Ref, Set P1.0 if A0 > 0.5*AVcc |
| msp430x41x2_adc10_02.asm | ADC10, Sample A0, 1.5V Ref, Set P1.0 if A0 > 0.2V |
| msp430x41x2_adc10_03.asm | ADC10, Sample A10 Temp, Set P1.0 if Temp ++ ~2C |
| msp430x41x2_adc10_04.asm | ADC10, Sample A0, Signed, Set P1.0 if A0 > 0.5*AVcc |

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| msp430x41x2_adc10_05.asm | ADC10, Sample A11, Lo_Batt, Set P1.0 if AVcc < 2.3V |
| msp430x41x2_adc10_06.asm | ADC10, Output Internal Vref on P2.4 & ADCCLK on P1.0 |
| msp430x41x2_adc10_07.asm | ADC10, DTC Sample A0 64x, AVcc, Repeat Single, DCO |
| msp430x41x2_adc10_08.asm | ADC10, DTC Sample A0 64x, 1.5V, Repeat Single, DCO |
| msp430x41x2_adc10_09.asm | ADC10, DTC Sample A10 64x, 1.5V, Repeat Single, DCO |
| msp430x41x2_adc10_10.asm | ADC10, DTC Sample A2-0, AVcc, Single Sequence, DCO |
| msp430x41x2_adc10_11.asm | ADC10, Sample A0, 1.5V, TA1 Trig, Set P1.0 if > 0.5V |
| msp430x41x2_adc10_12.asm | ADC10, Sample A7, 1.5V, TA1 Trig, Ultra-Low Pwr |
| msp430x41x2_adc10_13.asm | ADC10, DTC Sample A1 32x, AVcc, TA0 Trig, DCO |
| msp430x41x2_adc10_14.asm | ADC10, DTC Sample A1-0 32x, AVcc, Repeat Seq, DCO |
| msp430x41x2_adc10_15.asm | ADC10, DTC Sample A10 32x to Flash, Int Ref, DCO |
| msp430x41x2_adc10_16.asm | ADC10, DTC Sample A0 -> TA1, AVcc, DCO |
| msp430x41x2_adc10_21.asm | ADC10, Sample A10 Temp and Convert to oC and oF |
| msp430x41x2_uscia0_irda_01.asm | USCI_A0 IrDA External Loopback Test, 4MHz SMCLK |
| msp430x41x2_uscia0_spi_09.asm | USCI_A0, SPI 3-Wire Master Incremented Data |
| msp430x41x2_uscia0_spi_10.asm | USCI_A0, SPI 3-Wire Slave Data Echo |
| msp430x41x2_uscia0_uart_115k_lpm.asm | USCI_A0, 115200 UART Echo ISR, DCO SMCLK, LPM3 |
| msp430x41x2_uscia0_uart_115k.asm | USCI_A0, 115200 UART Echo ISR, DCO SMCLK |
| msp430x41x2_uscia0_uart_9600.asm | USCI_A0, Ultra-Low Pwr UART 9600 Echo ISR, 32kHz ACLK |
| msp430x41x2_uscia0_uart_9600_02.asm | Ultra-Low Pwr UART 9600 String, 32kHz ACLK |
| msp430x41x2_uscia0_uart_2400.asm | USCI_A0, Ultra-Low Pwr UART 2400 Echo ISR, 32kHz ACLK |
| msp430x41x2_uscib0_i2c_04.asm | Master RX single bytes from MSP430 Slave |
| msp430x41x2_uscib0_i2c_05.asm | Slave TX single bytes to MSP430 Master |
| msp430x41x2_uscib0_i2c_06.asm | Master TX single bytes to MSP430 Slave |
| msp430x41x2_uscib0_i2c_07.asm | Slave RX single bytes from MSP430 Master |
| msp430x41x2_uscib0_i2c_08.asm | USCI_B0 I2C Master TX multiple bytes to MSP430 Slave |
| msp430x41x2_uscib0_i2c_09.asm | USCI_B0 I2C Slave RX multiple bytes from MSP430 Master |
| msp430x41x2_uscib0_i2c_10.asm | USCI_B0 I2C Master RX multiple bytes from MSP430 Slave |
| msp430x41x2_uscib0_i2c_11.asm | USCI_B0 I2C Slave TX multiple bytes to MSP430 Master |
| msp430x41x2_uscib0_spi_09.asm | USCI_B0, SPI 3-Wire Master Incremented Data |
| msp430x41x2_uscib0_spi_10.asm | USCI_B0, SPI 3-Wire Slave Data Echo |
| msp430x41x2_flashwrite_01.asm | Flash In-System Programming, Copy SegC to SegD |

.s43 code examples – IAR

| File name | Description |
|----------------------------|---|
| msp430x41x2_1.s43 | Toggle P5.1 in software |
| msp430x41x2_1_vlo.s43 | Software Toggle P5.1, MCLK = VLO/8 |
| msp430x41x2_lpm3_vlo.s43 | Basic Clock, LPM3 Using WDT ISR, VLO ACLK |
| msp430x41x2_clks.s43 | FLL+, Output 32kHz XTAL + Internal DCO |
| msp430x41x2_fll_01.s43 | FLL+, Runs Internal DCO at 2.5MHz |
| msp430x41x2_fll_02.s43 | FLL+, Runs Internal DCO at 8MHz |
| msp430x41x2_LFxtal_nmi.s43 | LFXT1 Oscillator Fault Detection |
| msp430x41x2_P1_01.s43 | Software Poll P1.4, Set P5.1 if P1.4 = 1 |

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|--------------------------------------|---|
| msp430x41x2_P1_02.s43 | Software Port Interrupt on P1.4 from LPM4 |
| msp430x41x2_bt_01.s43 | Basic Timer, Toggle P5.1 Inside ISR, DCO SMCLK |
| msp430x41x2_bt_02.s43 | Basic Timer, Toggle P5.1 Inside ISR, 32kHz ACLK |
| msp430x41x2_wdt_01.s43 | WDT, Toggle P5.1, Interval Overflow ISR, DCO SMCLK |
| msp430x41x2_wdt_02.s43 | WDT, Toggle P5.1, Interval Overflow ISR, 32kHz ACLK |
| msp430x41x2_wdt_04.s43 | WDT+ Failsafe Clock, DCO SMCLK |
| msp430x41x2_wdt_06.s43 | WDT+ Failsafe Clock, 32kHz ACLK |
| msp430x41x2_ta_01.s43 | Timer_A, Toggle P5.1, CCR0 Cont. Mode ISR, DCO SMCLK |
| msp430x41x2_ta_02.s43 | Timer_A, Toggle P5.1, CCR0 Up Mode ISR, DCO SMCLK |
| msp430x41x2_ta_03.s43 | Timer_A, Toggle P5.1, Overflow ISR, DCO SMCLK |
| msp430x41x2_ta_04.s43 | Timer_A, Toggle P5.1, Overflow ISR, 32kHz ACLK |
| msp430x41x2_ta_05.s43 | Timer_A, Toggle P5.1, CCR0 Up Mode ISR, 32kHz ACLK |
| msp430x41x2_ta_16.s43 | Timer_A, Timer_A, PWM TA1-2 Up Mode, DCO SMCLK |
| msp430x41x2_ta_17.s43 | Timer_A, PWM TA1-2, Up Mode, 32kHz ACLK |
| msp430x41x2_svs_01.s43 | SVS, POR @ 2.5V Vcc |
| msp430x41x2_svs_03.s43 | SVS, Toggle port 5.1 on Vcc < 2.8V |
| msp430x41x2_compA_01.s43 | Comparator A, Poll input CA0, result in P5.1 |
| msp430x41x2_compA_02.s43 | Comparator A, Poll input CA0, CA exchange, result in P5.1 |
| msp430x41x2_compA_04.s43 | Comparator A, Poll input CA0, result in P5.1 |
| msp430x41x2_compA_05.s43 | Comparator A, Poll input CA0, interrupt triggered |
| msp430x41x2_adc10_01.s43 | ADC10, Sample A0, AVcc Ref, Set P1.0 if A0 > 0.5*AVcc |
| msp430x41x2_adc10_02.s43 | ADC10, Sample A0, 1.5V Ref, Set P1.0 if A0 > 0.2V |
| msp430x41x2_adc10_03.s43 | ADC10, Sample A10 Temp, Set P1.0 if Temp ++ ~2C |
| msp430x41x2_adc10_04.s43 | ADC10, Sample A0, Signed, Set P1.0 if A0 > 0.5*AVcc |
| msp430x41x2_adc10_05.s43 | ADC10, Sample A11, Lo_Batt, Set P1.0 if AVcc < 2.3V |
| msp430x41x2_adc10_06.s43 | ADC10, Output Internal Vref on P2.4 & ADCCLK on P1.0 |
| msp430x41x2_adc10_07.s43 | ADC10, DTC Sample A0 64x, AVcc, Repeat Single, DCO |
| msp430x41x2_adc10_08.s43 | ADC10, DTC Sample A0 64x, 1.5V, Repeat Single, DCO |
| msp430x41x2_adc10_09.s43 | ADC10, DTC Sample A10 64x, 1.5V, Repeat Single, DCO |
| msp430x41x2_adc10_10.s43 | ADC10, DTC Sample A2-0, AVcc, Single Sequence, DCO |
| msp430x41x2_adc10_11.s43 | ADC10, Sample A0, 1.5V, TA1 Trig, Set P1.0 if > 0.5V |
| msp430x41x2_adc10_12.s43 | ADC10, Sample A7, 1.5V, TA1 Trig, Ultra-Low Pwr |
| msp430x41x2_adc10_13.s43 | ADC10, DTC Sample A1 32x, AVcc, TA0 Trig, DCO |
| msp430x41x2_adc10_14.s43 | ADC10, DTC Sample A1-0 32x, AVcc, Repeat Seq, DCO |
| msp430x41x2_adc10_15.s43 | ADC10, DTC Sample A10 32x to Flash, Int Ref, DCO |
| msp430x41x2_adc10_16.s43 | ADC10, DTC Sample A0 -> TA1, AVcc, DCO |
| msp430x41x2_adc10_21.s43 | ADC10, Sample A10 Temp and Convert to oC and oF |
| msp430x41x2_uscia0_irda_01.s43 | USCI_A0 IrDA External Loopback Test, 4MHz SMCLK |
| msp430x41x2_uscia0_spi_09.s43 | USCI_A0, SPI 3-Wire Master Incremented Data |
| msp430x41x2_uscia0_spi_10.s43 | USCI_A0, SPI 3-Wire Slave Data Echo |
| msp430x41x2_uscia0_uart_115k_lpm.s43 | USCI_A0, 115200 UART Echo ISR, DCO SMCLK, LPM3 |
| msp430x41x2_uscia0_uart_115k.s43 | USCI_A0, 115200 UART Echo ISR, DCO SMCLK |
| msp430x41x2_uscia0_uart_9600.s43 | USCI_A0, Ultra-Low Pwr UART 9600 Echo ISR, 32kHz ACLK |
| msp430x41x2_uscia0_uart_9600_02.s43 | Ultra-Low Pwr UART 9600 String, 32kHz ACLK |
| msp430x41x2_uscia0_uart_2400.s43 | USCI_A0, Ultra-Low Pwr UART 2400 Echo ISR, 32kHz ACLK |

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| mmsp430x41x2_uscib0_i2c_04.s43 | Master RX single bytes from MSP430 Slave |
| mmsp430x41x2_uscib0_i2c_05.s43 | Slave TX single bytes to MSP430 Master |
| mmsp430x41x2_uscib0_i2c_06.s43 | Master TX single bytes to MSP430 Slave |
| mmsp430x41x2_uscib0_i2c_07.s43 | Slave RX single bytes from MSP430 Master |
| mmsp430x41x2_uscib0_i2c_08.s43 | USCI_B0 I2C Master TX multiple bytes to MSP430 Slave |
| mmsp430x41x2_uscib0_i2c_09.s43 | USCI_B0 I2C Slave RX multiple bytes from MSP430 Master |
| mmsp430x41x2_uscib0_i2c_10.s43 | USCI_B0 I2C Master RX multiple bytes from MSP430 Slave |
| mmsp430x41x2_uscib0_i2c_11.s43 | USCI_B0 I2C Slave TX multiple bytes to MSP430 Master |
| mmsp430x41x2_uscib0_spi_09.s43 | USCI_B0, SPI 3-Wire Master Incremented Data |
| mmsp430x41x2_uscib0_spi_10.s43 | USCI_B0, SPI 3-Wire Slave Data Echo |
| mmsp430x41x2_flashwrite_01.s43 | Flash In-System Programming, Copy SegC to SegD |

| C code examples – IAR & CCS | |
|-----------------------------|---|
| File name | Description |
| mmsp430x41x2_1.c | Toggle P5.1 in software |
| mmsp430x41x2_1_vlo.c | Software Toggle P5.1, MCLK = VLO/8 |
| mmsp430x41x2_lpm3_vlo.c | Basic Clock, LPM3 Using WDT ISR, VLO ACLK |
| mmsp430x41x2_clks.c | FLL+, Output 32kHz XTAL + Internal DCO |
| mmsp430x41x2_fll_01.c | FLL+, Runs Internal DCO at 2.5MHz |
| mmsp430x41x2_fll_02.c | FLL+, Runs Internal DCO at 8MHz |
| mmsp430x41x2_LFxtal_nmi.c | LFXT1 Oscillator Fault Detection |
| mmsp430x41x2_P1_01.c | Software Poll P1.4, Set P5.1 if P1.4 = 1 |
| mmsp430x41x2_P1_02.c | Software Port Interrupt on P1.4 from LPM4 |
| mmsp430x41x2_bt_01.c | Basic Timer, Toggle P5.1 Inside ISR, DCO SMCLK |
| mmsp430x41x2_bt_02.c | Basic Timer, Toggle P5.1 Inside ISR, 32kHz ACLK |
| mmsp430x41x2_wdt_01.c | WDT, Toggle P5.1, Interval Overflow ISR, DCO SMCLK |
| mmsp430x41x2_wdt_02.c | WDT, Toggle P5.1, Interval Overflow ISR, 32kHz ACLK |
| mmsp430x41x2_wdt_04.c | WDT+ Failsafe Clock, DCO SMCLK |
| mmsp430x41x2_wdt_06.c | WDT+ Failsafe Clock, 32kHz ACLK |
| mmsp430x41x2_ta_01.c | Timer_A, Toggle P5.1, CCR0 Cont. Mode ISR, DCO SMCLK |
| mmsp430x41x2_ta_02.c | Timer_A, Toggle P5.1, CCR0 Up Mode ISR, DCO SMCLK |
| mmsp430x41x2_ta_03.c | Timer_A, Toggle P5.1, Overflow ISR, DCO SMCLK |
| mmsp430x41x2_ta_04.c | Timer_A, Toggle P5.1, Overflow ISR, 32kHz ACLK |
| mmsp430x41x2_ta_05.c | Timer_A, Toggle P5.1, CCR0 Up Mode ISR, 32kHz ACLK |
| mmsp430x41x2_ta_16.c | Timer_A, Timer_A, PWM TA1-2 Up Mode, DCO SMCLK |
| mmsp430x41x2_ta_17.c | Timer_A, PWM TA1-2, Up Mode, 32kHz ACLK |
| mmsp430x41x2_svs_01.c | SVS, POR @ 2.5V Vcc |
| mmsp430x41x2_svs_03.c | SVS, Toggle port 5.1 on Vcc < 2.8V |
| mmsp430x41x2_compA_01.c | Comparator A, Poll input CA0, result in P5.1 |
| mmsp430x41x2_compA_02.c | Comparator A, Poll input CA0, CA exchange, result in P5.1 |
| mmsp430x41x2_compA_04.c | Comparator A, Poll input CA0, result in P5.1 |
| mmsp430x41x2_compA_05.c | Comparator A, Poll input CA0, interrupt triggered |
| mmsp430x41x2_adc10_01.c | ADC10, Sample A0, AVcc Ref, Set P1.0 if A0 > 0.5*AVcc |

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|------------------------------------|--|
| msp430x41x2_adc10_02.c | ADC10, Sample A0, 1.5V Ref, Set P1.0 if A0 > 0.2V |
| msp430x41x2_adc10_03.c | ADC10, Sample A10 Temp, Set P1.0 if Temp ++ ~2C |
| msp430x41x2_adc10_04.c | ADC10, Sample A0, Signed, Set P1.0 if A0 > 0.5*AVcc |
| msp430x41x2_adc10_05.c | ADC10, Sample A11, Lo_Batt, Set P1.0 if AVcc < 2.3V |
| msp430x41x2_adc10_06.c | ADC10, Output Internal Vref on P2.4 & ADCCLK on P1.0 |
| msp430x41x2_adc10_07.c | ADC10, DTC Sample A0 64x, AVcc, Repeat Single, DCO |
| msp430x41x2_adc10_08.c | ADC10, DTC Sample A0 64x, 1.5V, Repeat Single, DCO |
| msp430x41x2_adc10_09.c | ADC10, DTC Sample A10 64x, 1.5V, Repeat Single, DCO |
| msp430x41x2_adc10_10.c | ADC10, DTC Sample A2-0, AVcc, Single Sequence, DCO |
| msp430x41x2_adc10_11.c | ADC10, Sample A0, 1.5V, TA1 Trig, Set P1.0 if > 0.5V |
| msp430x41x2_adc10_12.c | ADC10, Sample A7, 1.5V, TA1 Trig, Ultra-Low Pwr |
| msp430x41x2_adc10_13.c | ADC10, DTC Sample A1 32x, AVcc, TA0 Trig, DCO |
| msp430x41x2_adc10_14.c | ADC10, DTC Sample A1-0 32x, AVcc, Repeat Seq, DCO |
| msp430x41x2_adc10_15.c | ADC10, DTC Sample A10 32x to Flash, Int Ref, DCO |
| msp430x41x2_adc10_16.c | ADC10, DTC Sample A0 -> TA1, AVcc, DCO |
| msp430x41x2_adc10_21.c | ADC10, Sample A10 Temp and Convert to oC and oF |
| msp430x41x2_uscia0_irda_01.c | USCI_A0 IrDA External Loopback Test, 4MHz SMCLK |
| msp430x41x2_uscia0_spi_09.c | USCI_A0, SPI 3-Wire Master Incremented Data |
| msp430x41x2_uscia0_spi_10.c | USCI_A0, SPI 3-Wire Slave Data Echo |
| msp430x41x2_uscia0_uart_115k_lpm.c | USCI_A0, 115200 UART Echo ISR, DCO SMCLK, LPM3 |
| msp430x41x2_uscia0_uart_115k.c | USCI_A0, 115200 UART Echo ISR, DCO SMCLK |
| msp430x41x2_uscia0_uart_9600.c | USCI_A0, Ultra-Low Pwr UART 9600 Echo ISR, 32kHz ACLK |
| msp430x41x2_uscia0_uart_9600_02.c | Ultra-Low Pwr UART 9600 String, 32kHz ACLK |
| msp430x41x2_uscia0_uart_2400.c | USCI_A0, Ultra-Low Pwr UART 2400 Echo ISR, 32kHz ACLK |
| msp430x41x2_uscib0_i2c_04.c | Master RX single bytes from MSP430 Slave |
| msp430x41x2_uscib0_i2c_05.c | Slave TX single bytes to MSP430 Master |
| msp430x41x2_uscib0_i2c_06.c | Master TX single bytes to MSP430 Slave |
| msp430x41x2_uscib0_i2c_07.c | Slave RX single bytes from MSP430 Master |
| msp430x41x2_uscib0_i2c_08.c | USCI_B0 I2C Master TX multiple bytes to MSP430 Slave |
| msp430x41x2_uscib0_i2c_09.c | USCI_B0 I2C Slave RX multiple bytes from MSP430 Master |
| msp430x41x2_uscib0_i2c_10.c | USCI_B0 I2C Master RX multiple bytes from MSP430 Slave |
| msp430x41x2_uscib0_i2c_11.c | USCI_B0 I2C Slave TX multiple bytes to MSP430 Master |
| msp430x41x2_uscib0_spi_09.c | USCI_B0, SPI 3-Wire Master Incremented Data |
| msp430x41x2_uscib0_spi_10.c | USCI_B0, SPI 3-Wire Slave Data Echo |
| msp430x41x2_flashwrite_01.c | Flash In-System Programming, Copy SegC to SegD |

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