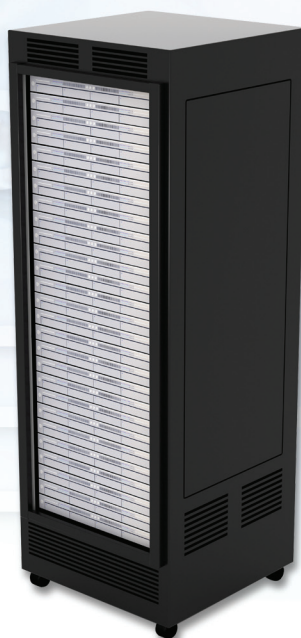


Clock & Timing Solutions

Complete, Flexible and Easy-to-Use Portfolio
for Wired Communications



Low Noise Clocks



Accelerate Time-to-Market with Easy-to-Use Clocking Solutions

Texas Instruments offers the industry's broadest selection of clock products and complete solutions, delivering unmatched jitter performance and ultimate flexibility.

Clocking solutions from TI deliver:

- Best-in-class jitter performance
- Unparalleled phase noise performance
- A comprehensive, flexible, easy-to-use portfolio

Addressing broad applications:

- Wireless, wired, and optical communications
- Networking, SOC, FPGAs, servers, and storage
- Mass market: video surveillance, industrial, test & measurement, medical, and many more

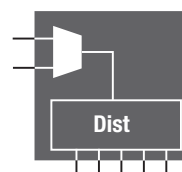
Flexible and Easy-to-Use Clocking Portfolio

Distribution:

LMK00101/5
LMK01801
LMK00301/4/6/8
CDCLVC1310

Features:

- Lowest additive jitter CLK fanout
- Programmable dividers/delays for flexibility



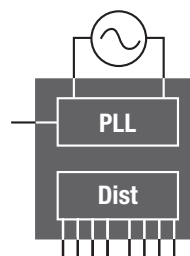
Jitter Cleaning/

Distribution:

LMK02000/2

Features:

- Low noise PLL + external VCXO cleans CLK
- Includes distribution functionality



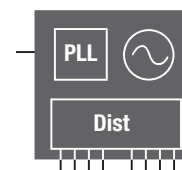
Generation/

Distribution:

LMK03806
CDCM6208

Features:

- Integrates PLL + VCO cleans and/or multiplies CLK
- Includes distribution functionality



Jitter Cleaning/

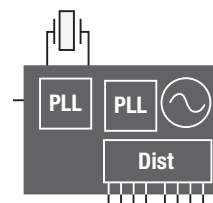
Generation/

Distribution:

LMK04800 Family
LMK04906
LMK04816

Features:

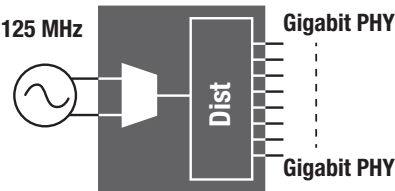
- Cascaded PLL + VCO provides low-cost jitter cleaning
- Crystal oscillator can be used for CLK generation
- Includes all functionality of LMK01801



LMK0030x – High-Performance Buffers

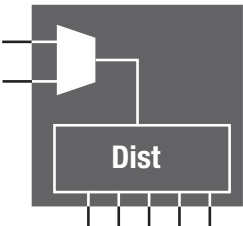
Delivers industry-leading jitter performance and reduces BOM inventory

The LMK0030x clock buffer family provides high performance, versatility, and power efficiency, making it ideal for replacing fixed-output buffer devices while increasing timing margin in the system.



Key Features and Benefits

- Two universal inputs operate up to 3.1 GHz and accept LVPECL, LVDS, CML, SSTL, HSTL, HCSL, single-ended clocks
- One crystal input accepts 10 to 40 MHz crystal or single-ended clock
- LVPECL, LVDS, HCSL, or Hi-Z (selectable per bank)
- Additive jitter with LMK03806 clock source
 - 20 fs RMS at 156.25 MHz LVPECL (10 kHz to 1 MHz)
 - 51 fs RMS at 156.25 MHz LVPECL (12 kHz to 20 MHz)
 - 65 fs RMS at 100 MHz HCSL (PCIe Gen 3 filter)
- High PSRR: –65/–76 dBc (LVPECL/LVDS) at 156.25 MHz
- LVCMOS output with synchronous enable input
- Three independent VCCO output supplies: 3.3 V/2.5 V ±5% for voltage translation



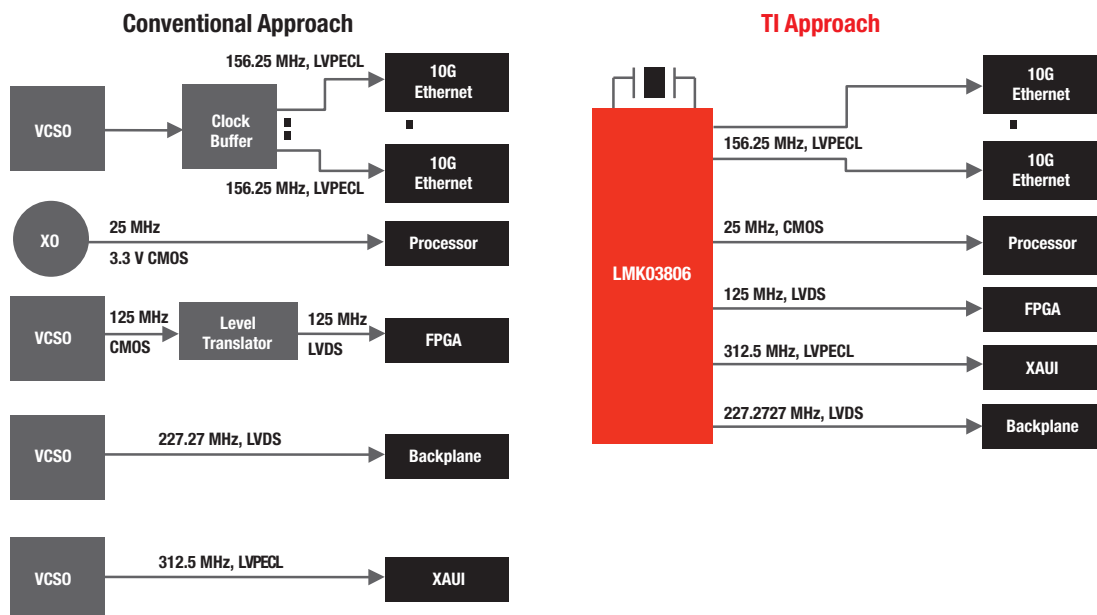
Device	Freq Range	Input Format	Number of Outputs	Output Format
LMK00304	DC~3.1 GHz	Universal (LVPECL, LVDS, CML, SSTL, HSTL, HCSL, LVCMOS/LVTTL)	4	Universal (LVPECL, LVDS, HCSL, Hi-Z)
LMK00306	DC~3.1 GHz		6	
LMK00308	DC~3.1 GHz		8	
LMK00301	DC~3.1 GHz		10	

New products are listed in **bold red**.

LMK03806 – Ultra-Low Jitter Clock Generator

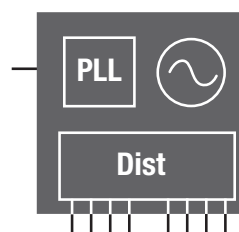
Reduces BOM cost and simplifies timing design

The LMK03806 clock generator simplifies timing architectures by replacing fixed-frequency clock generators, discrete level translators, fanout buffers, XOs, VCXOs, and VCSOs with a single low-cost crystal + LMK03806 reducing board space by up to 80% and BOM cost by up to 50% — with jitter performance unmatched in the industry.



Key Features and Benefits

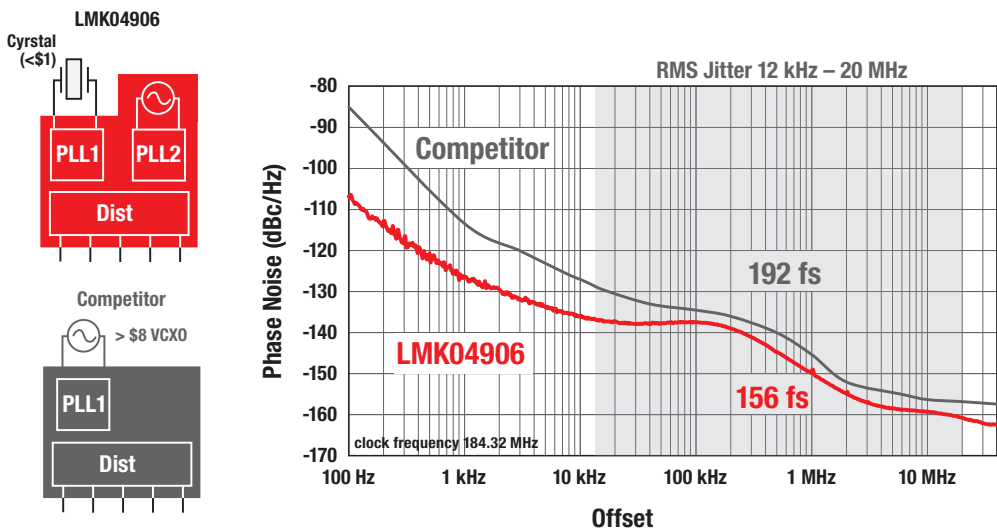
- High-frequency VCO and programmable output dividers:
Simplifies timing design by simultaneously generating a wide array of common frequencies
- Ultra-low jitter: Sub-50 fs RMS jitter at 312.5 MHz output frequency improves bit error rate and carrier-to-noise ratio performance
- Programmable LVDS, LVPECL and LVCMOS outputs: Each output clock is independently configurable, eliminating the need for level translators and fanout buffers
- Crystal interface: Allows designers to use a low-cost crystal to simultaneously generating multiple clocks



LMK04906 – Industry’s Lowest Phase Noise Clock Conditioner

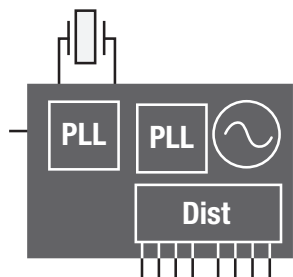
Enhances system performance and reduces clocking BOM cost

The LMK04906 clock conditioner family with dual PLL architecture enables simple and cost-effective implementation of jitter cleaning and clock generation in a single chip, eliminating the need for pricey and bulky high-performance VCXO modules.



Key Features and Benefits

- Cascaded PLL architecture and integrated crystal circuit: enables sub-200 fs performance without the need for costly high-performance VCXOs
- Integrated features — holdover, switchover, multiple inputs, digital delay, analog delay, odd/even dividers and 12 outputs with programmable output format drivers: highly flexible and configurable to support a variety of different architectures



Device	VCO Freq. (MHz)	Input Format	Number of Outputs	Output Format
LMK04906	2370 to 2600	LVPECL, LVDS, LVCMOS	6	LVCMOS, LVPECL, LVDS
LMK04803B	1840 to 2030		12	LVCMOS, LVPECL, LVDS
LMK04805B	2148 to 2370		12	
LMK04806B	2370 to 2600		12	
LMK04808B	2750 to 3072		12	
LMK04816	2370 to 2600		12	LVCMOS, LVPECL, LVDS

New products are listed in bold red. Preview products are listed in bold blue.

Design Resources and References

Clock Design Tool

1 Input

Requirements for clock architecture, frequencies, and formats

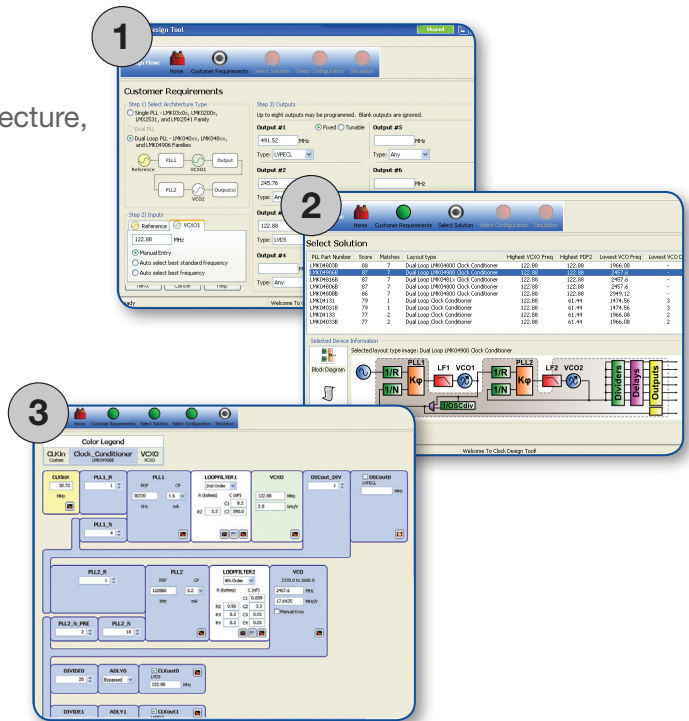
2 Select

Solution and configuration

3 Simulate

Phase noise and jitter optimize device parameters and loop filters

Start your design today at
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Get more information on TI's family of clocking products for wired communications at

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