

TI's latest high-speed ADC “winning combo” for defense radar applications

Prepared for BAE Systems

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Reliable technologies,
long-term commitment.

Key parameters: Defense radar designs

Analog to digital converter (ADCs)

- Higher sample rate → higher signal bandwidth → more range resolution ($dR \sim c/(2 \cdot BW)$)
- Highest possible SNR for bandwidth required enables higher object discrimination
- SDR of 90dBc or better (16b), 65dBc or better (12b, >1GHz signal BW)
- Multi-channel ADCs if system is designed as a phased array or active scanning element array (ASEA)

IF digital variable gain amplifier (DVGA)

- Multi-channel solutions for driving multi-channel ADCs
- Low noise with gain range to enable higher system dynamic range
- Higher linearity – greater than 35dB OIP3 at typical ADC IFs (150 – 350 MHz)

LO synthesizer (PLL/VCO)

- Low phase noise, both close in (10KHz) and far out (20MHz)
- Low spur count and energy
- Multiple outputs for driving multiple mixers on RX and TX elements

Transmit digital to analog converter (DACs)

- >70 dBc SFDR across TX bandwidth for pure chirp / pulse generation
- >500MHz of signal bandwidth
- Multi-DAC and multi-chip synchronization for element-to-element phase control

Clocking

- <100 fs additive jitter for clocking receive ADCs
- Fine analog delay adjustments to support JESD data converters
- Multiple outputs for clocking ADCs, DACs, FPGA/DRE and providing RF references from one source

Power

- High PSRR, especially at 1MHz to filter out DC/DC switching noise
- Low output noise to decrease size of spurs in sensitive RF components

ADC12J4000 family

Single, 12-bit, 4.0/2.7/1.6 GSPS JESD204B ADCs

Why were these parts developed?

The ADC12J4000 devices were developed to provide the widest bandwidth sampling capabilities with low power, high speed serialized data output rates and integrated signal processing (DDC), all of which provide design flexibility that can reduce design time and cost.

What makes these parts unique?

The ADC12J4000 is the fastest 12b ADC on the market. This device provides >3.0GHz of input bandwidth, frequency conversion, filtering, and sample rate down conversion in one device. The ADC12J4000 and speed variants utilize the JESD204B serial interface, which can output data on 1 to 8 lanes depending on the decimation and link output rate settings.

ADC12J4000/J2700/J1600 (& LM15851)

Single, 12-bit, 4.0/2.7/1.6 GSPS JESD204B ADC

Samples available

Features

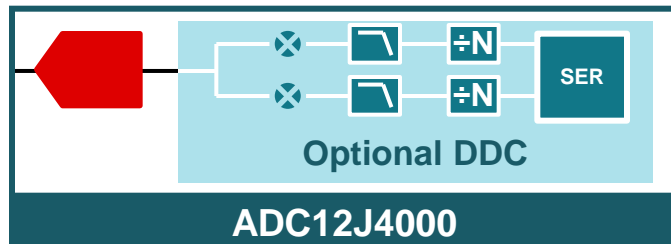
- Buffered input
- Power (1.2/1.9V supplies) at 4 GSPS
 - With DDC: 2W
 - Bypass DDC: 1.8W
- Noise floor: -149 dBFS/Hz
- IMD3 (2.1 GHz, -13dBFS ea): -64 dBc
- JESD204B (DX)
 - Supports Subclass 1
 - Up to 8 lanes at 10 Gbps (max)
- DDC (digital down-converter)
 - Complex decimation: 4/8/10/16/20/32x stop-band suppression: 80 dBc @ 80%
 - NCO frequency resolution: 32-bit
- Package: 68-pin QFN

Benefits

- Optional DDC greatly reduces output data rate, simplifying receiver requirements, reducing FPGA gates
- Excellent performance beyond 3 GHz allows RF-sampling for 3G/4G BTS and other applications, saving size, weight, and power and greatly increasing flexibility
- JESD204B interface minimizes output lanes, simplifies system, enables deterministic latency across multiple lanes and multiple chips
- Low power dissipation and small package reduce system size and complexity

Applications

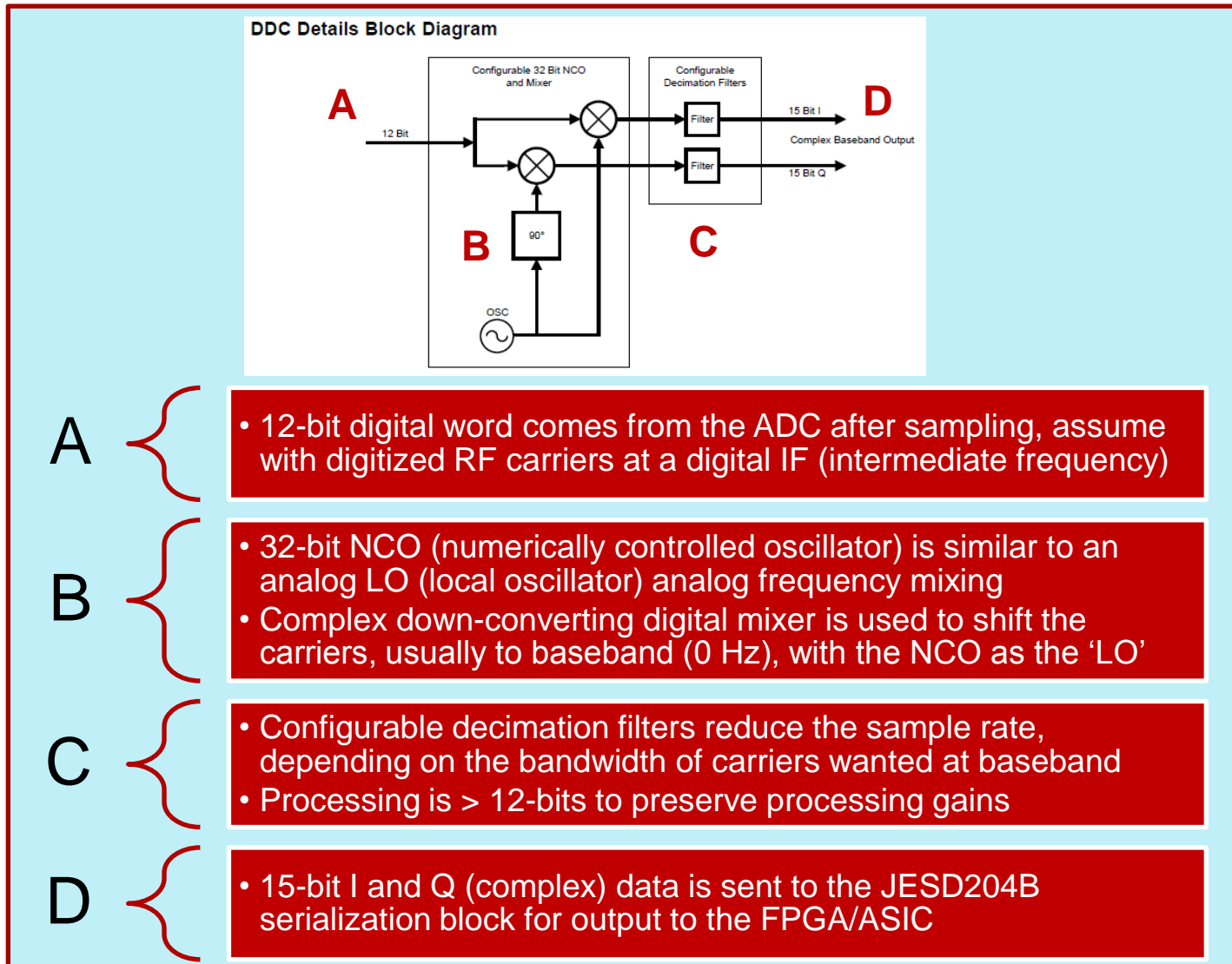
- Wideband communications, 3G/4G receive and DPD
- Military radar, communications, EW and SIGINT
- Test & measurement, data acquisition, spectrum analyzer



Part Number	Sampling Rate	Power	DDC
ADC12J4000	4GspS	2.0W	Optional
ADC12J2700	2.7GspS	1.8W	Optional
ADC12J1600	1.6GspS	1.6W	Optional
*LM15851	4GSPS	2.0W	Required

*Does not require US export license

Why the digital down converter (DDC)?

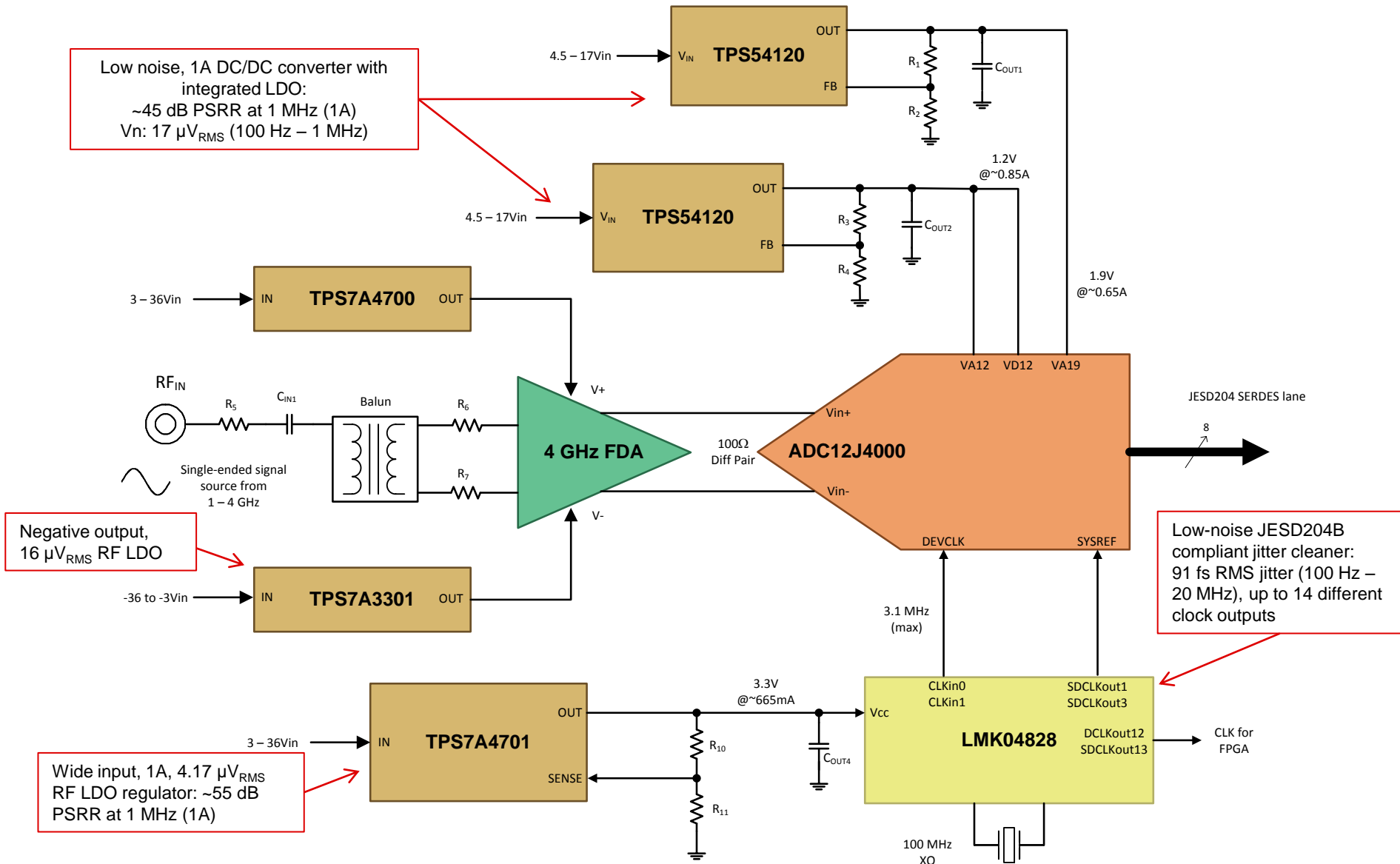


ADC12J4000 versus current ADC12Dxx00RF

Key Product Improvements

- | | |
|--|--|
| 1 >7 dB distortion improvement | Increased performance margin |
| 2 60-70% power reduction | Lower power than IF/ZIF-sampling solutions |
| 3 JESD204B outputs | Simplified interface to FPGA/ASIC/DSP |
| 4 Integrated digital processing | Minimize output data rate |
| 5 Smaller, standard plastic pkg | Smaller size, easier to design board |
| 6 Background calibration | Maintain performance over temperature |

Radar “winning combo”: Block diagram



Benefits of TI's radar “winning combo”

- [ADC12J4000](#) allows for direct sampling in the L-band (1-2GHz)
 - Nearest known competitor is sampling at 1.5 GSPS (@ 12-bits)
 - [ADC12J4000 EVM tool](#) and [ADC12J4000EVM GUI](#) available for evaluation today
- JESD204B interface decreases the overall board size
- Full clocking solution for JESD204B decreases clocking complexity of this interface to an FPGA
- TI clocking solution provides low jitter for maximum ADC SNR performance
 - [LMK04828](#): 88 fs RMS jitter (12 kHz – 20 MHz)
 - Highest-performing clocking solution available today for JESD204B interfaces
 - Higher SNR enables higher object discrimination
- Low output noise voltage and high PSRR from [TPS54120](#) and [TPS7A4701](#) ensure smaller spurs and higher ADC performance
 - [TPS54120](#): Vn: 17 μ V_{RMS} at 100 Hz – 1 MHz, PSRR: 45 dB at 1 MHz
 - Ideal for space constrained, power conscious, [low noise applications](#)

Additional tools & resources

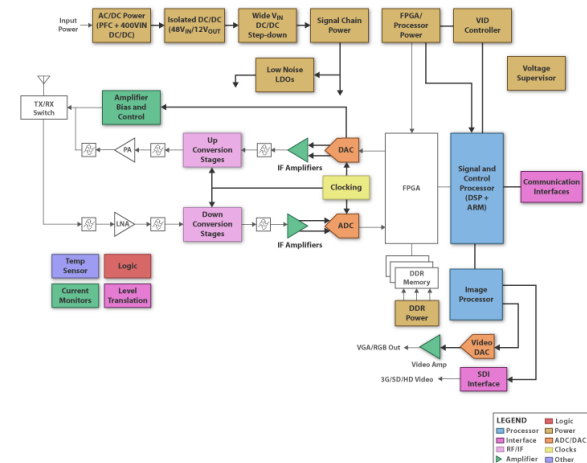
Product Info:

- Product folder: [ADC12J4000](#)
- Support (E2E): [High speed converters forum](#)
- Evaluation modules: [ADC12J4000EVM](#)
- Evaluation software: [ADC12J4000EVM GUI](#)



Additional resources:

- [TSW14J56EVM](#) JESD204B capture/generator card
- [JESD204B](#) data converters and clocking information
- [Radar/electronic warfare SBD](#) information
- [High speed data converter pro software](#)



Thank you! For questions or sample/tool requests, please contact:

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