History of FET Technology and the Move to NexFET™

The advantage comes from the low-input gate charge

Introduced as a substitute for bipolar transistors, power MOSFETs were used as an electronic switch for power management applications. A power MOSFET has a high input impedance. This means it is a voltage-controlled, unlike the current-controlled, bipolar switch. In other words, a power MOSFET can achieve high switching speed even when using a low-power driver. With time, the power MOSFET became the most popular power switch for applications requiring input voltage lower than 200V.

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As the power MOSFET's performance improved, it followed the evolution of CMOS technology introduced in the late '70s to produce integrated circuits. Typically, power FET technology uses depreciated CMOS foundries, following the leading edge with a time delay in the order of three-to-five years with a feature size of: 1µm, 0.8µm, 0.5µm, 0.35µm, 0.25µm, 0.18 µm, etc. Geometry scaling leads to drop-in supply voltage of very large scale integrated (VLSI) circuits used in electronic applications like computing, portable electronics and telecommunications. As a consequence, power supply converter topologies moved towards lower voltage, higher current and a need to better control the power level delivered to the load.

The first-generation of macrocell power MOSFET transistors, double-diffused MOSFET (DMOS), was successfully introduced into the market in the early '80s by International Rectifier. This technology was a vertical MOSFET with a planar gate structure, known as planar power MOSFET. The second-generation of macrocell technology, TrenchFET® introduced by Siliconix, became popular in the '90s. This technology delivered an improved switch resistance (R_{DSON}). TrenchFET technology has a clear superiority over DMOS in terms of resistance and gate charge for a specific product when designed for a drain voltage capability lower than 100V. The dominant low-voltage technology in the market today, nearly all power MOSFET suppliers offer it. Low-switch resistance reduced the conduction power loss in the supply circuits. However, switching loss, which is very important in switch-mode power supply (SMPS), remained the main obstacle. By the end of '90s, in order to reduce cost, size and improve performance such as transient response of the whole power management system, the converter's switching frequency needed to be increased.

A third-generation of macrocell power MOSFET technology recently introduced by Texas Instruments, NexFETTM technology, offers a specific R_{DSON} competitive to the TrenchFET, which reduces the input and Miller capacitances significantly. Low capacitances mean low input gate charge and short voltage transients during switching. This new generation MOSFET reduces switching losses in SMPS applications and enables operation at high switching frequencies. This technology is most advantageous at 30V and below, which is desirable for distributed bus architectures prevalent in today's end systems.

Technology Generations

The difference between DMOS and TrenchFET transistors is illustrated in Figure 1. A DMOS device has a planar gate structure and takes advantage of a vertical current flow between the source and drain electrodes placed at the front and back side of silicon die. Current flows under the planar gate, then turns down between the P-body regions and flows vertically through the epitaxial layer to the substrate. The lightly doped epitaxial layer easily supports high breakdown voltage. Vertical current flow allows large current densities to be handled as opposed to the difficulties in scaling up the area of MOSFETs with lateral layout. The basic cell's pitch or lateral dimension is relatively wide in order to keep enough spacing between the P-body regions.

Large spacing is important to minimize the JFET effect created by the body regions to opposed PN junctions. The DMOS transistor's R_{DSON} is built up by the channel region's resistive contributions underneath the gate, the JFET effect between P-body regions, and the epitaxial layer's and substrate's resistance. The higher the breakdown voltage designed into the device, the larger the epitaxial layer's resistive contribution. In a device designed for low-voltage applications, the MOS channel's resistive contribution and JFET region are becoming more significant.

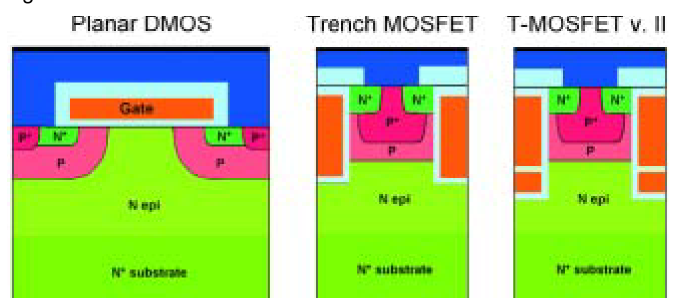

Figure 1:
Comparison of planar DMOS and TrenchFET device structures

In a TrenchFET, the MOS channels are designed along the vertical walls of the trenches. This allows for a high density of channels per silicon unit. By removing the JFET structure, the cell pitch can be made small, reducing the specific R_{DSON} (MOSFET resistance per area). In the late '90s, the transistor's low R_{DSON} made TrenchFET

technology a de facto standard area for low-voltage power MOSFETs. However, the large trench wall area leads to a large value of built-in capacitors. When the trench bottom overlaps the epitaxial layer, which is part of the drain terminal, it creates a large capacitance from gate-to-drain (CGD). This is a major drawback, especially if a high switching speed is required.

At the onset of the 21st century, the trend towards DC/DC converters with higher switching frequencies ignited a demand to minimize MOSFET-related switching losses. Developing TrenchFET structures continues. The first improvement incorporated a thick oxide at the trench bottom, reducing the Miller capacitance (CGD) value. Even more significant improvement was achieved by splitting the gate electrode and connecting the lower part to the source terminal. The lower part of the gate electrode has a shielding effect, decoupling the gate from the drain to significantly reduce CGD. By mid-2000, this second version of the trench power MOSFET structure dominated low-voltage power management applications.

The third-generation or NexFET power MOSFETs delivers a breakthrough in the switch's dynamic performance (see Figure 2). This device has its roots in the LDMOS transistor used for RF signal amplification in a frequency range up to 2GHz. To achieve this level of dynamic performance, it is critical to reduce the Miller capacitance to single picofarads. The overlap of the gate electrode over the lightly doped drain extension (LDD) is kept at a minimum. Additionally, the unique topology of the source metal wrapping the gate electrode and creating a field-plate element over the LDD region makes an effective electrostatic shield between the gate and drain terminals.

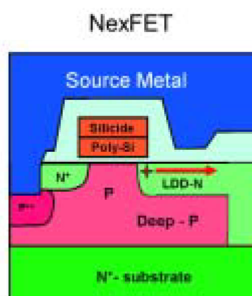

Figure 2: NexFET device structure

The field-plate created by the source metal is also important in stretching out the distribution of the electric field along the LDD surface. This feature lowers the height of the electric field peak at the drain corner of the gate electrode. By doing so, the hot-carrier effects of creating reliability issues in the conventional LDMOS devices are avoided. The LDD region itself is designed following the charge balance design rule. Here, doping in the LDD region is counter-balanced by the charge in the depleted deep-P region, and is additionally influenced by the source field-plate. The charge balance approach allows the carrier concentration in the LDD region to be increased by roughly one order of magnitude.

The R_{DSON} of NexFET devices take advantage of the short MOS channel and short length of the highly doped LDD region. Moreover, the small cell pitch achieved by the contemporary fine line lithography makes the specific R_{DSON} of NexFET devices competitive to TrenchFET technology. The advantage of the NexFET approach comes from the low-input gate charge and very low CDG values, not achievable with the TrenchFET devices.

NexFET™ Performance

NexFET technology provides excellent figure of merit (FOM) values so important for SMPS applications. The classic way to judge how good a power MOSFET platform technology is in switching applications is to look at the resistance multiplied by the total gate charge or the Miller capacitance. The recent history of FOM improvements and breakthroughs achieved by introducing NexFET technology is illustrated by Figure 3. TrenchFET technology, after almost two decades of development, shows a saturation effect in the tempo of the FOM improvements. The NexFET approach, being at its early stage of maturation, promises on-going improvements for the foreseeable future.

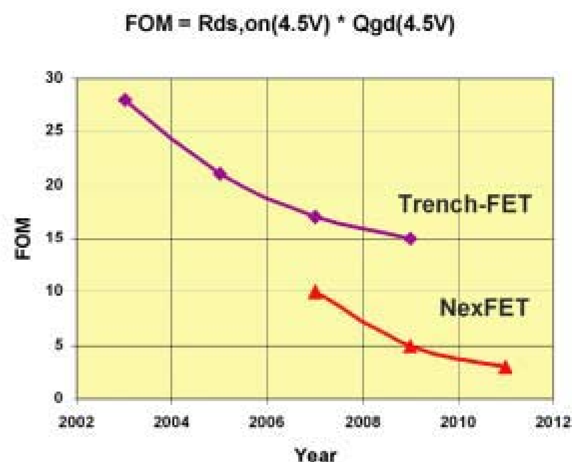

Figure 3: Comparison of FOM for TrenchFET and NexFET technologies

The level of improvement made possible by implementing NexFET devices is demonstrated in Figure 4, which shows the efficiency of a six-phase synchronous buck 12V converter running at 635 kHz. In general, simply dropping-in these devices into an existing application allows up to double the switching frequency of a DC/DC converter without significant penalty in conversion efficiency. Further advantage can be achieved by dedicated optimization of driving conditions as dictated by the gate driver circuit.

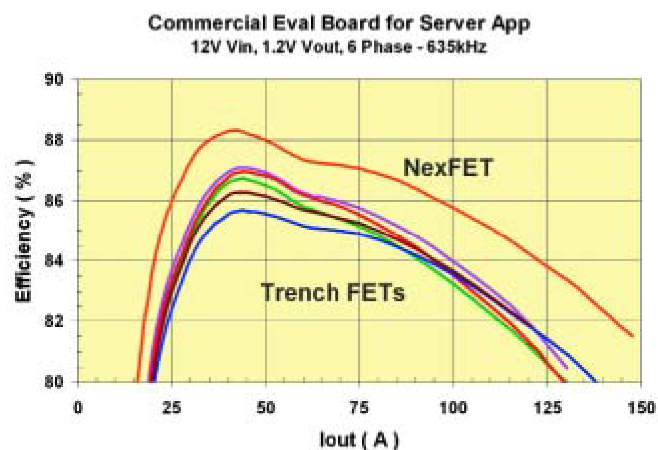

Figure 4: Superior efficiency of a 6 phase converter enabled by NexFETs

Conclusion

NexFET technology is a new generation of silicon-based power MOSFETs with an inherently low-charge structure, which increases efficiency in existing switching converters as well as enabling the next generation of switching power converters with multi-megahertz operation.

References

For more information about NexFET technology, visit: www.ti.com/mosfet-ca.

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