Next Generation of Power MOSFETs

NexFET technology is a new generation of MOSFETs for power applications with its roots in a laterally diffused MOS (LDMOS) device used successfully for RF signal amplifications. The RF heritage provides minimum internal capacitances, and the vertical current flow offers a high-current density without gate de-biasing issues. By using NexFET switches, a converter's efficiency can be significantly improved.

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Power MOSFETs are used, for example, as switches for high-frequency pulse width modulation (PWM) applications such as voltage regulators and/or switches that control current to and from a load in power applications. When used as a load switch where switching times are usually long, the device's cost, size and on-resistance are the prevailing design considerations. When used in PWM applications the transistors must exhibit minimal power loss during switching, which imposes an additional requirement of small internal capacitances that make the MOSFET design challenging and often more expensive. Special attention has to be payed to the gate-to-drain (C_{gd}) capacitance, as this capacitance determines the voltage transient time during switching. It is the most important parameter affecting the switching power loss!

Pursuing the ideal switch

The requirements for an 'ideal' switch used in a synchronous buck converter, which is the most popular converter topology used for computer applications, are low conduction losses (low $R_{DS(on)}$), low switching losses (small C_{gd}), low driver losses (small C_{iss}), no cross-current losses (small C_{gd}/C_{iss} ratio to avoid shoot-through effect), and low body diode losses (small Q_{rr} and hard switching enabling short break-before-make delay time).

Of course, the device used as a switch must have a robust structure allowing large amounts of avalanche energy to be dissipated, ensuring reliable operation over the full safe operating area (SOA) range.

In NexFETs (see schematic cross-section in Figure 1) the current flows from the source terminal provided by the top metallisation through the lateral channel underneath the planar gate, into the lightly doped drain extension region (LDD), then forwarded to the substrate by the vertical sinker with low resistance. The RF heritage provides minimum internal capacitances, and the vertical current flow offers a high-current
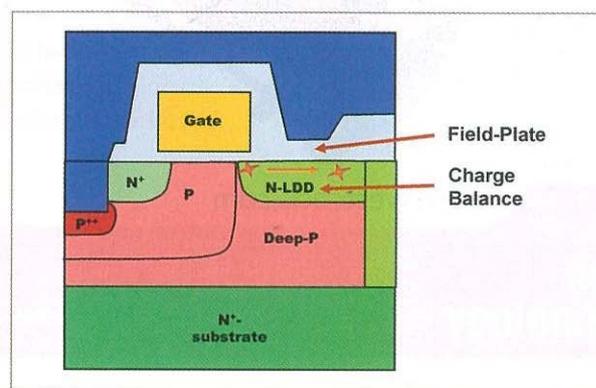

Figure 1: Schematic cross-section of a NexFET device

density without gate de-biasing issues, typical for LDMOS transistor planar layouts.

The NexFET device's source metallisation has a unique topology, providing a field-plate effect at the gate's drain corner. The field-plate stretches the electric field distribution along the LDD region, reducing the high electric field peak at the gate corner. In turn, it provides good reliability against hot carrier effects that deteriorate the gate oxide quality in conventional LDMOS transistors.

The LDD region is doped to a high level of carrier concentration taking advantage of the charge balance between the LDD, the field-plate, and the deep-P region underneath. This helps minimise the device's resistance ($R_{DS(on)}$). The deep-P doping is also used to provide a large charge below the channel region, suppressing short channel effects. By doing so, short channel length can be designed without problems related to punch-through effects. The source contact is performed in a shallow trench reaching through the source implant region. A doping profile engineering technique is used to pin the location of the electric breakdown at a
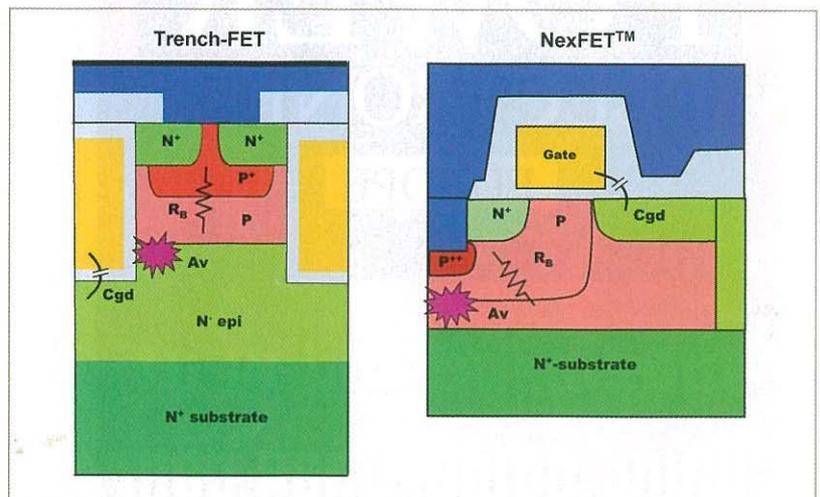

Figure 2: Technology comparison between Trench-FET (left) and NexFET

high-drain voltage. This locates the avalanche generation's hot carriers far away from the gate oxide, and guarantees that the internal bipolar transistor structure will not be triggered up to very high avalanche current densities.

In the last two decades, the trench MOSFET has established itself as the most successful technology for low-voltage (< 100V) power switches. Figure 2 compares trench and NexFET technologies. The major advantage of the trench approach is the high-channel density within a small pitch of the active cell. Alternatively, the large area of the trench walls makes it difficult to keep the internal capacitances small. Also, the moderate doping level of the epitaxial layer below the trench results in a non-scalable contribution to the transistor's resistance, and limits the advantage of designing the FETs for low-drain voltage applications (e.g., below 20V V_{DSmax}).

By taking advantage of readily available modern, fine lithography fabrication processes, you can combine a narrow gate line coupled with a high doping of the LDD region. This novel new structure now has resistance competitive with trench MOSFET technology, yet retains very low charge characteristics. The gate's minimum overlap over the source and drain regions keeps the internal C_{GS} and C_{GD} capacitances small, thus, delivering excellent switching performance. Additionally, the source metal field-plate over the LDD region acts as a shield decoupling gate from the drain terminals. This forces C_{GD} to drop significantly, even at small drain voltages. Low C_{ISS} and C_{GD} values make the NexFET-FOM ($R_{DS}* Q_G$ and $R_{DS}* Q_{GD}$ figure of merits) much better than the FOM observed for leading edge trench MOSFETs.

NexFET switching performance

Experimental data on benchmarking NexFET devices versus state-of-the-art trench MOSFETs (Figure 3) for application in PWM switching converters using synchronous buck topology is very popular in the field of low-voltage power supplies. Converter efficiency is shown as a function of the output current for the case of a six-phase commercial evaluation board. The results obtained using leading edge trench devices lay within a close group of data and differ by ±0.5% only. The converter efficiency achieved by a NexFET chip set is higher by 2 to 3% in the full range of load current.

The NexFET transistor has a comparable body diode reverse recovery behaviour to an optimised trench device. The difference is that the NexFET can take advantage of a hard PWM drive where the turn-off of the transistor is sharp and has minimal tail current. Thus, the break-before-make delay time can be made very short, minimising the
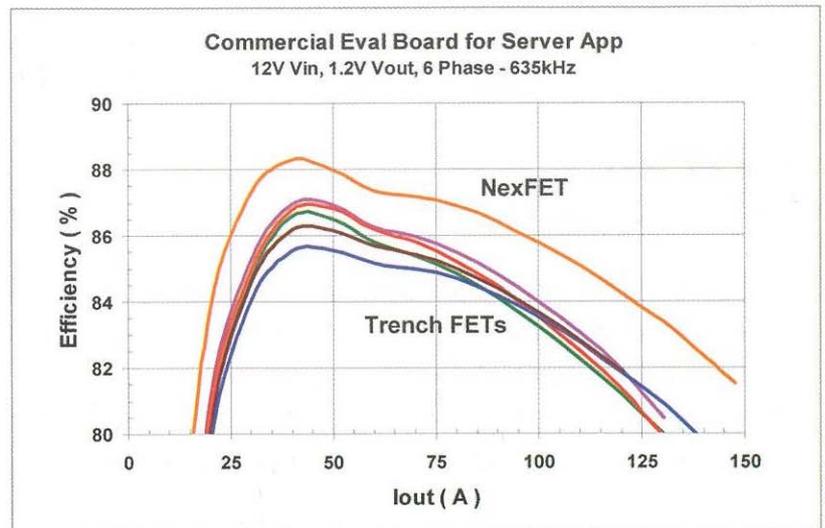
Figure 3: Efficiency of synchronous buck converter for server applications

diode conduction time and, hence, the associated diode conduction power loss. In other words, you can expect that when using NexFET switches the converter's efficiency can be further improved by reducing delay times dictated by the gate driver stage.

Figure 4 compares a plot of power loss versus the switching frequency of a 12V synchronous buck converter for a leading edge trench FET chip set compared to a NexFET solution. In conclusion, the converter's efficiency can be kept above 90% (power loss of 3W). The switching frequency can be increased from 500kHz to 1MHz by using NexFET devices. It is actually feasible to increase this frequency beyond 1MHz by optimising driving conditions.

Summary and Outlook

In response to the quest for an ideal switch, the NexFET technology delivers following features:
- Specific $R_{DS(on)}$ is comparable to state-of-art trench FETs,

- much lower C_{ISS} and C_{GD} improves FOM,
- switching losses and driver losses are significantly improved,
- the ratio of C_{GD} to C_{ISS} is similar to trench FETs, but absolute C_{GD} value is very small and shoot-through immunity is improved by minimising the total amount of charge feedback through Miller capacitance,
- The body diode's Q_{rr} is similar, but NexFET transistors can be switched much harder, and the dead time dictated by the driver can be made significantly shorter.

A distinct advantage in converter efficiency can be observed simply by dropping-in NexFET chip sets into an existing system. NexFET technology enables converters to run at much higher switching frequencies, minimising both size and cost of filter components.

Literature

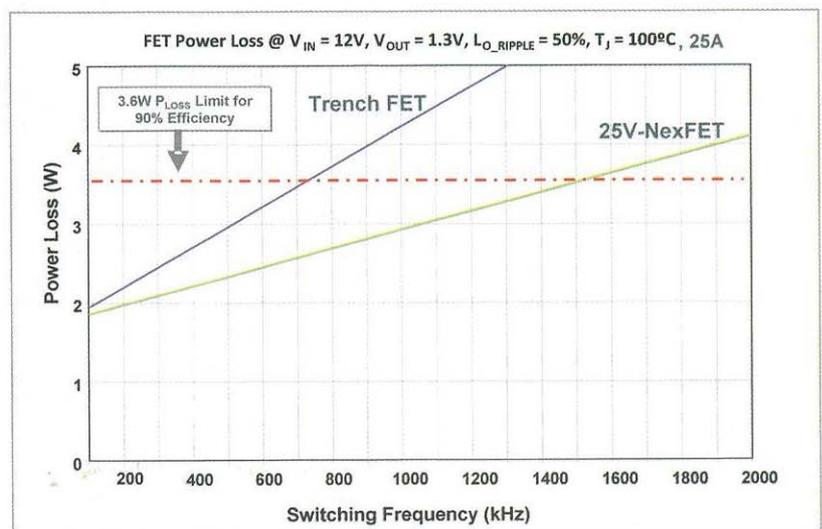*APEC 2009, 'TI enters discrete high-power MOSFET market', Power Electronics Europe 2/2009 (March), page 23*

Figure 4: NexFET enabling converter operation at high switching frequency

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