Practical Considerations in Troubleshooting and Optimizing Power Supply Control Circuits and PCB Layouts

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ABSTRACT

This Topic is intended to address the most common difficulties incurred during the breadboarding stage of a power supply circuit, unveil detailed information and offer practical solutions to overcoming difficult prototype and layout problems. Numerous examples from basic Pulse Width Modulators (PWMs) through high voltage, off-line Power Factor Correction (PFC) applications are cited. Two common "tools of the trade" will be explored in greater detail. Finally, a step-by-step procedure from initial circuit design and review through the first "power-up" sequence is presented along with a troubleshooting guide.

INTRODUCTION

Initial construction and troubleshooting of switchmode power supply control circuits and power stages can be a time consuming and frustrating ordeal, especially for newcomers to the power management industry. Those familiar digital circuit logic level "ones" and "zeros" immediately translate into unforgiving high power "on's" and "off's" in a power supply environment. A point is reached when you've carefully breadboarded that new control circuit, started bringing it to "life" and have quickly determined that something, somewhere in the circuit is NOT working as it's supposed to, or at least not as you had intended it to. Well, fear not! This Topic will highlight the numerous steps - some frequently overlooked and/or omitted which are necessary to transform that new control circuit from a problematic prototype to fully functional PWM solution. It is intended to enhance and expand the troubleshooting skills for those of all levels of experience in power management.

The "Ground" Rules : Exactly where is the one and only real circuit "ground" ?

Nearly every circuit schematic and PC Board layout contains at least one point referred to as "ground", "system ground", "chassis ground" or "common". But when critical measurements are made using this point as the reference, noise and voltage drops between this and any other "ground" points in the system are observed. Although they are all perceived to be at the same electrical potential, these two "grounds" are NOT. Physically locating two points (nodes) at some distance away from one another introduces series parasitic elements; resistance and inductance. As current flows in these paths, especially at higher frequencies and power levels, any finite series circuit impedance's will have considerable effects on signal integrity and fidelity. This situation is generally worsened by any distributed capacitance to other parts of the circuit, which can cause coupling to other nodes. Rarely, can many of the parasitic effects be seen from a view of the PC board layout, and even less is visible from the circuit schematic. Nevertheless, these parasitics are responsible for electrically separating ground connections from one another to where it may not be clear which one, if any, is the "true" circuit ground.

Every cycle of a switchmode power system is determined by the control circuit, normally a Pulse Width Modulator (PWM) Integrated Circuit. All analog signals representing the voltage and current loops to be controlled are brought to PWM comparator inputs to deliver the exact pulse width required by the system to perform and maintain regulation. Each of these signals is referenced to the integrated circuit's internal substrate or "ground",

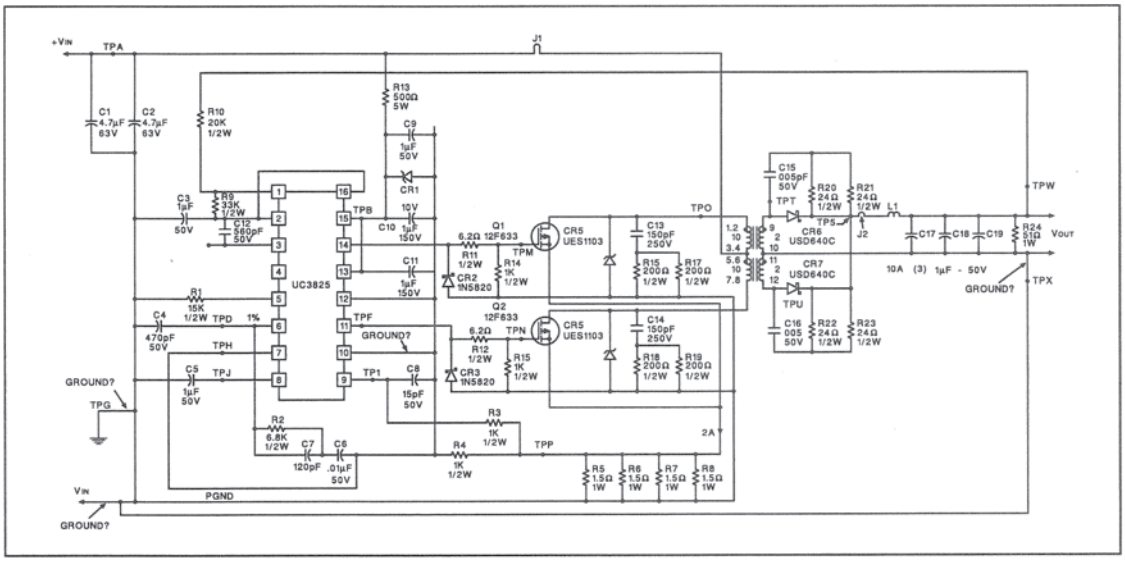

Figure 1. Circuit schematic with multiple "ground" locations

thereby making it the sole point in the entire system for absolute referencing of the parameters to be controlled.

" The control circuit ground, to which all signals are referenced, is the sole "ground" connection of the system and for making all measurements."

SGND vs PGND vs "circuit" ground

Many PWM's contain both low level analog functions and high current, high speed outputs for driving larger power MOSFETs. Integrating both of these functions within a single chip is difficult, due to the simultaneous yet opposing requirements for low noise and high power. To help alleviate this, many newer PWM IC's have separate "signal ground" (SGND) and "power ground" (PGND) pin connections. The goal is to localize the high current gate drive noise into an "independent" loop that does not interfere with the more sensitive analog control functions. As evidence, notice that many PWM's "sandwich" the gate drive output pin between two well bypassed, "stiff" DC potentials; power ground (PGND) and the output driver stage collector (VC) [or drain (VD)]. This configuration minimizes the capacitive coupling of the output to analog circuits by more closely coupling it to the supply "rails", VC and PGND.

The adjacent pins of the IC leadframe will also see noise from one pin to another, induced by quickly rising or falling currents from the high di/dt output totempole stages. Pins act as parallel conductors and the field created at one pin is also "loosely" coupled to the next pin. This is similar to poorly coupled windings in a transformer where the field of one is also imposed upon the other. In dual output PWMs, an additional "stiff" DC supply is frequently used to buffer the effects of the second output from otherwise adjacent pins. Typically, another well bypassed, DC potential such as the IC supply voltage (VCC) or the reference voltage (Vref) is recruited for the task.

Note also that the most noise prone functions of the IC *should* use the shortest pins of the package - located near the center of the body. This further minimizes the parasitic effects, and makes bypassing more effective. Any high speed, high current output using longer - or worst - the corner pins of the IC package is certain to effect any high impedance circuits on the IC or in close physical proximity. Take special precautions in these instances.

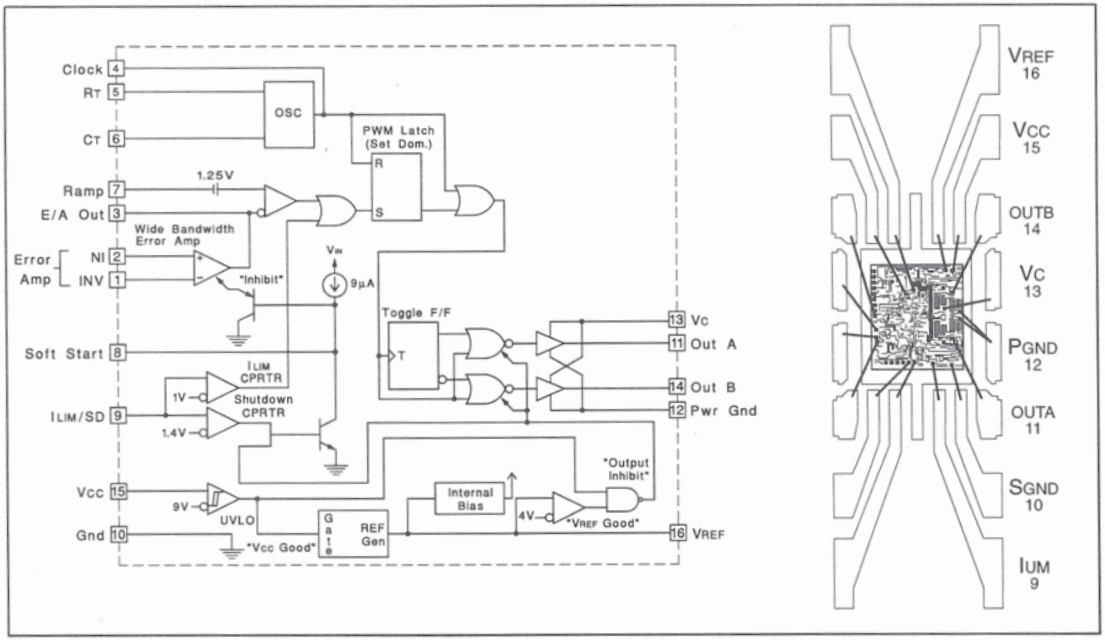

Figure 2. UC3825 example

SGND = PGND

Electrically and also physically on the PC layout both signal and power ground connections come together at one point. It's at the substrate of the Integrated Circuit itself, inside the package, and not on the PC board where the two traces and two IC pins are connected. A small, but finite inductance, resistance and capacitance of each pin from the board to the IC "dice" in addition to the bond wires from the lead to the IC dice electrically effect the circuit "ground", and generally degrade optimal bypassing. The substrate of the IC is the true circuit "ground" to which all signals are referenced. Then why use separate pins?

" SGND must be connected directly to PGND right at the IC pins"

With eight pin IC's, such as the UC3842 and UCC380x families, only one pin is available to serve for both, and optimal bypassing can be difficult, but is possible. Even when separate SGND and PGND pins are available to the user on IC's with 14 or more pins, proper bypassing is still essential for noise free operation. Specifically, the two grounds (SGND and PGND) must be connected together on the PC board layout with an absolute minimal distance between them. Otherwise, and depending on the physical location and connection of the bypass capacitors, it is possible for the high frequency, high current path to become SGND instead of PGND. This could occur with optimal bypassing to SGND and a long PC trace connection to PGND with a poor quality bypass capacitor - to where the increased R and L of the series connection and capacitor present a higher impedance than the path to the SGND, quality bypass capacitor. In other words, the PGND bypass is ineffective.

Inductance "Kills"

To demonstrate the problematic effects of inductance on a PWM IC's operation in circuit, several inches of wire were deliberately added between the PWM IC ground pin and PC Board connection. For this example, a UC3825 High Speed PWM was used - although all apply - and the PGND and SGND pin leads were bent, soldered together to the loop of wire whose other end was soldered to the board. All bypass capacitors, Schottky clamp diodes etc. were in their normal locations on the PC board. Ground was referenced to the IC SGND and PGND "ground" pins for all scope measurements. All waveforms reference the following IC functions :

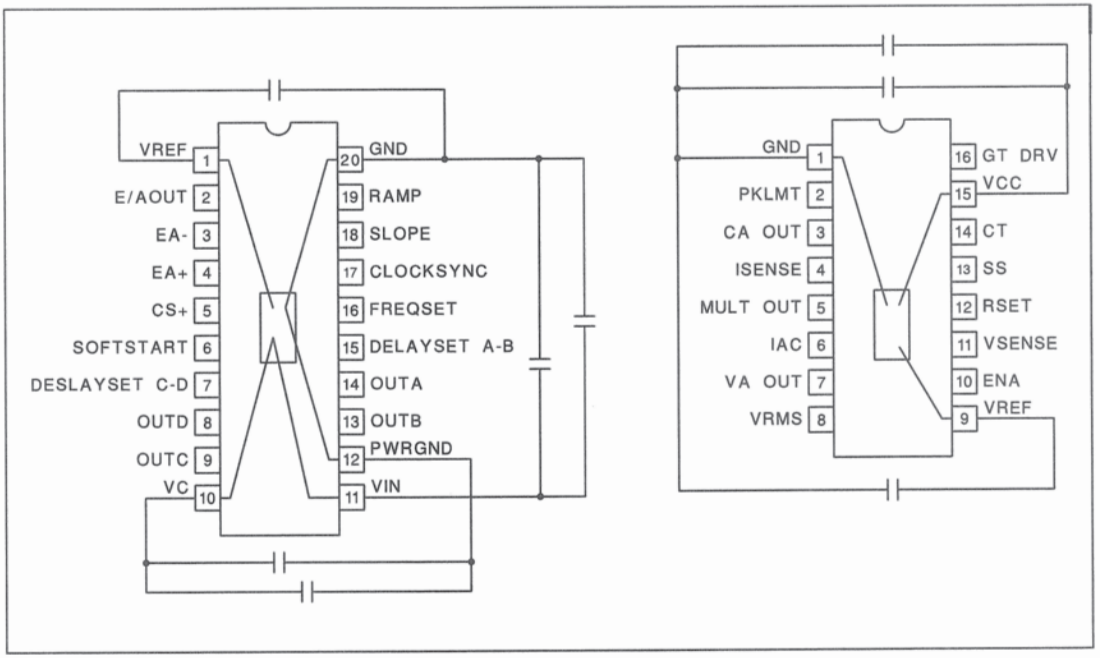

Figure 3. Examples of difficult bypass capacitor connections

top trace is the timing capacitor waveform (Ct), next is the voltage at output A followed by that of output B, and finally the IC's clock (CLK) synchronization output on the lowest waveform.

Oscillator details : Several internal circuits operate at the end, and only at the end of each oscillator clock cycle. These include the oscillator's timing capacitor's discharge transistor, the sync/CLK output, the toggle flip flop to direct the output pulse, and the PWM latch setting pulse. Ideally, these would require no propagation time or delay to activate, but in reality, that's never the case. For example, in order for the PWM IC to begin its next clock cycle immediately following the turn-off

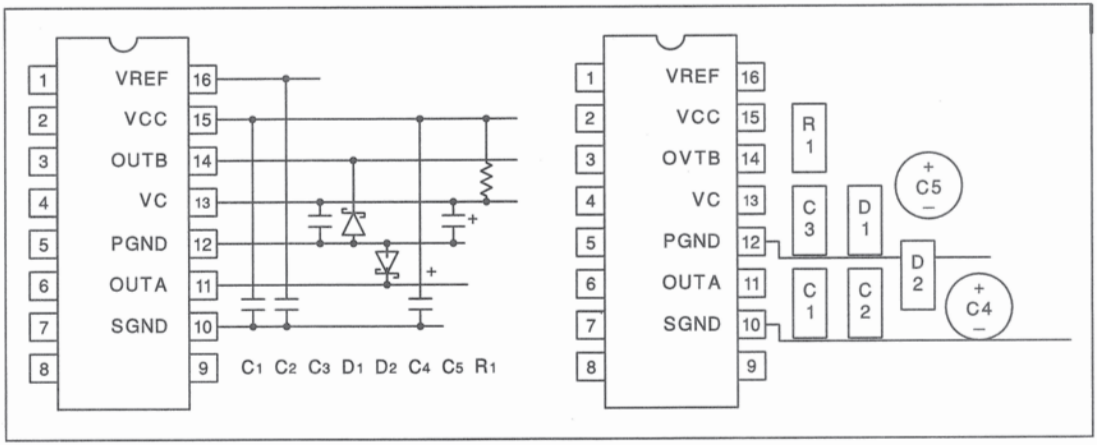

Figure 4. Proper layout and connections for the UC3825

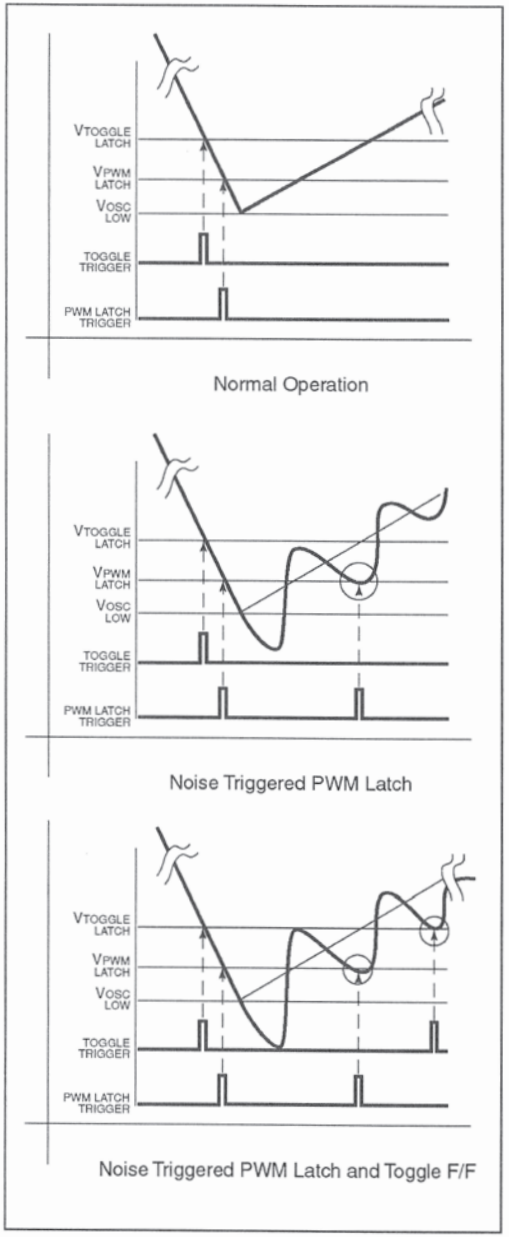

Figure 5. Diagram of internal oscillator circuitry

of the oscillator's discharge transistor, the toggle flip flop must be advanced and the PWM latch set at some brief time BEFORE the exact instant that the next cycle begins. One method to achieve this is by gating the triggering comparators to these circuits with the oscillator's discharge circuitry. Techniques to match the brief - but slightly different internal delays can be realized by setting each of the comparator's thresholds at slightly different amplitudes. This provides a secondary function of minimizing the instantaneous noise on the IC dice caused by each circuit. An example of this is shown in figure 5.

Diagram of Internal Oscillator Circuitry

The problems occur when any series inductance in the timing capacitor, ground or either of these connections is added. The sharp turn on and off of the oscillator discharge circuitry can cause ringing of the timing capacitor (Ct) waveform at the respective times. Worse, however, is when the high power outputs of the IC influence the signal due to the high di/dt induced voltage spikes across the inductance. Typically, what happens and can be seen is the false triggering and /or terminating of the PWM output(s). Note that by intentional circuit design, the PWM latch - with a LOWER threshold, is triggered first by the ringing - and not the toggle flip flop. Had these internal comparator thresholds been reversed with each other, output B could be turned on immediately after output A is terminated. The PWM's output B would stay high until the normal error amplifier and PWM RAMP inputs intersected, or when the maximum programmed duty cycle has been reached. In either case it would generally present a serious problem to the power stage's normal operation.

To further demonstrate the effects of this, the PWM breadboard was deliberately modified such that output A injected enough noise to cause false triggering of the PWM latch. Output B was configured not to cause the same condition for this test.

Referencing Figure 6, note the large spike on the timing capacitor waveform and excessive ringing when output A turns on. Evident is that there is enough noise to trigger the PWM latch and terminate the output pulse. While excessive inductance in the ground connection and timing capacitor is the cause in this demonstration, not having Schottky clamp diodes from output A to Vc, the collector supply voltage of the totem poles or to

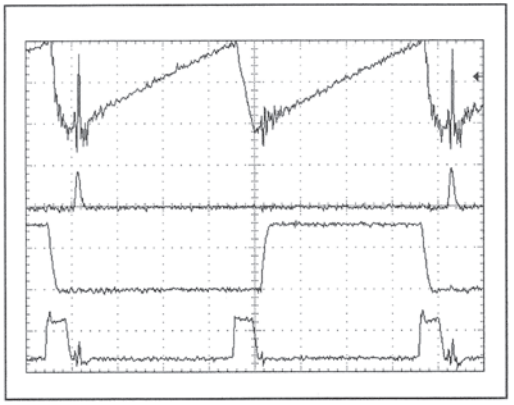

Figure 6. Noise spike on timing capacitor

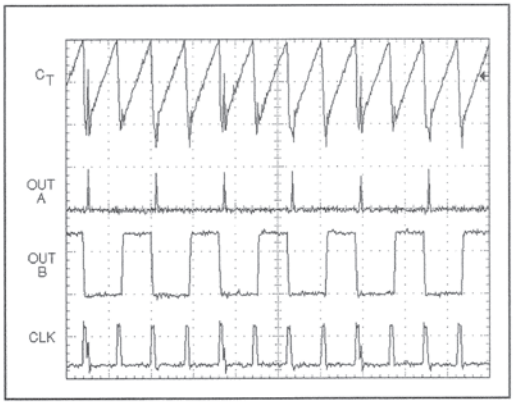

Figure 8. Early termination of output A due to noise triggering

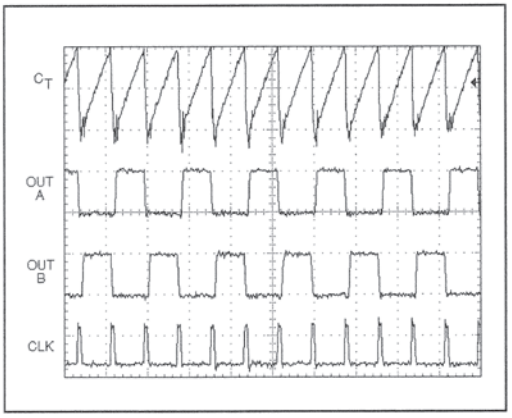

Figure 7. Normal maximum duty cycle waveforms

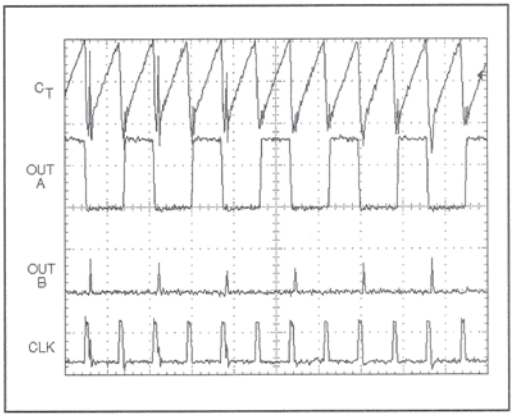

Figure 9. Early termination of output B due to noise triggering

Vcc, the input supply rail is another possible cause. Notice on the next clock cycle, however, that output B is normal and not prematurely terminated by the noise.

A series of possible, problematic waveforms is shown in the next few figures for further emphasis. All again, were intentionally "staged" or caused by deliberately miswiring or poorly laying out the control circuit breadboard. In all, the timing capacitor (Ct), two IC outputs and CLocK waveforms are displayed and the circuit adjusted to yield the maximum duty cycle on both outputs. Despite fairly noisy waveforms, especially on Ct, figure 7 shows normal operation with Vin (Vcc) equaling 10VDC.

In the next photo, Figure 8, the input supply voltage was raised to approximately 14 VDC, and enough noise was generated by output A in this case to trigger early termination of the output.

Further increasing the supply voltage to around 16VDC causes output B to false trigger as shown in Figure 9, yet output A returns to normal operation! Both of the IC outputs can also be made to cause mis-operation as shown in Figure 10.

"Flipping Out" the PWM's Toggle Flip Flop

Intentionally degrading the circuit board layout even further can cause not only the PWM latch to trigger, as shown, but also the internal toggle flip flop which directs which output of the IC will be driven. Figure 11 shows what happens to the outputs

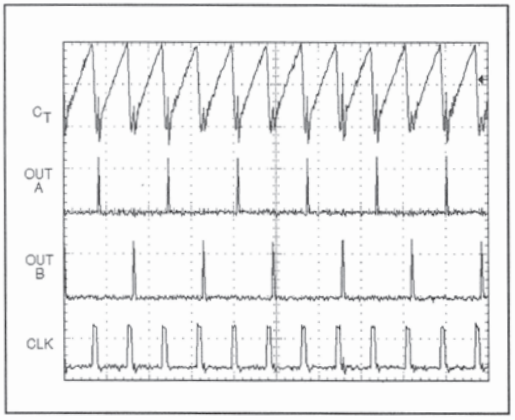

Figure 10. Mis-operation of both outputs caused by noise

when this mode is achieved. Essentially, the toggle flip-flop is toggled twice each cycle - once normally by the oscillator discharge and once again by the circuit noise. This triggering directs all output pulses to output A in this example and none to output B. Fortunately, and again by intentional design of the IC, the pulse width is terminated first, and then the toggle flip-flop is triggered. Otherwise, it would be possible to get the pulse width first appearing on output A, then the rest of the pulse on output B !

In a noisy environment, it is also possible to falsely trigger the toggle flip-flop at some other rate - like every other (second) pulse on output A (only) as shown in Figure 12. This results in the output sequence of A-B-A-A- and repeats. For

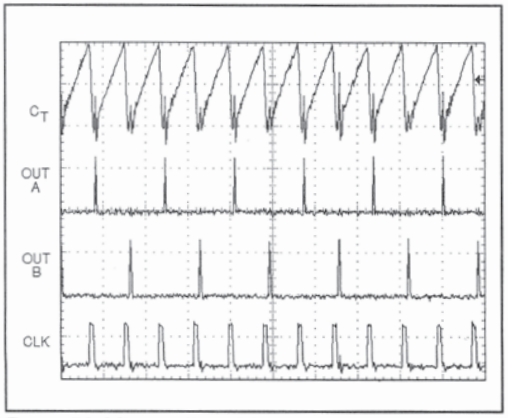

Figure 11. Mis-toggling of the toggle flip flop due to noise

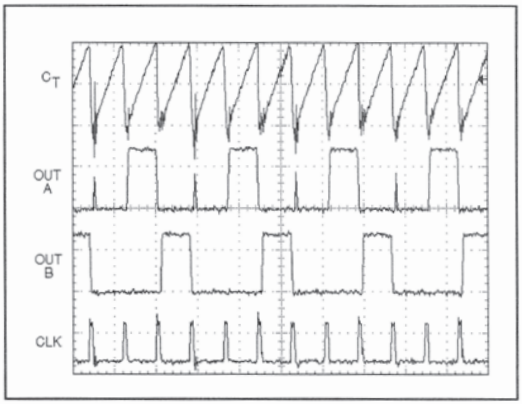

Figure 12. A-B-A-A false toggling of outputs due to noise

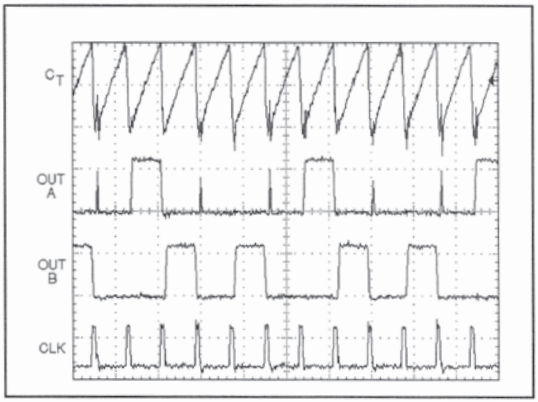

Figure 13. A-A-B-A-B false toggling of outputs due to noise

completeness, other possibilities are shown in Figure 13 which is an A=A=B=A=B sequence ,or A-A-A-B and repeated as shown in Figure 14. Other false output sequences are possible - and likely, with asynchronously triggered system and ground noise such as encountered in transients on the power supply input and output terminal.

Bypassing Capacitors

The optimal bypassing scheme is to separately bypass the analog and power sections of the IC power supply rails (when possible). Place a high frequency bypass capacitor between VCC and SGND to reduce noise and ripple for the low level analog functions. A high value, low ESR and low ESL type bypass capacitor is absolutely required for the high power output totem pole driver section of

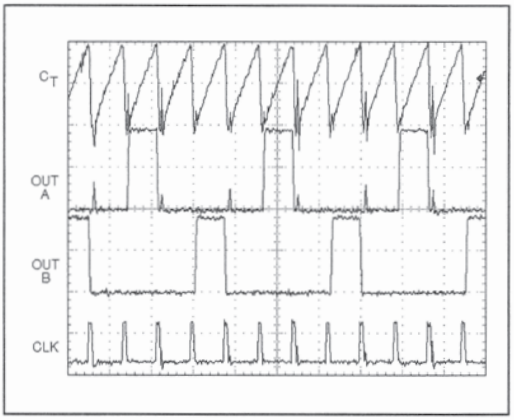

Figure 14. A-A-A-B false sequence due to noise

the IC, connected directly from VC (collector supply) to PGND. [These pins are commonly made available on PWMs with 14 or more pins, aimed at higher power and generally noisier environments.]

Selecting Bypass Capacitors

Capacitor types and values commonly used in the industry vary , but the 0.1 µF ceramic (monolithic) generally prevails as the most commonly used for bypassing, especially in Surface Mount applications. Tantalum electrolytics are another popular option and usually quite less expensive than ceramic for higher capacitance or lower ESR/ESL applications. Other popular types for thru-hole mounting bypassing are polycarbonate, polystyrene and polypropolyene or simple ceramic "disc"s. A comparison of impedance versus frequency for several different types of 0.1µF capacitors is shown in Figure 15 for comparison and reference.

This curve represents the typical impedance versus frequency not just for the electrical circuit equivalent of a capacitor, but applicable to any series RLC network. At lower frequencies, below the self resonance point, the impedance decreases with increasing frequency. This is indicative of a capacitive type impedance where X = 1/ 2*pi*F*C. Another practical use for this measurement is to determine the exact capacitance of an unknown device, part of a circuit or section of a PCB layout.

Self resonance is reached at the lowest point of the impedance axis where the impedance of the capacitance (XC) equals that of the inductance

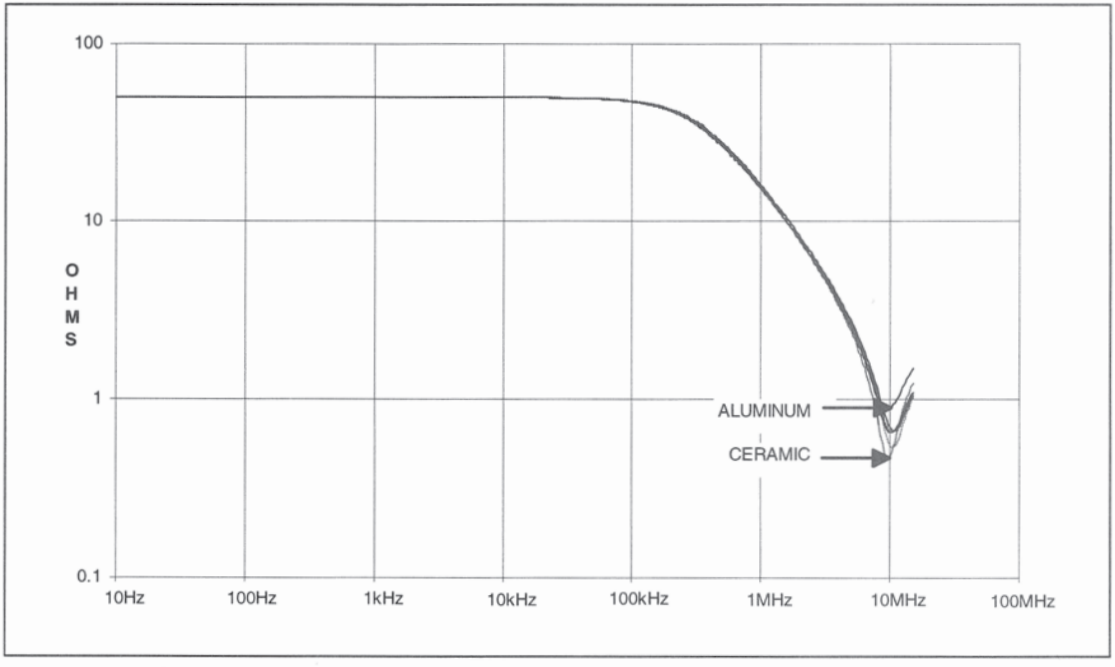

Figure 15. Impedance vs Frequency for various 0.1µF capacitors

(XL). Since these two impedances are 180 electrical degrees out of phase with each other, their impedances effectively cancel one another, and the remaining component of the impedance is purely resistive. Therefore, the impedance measured at the lower peak of this curve is a capacitor's Equivalent Series Resistance, or ESR.

Increasing the test frequency above resonance will demonstrate the series inductance of the component under evaluation. So, in instances where the Equivalent Series Inductance, or ESL of a device is unknown, it too can be obtained from this simple impedance versus frequency measurement. Having a low ESL is critical to maintaining tight output voltage regulation in high transient current or switched load applications, typical of many of today's microprocessors. For many capacitors, this is a parameter which may not be well characterized, unspecified, or often deliberately overstated to guarantee the worst case parameter over all manufacturing variations. In some instances, designers might elect to use empirical measured data, statistical probability and distribution curves to reduce total parts. This applies to both a capacitor's ESL and ESR for transient load conditions.

Commonly found in parallel with the 0.1 µF bypass capacitor is a larger value electrolytic capacitor between 4.7µF and 1000µF to facilitate the bulk energy storage requirements of the load. Even an inexpensive variety will achieve the reasonable performance in most applications when laced in parallel with the low impedance 0.1µF bypass capacitor, right at the IC's pins.

Guidelines on Selecting the Best Bypass Capacitor Value and Combination

Begin with a measurement of the frequency or duration of the transients, spikes or noise on the power supply lines to determine the appropriate value of capacitance needed. A plot of impedance versus frequency for the more common values of

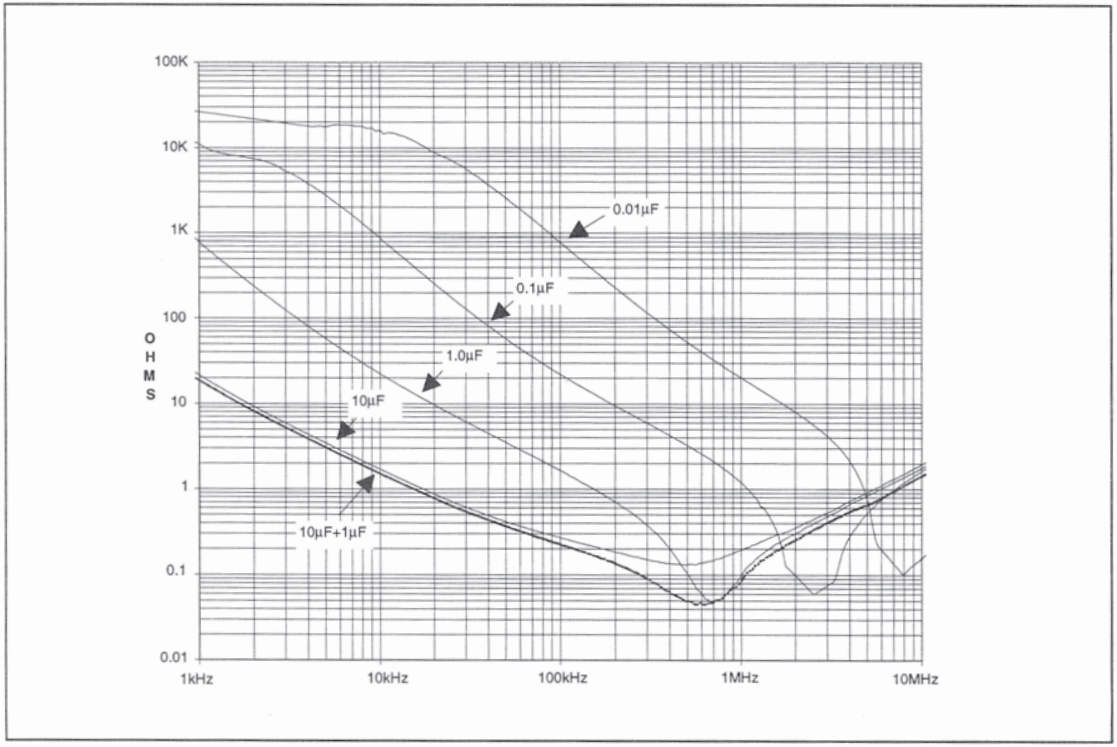

Figure 16. Impedance vs frequency for different value capacitors

bypass capacitors used from 10 nF through 10 µF is shown in Figure 16. Match the effective frequency of the noise to be filtered with the capacitor reaching its lowest impedance at the same, or closest frequency. For example, if switching transitions have 100 nanosecond periods, the frequency of interest to achieve optimal bypassing is 1/100 ns, or 10 Mhz. If other noise at different frequencies exist, then consider paralleling different capacitor values - with different resonant impedance minimums to adequately bypass each noise frequency of interest. Overcome the tendency and loyalty to not use values less than 0.1µF in high frequency applications. Quite often, many smaller value capacitors between 0.001µF and 0.047µF provide the same - if not better bypassing to the high frequency noise in a switchmode power supply environment.

To obtain a lower impedance bypass capacitance at a specific frequency, consider using two or more capacitors - of the same value and resonance point placed in parallel to achieve the lowest impedance at that frequency. Note, however, that there is a practical limit to the effectiveness of this technique. As more capacitors are placed in parallel, the small, yet finite interconnection resistance and inductance between capacitors adds in series with the capacitor's self impedance. This will effect the resonance frequency of the capacitor network by lowering it slightly along with not completely halving the impedance of the two capacitors in comparison to one. Depending on the relative magnitudes of the self to series impedances, this technique may also widen and round-out the impedance minimum value. Examples of this are shown in Figure 17.

A lower impedance bypass over a wider frequency range is obtainable by paralleling several bypass capacitors - with different self resonant frequencies. For example, a 10µF, 1µF, 0.1µF and

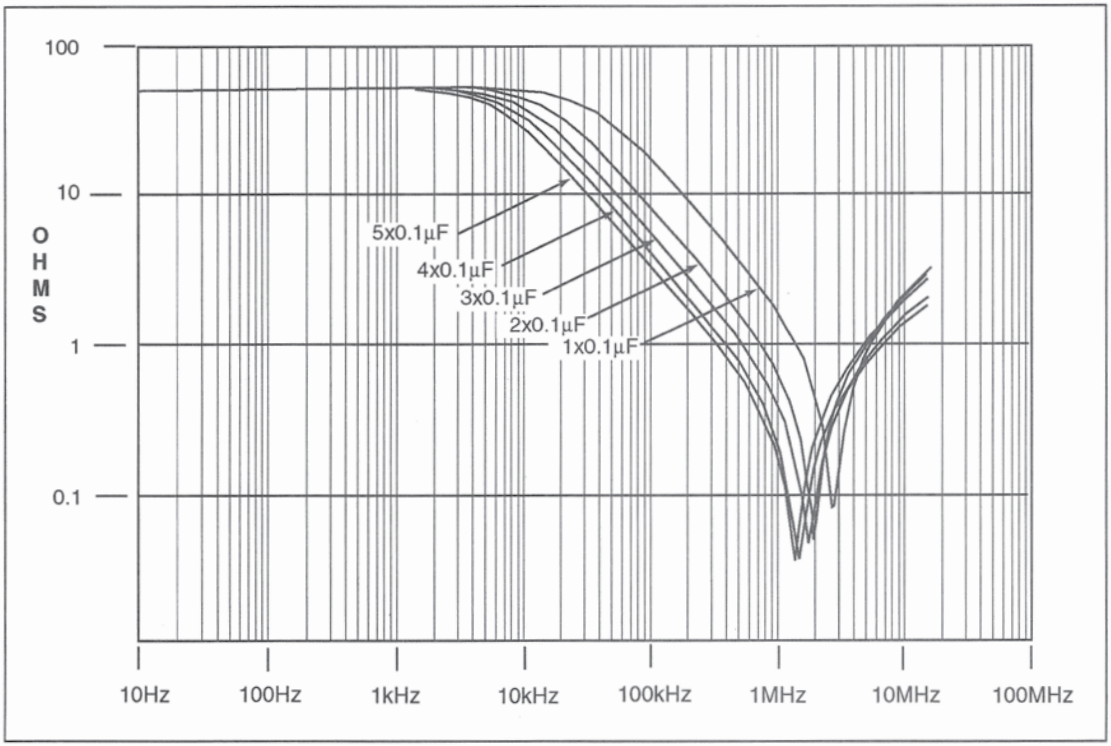

Figure 17. Paralleling capacitors of the same value

0.01μF capacitor parallel bypassing network would reduce the effective impedance over a much wider span of noise frequencies that any one capacitor in particular. One example of this is shown in Figure 16 where the impedance of a 1μF in parallel with a 10μF capacitor closely approximates the attributes of each, over frequency

Note, however, that when this technique is implemented, the ***smallest capacitance value*** should be physically placed ***closest*** to the IC to minimize any series connection inductance, thus increasing its impedance over ideal. Placing the largest value capacitors - with generally the higher internal inductance (ESL) furthest away, yet still physically as close as possible has a far lesser effect on overall impedance than putting these closest and the smaller capacitors further away. Always label and draw the high frequency bypass capacitors next to the IC on the schematic.

Reducing High Frequency Noise on Power Supply Outputs

Similarly, the technique described is applicable to reducing output ripple and noise on a power supply terminals. Envision the user's connection as the IC pin in the previous example. Working from the outside (terminal blocks) inwards, place the lowest ESR/ESL "high frequency bypass" capacitors right on - or at the output terminals of the power supply. This makes them the most effective as the series impedance from the capacitor to the terminal is the lowest possible. Generally, furthest away - or as in this case - towards the inside of the power supply should be the large bulk capacitors used for raw filtering and energy storage. High frequency noise spikes on these capacitors must still flow through the output bus bar or printed circuit board traces to the terminal blocks. This network can be modeled as a series resistance and inductance shunted by the distributed capacitors forming an RLC network, and providing further filtering. The low ESR/ESL "bypass" capacitors right on the output terminals provide the final level of filtering, especially for the high frequency noise. Here again, a network analyzer is an indispensable tool for measuring a power supply's output impedance versus frequency, and optimizing the output power section of the power supply.

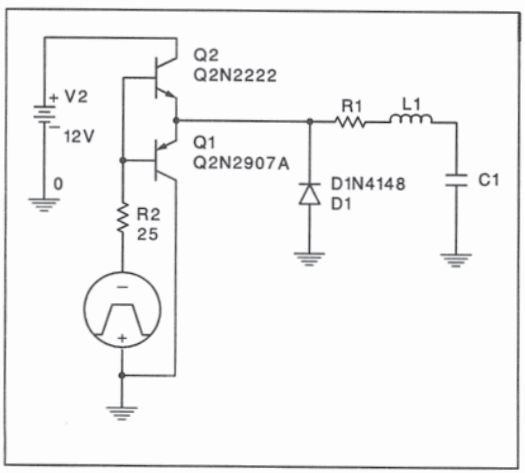

Figure 18. Schematic of RLC circuit

Gate Drive Circuits

The finite and generally parasitic impedance of any physical component and connection causes the MOSFET gate circuitry to look like a series resistor-inductor-capacitance (RLC) circuit back to the driver IC output. This is a reasonable approximation, although a simplification of the true circuit which could include the parasitic effects of high voltage section and contribution of load current to MOSFET source inductance (etc.). But a simple series RLC circuit will be used for this general purpose example.

A bipolar IC's totem-pole driver output can be simulated by as an NPN-PNP pair driven from a switched voltage source as shown in Figure 18. Thirty nanosecond rise and fall times were used as a standard value for slew rates on the base drives. The series RLC circuit is presented as the load, and a clamping diode to keep the output from going far below ground is also incorporated. Generic components from Microsym's PSPICE evaluation library were used. The two intervals of most interest are turn-off at the driver output and turn-on of the MOSFET gate. Turn-off will be examined first with various values of R, L and C, and the effects these have on gate turn-on will be presented.

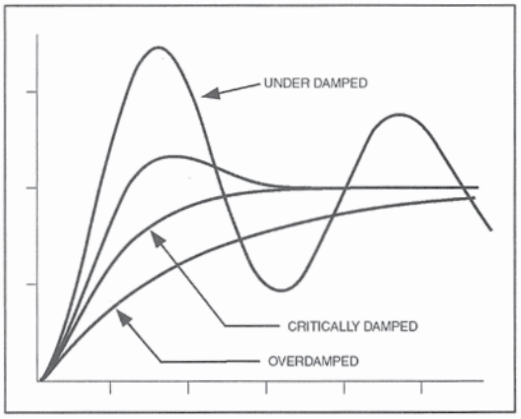

Figure 19. Response for four damping conditions

General equations for the series RLC circuit :

The resonant frequency of the LC tank is :

1. Fr = 1 / [2 * Pi * SQRT(L * C)]

Zn, the load's LC resonant "tank" natural impedance is described by :

2. Zn = SQRT (L / C)

The general circuit response can be expressed as:

3. Overdamped when C > (4 * L) / R ^2

4. Critically damped when C = (4 * L) / R ^2

5. Underdamped when C < (4 * L) / R ^2

Which can also be expressed in terms of the ratio of the resistor's to tank's impedances:

3A. Overdamped when R > 2 * Zn

3B. Critically damped when R = 2 * Zn

3C. Underdamped when R < 2 * Zn

Note that the circuit response will reach it's final value in the shortest time when R = Zn. Under this condition, the network will overshoot the final value, once, with no undershoot before converging on the final value. This criteria will be used as the starting point for the following several examples.

The circuit schematic is shown along with the PSPICE PROBE output waveforms for reference. Two waveforms are shown in the upper display; the voltage waveform across the load capacitor in the top, and then gate current. In the lower display, shown are the IC's totem pole output voltage at 1V/division, the totem pole output current and also the clamp diode current at 100mA/division. NOTE : the vertical scale legends are from -25 to +25, which corresponds to -25V to +25V for the voltage waveform, and -2.5A to + 2.5A for the current waveform. All currents are simply plotted at 10X the actual simulated value as indicated in the lower left of each plot.

Example Circuit #1: R=3, L=10µH, C=1µF

Circuit values : For a starting point, values of 3 ohms, 10 nanohenries and 1 nanofarad were used for the RLC load in the reference simulation. This represents a fairly tight layout and near "ideal" conditions between the series resistor, capacitor (load) and the IC output. As it turns out with these values, Zn equals 3.1 ohms which is nearly identical to the 3 ohm series resistance, and the statement mentioned previously about this condition applies. It's a reasonable approximation to have a 1nF test load capacitor physically placed very close to the IC output with the diode placed directly across the IC's ground and output pins for this evaluation. Note the combined 3 ohm resistance and 10 nH inductance can be either considered as individual "passive" components, physically in series with an "ideal" 1nF capacitor, or it could represent the equivalent series impedance (ESL) and resistance (ESR) of the load capacitor at the test conditions.

The first set of plots (Figure 20) shows a slight - but not severe undershoot below ground of the totem-pole voltage due to this load. Current in the diode is essentially zero, as the amplitude of the voltage undershoot is not enough to strongly forward bias the diode on. Note that there is a minor amount of ringing indicating that the circuit is below, but not very far from the critical damping condition where R equals 2 * L. In this example, the RLC load does not cause the totem-pole output

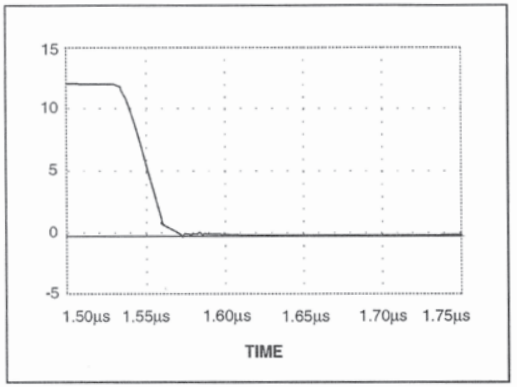

Figure 20. Example #1 : R=3, L=10nH, C=1nF

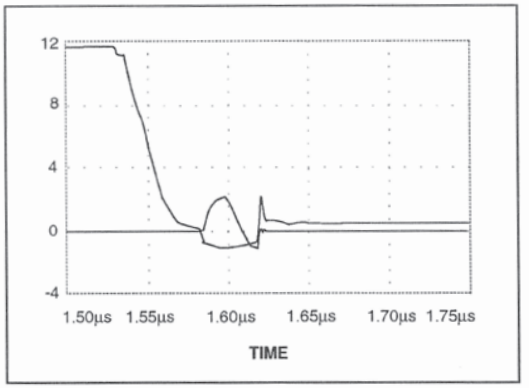

Figure 21. Example #2 : R=3, L=100nH, C=1nF

voltage to resonate far below ground or much current to flow in the clamp diode. The stored energy and inductor's function to maintain current flow does not result in a problem in this example.

Example #2 : The real world PC layout - add series inductance

Examine what happens to this circuit when the load capacitor is placed a few inches away form the IC, adding inductance to the circuit This load is fairly representative of what happens in a physical PCB layout where the power MOSFET is inches away from the IC pin. Use an approximation of 100 nH for this example, which corresponds to just a "few" inches of total path length from the IC output to the MOSFET gate and back. Other sources of potential series inductance found in a typical application are the power MOSFET package bonding wires and leads, current sense resistor series inductance (for current mode control) PCB "feedthru's" and "vias", and interconnection inductance.

R=3, L=100µH, C=1µf

Under these test conditions, it is demonstrated that the totem-pole output rings below ground, and continues to a peak of approximately -1V. Note that the current in the diode goes positive during this period with a peak value above +200 mA. (Remember the x10 factor involved for the current measurement displayed). Looking at the circuit from the output totem-pole transistor; the voltage is negative and the current is positive. Had the diode NOT been in the circuit, current would have to flow entirely from the circuit ground up through the lower totem-pole transistor - in this case from the collector to the emitter of a PNP transistor. This flow is opposite to convention, and the resultant totem-pole output voltage due to any finite resistance or junction here is negative. A negative voltage and positive current is seen by the IC's totem-pole transistor - but can it handle that?.

This condition is the cause of an overwhelming majority of the "noise" related problems with bipolar integrated circuit driver transistors : negative output voltage and positive output current. Within the IC, right on the die, current flows from the substrate (ground) through all available paths (junctions) to the output in order to fulfill the requirements of the external load, the resonant tank. The current is forced through the numerous and otherwise unrelated other PN junctions within the IC. Rebiased are current mirrors, amplifiers and logic gates from other functional blocks within the IC. The result is noise gets injected into many high impedance nodes which can cause "slaving" or triggering of the various building blocks due to their high speed and sensitivity.

Check the RLC circuit damping :

Zn = SQRT(L / C) = SQRT (100nH/1nF) = 10.00 ohms

R << 2 * Zn
(3 vs 20 ; it's considerably underdamped)

Example #3 : Increase the resistance

The practical method to reduce the ringing and undershoot in this example is to increase the series circuit resistance, as L and C are determined by layout and MOSFET size. Changing the resistor's value to ten ohms will swamp-out the overshoot and prevent reverse current in the diode, and more importantly, the IC output transistor. This is shown in example #3. Note, however, that the peak gate current is reduced, and gate voltage rise time has increased. Thus, the penalties paid for reducing undershoot are increasing MOSFET turn-on delay and switching transition power loss in the main MOSFET switch.

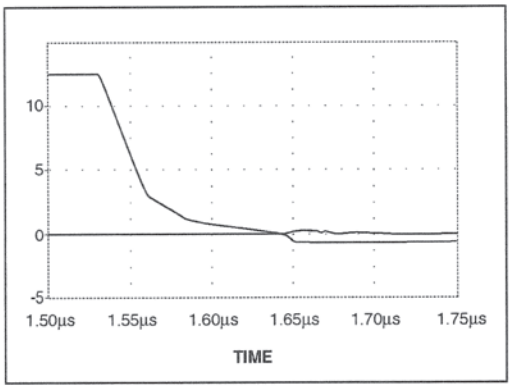

Figure 22. Example #3 : R=10, L=100nH, C=1nF

Example #4 : Alternative damping : add capacitance instead of resistance.

The previous example (#3) added resistance to increase the damping but another option was to increase the load capacitance instead. Since it is in the denominator of the tank impedance formula, adding capacitance will lower Zn, hence increasing the circuit damping. This will come at the expense of measurably increasing the gate drive voltage

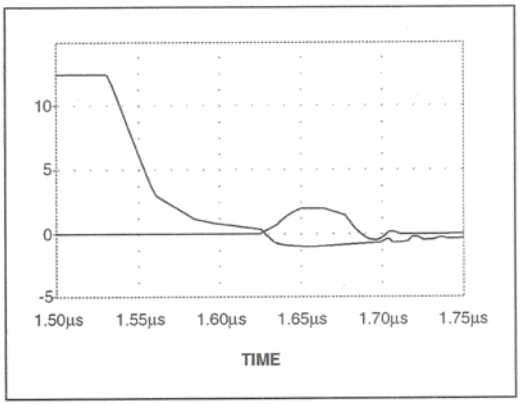

Figure 23. Example #4 : R=3, L=100nH, C=4.7nF

waveform rise and fall times, thus worsening the power MOSFET's switching losses. In most high frequency applications, this is not advisable, but is shown for reference where slower transitions are acceptable, or desirable. This might be incorporated in soft switching, zero voltage switching, sensitive EMI/RFI or low frequency power conversion applications where "razor" sharp transitions are unnecessary. Observe the slight amount of overshoot and diode current in this example where the series capacitance is raised form 1 nF to 4.7nF.

R= 3, L=100nH, C=4.7nF, Zn = 4.6

Check the damping : R < 2 * Zn
(3 vs 4.6 - still underdamped)

The results are also applicable to circuits incorporating large power MOSFETs with high gate capacitance and gate total charge (Qg).

Example #5 : Increasing the peak gate drive current

In an attempt to speed up turn-on and turn-off of the main switch and reduce switching losses, the series (gate) resistance value will be reduced from three ohms to one ohm and analyzed. Now, the resistor is one-fourth the value of the tank impedance, and the circuit is considerably underdamped as shown by the waveforms in Figure 24.

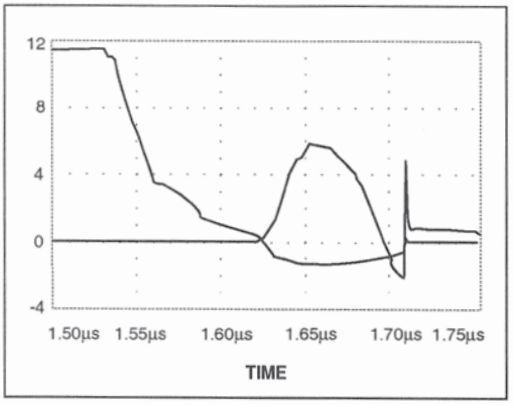

Figure 24. Example #5 : R=1 , L=100nH, C=1nF

In comparison to the previous example using three ohms, the drive voltage and current waveforms change noticeably. The voltage overshoots the supply rails on both edges, in addition to the gate current. The peak current is higher (1.5A vs. 1.2A) along with the peak over and undershoot values exceeding 500 mA. Note that the clamp diode current has increased from approximately 200 mA to 600mA following turn-off. This current causes the diode's forward voltage drop to increase to approximately 1.5V as well.

Note the parallel arrangement of the external clamp diode and the PWM or Driver IC's internal substrate diode as shown in figure 25. In this example, the external 1N4148 diode's forward voltage drop is sufficiently high enough to cause the IC's internal substrate diode to conduct. Notice the polarity of the voltage and current on the output pin. Voltage is negative and current is positive with respect to the terminal ! This condition indicates that current must flow in from the ground connection of the IC and out the output terminal pin connection. Yet the lower totempole transistor is reverse biased, and current is opposite of that normally found - it must flow from the collector to the emitter, which doesn't really occur in the transistor. Instead, this current, fueled by the circuit inductance flows from ground through the IC along any low impedance internal path back to the output pin. And the paths available to facilitate this start at any of the IC's substrate junctions, causing severe noise problems within the IC. This current causes perturbations of numerous internal bias currents and node voltages, and can falsely trip high speed circuitry such as the oscillator and protection latches.

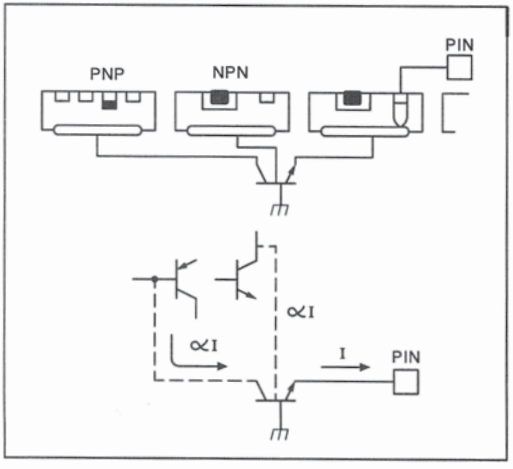

Figure 25. Internal IC substrate diode

At the 600mA peak clamp diode current indicated, the forward voltage drop of the external device must be lower than the internal PN junction drop within the IC or the IC will conduct the current - not the external clamp diode. What makes matters worse is that the IC is generally running at a higher junction temperature because of internal heating caused by the numerous circuits in operation, drawing supply power. Therefore, because of the negative temperature coefficient of a PN junction,

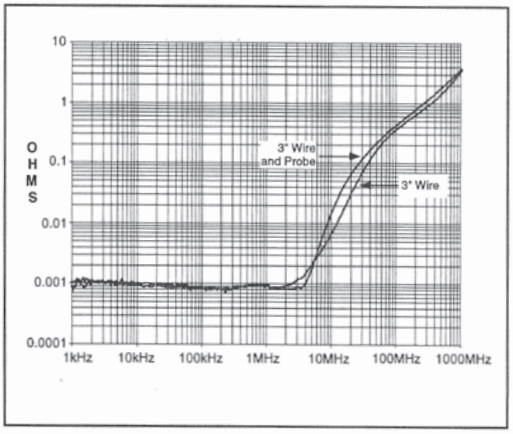

Figure 26. Impedance vs Frequency for a current probe

the IC's internal voltage drop would be considerably lower than the external clamp diode at the same ambient temperature. So, the external diode MUST have a significantly lower forward voltage drop, mandating a Schottky diode. ***Most 3 amp, 1N5820 Schottky types - or equivalent, will clamp properly.*** Use those with less than a 0.3V forward voltage specification at 1 amp at 25 degrees C. Under less demanding conditions with little reverse current flowing, it is possible to use a 1A, 1N5817 or equivalent Schottky diode for the clamp, but check the forward voltage drop specifications carefully. This rating varies greatly with different manufacturers and must be lower than the IC's internal substrate diode drop at the IC's operating junction temperature. ***NEVER use a 1N4148 signal diode or 1N4001 type general purpose rectifier for this application as they will NOT prevent current from flowing through the IC in most applications, and do little to nothing for protection.*** Their forward voltage drop is too high, and the reverse recovery characteristics of the 1N4001 are too slow for high frequency power conversion.

More on the Schottky clamp diode(s) :Don't bother trying to measure the current in the clamp diode with a standard current probe and amplifier as one might normally measure current. During these fast turn-off transitions, the added series inductance of the small wire loop used to measure current with the clip-on probe in the circuit will nearly ALWAYS guarantee that no current flows through the diode. Worse, is that this situation falsely supports any efforts prove that diode is required. But according to the scope measurements, the diode does little-to-nothing and never conducts current - due to the series inductance of the measurement technique.

Upper totem pole Schottky diode clamps : The same conditions as just stated apply for the diode to the ICs upper totempole transistor. Typical resulting problems result such as increased delay times and inability to quickly turn off during the overshooting periods and immediately afterwards.

Example #6 : Perfecting the gate drive circuitry by increasing the gate resistance

Raising the series resistance to equal the tank impedance such that the shortest transition times with minimal overshoot and undershoot is about the best compromise possible. This tradeoff results in the highest gate drive current and fastest gate transitions with minimal clamp diode expense. The penalty, however, is that a slight amount of undershoot at turn-off is to be expected, and a Schottky clamp diode is still required. Since the LC tank impedance is 4.6 ohms in this example, increase the series resistance to approximately 5 ohms (5.1 ohms used) to achieve the desired damping.

R=5, L=100nH, C=4.7nF

Changing the resistance to 5 ohms reduces the large negative voltage and positive current problematic situation. It doesn't eliminate current from flowing in the diode, however does help to minimize the effects.

Eliminating the Schottky diodes ???

Sine the present tank impedance is around 5 ohms, and the series resistance needs to be twice this value to completely eliminate the negative transitions, or ten ohms.

R = 10, L=100nH, C=4.7nF

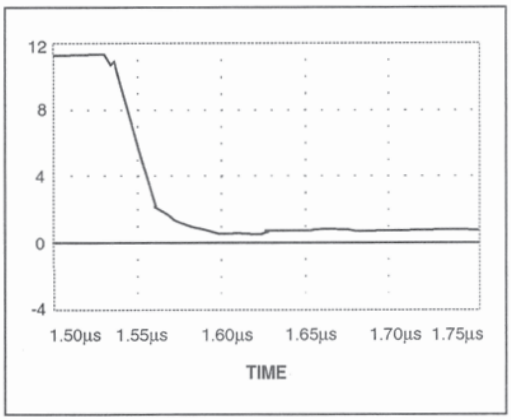

Figure 27. Improved performance ; R = 10, L=100nH, C=4.7nF

The simulation clearly demonstrates that with a properly designed damping, no undershoot below ground is present and no diode current flows. The IC's driver output always remains above zero during turn-off with no ringing. Unfortunately, this was achieved at the penalty of slower rising and falling gate voltage transitions, and resultant slightly higher power dissipation in the main switch.

Practical Circuit Layout Recommendations:

To obtain optimal gate drive performance in a high frequency power supply design, keep the interconnection *inductance as low as possible*. To achieve this, limit the distance between the IC driver output and power MOSFET to one or two inches (at most) to minimize series inductance. Ideally, the best results are obtained by locating a well bypassed and Schottky diode clamped gate driver IC right at the power MOSFET gate and source leads or connections. Use a low impedance command signal from the PWM control circuit to the driver IC to minimize interference from the associated high voltage, high power circuit parasitic elements and radiated emissions. Avoid high impedance interfaces. Furthermore, twisted pair wires or coaxial cable will yield the highest gate drive command signal integrity over long distances, although this may not be feasible in manufacturing. Running one trace for the command signal from the PWM to the driver IC on the top layer of the PC board with a return path directly under this trace is the next best alternative. Make sure that no other circuitry is connected to or tapped from these traces as that will introduce circuit parasitics, unintended current paths and signal distortion.

OSCILLOSCOPE MEASUREMENTS : ALLIGATOR CLIPS = PROBLEMS

WYSIN-WYG : What You See Is NOT What You've (really) Got"

The only "ground" reference for all measurements is physically and electrically at the GND, SGND and/or PGND pins of the control IC, as previously described. In practice, all oscilloscope waveforms measurements must have a good connection to this point in the circuit without adding any parasitic effects. Most commonly, the connection made between the oscilloscope's

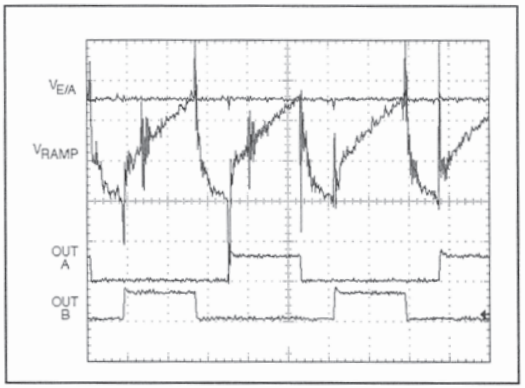

Figure 28. Oscilloscope probe "pick-up" noise

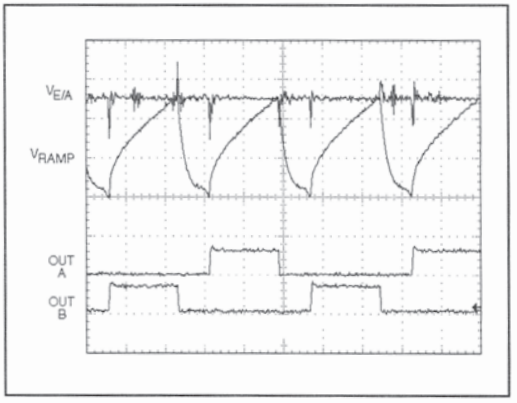

Figure 29. Reduced noise measurement using short probe ground lead

"ground" and the circuit "ground" is made using the standard oscilloscope ground lead, which is a small length of wire with an alligator clip attached. Although convenient, this single connection is usually responsible for delivering the overall poor quality of waveforms being viewed. Scope "pick-up" noise is the term most commonly used to describe the large spikes visible on all measured waveforms. These spikes are generally in perfect synchronization with turn-on and turn-off of the main power switch(es), but there are other sources of noise as well. In some cases, the amplitude of these spikes greatly exceeds the amplitude of any signal under observation or interrogation, which presents as much, if not more of a problem to the control IC as it does to the scope user. But the biggest question is whether or not the visible noise

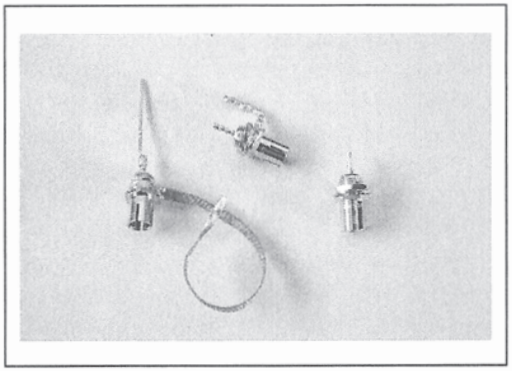

Figure 30. Photo of scope probe tip adapters Tektronix Part # 131-0258-00

is truly just "pick-up" noise to the high impedance scope probe - or is it real noise on the "ground" and everywhere in the circuit?

One of the best techniques in minimizing the scope probe's "pick-up" noise is to eliminate the use of its "ground" lead entirely. Making this "ground" connection as short as possible will result in the highest signal integrity and ability to decipher what is "real" from what is not. Simply switching to a shorter ground lead won't work as well as getting rid of the ground lead completely. One of the more common tools available to facilitate improved scope measurements is a " chassis scope probe tip adapter socket." Although designed for more permanent type installations of scope probes, these are easily modified for temporary use in control circuits and power supplies. A small length (2 inches or less) of ordinary solid "bus bar" or bare wire equivalent to an AWG 18 (approximate) can be wound around the socket adapter, soldered, and bent to work as the ground connection. This lead, and the signal lead from the center of the socket should be soldered directly to the printed circuit board at the closest possible location to the point of measurement needed. Other adaptations of this type of scope probe adapter, including a "homebrew" or Do-It-Yourself (DIY) coil of wire wrapped around the scope's ground connection "sleeve" can give similar performance.

Both the scope probe's ground wire lead and probe's plastic "tip" must be removed before insertion into the adapter, prior to use. If a short connection distance is not possible in the circuit layout, then a longer ground wire can be used, and a small piece of similar wire can be added to complete the "tip" connection. If the probe needs to be moved for observation of several points of interest, a flexible or stranded wire should be used for the ground connection from the adapter to the circuit board. One hint is to use a piece of "solder wick" or braided fine copper wire to make a low impedance path. Note, however, that as the length of the wire increases, this technique becomes more similar to the original method of using the supplied scope ground lead and alligator clip, and should be avoided. Keep the interface and wire lengths as short as physically possible for optimal results. A photo of the adapter and several possible arrangements is included.

"Differential" Scope Measurements

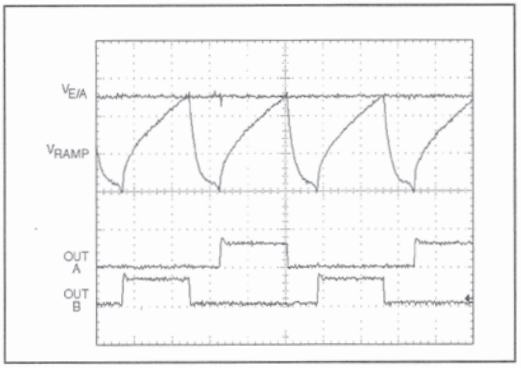

Figure 31. Scope tip adapter measurements

Another popular technique to reduce the amount of oscilloscope measurement noise is frequently called "differential" mode. This is where two scope probes are used to attempt to measure one signal differentially. The "positive" tip of one probe measures the signal to be monitored and it's ground lead is referenced to ground, as normal. The other probe's ground lead is also connected to the first probe's ground lead at the alligator clip. This second probe's tip, however, is frequently connected to ground as close as possible to the circuit ground nearest the first probe's tip. In theory, the second probe measures the ground noise between where the alligator ground clips are located, and the ground

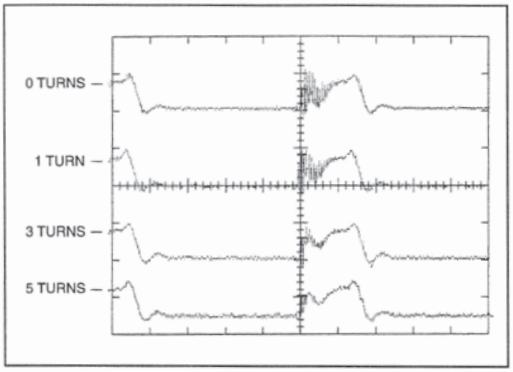

Figure 32. "Home-brew" common mode scope probe toroidal filter

where the measurement is being made. In theory, one can subtract this ground-to-ground noise measurement from the first scope probe's measurement and eliminate the noise on the ground plane or layout. On older (analog) models of oscilloscopes, this is performed by inverting the second probe's display and adding it to the measurement of the first probe. With newer, Digital Sampling Oscilloscopes, or DSO's, this is similarly done by using the internal math functions available on-screen. In either case, the slight, if any improvement gained with this technique is minimal. In many instances, the end result is just as bad as the original (first probe's) measurement, and can even be worse in some. This is most frequently caused by the high power radiated noise being received and measured differently (instead of differentially) across each of the two probe's ground leads. Therefore, instead of canceling perfectly, the slightly different signals wind up adding, and add more noise to the original signal than subtract, as shown in the photo attached.

One of the most unique attempts to reduce common mode noise in a differential probe measurement technique is to wrap the scope lead wires through a toroid of high permeability material. Similar to making a coupled inductor, several turns of the scope probe connection wires between the probe tips and amplifier inputs are wound side-by-side to replicate a common-mode choke for the probes. As shown in the traces of Figure 32, the effects varying from no choke (top trace) through 1,3 and 5 turns of the leads around a toroid demonstrate the measured improvements in signal integrity.

The last resort is to use the bandwidth limiting, sampling and smoothing functions of the oscilloscope, but while these help to clean up the displayed waveforms, they ***do nothing*** to help the IC perform its intended functions.

TOOLS OF THE TRADE

Other Uses for Network Analyzers : "Low" Impedance vs Frequency Measurements

The Network Analyzer is a useful tools to accurately measure the impedance versus frequency characteristics for a variety of electrical components including: capacitors, inductors and transformers. It can also be used to quantify the parasitics of low impedance circuits such as a printed circuit board or wiring harness. However, the first and most important step to obtaining accurate low impedance measurements is to "null-out" the fixture used to measure the Device Under Test (DUT). The procedure and equations are shown below along with a brief description and examples in a spreadsheet output form. When performed correctly, accurate measurements into the milliohm to tens of milliohm range are achievable.

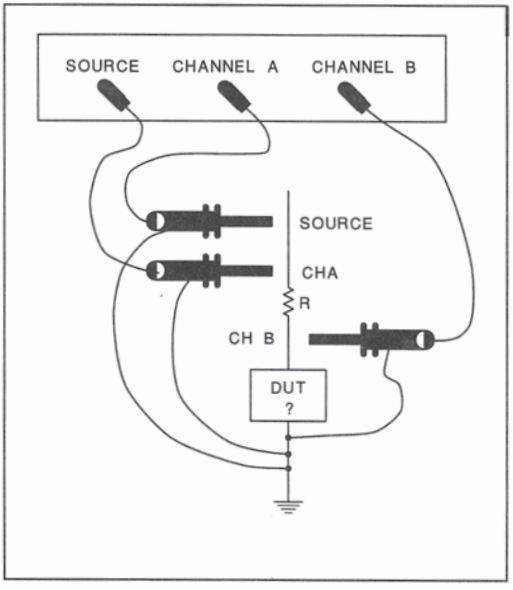

Figure 33. Electrical circuit and probe diagram

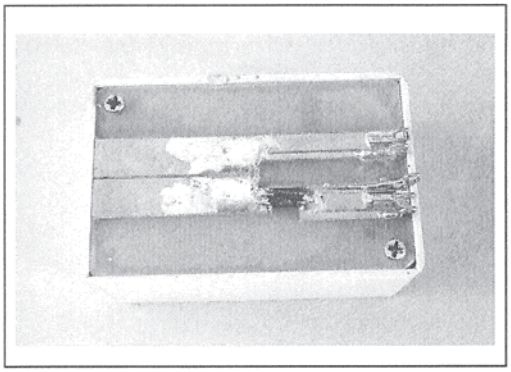

Figure 34. Photo of the fixture used

The electrical model for the test circuit is shown in Figure 33. The Network analyzer's three probe connections, the 50 ohm reference resistor, DUT and fixture are included. The fixture should be as small as possible, and a cut-up section of printed circuit board with short soldered leads as shown in Figure 34 for connecting the probes is suitable. Note that even though the lead resistance of the wires used to apply the signal might be as high, or higher, than the fixture resistance, they can be ignored for this analysis. This is because all measurements are taken on the fixture with respect to each other, so any losses or effects of the signal lead impedance have no bearing on the relative measurements. The same is true for the signal source amplitude, although a constant and precise source is available from most network analyzers anyway.

Step 1. Measure the exact resistance of the 50 ohm reference resistor, Rref.

Step 2. Connect the circuit as shown in Figure A1. Use a piece of AWG 18 or equivalent wire as a short circuit in the fixture's DUT location.

Step 3. Z(null) : Measure the Impedance vs. Frequency for the short circuited DUT fixture assembly to be used to "null-out" the fixture impedance. Save the magnitude and phase measurements versus frequency of Probes B and A individually, or the ratio of these (B/A in decibels (dB) and phase) in a spreadsheet format.

Step 4. Arrange the data in columns of a spreadsheet as :

Column A : Frequency (in Hz),

Column B : Gain in dB of the measurements taken of Probe B divided by Probe A; (B/A)

Column C : Phase Angle in degrees of the difference between the measurements of Probe B and Probe A; (Phase B/A).

Step 5: Two more columns are added to convert the polar coordinates of the previous magnitude (B/A) and phase (B/A) measurements into rectangular coordinates. This is required to be able to subtract these "null" measurements from the actual DUT measurements to eliminate the fixture impedance contribution.

To convert from polar coordinates to rectangular form, the following equations are used. Store the X and Y data into Columns D and E respectively.

Column D : X = [10 ^ ({MAG B/A in dB} / 20)] * COS [{ Pi/180 } * Phase B/A (in degrees)]

Column E : Y = [10 ^ ({MAG B/A in dB} / 20)] * SIN [{ Pi/180 } * Phase B/A (in degrees)]

Step 6 : Remove the short circuit from the DUT location and install the first component (DUT#1) to be evaluated in the DUT fixture. Do NOT move the connections or locations of the three probes or the previous fixture nulling data will no longer apply. If the probes must be removed to facilitate soldering of the DUT onto the fixture, make sure to reconnect the probes exactly as and where they were prior to their removal.

Step 7 : Measure the DUT#1 impedance and phase versus frequency and store the data. Next, move the two columns of data containing Magnitude of B/A (in dB) and Phase B/A (in degrees) into the previous spreadsheet into columns F and G respectively.

Step 8 : Repeat Step 5. to translate the DUT's polar coordinates to rectangular. Use (copy) the same equations from Columns D and E into Columns H and I of the spreadsheet, respectively. Verify that the correct Cells are being used in the equations for Magnitude and Phase. Once completed, the following information should be present in the spreadsheet.

Column F : Magnitude (B/A) DUT#1
Column G : Phase (B/A) DUT#1
Column H : X coordinate of DUT#1
Column I : Y Coordinate of DUT#1

Step 9 : To obtain the exact DUT impedance versus frequency characteristics, the next step is to subtract the fixture "null" X and Y rectangular coordinates from those of the DUT. Use Column J of the spreadsheet to subtract the numbers listed in Column D (x(null)) from those in Column H (DUT#1(x). The result (Column J) is the net X coordinate for DUT#1, with the fixture impedance nulled out.

Column J : X coordinate DUT#1 (net) = Column H - Column D

Step 10 : Next, repeat the procedure of Step 9 using Column K to obtain the net Y coordinate for DUT#1 by subtracting the data of Column E (y {fixture(null)}) from Column "I" (y {DUT#1}).

Column K : Y coordinate DUT#1 (net) = Column "I" - Column E

Step 11 : Once the X and Y coordinate information has been obtained for the DUT, the net magnitude and phase can be calculated. The magnitude of this vector is equal to the square-root of the "sum of the squares" of the X and Y rectangular coordinates. Column L will be used to calculate this from the data housed in Columns J and K.

Magnitude = SQRT (x(net)^2 + y(net)^2)

Column L : Polar magnitude of DUT#1

Step 12 : The polar angle of DUT#1 can be calculated using the arc-tangent (ATN) function of the spreadsheet mathematics functions. Specifically, the vector angle is the arctangent of the Y coordinates divided by the X coordinates. One feature of EXCEL is the ATAN2 function, where the x and y coordinates can directly be put into the equation solving for the arctangent. Note that most spreadsheet functions operate using radians as opposed to degrees, therefore, a conversion factor (180/Pi()) is required to output the phase in degrees. An example is shown below.

Phase (degrees) = 180 / Pi() * ATAN2 [x coord , y coord]

Column 13 : Phase of DUT#1 in degrees

Step 12 : Converting the nulled, relative characteristics of DUT#1 into absolute impedance is the final step in the spreadsheet. So far, all data has represented the ratio of the DUT impedance to that of the 50 ohm reference resistor, and therefore must be converted into an absolute impedance. This conversion is performed using Column N to multiply the DUT impedance magnitude (Column L) by that of the reference resistor value, in ohms. [The equations for this derivation are listed in the Appendix of this section.]

Z(DUT) = R(ref) * [Magnitude (DUT) / (1 - Magnitude(DUT))]

Column N : 50.0 * [Value of Column L / (1 - Value of Column L)]

Step 13 : The equations for one row (across) of the spreadsheet, by columns, has been presented. To complete the chart for all values of impedance versus frequency, the equations must be copied (down) from the top of each Column to the last cell in each column. This applies to all columns except those containing the measured readings, which are Columns A,B,C,F and G.

Frequency	NUL(B/A)	NUL phase	X NUL	Y NUL
101.4E+0	-64.3E+0	-128.9E-3	612.5E-6	-1.4E-6
1.0E+3	-63.3E+0	12.3E+0	670.4E-6	145.7E-6
10.1E+3	-61.9E+0	-23.9E+0	735.1E-6	-326.4E-6
102.1E+3	-66.4E+0	49.6E+0	311.7E-6	366.7E-6
Frequency	DUT (B/A)	DUT phase	X DUT	Y DUT
101.4E+0	-8.6E-3	-4.0E-3	1.0E+0	-70.2E-6
1.0E+3	-566.8E-3	-284.7E-3	1.0E+0	-5.0E-3
10.1E+3	-10.2E+0	-1.9E+0	999.4E-3	-33.5E-3
102.1E+3	-30.0E+0	-18.5E+0	948.3E-3	-317.4E-3
Frequency	X DUT NULD	Y DUT NULD	DUT MagN	DUT AngN
101.4E+0	999.4E-3	-68.8E-6	999.4E-3	-3.9E-3
1.0E+3	999.3E-3	-5.1E-3	999.3E-3	-293.3E-3
10.1E+3	998.7E-3	-33.2E-3	999.3E-3	-1.9E+0
102.1E+3	948.0E-3	-317.7E-3	999.8E-3	-18.5E+0

Figure 35. Excel spreadsheet column data

Step 14 : The DUT's "true" impedance (and phase if desired) versus frequency characteristic have been calculated in Step 13 and can now be plotted. For conversion to most spreadsheet based graphs, it is recommended to enter the chart's "x" axis data in the first column, then the "y" axis data in the second. If more than one DUT are to be charted on the same graph, data should follow starting with the third column and continued as needed. An example of the data and charts developed for this example is given below for clarity.

POWER FACTOR CORRECTION APPLICATIONS

Total Harmonic Distortion (THD) Measurements - Fact or Fiction ?

Indispensable for power factor applications, precision equipment such as the VOLTEC PM 1200 and PM3000 analyzers provide accurate measurements of the Total Harmonic Distortion (THD) of line current and details of individual harmonics. However, these instruments compare the current drawn by the unit under test to a pure, reference sine wave to determine the individual harmonic content. The output of this equipment therefore generates the *absolute* harmonic distortion and individual harmonics as compared to an ideal sine wave.

While this is important information, however, the problem is that it does NOT provide the *relative* relationship of the current drawn to the actual line voltage supplied. Specifically, it does NOT take into account any noise or distortion of the AC input source's voltage waveform. Erroneous measurement, both good and bad - are the net result. Days can be spent trying to "tune-in" a power factor corrector to achieve a lower harmonic distortion of the current waveform than the input voltage source will possibly permit, due to its own distortion. Note, that if a lower THD current waveform than the input *voltage* waveform's THD is achieved, it is most likely that the unit will have *worse* THD than ideal with a "clean" input source. This is because the unit was deliberately "tuned" to draw current out of shape or phase with the distorted input voltage waveform.

Shown in Figure 36 are the results of two THD measurement examples. The first incorporates a UC3852 power factor correction (boost) stage converting the AC input to a 385 V DC output loaded by a resistor. The second example is just a resistor placed across the AC line - no rectifiers or electronics involved. Note that the PFC stage measured 6.81% THD, yet a resistive load alone across the AC line recorded 5.68% distortion. This may at first indicate that the relative difference between the power factor corrector and a "pure" resistor load is only 1.16%, however the phase has a considerable effect on the exact difference. The real difference could be much higher if these two were completely out of phase with each other, which is also a possibility with a "misaligned" PFC Technique. But it will be much less in this case since the phase of the third harmonics are closer. The point worth noting here is that the voltage THD must be nulled out first before any quantitative current THD information is valid.

	UC3852 PFC	"Pure" Resistor
Watts	51.378	60.211
V*A	51.63	60.224
PF	***0.99504***	***0.99978***
Athd	***6.81%***	***5.65%***
AH3	6.57% / -55	5.12% / -116
AH5	1.79% / -92	2.38% / -141
AH7	0.07% / -34	0.45% / -153
AH9	0.02% / -163	0.09% / -204
AH11	0.35% / -192	0.08% / -218
Vthd	***5.64%***	***5.68%***
VH3	5.14% / -112	5.12% / -116
VH5	2.30% / -138	2.42% / -141
VH7	0.34% / -123	0.44% / -154
VH9	0.001% / -66	0.10% / 157
VH11	0.001% / -192	0.10% / 127
A-VH3	5.69% / 90	0% / 0
A-VH5	1.65% / 90	0.03% / 90
A-VH7	0.77% / 90	0.005% / -90
A-VH9	0.03% / -90	0.01% / 90
A-VH11	0.35% / -90	0.003% / -90

Figure 36. THD measurements of resistor and PFC stage

The more common causes of voltage waveform distortion are industrial phase-controlled (SCR/TRIAC) high power equipment, Heating Ventilating and Air Conditioning (HVAC), lighting ballasts and other, non-corrected loads including computers. While applicable to all line voltage including household 120VAC mains this is especially true for higher input voltages, for example, 277VAC which is derived from one phase of the 480 VAC 3 phase power in the United States. One advantage of using 277 VAC line is that it will provide the necessary "high line" for universal input testing (264VAC) without the need for a step-up transformer. Other potential sources of voltage distortion are when an isolation transformer or "variac" (variable transformer) is used in series with the AC input supply "mains". The more frequent problems encountered are some phase shift of the current waveform due to added series inductance and "flat topping" or distortion near the peak of the voltage waveform at higher currents, especially in "step-up" applications due to the "IR" drops.

In order to more accurately measure the "***relative***" current harmonic distortion of the unit, the input voltage waveform must first be analyzed. Fortunately, this is easily performed by most power factor instruments by monitoring the voltage waveform distortion by its individual harmonics amplitudes and phases, just as is done to monitor the current. First, it is advisable to load the line with a suitable "pure" resistor, approximately equal to the input power to be drawn by the actual unit to be tested. This loading will best simulate the effects placed upon the AC source and any series impedances of the actual load. Don't measure the voltage distortion terms at no load and apply them to a several hundred watt converter as they are probably not applicable.

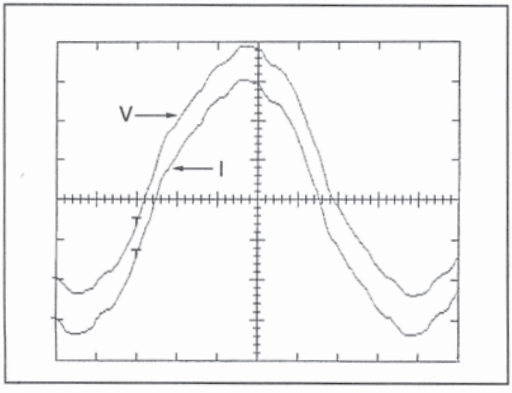

Figure 37. Photo of line voltage and current for a resistor

Measure the input voltage amplitude and phase of the fundamental and each odd harmonic from the third through the fifteenth. One choice to be made is whether to measure these harmonics in absolute amplitudes, or as a percentage of the fundamental amplitude. Either can be used to "null-out" the effects of the voltage distortion on the power factor correction, but having the data as a percentage of the fundamental is generally easier to manipulate in the spreadsheet equation, so use the percentage option. This is often selectable as a option in the user programming modes. Another feature worth using is the option to output only the "odd" (ex 3,5,7..) harmonics, also advisable.

Once the voltage distortion data has been obtained, then the unit can be tested as normal. For the current measurements, similar information to the previous voltage distortion measurements needs to be obtained. Measure and record the input current amplitudes and phases of the fundamental and each odd harmonic from the third through the fifteenth as a percentage of the fundamental amplitude. Similar to the procedure described elsewhere in this presentation, a spreadsheet program is incorporated to convert from the polar to rectangular coordinates, then subtraction of the voltage distortion from the current distortion (by individual harmonics), then converted back to polar data. A summary of the results is shown below including general equations used.

I(thd) =SQRT (IFun^2 + IH3^2 + ... IHn^2)

[if the amplitudes of each current harmonic are used]

I(thd)= SQRT (I Fund^2 * (1 + IH3(%)^2 + ... IHn(%)^2))

[if percentages of fundamental current for each harmonic amplitude are used]

Vrms = SQRT (V Fund^2 * (1 + VH3(%)^2 + ... VHn(%)^2))

[if percentages of fundamental voltage for each harmonic amplitude are used]

To null out the measurements, subtract the percentage of fundamental voltage distortion for a given harmonic from the fundamental current percentage of that harmonic. For example, review this equation using the ideal condition of a resistor across a line with a specific amount of voltage THD. If both the voltage and current third harmonic percentages of their respective fundamental were 5% and in phase with each other, the net result would be zero, or no net - or relative distortion. For another example, let these two measurements be 180 degrees out of phase with each other. After converting each to rectangular coordinates and subtracting the voltage from the current, and converting back into polar, the result would be a doubling, or 10% distortion of the third harmonic. Use the data up to the 15th harmonic to obtain the highest accuracy, however little effect is generally seen above the 7th harmonic due to the small amplitudes in comparison.

Before the Breadboard : "Know this or suffer"

Schematics : Probably the best place to start the control circuit section of the PCB layout is from a well organized circuit schematic. Nearly all PC layout designs begin at the control IC and gradually work their way out to the associated components, so it's important to get off to a good start. First, the IC should be drawn on the schematic as it would physically appear on the PC board layout when viewed from the top with Pin 1 in the upper left hand corner. Using a 16 pin DIL package for reference, then pin 8 will be in the lower left hand corner, pin 9 in the lower right, and pin 16 in the upper right hand corner.

All functions of, and connections to the IC should enter and exit the schematic at their respective pin's physical location. If the IC's error amplifier inverting input is at pin 8 and the amplifier output is at pin 18, for example, DON'T draw the two pins next to each other on the schematic on the same side. Doing this might simplify drawing of the compensation network onto the schematic - which goes between the two pins, but this will generally make the PCB layout far more difficult to envision. Here's why. Physically having to draw the line connecting the component going to pin 16 (upper right) with the other end of the same component which goes to pin 8 (lower left) is less convenient than drawing them right next to each other. However, that is exactly how the PCB trace must be run to connect a component on opposite corners of the IC - inconveniently. But there are exceptions, where traces can be run between other pins of the IC to get from side to side or by using "vias" or "feed-thru's" to make the connections. Note, that nearly every time that the schematic connection has to run across or through the centerline of the IC on the schematic, then so too does the trace. In general, these connections will be longer than others, something to factor-in for high frequency and high impedance layouts.

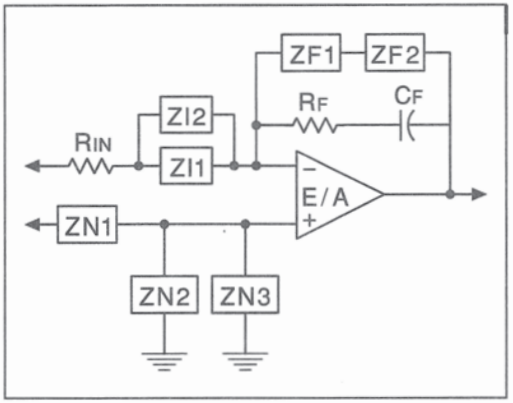

Figure 38. Additional component locations in initial design

Start the schematic and layout with the bypass capacitors. These should be placed as close as possible to the IC pins, and sometimes this might not be optimal due to the pins assigned. If there is a choice between putting either the ground side of the capacitor closer to the IC pins or the high side (Vcc, Vref etc) - go with having the ground side closer. Ground is the "catch basin" for various currents flowing in the IC and not all from the source connected to the other pin of the bypass capacitor. So it's best to keep the ground connection to the capacitor as the shortest connection. An example of

this is when the oscillator discharges the timing capacitor, and a brief pulse of current flows out of the capacitor to ground, but not simultaneously through Vref or Vcc.

Next, add all circuitry which need very low inductance interconnections such as the high speed gate drive outputs of the IC. First put the Schottky clamp diodes on the board from output(s) to ground, then continue with another diode from the output(s) to the totem pole collector supply, Vc. Consider adding a few ohms between Vc and the IC's Vcc (or Vdd) supply to minimize noise from the totempole(s) from getting into the IC's power supply (Vcc). Since the average current into Vc is in the order of ten or so milliamps in most applications, even 10 ohms will help yet not impact the supply voltage amplitude much. The merits and necessity of each of these components could be evaluated at some point in the future, however it's better to begin the PC layout with them in, and removed later - not vice-versa. Another straightforward option is simply just not to "stuff" these locations with components in production.

Keep ALL other components and traces related to any high impedance circuits OUT of the neighborhood for the gate drive circuits. The associated high speed, sharp transitions found here will easily couple spikes on to high impedance networks such as an amplifier's compensation components, etc. "Block off" an area just for the gate drive circuits and stay away from it with everything else.

The next area of concern is found at the oscillator's timing capacitor, Ct. Make this as close as possible on the board to the respective IC pin and the IC's ground pin connection. If synchronization of the power supply will be required, then add a series resistor location between ground and the lower end of the timing capacitor. A positive going sync pulse applied across the resistor will synchronize nearly all PWMs, and is one of the most common and universal circuits used in the industry. Unfortunately, however, this adds a small amount of series inductance in the Ct ground path which has already been demonstrated to potentially lead to problems. Keep all traces as short as possible for best results, as this circuit can be made to work well - even in noisy environments.

Continue the PCB layout with any other noise filtering capacitors next. Common examples of these are found at the current limit pins where a 1k ohm resistor from the main switch's current sense resistor feeds a small (100pf to 1nF) filter capacitor. Other places to look are at any of an IC's time delay programming pins where the capacitor is a critical timing element. Here too, keep the ground connections short and stay especially clear from the high power outputs.

Other filter capacitors can be found at the IC's programmable functions where a comparator's threshold is set or adjusted. And even though these may programmed with a resistor divider network coming from a well bypassed reference voltage such as the IC's Vref pin, the impedance's are generally high to keep the quiescent (bias) current low. This tends to makes these critical inputs more vulnerable to noise and spikes from the high speed PWM outputs, so a bypass capacitor is recommended on these threshold inputs.

High impedance networks such as the voltage and/or current amplifier feedback and compensation loops also need special attention. All of the warnings about avoiding the gate drive circuitry applies equally to the amplifier section. As a "rule of thumb", add locations for components that might not be required in both the input and feedback sections of the loop. Specifically, wherever only a resistor would normally be found, add the locations to put a capacitor in parallel with this resistor, and add a location for a component in series with the resistor as well, simply called component Zin for now. Because of the universal sizes of surface mount resistors and capacitors, each of these is completely interchangeable in assembly with one another. Therefore, it's easy to just leave a location for a generic component - resistor OR capacitor for now - which will be determined at some time in the future. Again, if not needed, the breadboard can be stuffed with zero ohm resistors for short circuits or left unpopulated for open circuits. But having the provisions to potentially add these components during the prototype period - and even down

through the production stage is a small luxury worth consideration if room is available.

Mixing SMT Capability with Through-Hole Assembly Techniques

One option also worth considering is to lay-out a thru-hole PCB for both thru-hole and SMT components. This can be accomplished by simply adding the device's SMT footprint on the top side of the PCB artwork between the thru-hole component leads as shown in figure UCC3889 PC). For most components such as resistors and capacitors, their SMT counterparts fit with plenty of room to spare within the thru-hole footprint, but there are exceptions. For example, the 8 pin SOIC doesn't fit inside the 8 pin DIL (thru-hole) version - and the lead spacing are different. But offsetting the two package centerlines slightly such that they overlap a little will make both layouts possible. Most PWMs use the same "pinouts" for both packages which simplifies matters although there are exceptions, especially when an LCC or a PLCC version is preferred. Some other reasons for considering a dual layout are component availability, component pricing and having the ability to be forward compatible with SMT assembly technologies - without having to relay out the PC board even for a trial run.

Reinventing the Wheel

Rather than begin a new design entirely "from scratch", possibly with a new, yet unproven layout, magnetic design, power stage and/or control circuit, a great timesaver is to start with at least one, or more, known working pieces of this overall design. One example of where this is applicable is when a low power second or auxiliary output needs to be added to an existing power supply. Following the initial calculations, the most logical shortcut is to start by adding the required turns for the new output to the existing transformer - regardless of its output voltage. Don't remove the original output's winding - if at all possible. Just add the second winding over the outside of the existing transformer windings. Granted, the coupling of this arrangement will not be ideal, nor as good as once wound properly, but in generally will work well enough to get reasonable results at low power.

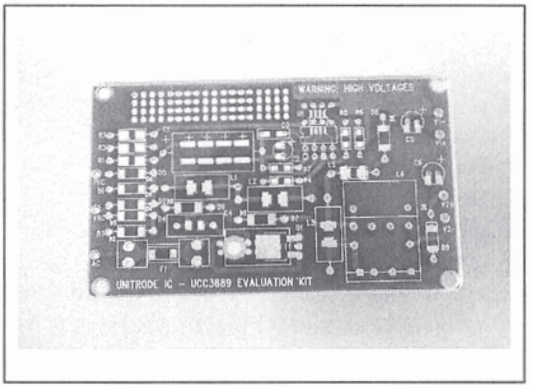

Figure 39. UCCC3889 Demo Kit PC Board - SMT and/or thru-hole

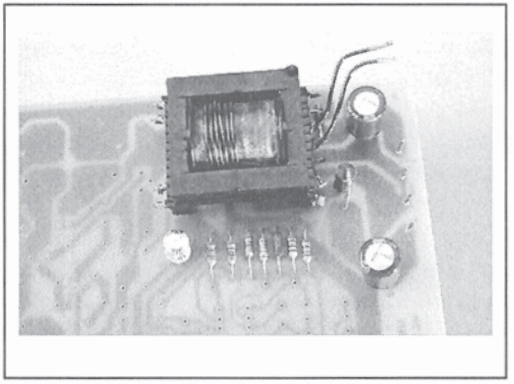

Figure 40. Photo of second winding on outside of existing transformer and additional PC board

If adding the complete number of turns for the new winding is not possible due to lack of available transformer window area, then there is another option. Use the first output's turns as a part of the new windings secondary, and add only the additionally number of turns required. For example, if the 3V output had one turn, and the 5V requires two turns, then add only one turn and place it in series with the existing one turn for the 3V output. The copper losses will most likely be lower due to the abundance of copper found on the original, higher current winding, which is something to take into consideration. In fact, this technique has been widely used to develop the 12 Volt outputs on

flyback converters which have a 5 Volt main output. The 12V winding consists of only the additional turns required connected in series with the main 5V winding transformer taps. This configuration tends to improve cross regulation by forcing the 5 volt output's voltage loop to compensate accordingly for any voltage drops in the copper, which is dependent on the sum of the 5 and 12 volt currents. In either case - whether the entire second winding or only a part of it was added to the transformer, place the additional output inductor and capacitor filter section of the second output on a separate prototype PC board. Install this as physically close to the transformer's secondary winding to minimize layout parasitic effects.

It might seem logical to jump right ahead to the next step of redesigning the PC board for two outputs, etc, without first - even crudely - evaluating the more obvious choice of modifying a working unit. Seasoned professionals may qualify to omit this step, although it 's more likely to find them proceeding along these lines and getting the design completed more quickly. The brief time it takes to modify an existing unit first to develop the complete schematic and list of materials is generally worth the slight schedule delay.

When adding a second (or more) output(s) to an existing unit, one concern is power dissipation of the primary side power switches. There are two easy ways around having to change the existing amount of heatsinking to run preliminary tests. The most obviously choices are to use an external fan to keep temperatures under control, and the other is to simply keep the total output power of the unit the same as the original rating. This is done by reducing the power of the main output by the same amount of that delivered by the additional, second output. This assumes that the efficiency of the extra output is similar to the first. If not, then maintaining a constant input power to the unit by adjusting (lowering) the first output's power might be necessary.

Power Supply "Families"

Generating the full family of output voltages for a new series of units ranging from 3.3V, 5V, 12V through 48V can also be greatly simplified. Start with the more difficult case which is generally the highest output current, corresponding to the lowest output voltage. Beginning the initial PC board development to accommodate the highest output current (first) will result in PC board traces which are significantly oversized for the lowest currents for the model family. This is also the best time in the design procedure to review any high voltage spacing requirements to meet safety agency requirements. But going through this initial exercise of designing the PC board traces to handle the two worst cases - highest current with adequate spacing for the highest voltage will minimize the number of PC board relay outs necessary. Take note of the maximum voltage and power dissipation ratings of resistors used in the voltage feedback divider network and output preload as this may effect the number required for higher voltage outputs.

Another good reason to start the PCB layout with the highest output current rating is to provide enough room for the number output capacitors required to achieve the specified (low) output voltage ripple. Two factors make the lowest output voltage require the largest number of capacitors : inductor ripple current and output ripple voltage. Generally, the output inductor value is selected based upon handling a certain percentage of the full output current as ripple current. Ten through even twenty percent is a common range for continuous current applications. Usually, the higher percentage ripple corresponds to the lower output voltage in an attempt to keep the inductor volume low. Note, that the worst case (highest) for the ripple current amplitude is in the highest output current application, which is also the lowest output voltage. What makes matters worse is that this also corresponds to the condition for the lowest allowable output ripple voltage. That's because it is generally rated as a percentage of the output voltage, usually around 1% maximum. Here's an example of two 100 Watt outputs with the assumption that all ripple voltage is attributed to ESR, ignoring the effects of ESL, etc, for this review.

A: Vout = 3.0V @ 33 A, Output voltage ripple = 30mV, ripple current = 3.3A

B : Vout = 5.0V@ 20A, Output voltage ripple = 50 mV, ripple current = 2.0A

In the first case of the 3.0V output, the maximum allowable output capacitor ESR is 30mv/3.3A = 9 milliohms. For the 5V output, this becomes 50mV/2.0 = 25 milliohms. Using an estimate for the lowest ESR rating of available capacitors of 35 millliohms, it's clear the 5 volt output has margin with only two capacitors yet the 3.0 V output needs four capacitors with minimal margin. Therefore, the PC board main output initial layout should be designed to accommodate four output capacitors altogether to service the 3.0V requirement, although only two are needed for the 5.0V, and probably only one used in the higher voltage outputs. Always start the layout with the worst case consideration of highest number of required components to be safe in all other examples.

Synchronous Rectification??? :
More on High Current Outputs

If there is even a remote possibility that a synchronous rectified output technique might be considered in the future, then plan accordingly. Lay out the output rectifier PCB locations for three lead devices to accommodate the drain, gate and source connections of the MOSFETs instead of only two for the rectifier anode and cathode. Add two more small holes, one each directly next to the center (gate) lead and left (source / anode) lead to facilitate the potential gate drive connections - which could be leads of a twisted pair of wires. Verify also that only one FET will be needed to achieve the desired results. Otherwise, add the number of device locations in parallel to accommodate additional FETs. Note, that one very low on-resistance MOSFET could be more expensive that two slightly higher resistance MOSFETs. Yet when paralleled, the lower performance devices yield a lower net on-resistance than the single FET. Beyond cost, availability is another concern to be factored-in early in the PCB design. Having the flexibility to satisfy the electrical requirements in more than one way is another advantage to providing the additional device footprints "up front" in the initial PCB layout. If for no other reason, consider these provisions in anticipation of forthcoming higher output current requirements.

Spreading the total power dissipation amongst two or more devices is another issue which could favor the use of multiple devices. Heatsinking these to large PC board copper traces designed as heatspreaders could be more cost effective in manufacturing than mounting one device on a heatsink. Keep in mind that each manual subassembly operation is labor intensive and probably far more expensive than the fractions of a second required by automatic insertion, SMT "pick-and-place" machinery.

DESIGN, LAYOUT, TESTING AND TROUBLESHOOTING THE CONTROL CIRCUIT BREADBOARD :

Guidelines and hints :
"Do these or suffer later"

A: Read all product datasheets, minimum and maximum ratings, specifications, application notes, design notes and any other relevant material first. Check with a Field Applications Engineer that the protection functions work as described by, or understood from the product literature.

B : With any "new" PWM, PFC or other control IC, build the "Open Loop Test Circuit" as shown in the datasheet first. Familiarize yourself with how the various functions actually work and will perform in a typical application. Keep all notes handy for future debugging.

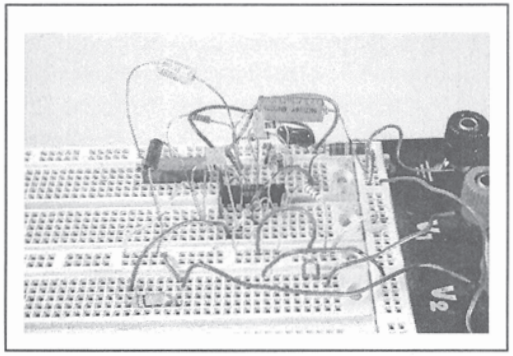

Figure 41. Do not use plug-in experimenter boards

Laying-out the prototype circuit:

C: ***NEVER*** use "experimenter" or "plug-in" protoboards for high frequency applications - ***they won't work*** in a high frequency, power environment. Whenever possible, start with a know working PC Board layout if the control IC was previously (and successfully) used. If this is a completely new designs, start with a double sided copper clad board and remove copper as required to run traces and fit components. While this is tedious and time consuming, the results are well worth the investment. The alternative is to use a "quality" pre-drilled prototyping PC Board, preferably with a ground plane. Keep all connections short and use wires for interconnections sparingly. Although used successfully and often necessary in some RF applications, avoid the three dimensional "sky-wired" assembly. Transitioning this circuit to a two dimensional PC Board layout is not only difficult, but more often impossible due to newly introduced parasitic (layout) effects.

D: Use plenty of bypass capacitors located as close to the IC pins as physically possible. Put the smallest valued one right up against the pins, and higher values next closest. If a choice must be made between getting the ground lead or supply lead connection closer due to physical limitations, keep the ground side of the capacitor closest.

The "Pre-flight" checkout : Initial power-up and debugging *: "Hall of Fame or Ball of Flame"?*

E: "Ohm-out" the breadboard before applying any power. Verify each of the IC's pin impedances to ground, to the supply rail and pin-to-pin connections for certainty. Visually inspect the breadboard for potential solder shorts and open circuits. Check the polarities of all electrolytic and tantalum capacitors and diodes. Estimate what the typical IC supply current will be with the oscillator running and with no load on the outputs. As a reference, this might typically range from 1mA to 5 mA for BiCMOS PWMs such as the UCC3802 family, and between 15 and 30mA for high speed bipolar PWMs like the UC3825 - depending on frequency. Remove (break) any connections initially from the PWM totem-pole outputs to external loads such as the MOSFET gates, or driver ICs.

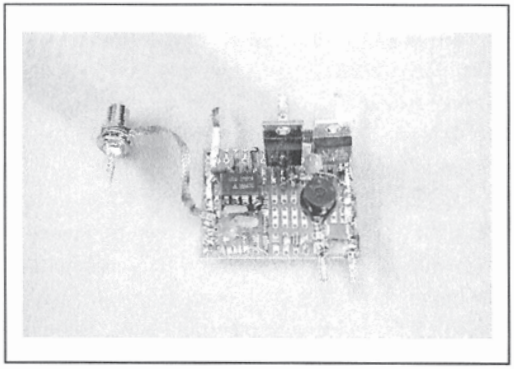

Figure 42. Example of a good high frequency breadboard

" Breathing Those First Pulse Widths " :

F: PWM power-up : Use an ISOLATED, CURRENT LIMITED LAB SUPPLY to power the control circuit IC's supply input, Vcc, Vin, or Vdd if BiCMOS. Break any connections from this rail to the remainder of the power supply if necessary to prevent current from flowing anywhere else in the supply under development. This includes any driver ICs used in the gate drive circuitry. For now, just power-up the PWM control IC.

Increase the supply voltage starting at zero while simultaneously monitoring the supply current. Provided that the supply current is below the expected maximum for the application, continue increasing the supply voltage until the IC's Undervoltage Lockout (UVLO) threshold is crossed. Consult the datasheet for ratings.

Note : If at any time during the testing stage the input supply self current limits or exceeds the expected maximum current - then **turn off the supply immediately**. Even with internal overtemperature (thermal) protection, it is possible to destroy the PWMs due to wiswiring or short circuits, in which case the protection is voided.

G : Vreference : With most PWMs, a precision reference voltage is available for external uses. Generally, it is derived from via an internal linear regulator from the IC's supply voltage, Vcc (or Vin). Once the UVLO is satisfied, the reference voltage will be valid and within specification. This

is generally a good indication that the input supply voltage is valid, too. If not, check (measure) Vin first, then check the Vref pin connection for excessive loading. Last, see if any internal fault protections circuit could disable the reference voltage if triggered. (consult datasheet)

H : Oscillator : Verify that the IC's sawtooth oscillator is running at the correct frequency as programmed. Also verify the programmed maximum duty cycle by monitoring the sawtooth waveform's duration from the lower to upper threshold as a percentage of the time for one complete timing cycle.

I : Output(s) : Verify that the IC is delivering an output pulse. Don't get alarmed at first if there is no output, as the PWM inputs could be biased for zero duty cycle. See next section for details.

J : Pulse Width Modulator operation : Temporarily, ground the error amplifier INVERTING input with a short "clip-lead" or jumper wire. This should cause the error amplifier output (compensation) pin to go high, and the IC to deliver maximum duty cycle pulse widths from the output(s). On dual and four output PWM controllers, verify that each of the outputs goes to maximum duty cycle. To verify that zero duty cycle is also achievable, remove the temporary jumper wire from the error amplifier inverting input at ground and connect it to the reference voltage, or an external 5V supply. This should cause most PWMs to go to zero duty cycle. If not, and a very brief pulse is noticed, check into the IC's leading edge blanking circuitry (internal or externally added), the device's minimum (non-zero) duty cycle or user programmed options, usually around the IC's fault management functions.

K : Current Limit : Continue verifying the protection features by applying the correct amplitude voltage to the IC's current limit pin to cause triggering. The PWM output(s) should go to zero duty cycle if the applied signal is held above the threshold, but some minimum pulse width is also possible with other PWMs. Again, check the device's datasheet for detailed operation.

L : Fault management : Triggering the current limit circuitry on some PWMs can also cause the IC to enter into one of many programmable types of fault protection modes. The more common are : complete latch-off with manual restart, automatic retry (restart) at a low repetition rate, frequency "foldback", or continue to deliver outputs at a minimum duty cycle pulse width. Whichever mode is utilized, verify that this function is operational and the timing is correct.

M : Miscellaneous other functions : Verify the performance of these which could include overvoltage protection, enable, low current standby operation and other user designed functions.

Control Circuit : Consider making these modifications BEFORE applying power !

N: Set the maximum duty cycle limiting below normal to avoid possible core saturation or overvoltage stress of the semiconductors. The worst thing that will usually happen is that the supply does not come into regulation until some voltage above the minimum (ideal) input voltage.

O: Set the current limiting threshold below normal AND VERIFY IN CIRCUIT ! Add a fuse in series with the input supply to protect against longer term faults.

P: Set the output overvoltage protection below normal. This circuit is generally only triggered when something is wrong, for example, the output voltage feedback path is "open" or incorrectly wired. Hint : DON'T use the output voltage feedback to trigger the overvoltage protection mechanism - use a separate divider network.

Q: Add a zener diode on the IC's "bootstrap" supply or in any other circuits such as the high voltage reset clamp circuit which are prone to overvoltages under abnormal conditions. While these may not be necessary in production, they could same time and effort during the breadboarding stages.

General Power Stage Precautions

R: Protection circuits pay for themselves in lost time. Consider an external high speed current limit circuit on the input supply instead of relying on a fuse or the supply's current limiting.

S: Consider a careful "hipot" test prior to applying input power. This is a test of the prototype unit's isolation resistance and any current flowing

will indicate that there is a probable breakdown of the isolation - somewhere in the unit. This is an important test as voltages can quickly climb during breadboarding as the input voltage is increased. Low voltage testing prior to this might not indicate that there's a potential for higher voltage breakdown of the isolation.

T: Verify that the input power source is FULLY isolated - especially in off-line (AC input) applications. There are several popular ways to check isolation between circuit grounds - consult the test equipment documentation. Hint#3 : The old "pigtail" fuse trick. If ever in doubt as to whether or not things are isolated from one another, use a very low current rating "pigtail" fuse in series with the ground lead. The fuse will "instantly" blow if the grounds are different upon making the connection from the scope to the unit under test.

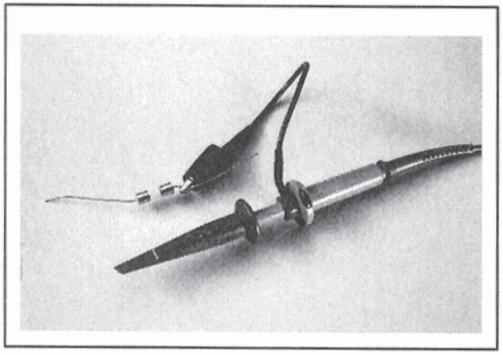

Figure 43. The "Pigtail" fuse "ground" tester

U : Proceed with testing while exercising caution. Monitor input power in addition to the various peak voltages and currents, both mentioned and not referenced.

SUMMARY :

A variety of new, yet practical circuit design, printed circuit board layout and prototype troubleshooting issues have been explored. With these tools, the overall power supply design time might be reduced, and at least the avoidable hurdles can be kept to a minimum. Common mis-uses or misunderstandings of two key precision instruments has been highlighted, along with necessary "fixes" to obtain more meaningful measurements. Finally, a general step-by-step "power-up" and troubleshooting guide for PWM control ICs and supporting circuitry is offered for reference.

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