
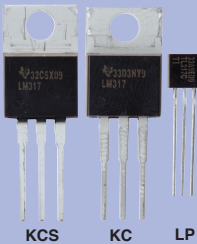














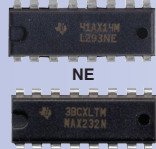
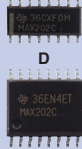






















Linear Packaging Migration

Pin	TO	PDIP	POWER FLEX	SOIC	SOP	SSOP	SOT	TSSOP	VSSOP	VFBGA
2			 KTP							
3	 KCS KC LP		 KTE				 PK DBZ			
4							 DCY			
5			 KTG				 DBV DCK			
8		 P		 D	 PS			 PW	 DDU DGK	
14				 D	 NS	 DB		 PW		
16	 NE N			 D DW	 NS	 DB		 PW		
18	 N			 DW						
20	 N			 DW	 NS	 DB		 PW		 GQN
24	 NT			 DW		 DB		 PW		
28				 DW		 DB		 PW		
48						 DL		 DGG		