Multichannel Data Acquisition Systems

Section 4

This section will look at considerations for multichannel data acquisition systems.

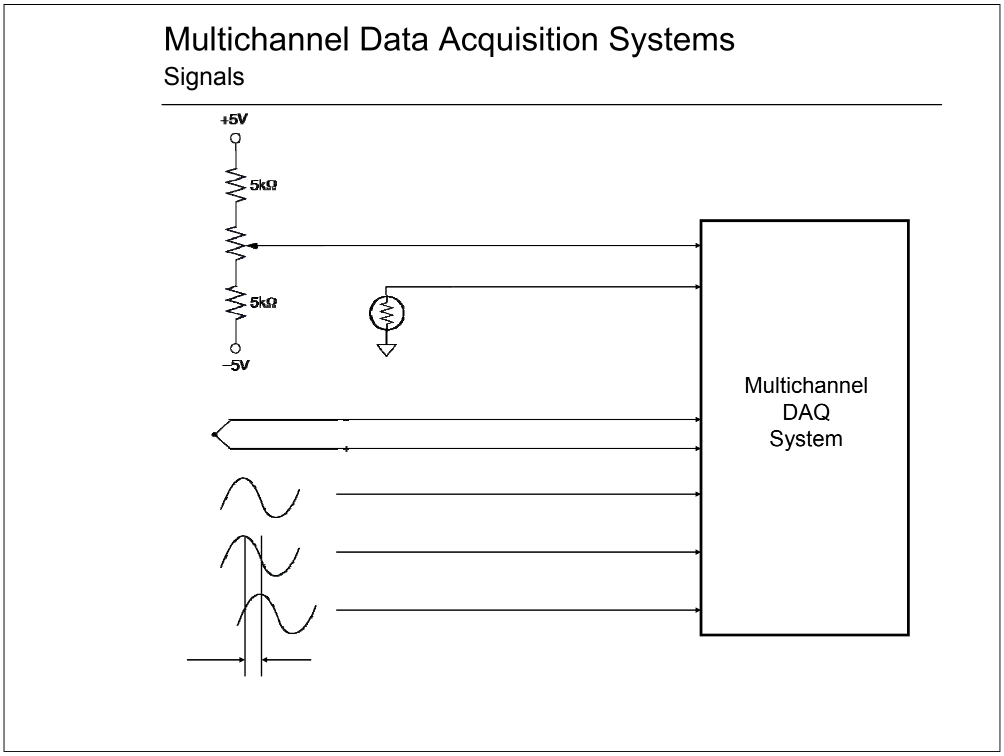
Multichannel Data Acquisition Systems
Outline

- Understanding the Requirements:
  - Signals to be digitized
  - Phase requirements between channels
- Handling Multiple Input Channels
  - Multiplexing
    - SAR vs Delta-Sigma
    - Driving SAR ADCs
  - Simultaneous Sampling
  - Using Multiple ADCs
- PCB Layout Tips

In this session, we'll be examining some of the issues present in designing a system with multiple channels. We must begin by knowing something about the signals we want to digitize, both in the frequency and the time domains. This will help us determine the approach that will best suit these requirements.

There are three main approaches: using a single converter and multiplexing each channel to it; using a similar approach but with individual sample/hold amplifiers on each channel to allow for the sampling instant of each channel to be simultaneous; and finally, using an individual ADC for each channel.

Along the way, we'll also look at the differences in multiplexing SAR and delta-sigma ADCs, issues with driving SAR ADCs, and some tips for preserving accuracy when creating a printed circuit board (PCB).



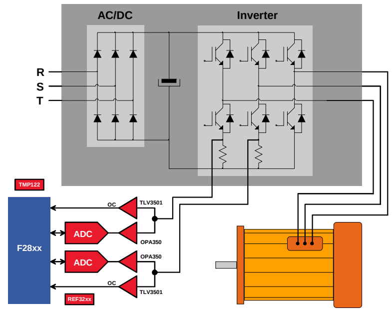
We must first know something about the signals we wish to digitize. Are they DC signals – perhaps from a number of thermistors or thermocouples? Or are they AC signals, perhaps the two microphones capturing a stereo signal? Or is a combination of both types of signals – perhaps the system needs to monitor power supply voltages while it measures power line frequency as well?

A multiplexed system is often the lowest cost, so it helps to look at that approach first. This means we must know the highest frequency of interest that is present in any one of the channels, as this may set our throughput requirements. But if each channel's needs are quite different, perhaps it makes more sense to use different converters that are more suited for each channel's requirements.

If the channels have some unique time relationship to each other, then simultaneous sampling may be required to preserve that phase information. This can be done with a multiplexed system and sample/holds, or perhaps it's easier with individual ADCs. We need to know more about these questions to determine what is the right approach.

Multichannel Data Acquisition Systems
Per Channel Phase Requirements

- Motor Control/Power Measurements:



- Vibration Analysis/Imaging:

One of the most strenuous requirements is preserving phase information between channels – particularly if the channels all must be sampled at the same time. For example, in a power measurement application, the voltage and current must be measured at precisely the same time in order to make an instantaneous power measurement and do it accurately.

For some systems, such as vibration analysis and imaging, the phase information between channels is significant. This means that the delays between channels must be matched and the channels must likely be sampled at the same time. The challenge to the system designer is thus also one of matching the external filtering to within the phase margin allowed.

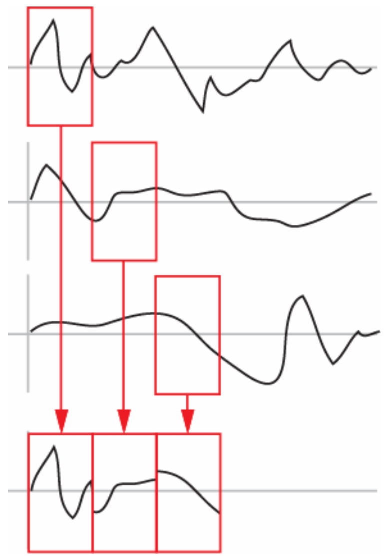
Which brings us to a point: what exactly does it mean to be “at the same time”? “Real-time” systems really aren’t, but they operate at a frequency which makes them appear “real-time” - if you need to sample 50Hz signals simultaneously, does that require 0ns difference between channels, or can your system tolerate a few microseconds delay?

Multichannel Data Acquisition Systems

Multiplexing

Multichannel Data Acquisition Systems

What is multiplexing?

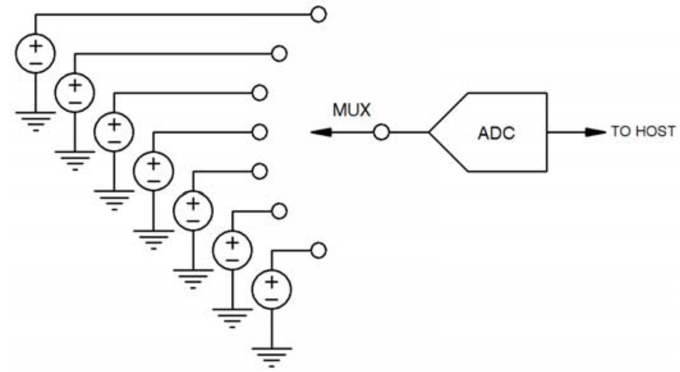


Multiplexing is the process of scanning through a number of input channels, and sampling each in rotation. In multiplexed systems, only one ADC is needed to acquire data from (potentially) many channels.

In a multiplexed system, multiple data streams are merged into a time-division multiplexed signal, which is then sampled.

Multichannel Data Acquisition Systems
Why multiplex?

- Fewer converters needed per channel – often only one needed
- Often lower power
- Often lower cost



Multiplexing allows one ADC to do the work of several in a multichannel system. Rather than dedicating an ADC to each channel, a single converter can read every channel in sequence. This can save power, since ADCs can use a significant amount of power while switches use very little, and it can save cost, since switches are much cheaper than ADCs.

Multichannel Data Acquisition Systems
Applications for multiplexing

- Temperature monitoring
- Multi-point weigh scales
- Pressure monitoring
- Control surface transducer readings (e.g., audio mixer control surface)
- General purpose low-speed sensor data acquisition

Multiplexing cannot be used if channels must be sampled simultaneously. It also tends to limit the data rate, since the available throughput of a single converter is divided among many channels.

Note that some applications which seemingly require simultaneous sampling can still use multiplexing if the requirement is for constant phase between samples, for example, the phase relationship between channels need not be zero degrees, but can be some fixed number.

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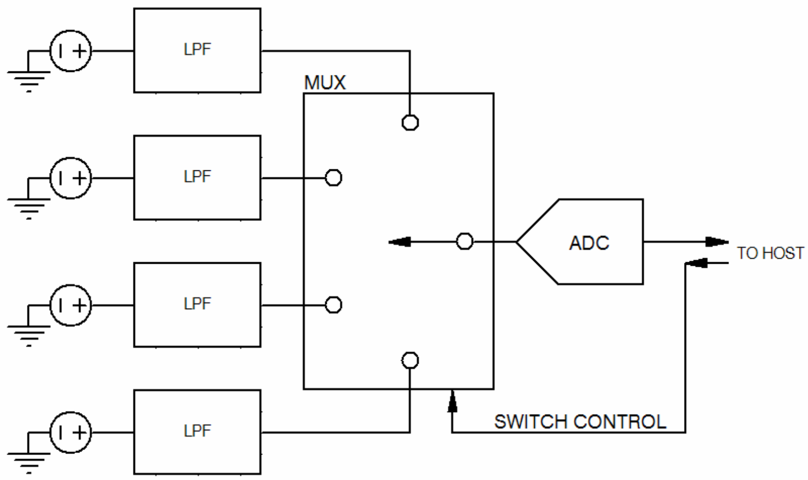
SAR-based multiplexed system



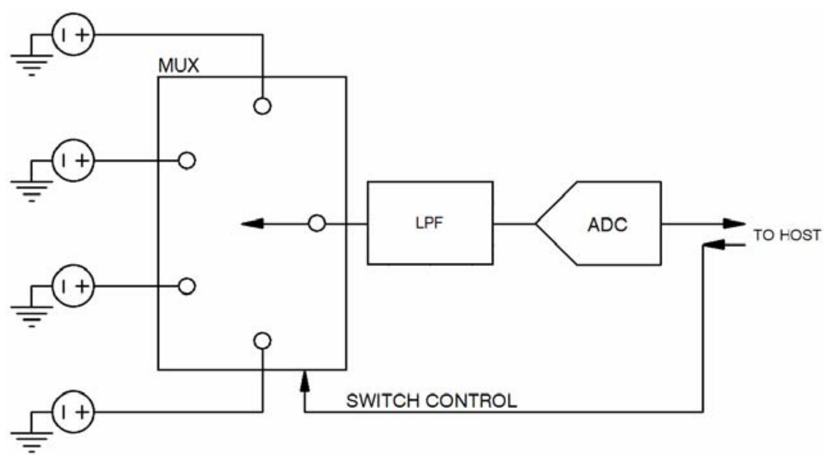
Multiplexing is typically done with SAR converters. The individual signals are anti-aliased before the multiplexer, and the SAR takes one sample from each time slot.

Aliasing at the converter is prevented by keeping the conversion time properly synchronised with the multiplexer switching.

As we will see, this method unfortunately cannot be used with delta-sigma converters.

Multichannel Data Acquisition Systems

Delta-sigma multiplexed system

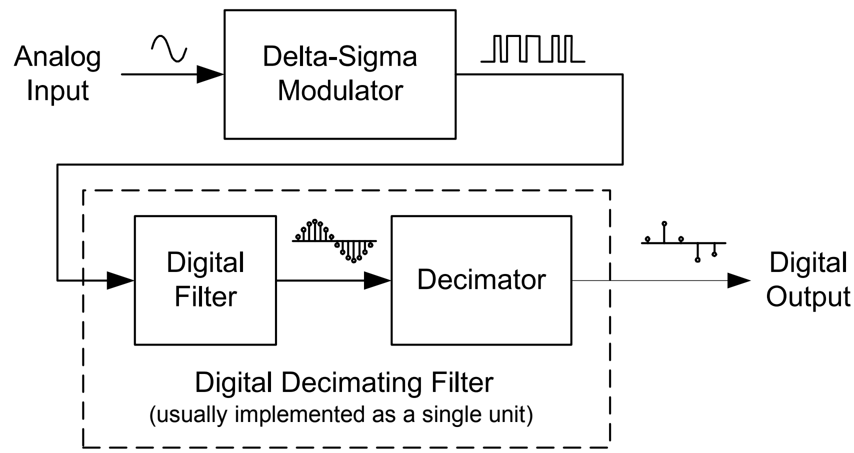


A multiplexed system using a delta-sigma converter typically has the form shown. The major change is that the anti-aliasing filter has been placed between the multiplexer and the ADC, and there are no longer anti-aliasing filters on each input channel.

There could be anti-aliasing filters on each input channel, but they would be redundant: the anti-aliasing filter in front of the ADC is an integral part of the delta-sigma.

Multichannel Data Acquisition Systems

Delta-sigma architecture

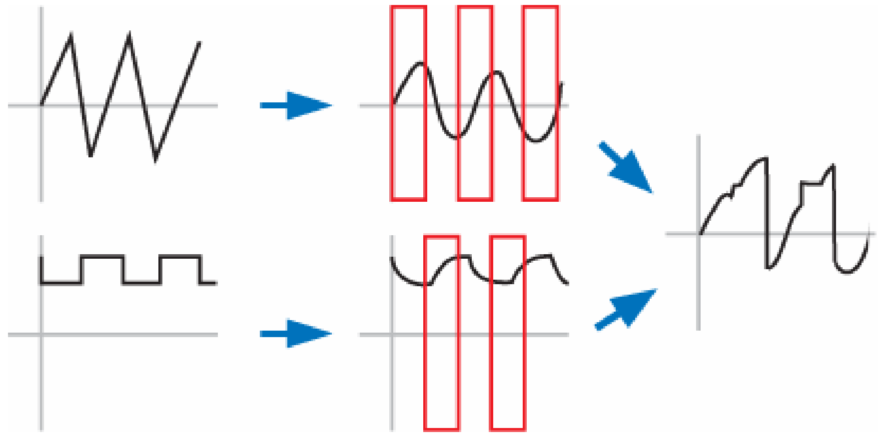


The low-pass filter is not optional in a (typical) delta-sigma converter. It is required to filter out the modulator's quantization noise. Its filtering action is also used to reject out-of-band frequencies that fall within the modulator's Nyquist bandwidth.

Because of this, in a delta-sigma system using a multiplexer, the multiplexer's switching action is always filtered, and we must consider the filter's settling time.

Multichannel Data Acquisition Systems

Time-division multiplexing



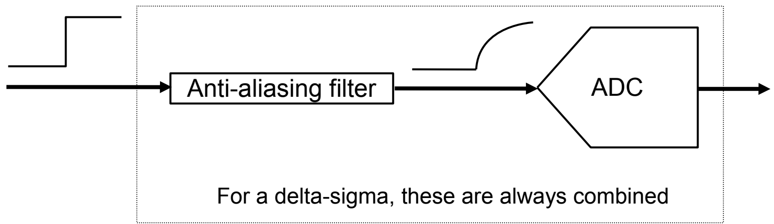
This diagram shows what a simple multiplexed signal might look like.

In this diagram, two signals are multiplexed. The signals have very different waveforms. A slice is taken of each, and the slices are concatenated alternately, as shown in the merged waveform. This waveform has high-frequency components – evidenced by the large and fast transitions – which are not present in the original signals; they are added by the multiplexing process.

A SAR converter can be configured to not sample these transitions, but the delta-sigma converter does not work this way. Its filter will react to the entire multiplexed waveform. This means that the fast transitions, which are like step functions, will be filtered, and the filter will have to “settle”. We will see this more clearly in the next slides.

Of course, a SAR converter can also be configured in the same way as a delta-sigma converter, by inserting the anti-aliasing filter between the multiplexer and the converter. If that is done, the issues become very similar.

Multichannel Data Acquisition Systems
Settling time



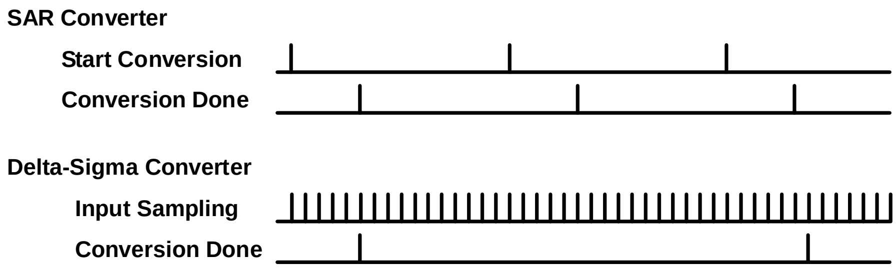
Settling time is a property of any low-pass filter. A step input, when low-pass filtered, becomes a slow rise, possibly with a ringing phase; eventually this settles to the step input's final value. The length of time this takes depends on the filter, and is the major component of settling time in delta-sigma converters.

Delta-sigma converters incorporate a low-pass filter, so it must be taken into account when determining settling time. These digital filters are linear systems with many of the same parameters as continuous-time filters; they too have a step response. It may be very short, as with most industrial delta-sigmas, or it may be very long, as with most audio converters.

Note that for SARs, settling time means something slightly different; it refers to the settling that occurs during the acquisition time. This is different from settling time through the system as a whole, including the effect of the low-pass filter.

Multichannel Data Acquisition Systems
SAR vs Delta-Sigma Conversions

- SAR conversions have Start Conversion Signal
- Delta-Sigma is always sampling/converting

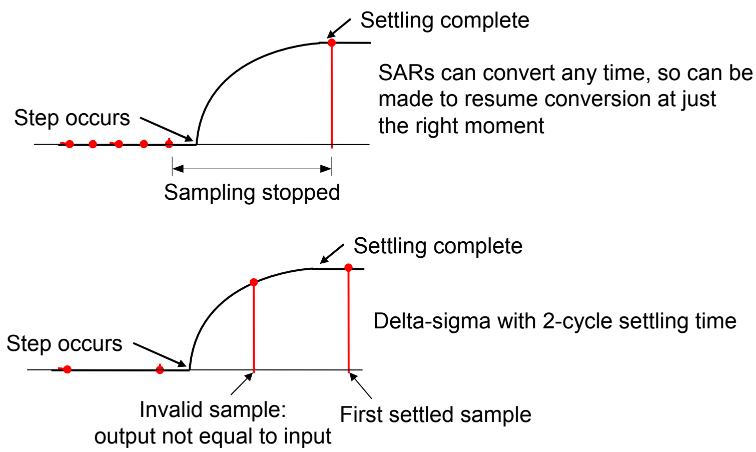


A SAR converter takes a “snapshot” of an input voltage and analyzes it to determine the corresponding digital code. A delta-sigma converter measures the input for a certain period of time and outputs a digital code corresponding to the average over that time. It is important to remember the way delta-sigma converters operate, particularly for designs incorporating multiplexing and synchronization.

It is very easy to synchronize delta-sigma converters together, so that they sample at the same time, but it’s more difficult to synchronize a delta-sigma converter to an external event.

Multichannel Data Acquisition Systems

Settling time: SAR vs. Delta-Sigma

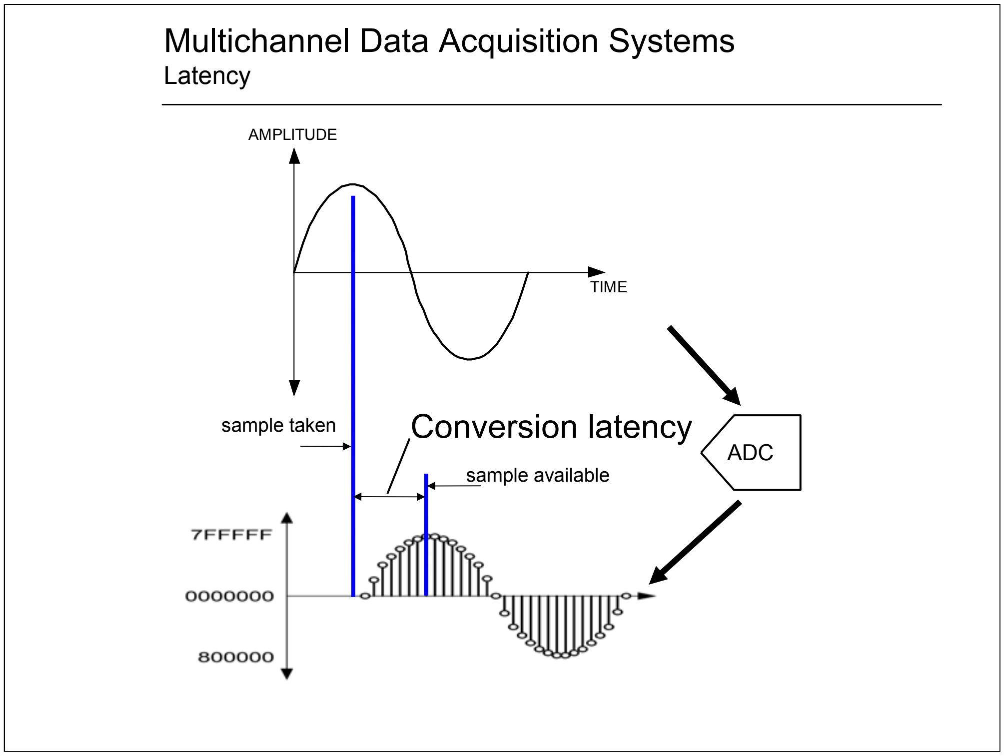


SARs have an advantage over delta-sigmas in one respect; their sample times can be made arbitrary, within device limits. Sampling can be made to cease until the precise moment when the filter has recovered from a step input.

Delta-sigmas are generally made so that one conversion period follows another immediately, so as to maximize throughput. You can start a conversion early by resetting the converter, so starting it over, but this causes the digital filter to refill and resettle. Some time is nearly always wasted, unless the settling time is exactly matched to the data rate and a full-scale step has occurred at the right moment.

For a delta-sigma, settling time can never be less than the conversion latency, but often is more, and is always measured in conversion cycles. For a SAR, settling time depends very little on the converter itself, and very much on the antialiasing filter's step response time – if there is one. SARs can be operated with no filter at all, if desired, and this is occasionally appropriate.

In multiplexed systems, this settling time is very important; there could be a maximum-scale step at every multiplexer transition. Therefore, the output of the delta-sigma must be considered invalid until the filter settling time has passed.



Latency and settling time are very commonly confused, but they are not at all the same thing. In fact, they have nothing to do with each other. Converter latency in multiplexed systems is far less important than settling time, being largely irrelevant to the process of multiplexing.

Conversion latency for an ADC is the amount of time that passes between the taking of a sample and the time that the sample is ready for retrieval.

For SAR ADCs, latency is typically very short, being the amount of time for the successive approximation process to complete. Data is typically available immediately afterward.

For delta-sigma ADCs, latency is a bit harder to define, since delta-sigma ADCs do not output a code corresponding to a single point in time. The code they output is the result of filtering or averaging the input during an interval of time; the interval is equal to the sample period. (Actually, this is also true for SARs, but the interval is extremely small compared to the sample period.)

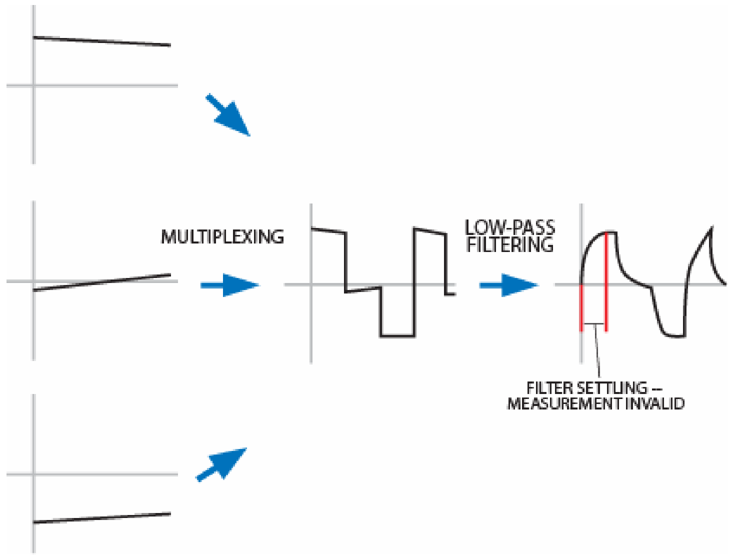
For this reason, we measure latency for a delta-sigma ADC by starting at the beginning of a sample period, and measuring to the time that data can be retrieved. It may also be practical to include in this the time needed to retrieve the data, since delta-sigma ADCs nearly always have serial interfaces.

Delta-sigma ADCs have an additional “disadvantage” compared to SARs; they always include a filter. Some latency may be incurred in the filter. For audio converters, this additional latency can be very significant, even up to several tens of sample periods. For low-speed industrial converters with sinc filters, it sometimes amounts to only a few modulator cycles.

The term “group delay” is often used in place of latency. For SARs, which generally have a continuous-time filter at the front-end, group delay can be a more useful measurement, since the latency may be frequency-dependent. For delta-sigma ADCs, filters with constant group delay are almost always used, so there is no difference with latency.

Multichannel Data Acquisition Systems

The effect of settling time



The effect of settling time on a multiplexed system is shown in the diagram.

Here we show three near-DC signals multiplexed into a single stream, which is then low-pass filtered. The multiplexer switches are filtered along with the individual signals, and this produces “settling”. After each channel switch, measurements must be withheld until this settling time passes. This reduces per-channel throughput, but each channel is effectively anti-aliased.

Multichannel Data Acquisition Systems
Why multiplex with delta-sigmas?

- A SAR-based system often requires low-pass filters on each channel, considerably increasing power and cost
- A delta-sigma system offers greater accuracy and lower noise floor than most SARs
- For a SAR design, using a post-multiplexer filter results in a system with settling-time issues almost identical to the delta-sigma design, but with higher noise

Many people get discouraged when they consider the settling penalty incurred for some delta-sigma filters. Despite this penalty, there are very compelling reasons to use a delta-sigma converter in a multiplexed design.

The primary reason is accuracy and noise; few SAR converters can even approach the noise floor possible with a delta-sigma converter. In systems where this is very important, the reduced throughput of the delta-sigma ceases to be an issue.

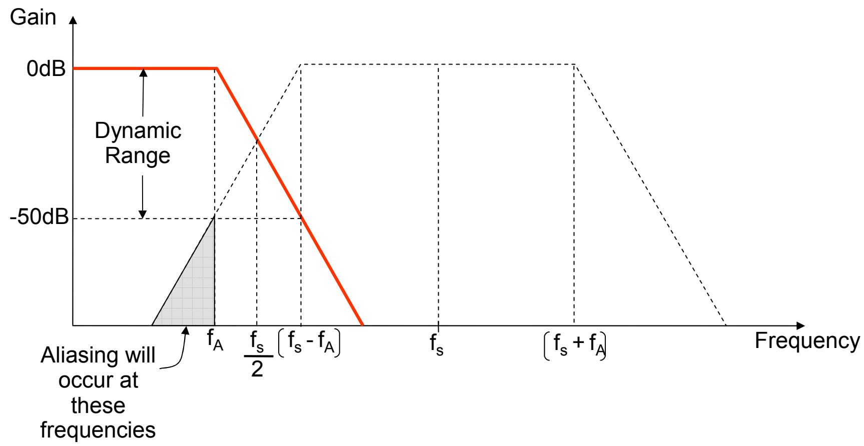
Furthermore, a SAR system often requires low-pass filtering on each channel, and since a SAR has no anti-aliasing at all, these filters may need to be complex multi-pole active designs. These can reduce accuracy and consume considerable power.

If this problem is circumvented by using only a single complex filter after the multiplexer, you obtain a design very similar to the delta-sigma configuration; but the noise and accuracy issues remain.

The cycles lost to settling time aren’t the critical issue in most designs; the real issue is overall throughput for a given level of accuracy, and on these counts the delta-sigma design often wins by a considerable margin.

Multichannel Data Acquisition Systems

Anti-aliasing Filter



50-dB, alias-free range is insufficient for 16 bits.

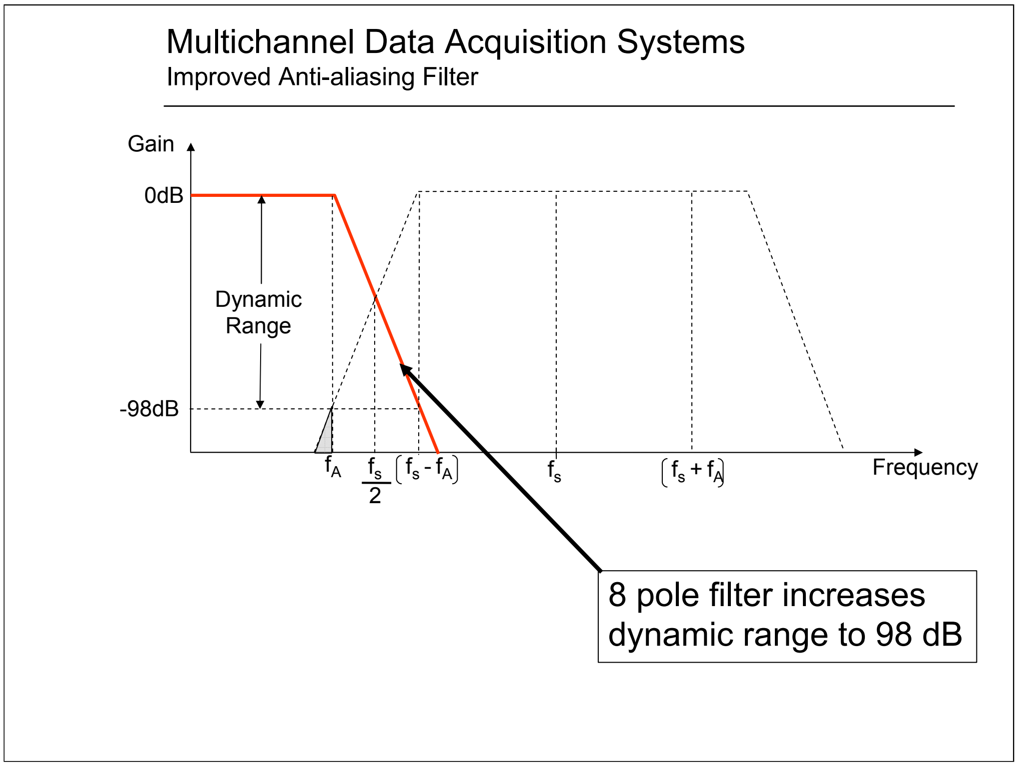
An anti-aliasing filter, with low-pass characteristics, may be placed in the signal chain — in front of the ADC. The purpose of the filter is to attenuate any high-frequency components in the signal and to ensure that the samples taken by the ADC satisfy Nyquist.

Consider the example shown here:

Suppose we have an ADC with a spectrum shown above and a maximum full-scale frequency content of 40 kHz. Also, at 70 kHz, the signal is attenuated by 50 dB (f_S-f_A).

We can see from inspection that at the frequency f_A, the alias component, limits the system's dynamic range to 50 dB.

The system requires an additional 48 dB of attenuation at 70 kHz to achieve the 98 dB of attenuation required for 16-bit performance.



If the application requires additional dynamic range, you will have to consider an anti-aliasing filter to provide more attenuation at 70 kHz.

For a 16-bit system, remembering that SNR = 6.02n + 1.76 dB, we arrive at an SNR of around 98 dB.

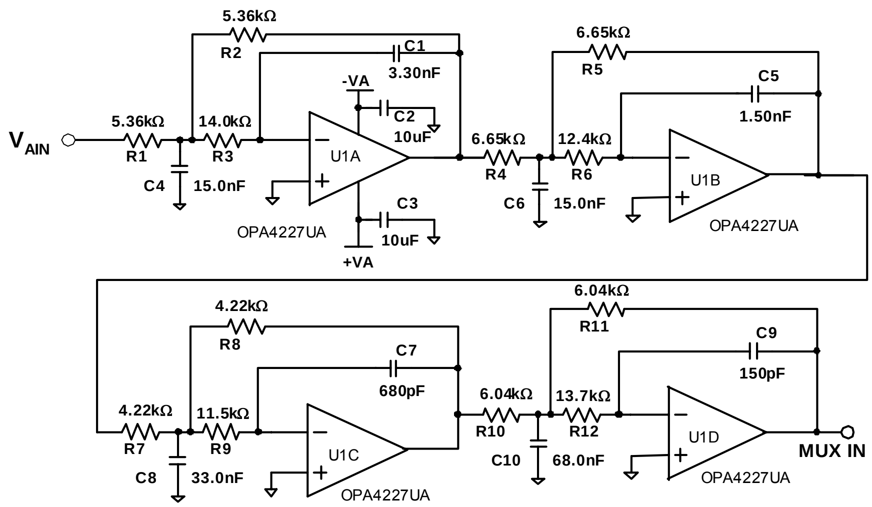
So, if you really want true 16-bit performance at 40 kHz, you need to add a filter that gives 48 dB of attenuation at 70 kHz.

From 40 kHz to 70 kHz almost doubles the frequency—this is an increase of one octave. Each filter pole will give 6 dB per octave. You will need an 8-pole filter to limit the input frequency of the signal and ensure the full dynamic range at the frequency of interest.

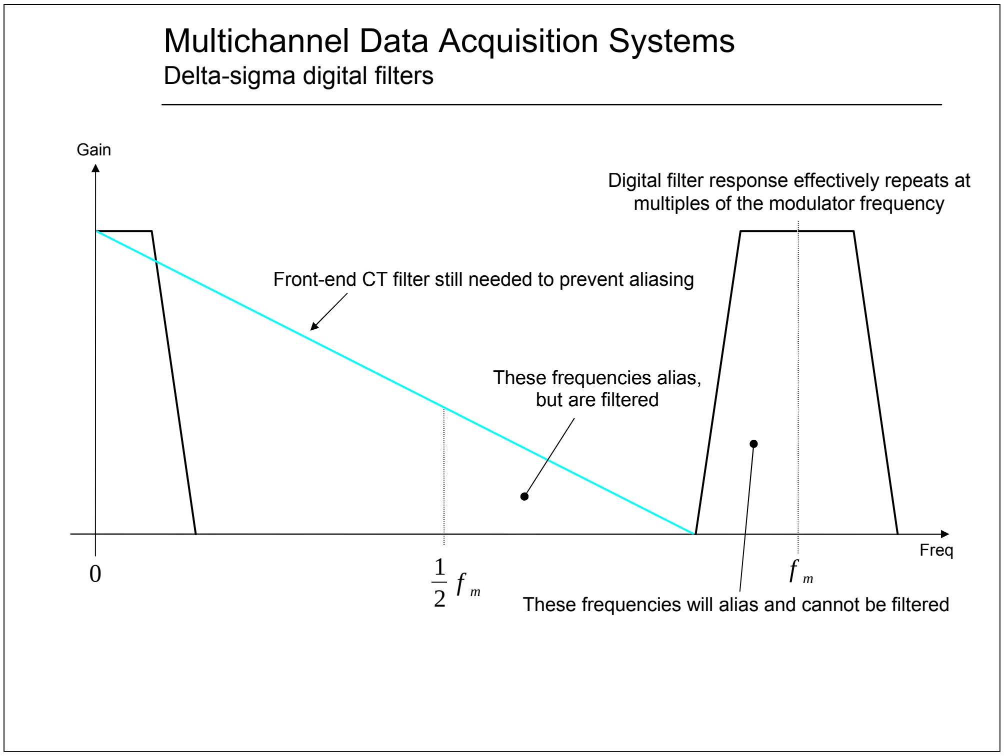
In applications that would require an anti-aliasing filter, the signal's spectral characteristics and the system's dynamic-range requirements must be completely understood before beginning.

Multichannel Data Acquisition Systems

Anti-aliasing Filter Circuit



An 8th order filter circuit is shown here. A quad op amp makes this complex looking circuit relatively small. Still, the cost of the circuit is approximately $5 – as much or perhaps more than the converter itself!



It is widely believed that delta-sigma converters do not require anti-aliasing filtering on the front end. While this may happen to work sometimes, in general it is not the case.

The problem is that a digital filter operates on a discrete-time signal, which contains in itself no information about time. A discrete-time signal sampled at a given rate contains all frequencies aliased into the Nyquist bandwith. What this means in the continuous-time domain is shown in the figure.

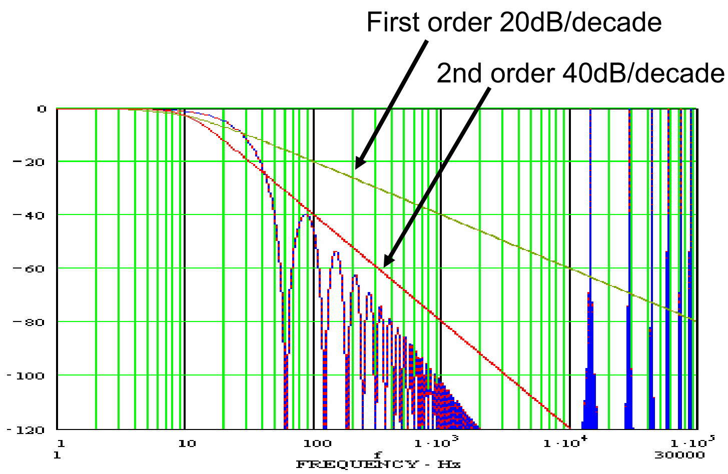
To be sure, in many circumstances the modulator frequency is at a point where there is little information at the Nyquist rate and above; but noise will always be present, and this aliases into the bandwidth of interest just as any other energy will, raising the final noise floor.

Worse still, if there is energy present around the modulator frequency, it will alias down: the digital filter is powerless to remove it, since from its point of view, these frequencies are in the baseband already. It is impossible for it to tell the difference.

For this reason, a continuous-time filter is often needed in front of a delta-sigma. Its stopband attenuation should at least begin at the point shown above. This is especially true for high-order delta-sigmas where the noise floor of the converter itself is very low. Fortunately, this filter often need not be very strong, especially if the digital filter has a very low cutoff frequency. This is why even a simple RC filter can sometimes suffice for a delta-sigma.

Multichannel Data Acquisition Systems
Analog Anti-aliasing Filter

- 10 Hz Butterworth filter



A single-pole RC anti-aliasing filter may work in some delta-sigma applications, but even here a stronger filter is sometimes needed, as in the above example.

You can see that by adding a single pole filter, signals at the modulator frequency may not be attenuated sufficiently. Using a two-pole filter may be necessary.

Multichannel Data Acquisition Systems
Aliasing Reality Check

- Signals at multiples of the sample rate will be aliased at full scale
- Aliasing signals usually are not full scale
- With a $Sinc^3$ filter, aliases above the data rate are attenuated by at least 40 dB (until the sample rate)
- Filtering must be applied with care

Of course, any time you consider an antialising filter, you may not have to assume the worst case – signals that may alias are likely not at full scale, but may be attenuated already by the sensor or system response. This is why it helps to know something about the nature of the signal you are attempting to digitize; it helps you know how much filtering is really required.

Multichannel Data Acquisition Systems
Calculating throughput

- Throughput: number of valid samples per second on all channels
  = converter data rate / filter settling time in cycles
- Per-channel data rate: number of valid samples per second on each channel individually
  = Throughput divided by number of channels to scan per cycle

For a multiplexed delta-sigma system, the throughput is the number of valid samples per second that can be obtained when a filter resynchronization is performed after every multiplexer switch. It is calculated by dividing the converter's data rate by the number of conversion cycles occupied by the filter's settling period. Note that this number does not depend on the number of channels to be scanned per cycle.

The actual sampling rate per channel depends on how many channels are to be scanned, and is obtained by dividing the throughput by the number of channels to be scanned.

Multichannel Data Acquisition Systems
Choosing a delta-sigma for multiplexing

- Important specifications:
  - Settling time: lower is better
- Unimportant specifications:
  - Latency / group delay
    - Watch out – occasionally settling time is called latency in datasheets!
- Important characteristics:
  - Ease of configuration & channel switching

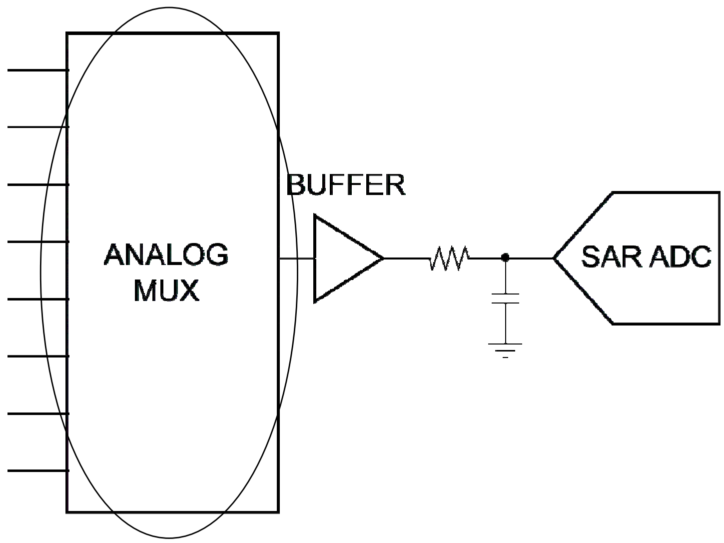
We will now consider a few delta-sigma devices and their suitability for use in multiplexed systems.

The important specification is filter settling time. If it is low, the part will be efficient in a multiplexed system.

Latency and/or group delay are **not** important for multiplexing. A part with a high latency may be good for multiplexing (although admittedly this is unusual, since high latency filters typically also have a long settling time).

A secondary consideration, but possibly of importance, is the ease with which a device can be used in a multiplexed system.

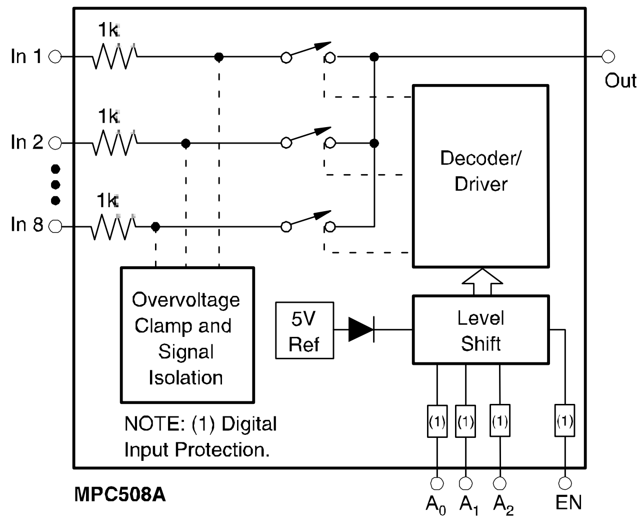
Multichannel Data Acquisition Systems
Block Diagram



A quick block diagram helps to frame the multiplexed system design. Each channel will require its own signal conditioning and an antialiasing filter, and then go into the multiplexer. The multiplexed signal will then be routed to the A/D converter through some type of buffer. We'll route the resulting digital data to the system processor.

Because the system is general purpose, we really don't know what kinds of signals or applications the measurement system may be required to handle. If the system were to be used in a high speed control loop, the time from measuring a channel to getting a precision digital representation of the signal should be minimized. Why are we concerned with this? It helps us to choose the converter type to use, as in the previous discussion of SAR versus delta-sigma converters.

Multichannel Data Acquisition Systems
Multiplexer



A multiplexer is simply a set of analog switches which have one common terminal, and can be easily addressed and turned on under digital control.

The first important parameter for a multiplexer is obviously the number of channels that it has, and whether or not it handles single-ended or differential inputs. In the system shown previously, the inputs are all single-ended, since our signal conditioning and filtering have provided us with single-ended signals. So a simple single-ended 8–channel multiplexer is all that is required.

The analog switches in a multiplexer may have significant on-resistance – in the one shown above, it is 1kΩ. Because of this, the output of the multiplexer is usually buffered with an op amp.

Multichannel Data Acquisition Systems

Throughput Issues

- Channel switching time
  - Usually specified
- Settling time
  - May or may not be specified, and probably not to 18 bits.
- Throughput limited by switching + settling times
  - MPC508: 4μs = 250kHz, but...
- Need to evaluate and see what is required for resolution required.

Since the multiplexer is the device responsible for switching from one channel to the next, another important parameter is the time it takes for the mux to switch from channel to channel. Once switched to a new channel, how long does it take for the output to settle?

The first parameter is often shown on a mux datasheet. Looking at the MPC508 which was shown on the previous slide, it takes 0.5μs to change from one channel to the next. Its settling time is only listed to 0.01% - and this takes 3.5μs! So switching from one channel to another would take at least 4μs – and that is only to 12 bits! Some experimentation is needed to determine the settling time required for a system with higher resolution.

Multichannel Data Acquisition Systems
Other Mux Parameters

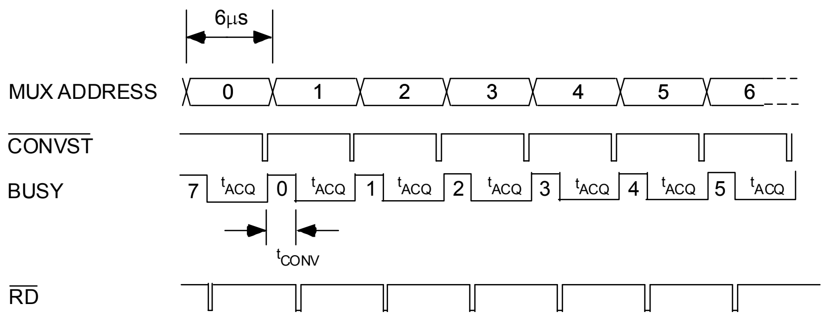
- THD vs Amplitude
  - Voltage coefficient of switches
- THD vs Frequency
  - Parasitic capacitances
- Settling Time
  - On resistance, parasitic caps

Some other parameters to consider on multiplexers are the dynamic performance when switched to a particular channel – especially total harmonic distortion (THD). Multiplexer switches have a significant number of parasitic capacitances which can affect the signal from a THD vs frequency and amplitude perspective.

From a more “industrial” or DC standpoint, the settling time of the multiplexer is significant, as this directly affects the throughput.

Multichannel Data Acquisition Systems

System Timing – First Look



- Overlapping mux and conversion
- Total throughput: 167kHz
- Per channel: 20.8kHz

We need to determine just what throughput our system will have, as this will affect decisions we make about other parts of the system.

Because we control the time at which the multiplexer switches, and the time the converter starts its conversion, we can take into account the overall settling of the multiplexer and its buffer op amp, if used. Shown here is the timing diagram of how we command the multiplexer to switch and start conversions. Assuming 6µs is required for full settling. The key here is to switch the multiplexer, wait 6µs, then start a conversion. Once the conversion has started, the A/D converter has the input held on its internal sampling capacitor, so we are free to change the multiplexer channel, allowing it to begin settling while the converter is converting the previous channel's data that it has acquired. Once that conversion is complete, we read it as quickly as possible, so that the reading of the data is not occurring during the critical acquisition time of the ADC, which could potentially cause noise and corrupt the acquired signal.

From this, we can see the overall throughput that is attainable by our system; 167kHz sample rate, which equates to a 20.8kHz rate per channel if we were scanning through all eight channels. However, if we wanted to switch to one channel and stay there, then we wouldn't have to allow for mux settling, and could potentially sample at a higher rate.

Multichannel Data Acquisition Systems
Crosstalk

- Amount of feedthrough from adjacent channels
- Could show up as noise or offset
  - MPC508: as much as 1% of OFF signal

A further specification that is often shown on multiplexer datasheets is crosstalk. This is the amount of signal that may feed through from ‘off ‘channels when one channel is selected. This would commonly show up as noise in the channel of interest, but may also manifest itself as an offset, depending upon the signals used and the particular multiplexer in use.

Again, this may or may not be specified. If it is, it may be in a curve plotted against signal frequency – higher frequencies will tend to feed through more as the mechanism of crosstalk is usually parasitic capacitances associated with the analog switches.

Multichannel Data Acquisition Systems
Error Sources in our Mux

- On-resistance
  - Not a problem if buffered on both sides
- Noise
  - Crosstalk
  - Digital feedthrough

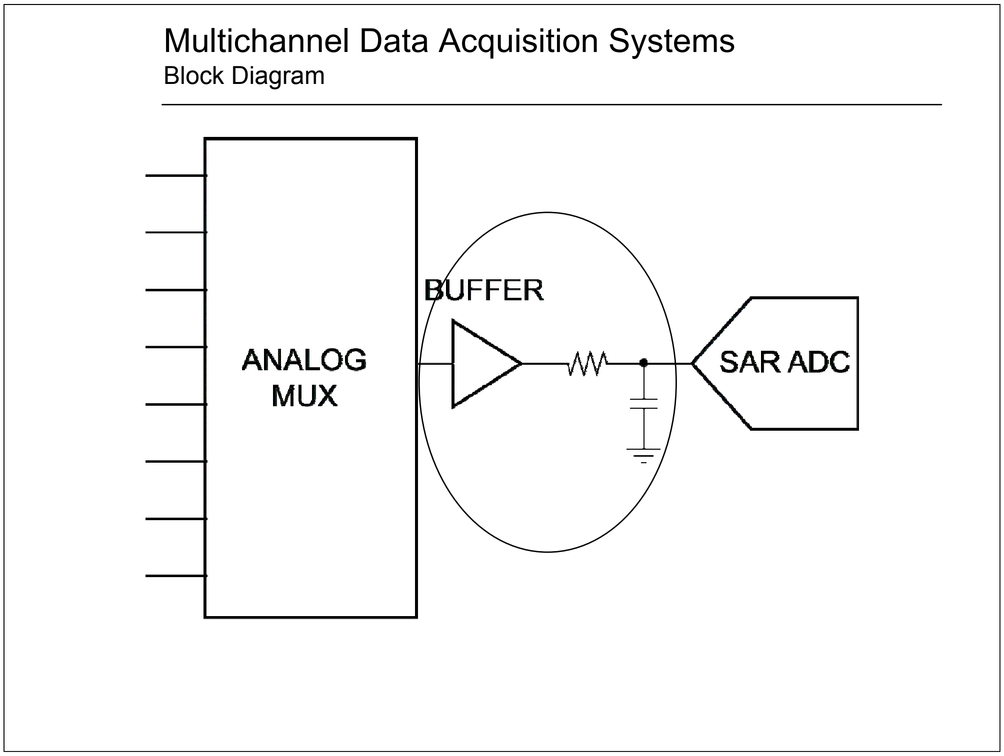
Since multiplexers are simply switches, and not so much an “active” component, they do not specify offset or gain errors. The main error source with multiplexers is their on-resistance, which is easily handled by driving them with an op amp and buffering the output with an op amp. In most systems, the antialiasing filter op amp drives the mux input, and the ADC buffer, buffers the output of the multiplexer, so this is not a concern.

Noise, however, can be a problem with multiplexers as the crosstalk and feedthrough of digital signals into the analog path can contribute noise.

Multichannel Data Acquisition Systems
Internal Multiplexers

- If converter is available with internal mux – use it!
  - Available on both SAR and delta-sigma
- Internal muxes are tailored to match the ADC performance
- Don't have to guess about switching and settling time

If an ADC that meets your system needs is available with an internal multiplexer, this is by far the best solution. Not only does it save space on the board, but the multiplexers internal to the ADC are designed and optimized to work well with that particular ADC. This eliminates a lot of the guesswork that comes with using an external mux.



Now that we've looked at the multiplexer, let's take a closer look at the buffer requirements and input circuitry needed for our ADC. SAR ADCs in particular require the RC circuit shown here. Choosing the values for the R and C as well as choosing the right buffer amplifier are important in preserving the accuracy of the system.

Multichannel Data Acquisition Systems

Simultaneous Sampling

Multichannel Data Acquisition Systems
Simultaneous Sampling

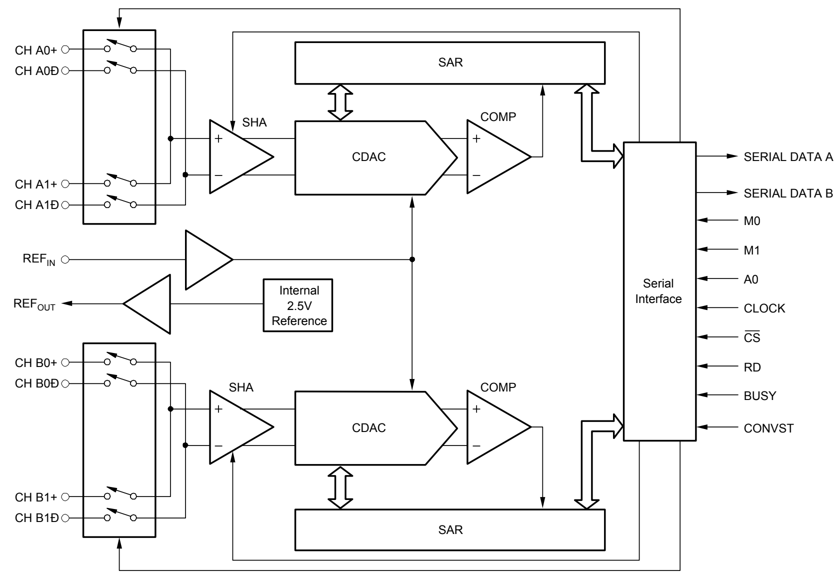
- 2x2 SAR – 2 ADCs with 2 S/Hs each
  - ADS7861
  - ADS7862
  - ADS8361
- 3x2 SAR – 2 ADCs with 3 S/Hs each
  - ADS7864
- 1x6 SAR – 6 ADCs with 1 S/Hs each
  - ADS8364
- Pipeline
  - THS12xx

As noted earlier, simultaneous sampling involves using individual sample/hold (S/H) amplifiers for each channel, then into a mux or individual converter. As it is difficult to purchase sample/hold amplifiers today, and is virtually impossible to get them with 16-bit accuracy, this scheme generally requires converters specially made to do this function.

We offer several types, and refer to them in an MxN way, where M is the number of sample/holds, and N is the number of converters.

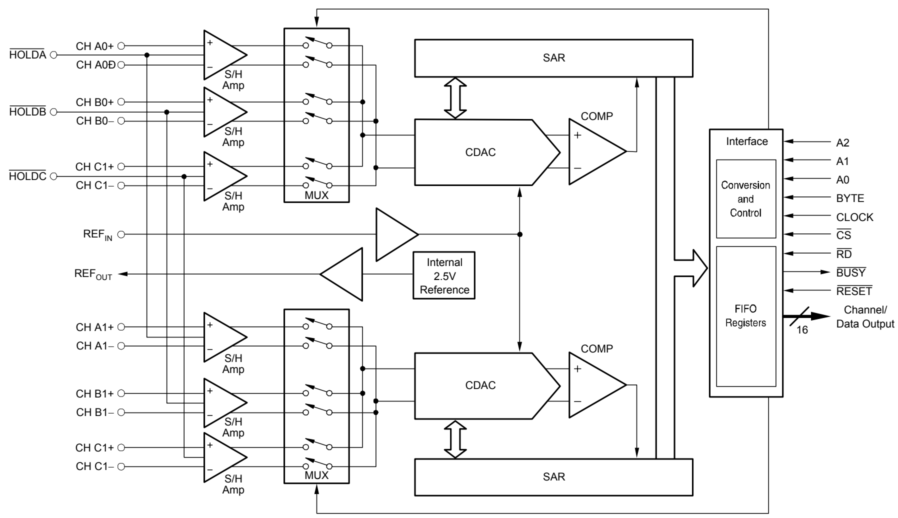
Multichannel Data Acquisition Systems

2x2 SAR



This 2x2 system uses two ADCs, each with a 2-channel mux before the sample/hold. Thus, two channels may be sampled at the same time, then the other two channels selected and sampled at the same time.

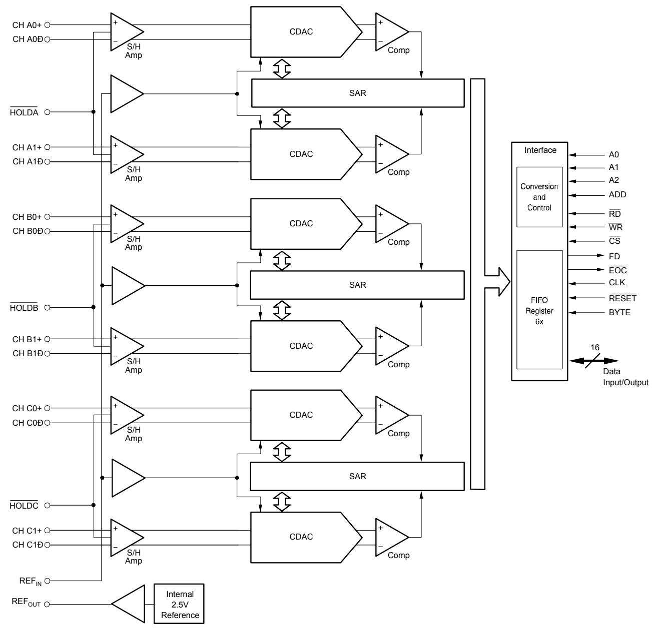
Multichannel Data Acquisition Systems
3x2 SAR



This 3x2 system puts the sample/hold ahead of the mux, so that all six channels can be sampled at the same time, then each converter can convert three of the channels one at a time.

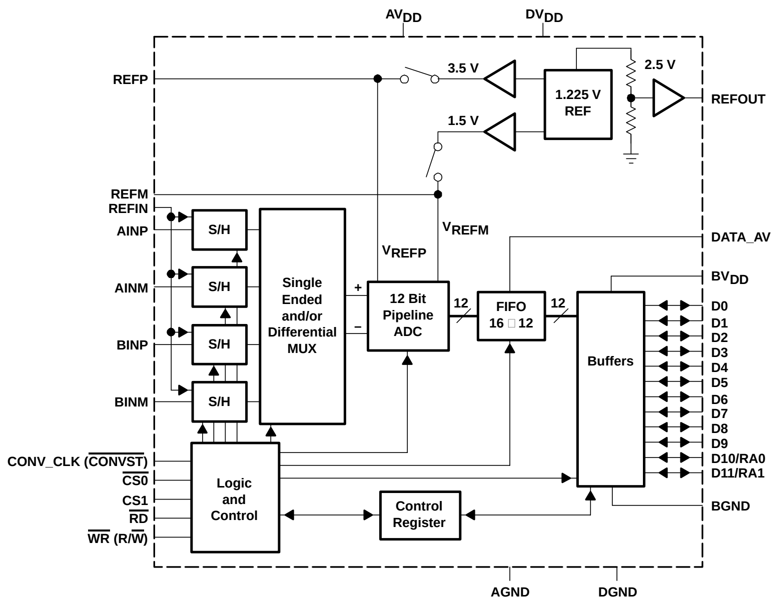
Multichannel Data Acquisition Systems

1x6 SAR



The 1x6 SAR is basically a converter-per-channel system, but all included in one IC. Each channel has its own converter and sample/hold, so no analog multiplexing is required.

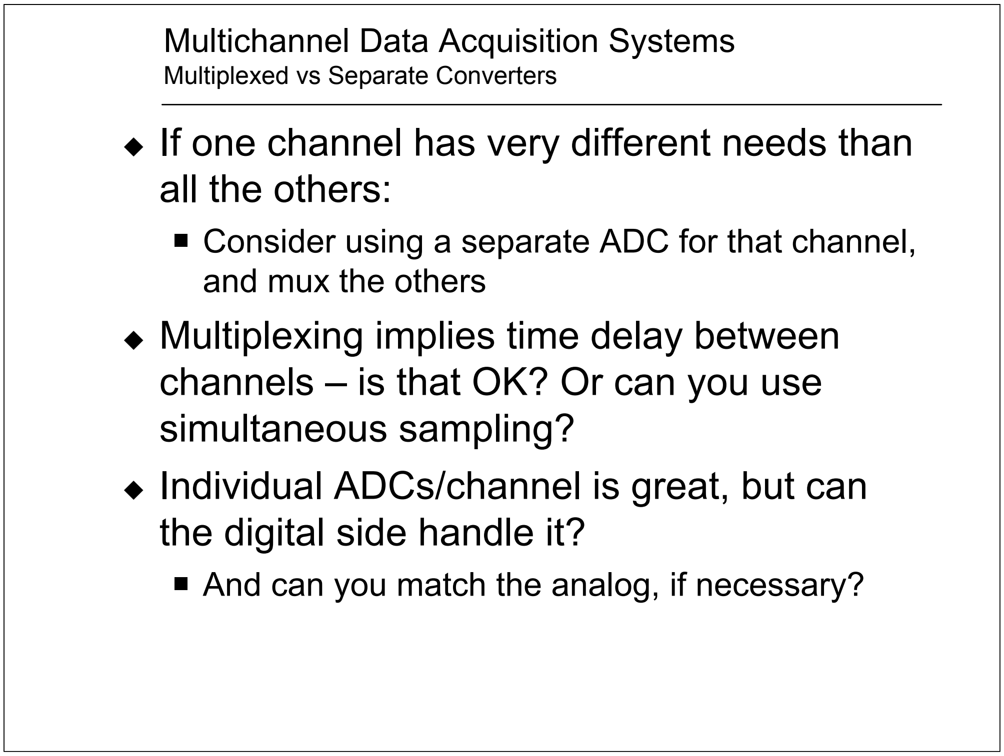
Multichannel Data Acquisition Systems
Pipeline



This is the THS1206, which is what we would call a 4x1 converter – 4 S/Hs multiplexed to one converter.

Multichannel Data Acquisition Systems

Using Multiple ADCs



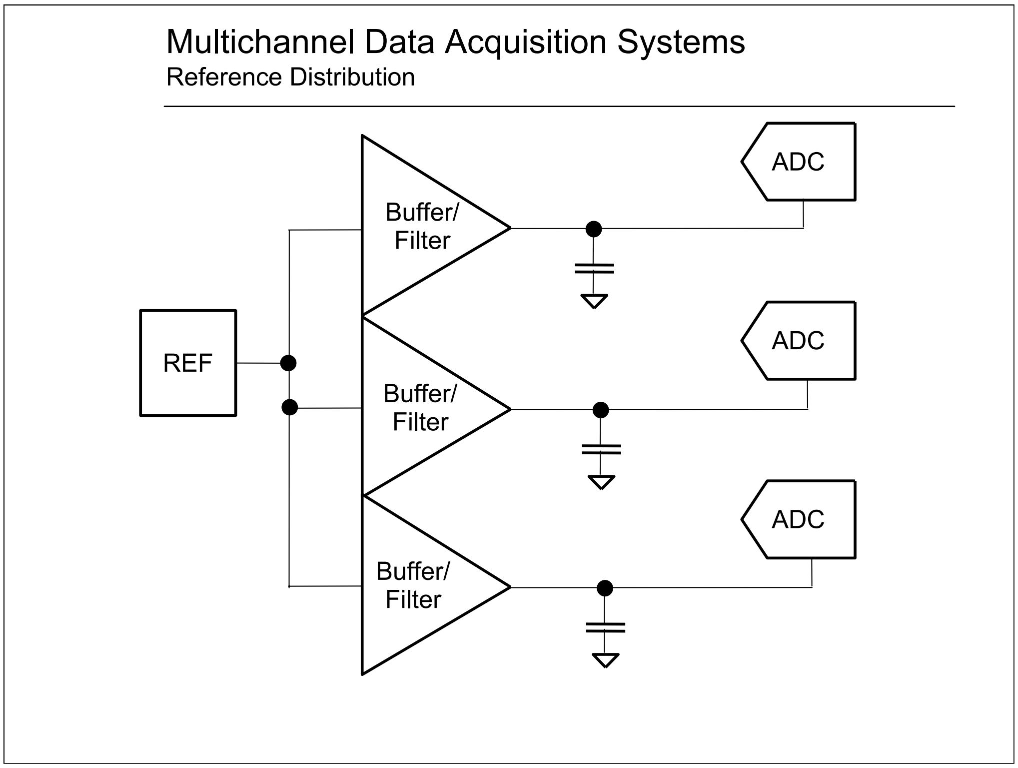
If your system consists of 7 thermocouples and 1 ultrasonic sensor, perhaps it doesn't make sense to try and multiplex all of those signals. Would it make more sense to use a high-speed ADC for the ultrasound path, and a multiplexed, slower ADC for the relatively slow temperature measurements? These days, the costs of ADCs have come down low enough that such a tradeoff is possible, and often results in higher performance. If you muxed those signals, you may have trouble keeping crosstalk from the ultrasonic channel from affecting your temperature measurements.

As we've seen, multiplexing means we'll only look at one channel at a time, so that there is a delay between the results of one channel vs. another. Within the time requirements of the system, is that OK? Or is simultaneous sampling required – and is it just sampling that's needed, or do you need the data all at the same time?

If so, you may need to consider using separate ADCs per channel. While this sells more ADCs for TI, there are some practical considerations that may advise against this. If you have all the converters convert at the same time, and your processor needs to read them all at the same time, does the processor have the resources (parallel/serial data ports) to do it? And if there's many channels and their time alignment must match, how confident are you that the signal conditioning matches, from channel-to-channel? How about over time/temperature? One nice thing about individual ADCs is you could calibrate them all separately to compensate for offsets and drifts of each channel – but this would be a very complex system.

Multichannel Data Acquisition Systems

Other Considerations



Reference distribution in multiple ADC systems is an interesting problem Certainly you wouldn't want to have multiple references if the results of the converters are all going to be compared and used in the same data set. Therefore, the system should have one central reference and the buffer/filter circuit. If only one buffer is used, make sure to have large bulk capacitors near the reference pin of each ADC.

Note that several buffers may be needed, as shown above, depending upon the system. Consider the reference loading of each converter, and buffer accordingly.

Multichannel Data Acquisition Systems
Summary

- Know your input signals
  - Speed, bandwidth
  - Time relationships to each other
- Choose the right scheme
  - Multiplexing
  - Simultaneous sampling
  - Multiple ADCs
- Choose the right converter architecture
  - SAR
    - Input Buffering and Drive Requirements
  - Delta-Sigma
    - Settling time of filters