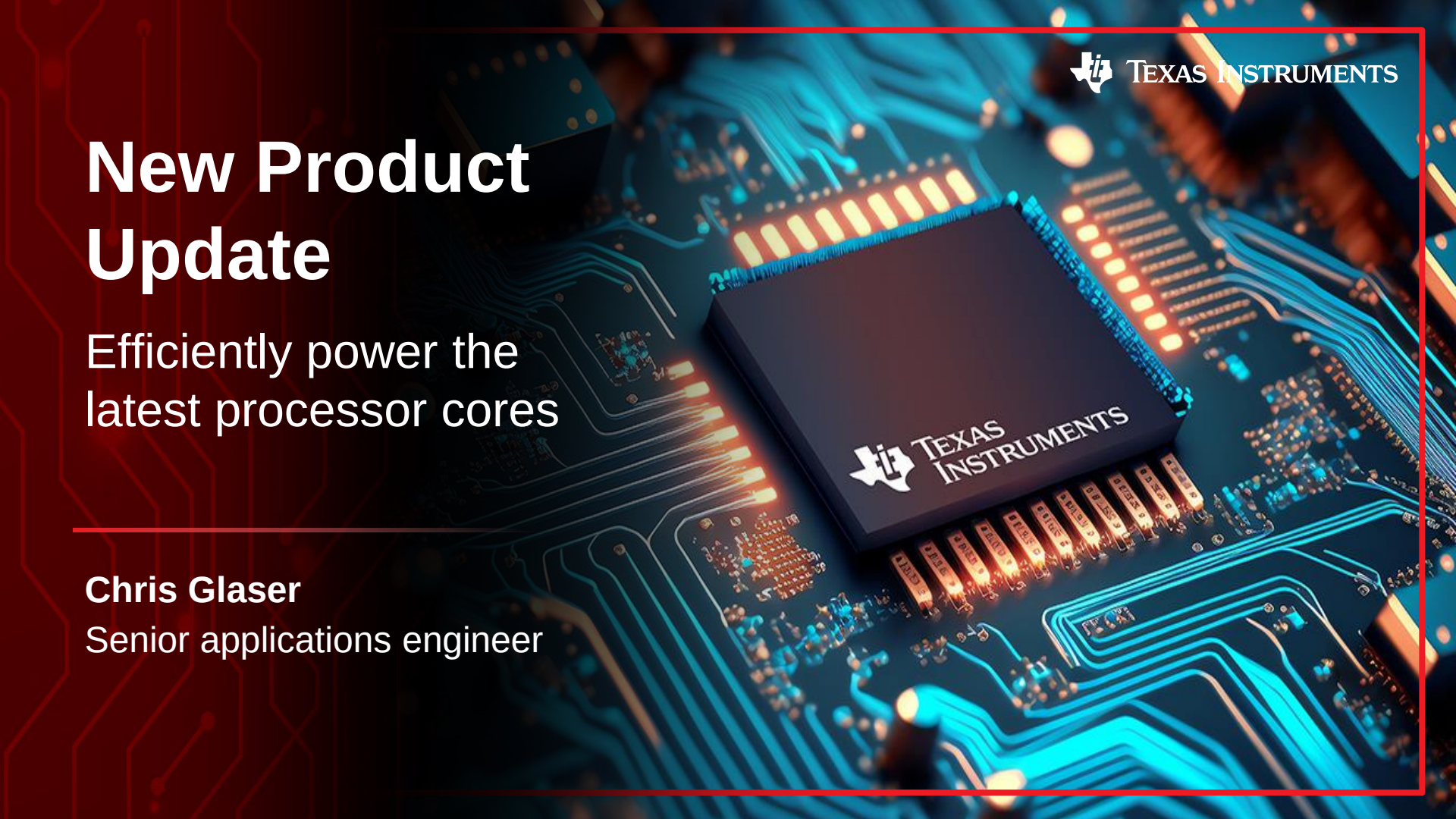
New Product Update

Efficiently power the latest processor cores



Chris Glaser
Senior applications engineer

Agenda

- Maintaining a high voltage accuracy at DC and during load transients
- Design example based on the JACINTO processor
- Small total solution size with the optimal amount of output capacitance
- Efficiency and good thermal performance

Processor core types: SoC, FPGA, DSP, ASIC, memory

XILINX

Micron

ALTERA

Qualcomm

MOBILEYE

BROADCOM

Jacinto™ Processors

Texas Instruments

Sitara™ MPU

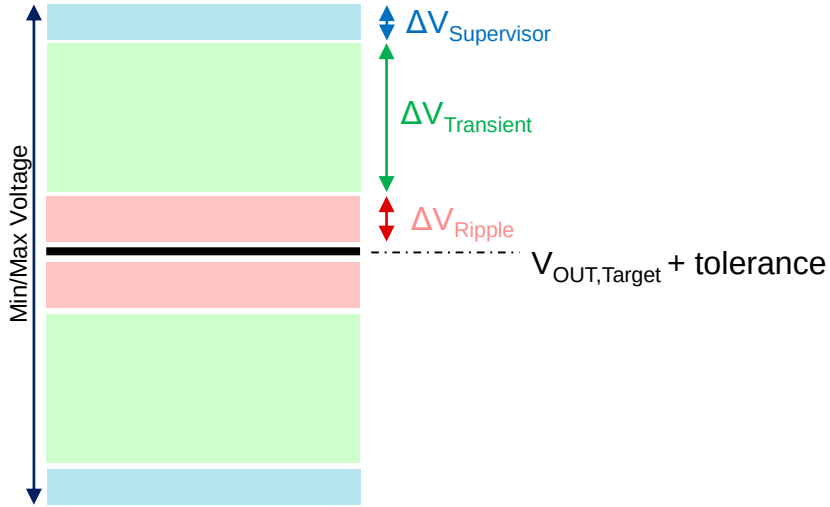
Texas Instruments

Numerous processor vendors → infinite applications!

Core supply for SoC, FPGA, DSP, ASIC, memory

Requirements	Solutions
• High output current	*up to 50 A single-phase, parallelable to 200 A+*
• Thermal performance	*High efficiency, very low $R_{DS(on)}$, power packages*
• Fast transient response	*enhanced-DCS-Control Topology, remote sensing*
• Tight accuracy	*<1% over temperature, fixed V_{OUT}, droop compensation*
• Low supply voltage	*down to 0.2 V for Core Supply and LPDDR5 Memory*
• Dynamic voltage scaling	*I^2C interface, V_{SELECT} function*

Core supply voltage tolerance



- Min/max voltage requirements
- Load step currents
- Ripple requirements
- Voltage for external supervisor required?
- Max current (DC and peak)
- DC accuracy (with remote sense)

Load transient is largest contributor to output voltage accuracy → drives output capacitance requirement

Example load transient requirement (Jacinto)

- V_{IN} = 3.3 V
- V_{OUT} = 0.8 V
- Accuracy +/- 3% (AC, transient), +/- 1% (DC)
- (1) Automotive (T_J max 125°C)
  - I_{OUTmax} 39.8 A
  - Load transient 27.9 A in 1 µs (11.9 A -> 39.8 A ->11.9 A)
- (2) Industrial (T_J max 105°C)
  - I_{OUTmax} 30.6 A
  - Load transient 18.7A in 1µs (11.9 A -> 30.6 A ->11.9 A)

Use this example

TPS62870/1/2/3

AEC-Q100 Grade 1 available

6 A / 9 A / 12 A / 15 A Stackable I²C Buck Converter in QFN w/ WF

Features

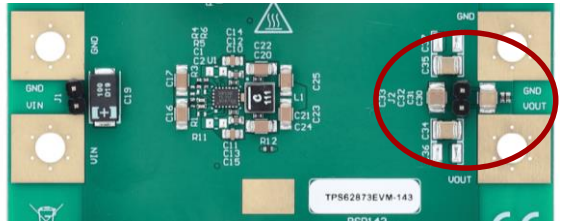
- Up to 15 A Output Current **with Remote Sense**
- 2.7 V to 6 V $V_{IN,}$ 1% output voltage accuracy
- **DVS/ AVS, 0.4 V to 0.71875 V with 1.25 mV step, 0.4 V to 1.0375 V with 2.5 mV step, 0.4 V to 1.675 V with 5mV steps and 0.8 V to 3.35 V with 10 mV step**
- **7 mΩ / 4.7 mΩ integrated power FETs**
- 1.5 MHz, 2.25 MHz, 2.5 MHz or 3.0 MHz Fsw with sync
- Adjustable soft start, adjustable compensation, Power Good
- **Stackability, I²C (optional), Spread Spectrum (optional)**
- Ease of power sequencing
- **Remote sense for core supply**
- Dynamic adaptation to processor loads, small steps for adjustable output voltage

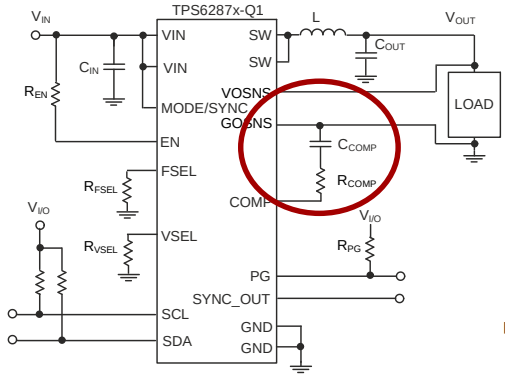
Applications

- **Auto: LPDDR5/ Infotainment & Cluster/ADAS**
  Reference design
- Industrial: IP network camera, ASIC core power supply, Vision & Smart City

Benefits

- Stackability: increase the load requirements and improve performance
- Functional safety capable: includes FIT, FMD and Pin FMA





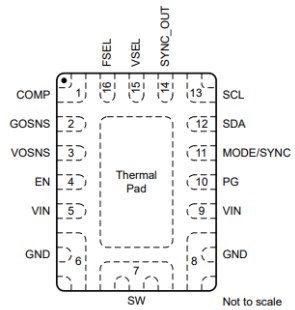
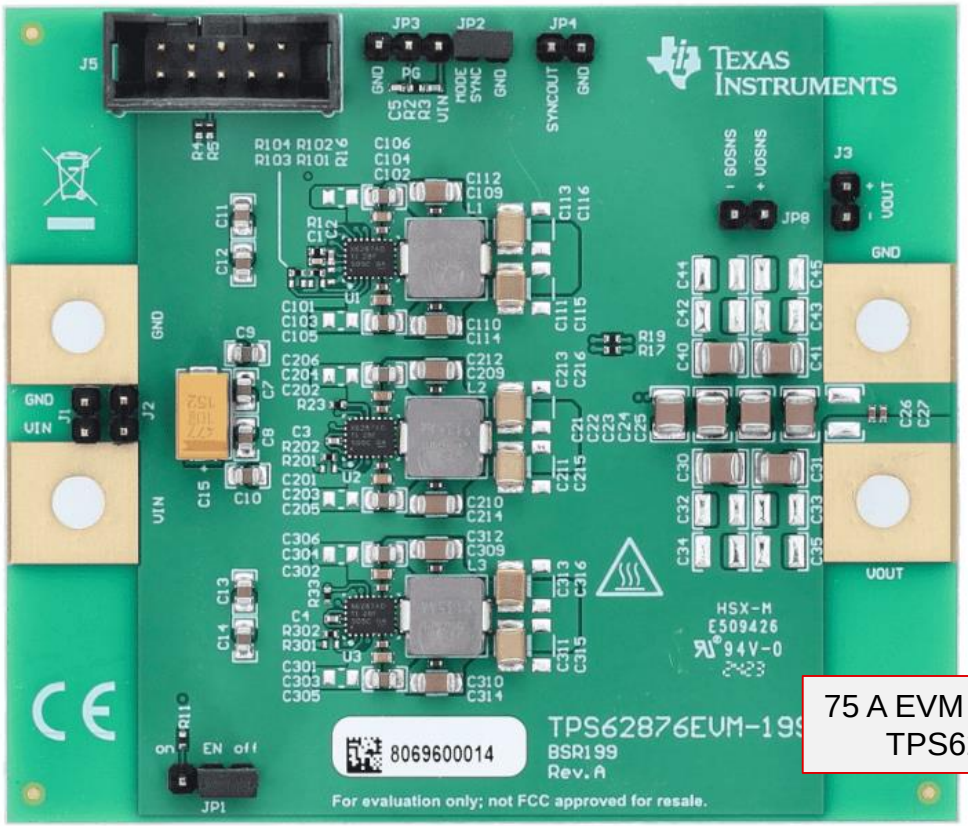


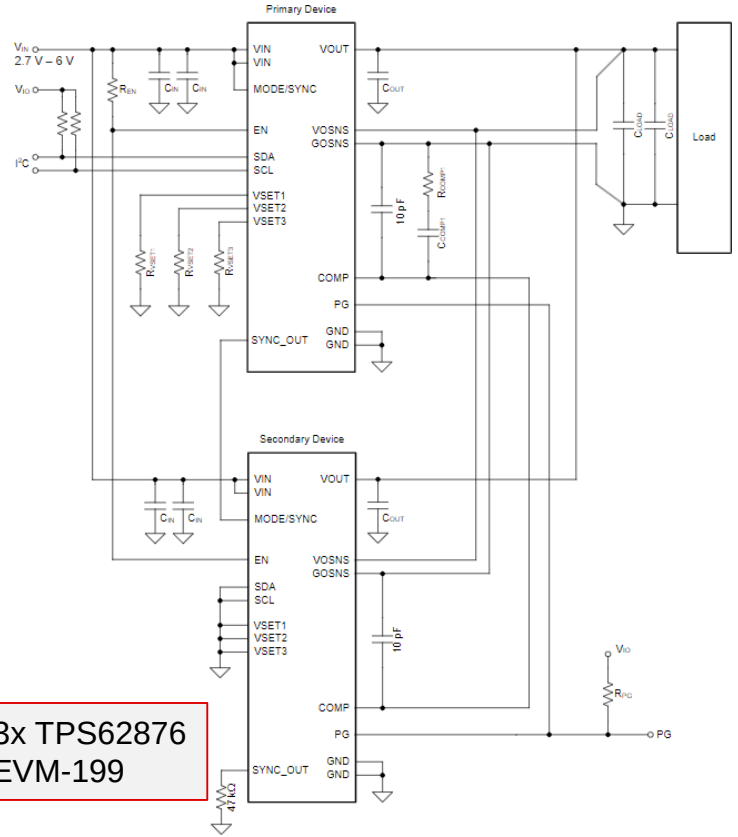
Figure 7-1. 16-Pin RXS VQFN Package (Top View)

3.55mm x 2.55mm QFN package

Texas Instruments

Outputs can be paralleled to support greater load currents





75 A EVM with 3x TPS62876
TPS62876EVM-199

Output capacitance and compensation calculator

PARAMETER	SYMBOL	VALUE	UNIT
Number of Phases	#	3	
Input Voltage	V_{IN}	3.3	V
Output Voltage	V_{OUT}	0.8	V
Load Current Step	$\Delta I_{OUT(step)}$	27.9	A
Maximum V_{OUT} Deviation	ΔV_{OUT}	3.0%	
		24.0E-3	V
Load Step Rise and Fall Time	t_r, t_f	1E-06	s
Error Amplifier Transconductance	g_m	1.5E-3	S
Internal Timing Parameter	τ	12.5E-6	s
Internal Timing Parameter Tolerance	TOL_{τ}	30%	
Switching Frequency	f_{SW}	2.25E+6	Hz
Switching Frequency Tolerance	TOL_{fSW}	10%	
Inductance	L	100E-9	H
Inductance Tolerance	TOL_{IND}	20%	
Maximum Bandwidth	BW_{max}	563E+3	Hz
Recommended Bandwidth	BW	200E+3	Hz
Target Bandwidth	BW_T	400E+3	Hz
Inductor Ripple Current	ΔI_L	0.9	A
Total Inductor Current Step Change	$\Delta I_{OUT(max)}$	28.3	A
Compensation Resistance (Calculated)	R_{Comp1}	1.30E+3	Ω
Compensation Resistance (Used)	R_{Comp1}	1.50E+3	Ω
Minimum Output Capacitance (regulated case)	$C_{OUT(min)(reg)}$	666.37E-6	F
Minimum Output Capacitance (saturated case)	$C_{OUT(min)(sat)}$	139.65E-6	F
Minimum Output Capacitance (Calculated)	$C_{OUT(min)}$	666.37E-6	F

Use multiple phases for higher currents

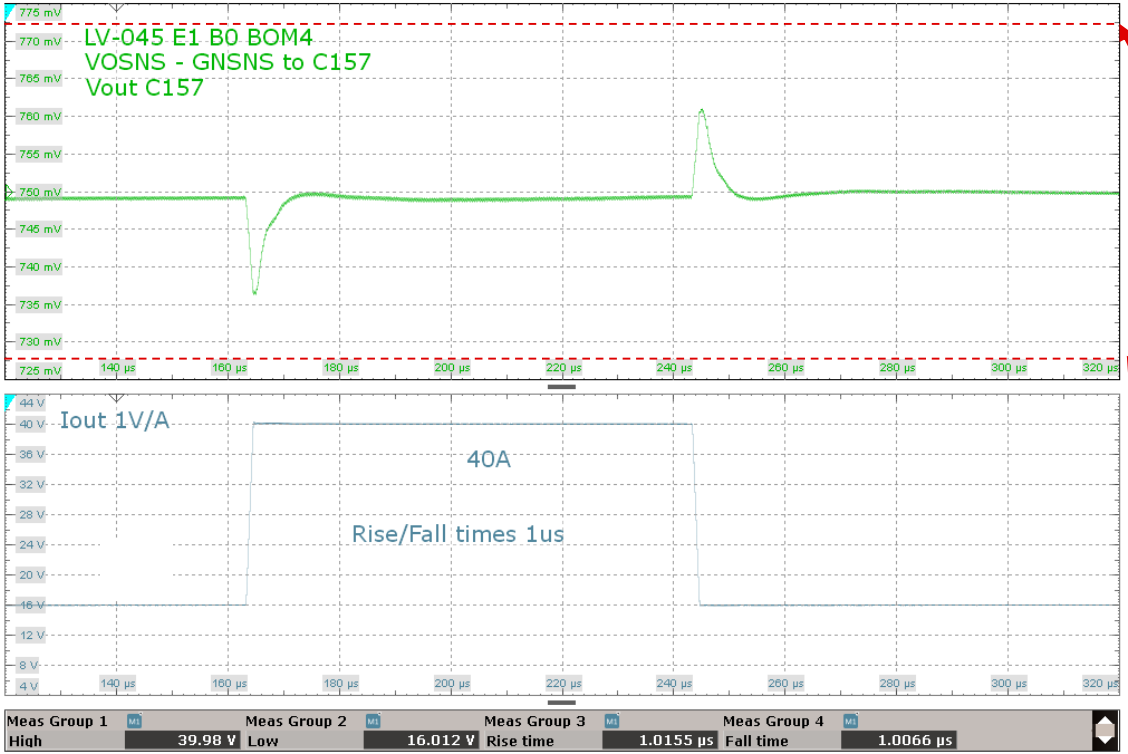
Load transient parameters

Design knobs

More knobs below

https://www.ti.com/product/TPSM8287A12#design-development

Load transient bench results



Spec target met with margin (component tolerances, etc.)

TPS62874/5/6/7

15 A / 20 A / 25 A / 30 A Stackable I²C Buck in QFN w/ WF

AEC-Q100 Grade 1 available

Features

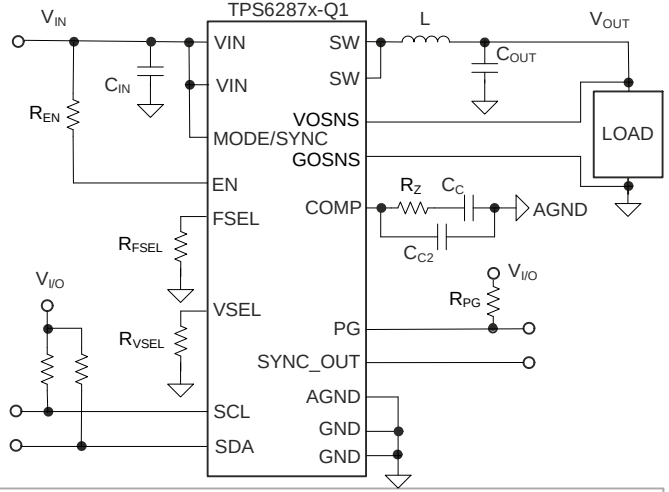
- 2.7 V to 6 V V_{IN}
- Device Temperature Grade 1 (Ta = -40˚C to 125˚C)
  - - 40ºC to 150ºC junction temperature range
- **DVS, 0.8% output voltage accuracy**
  - **0.4 V to 0.71875 V with 1.25 mV steps**
  - **0.4 V to 1.0375 V with 2.5 mV steps**
  - **0.4 V to 1.675 V with 5 mV steps**
- **2.6 mΩ / 1.5 mΩ integrated power FETs**
- 1.5 MHz, 2.25 MHz, 2.5 MHz or 3 MHz fsw; syncable
- **Stackability, I²C (optional), Spread Spectrum (optional)**
- 4.05 mm x 3.05 mm QFN Package with wettable flanks
- Functional safety capable
- **Droop compensation**

Applications

- ADAS Sensor Fusion, ECU/Domain Controller, Digital Cockpit
- Optical Network
- FPGA, ASIC & digital core supplies

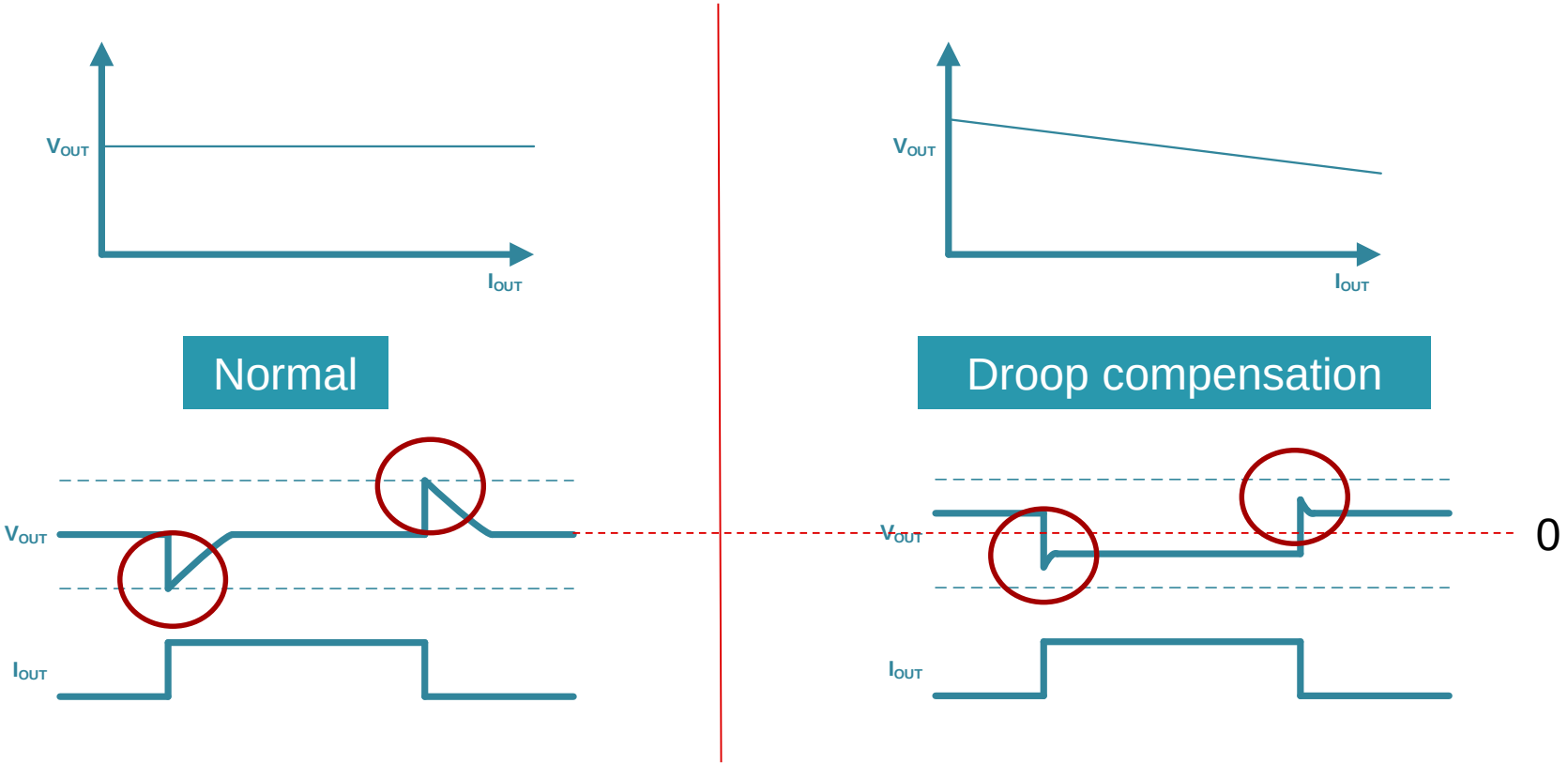
Benefits

- **Support load currents up to 30 A out of a small cost effective QFN package**
- **Remote sense for core supply allows to compensate PCB loss**
- Enables faster evaluation through I²C interface
- **Stackability to allow for smaller inductors and better heat distribution on the PCB**
- Dynamic adaptation to processor loads, small steps for adjustable output voltage



Texas Instruments

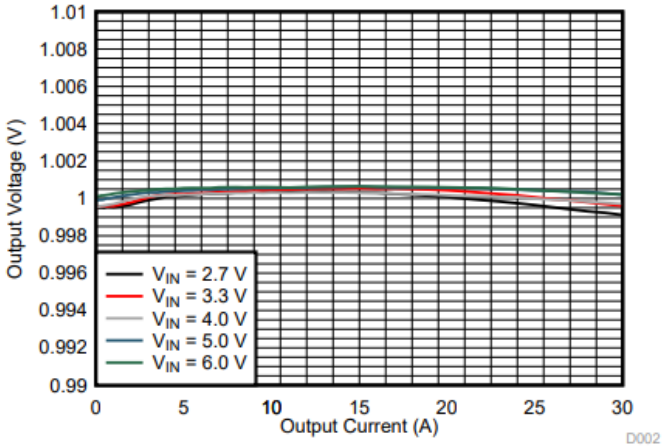
What is droop compensation?



What is droop compensation?

Extra room for load transients!

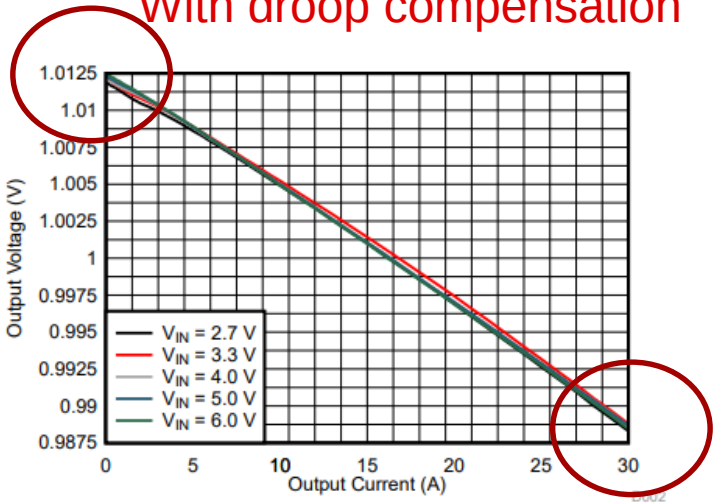
Normal



V_{OUT} = 1.0 V PWM; droop disabled T_A = 25°C

Figure 9-12. Output Voltage Versus Output Current

With droop compensation



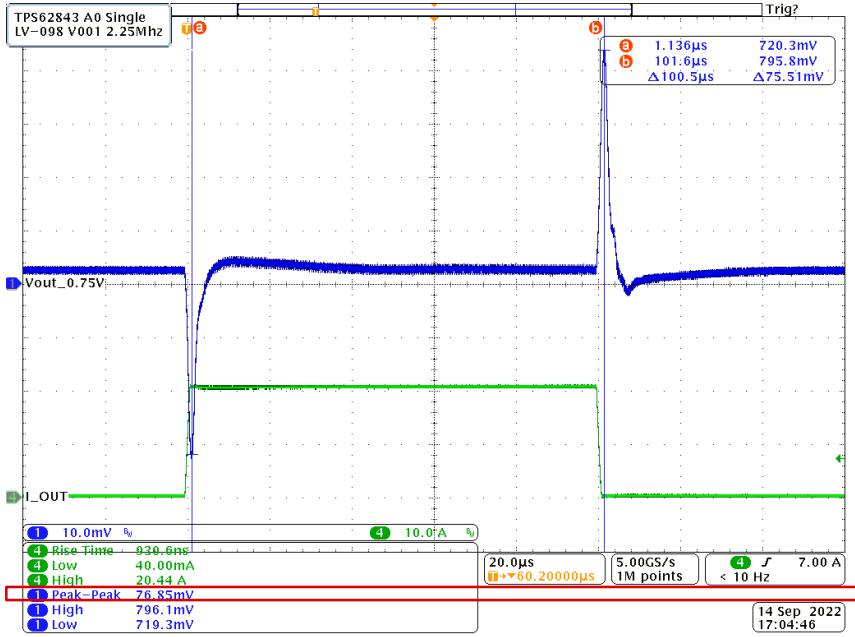
V_{OUT} = 1.0 V PWM; TPS62877 droop enabled T_A = 25°C

Figure 9-13. Output Voltage Versus Output Current

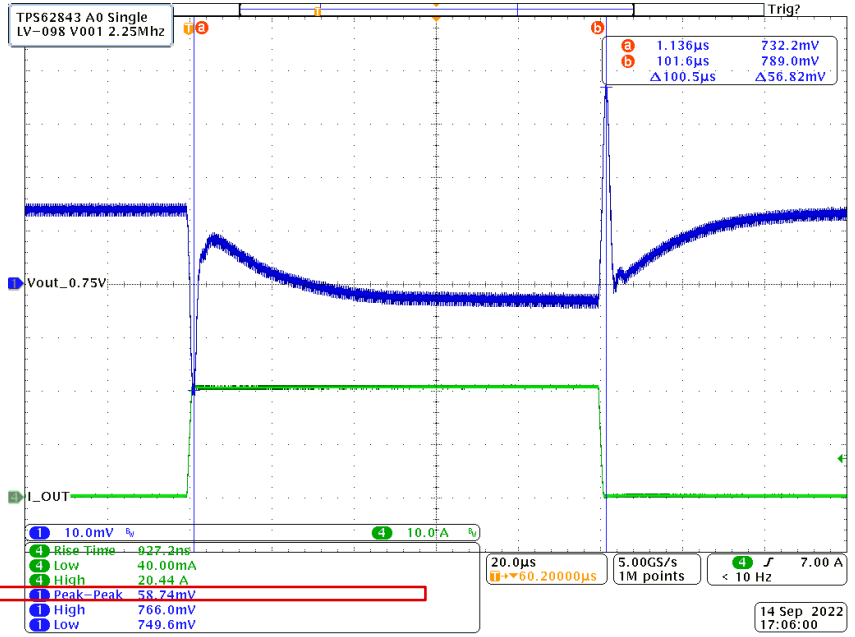
Load transient | ~25% peak-to-peak improvement

TPS62876EVM-198: Load Step 0↔20 A in 1 µs, V_{out}=0.835 V

Droop disabled



Droop enabled



Less output capacitance required!

TPSM8287A06/10/12/15

New
Sampling on TI.com

6 A & *12 A* / 10 A & 15 A Scalable Buck Module Family with I²C

Features

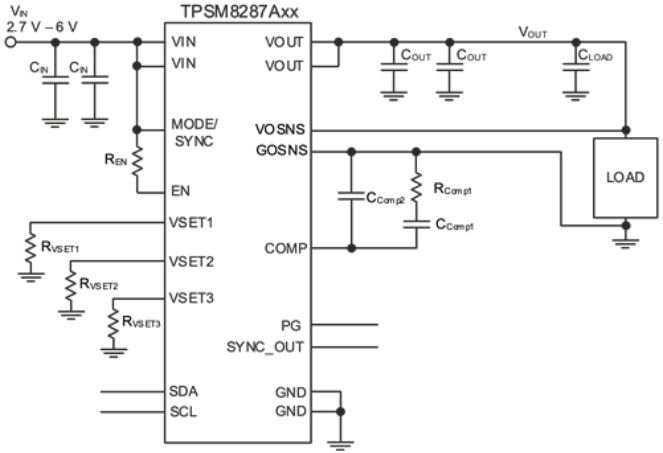
- Up to 15 A Output Current **with Remote Sense**
- 2.7 V to 6 V V_{IN}
- DVS/ AVS with 1% output voltage accuracy
  - 0.4 V to 0.71875 V with 1.25 mV step
  - 0.4 V to 1.0375 V with 2.5 mV step
  - 0.4 V to 1.675 V with 5 mV steps and
  - 0.8V to 3.35 V with 10 mV step
- **Selectable start-up Voltages (50 mV steps) between 0.4-3.35 V**
- **High Efficiency and 19.5 °C/W $R_{\theta JA}$**
- **Excellent EMI performance through Integrated Caps and L**
- 1.5 & 2.25 MHz Fsw, Spread Spectrum Clocking (opt) or sync
- **Parallel operation to increase Output current range**
- 4.5 mm x 6.5 mm x 1.8 mm QFN Package with Thermal Pad (6 A & *12 A*)
- 4.5 mm x 6.5 mm x 4.0 mm QFN Package with Thermal Pad (10 A & 15 A)

Applications

- FPGA, ASIC, Memory & digital core supplies
- Datacom modules, PLCs
- Communication equipment, wireless infrastructure
- Optical Network, storage

Benefits

- **Support load currents of 12 A / 15 A up to 85°C ambient temp with a total BOM size of 77mm²**
- **Remote sense for core supply**
- **Parallelable to allow simple current increase (e.g. larger FPGA need) and better heat distribution on the PCB, lower ripple**
- Dynamic adaptation to processor loads, small steps for adjustable output voltage



Designing for smallest size

Small size around IC

Minimum C_{out} at the load

Load transient bench results

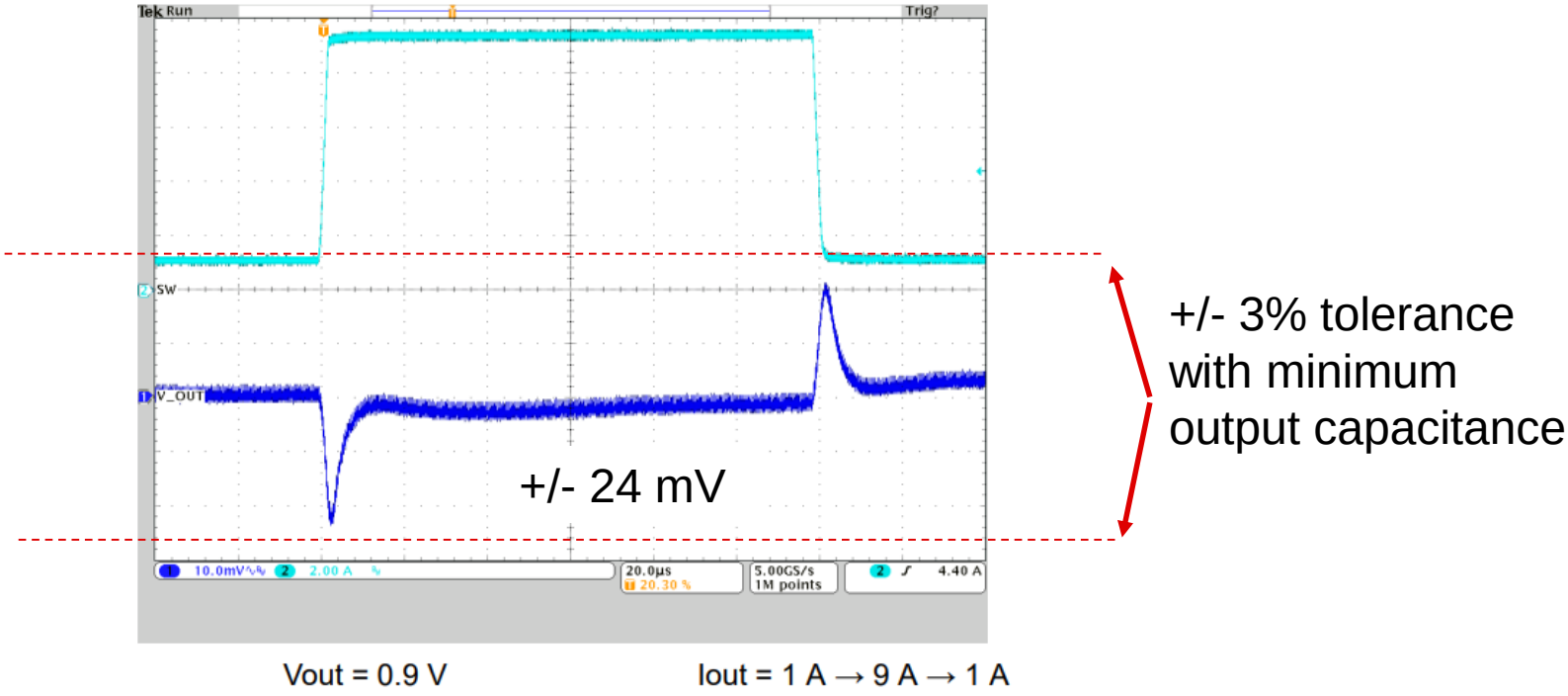
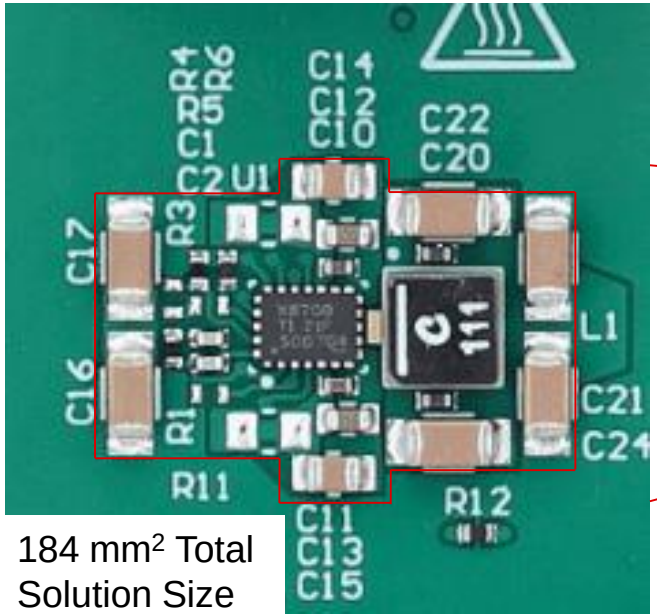


Figure 9-14. Load Transient Response
TPSM8287A12BBS

Power module gives a 58% smaller solution size

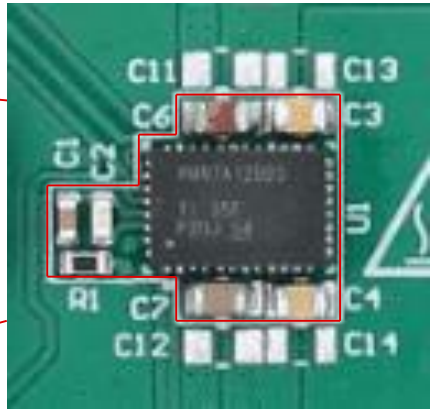
TPS62873-Q1 EVM



184 mm^2 Total Solution Size

Component count: 19

TPSM8287A EVM



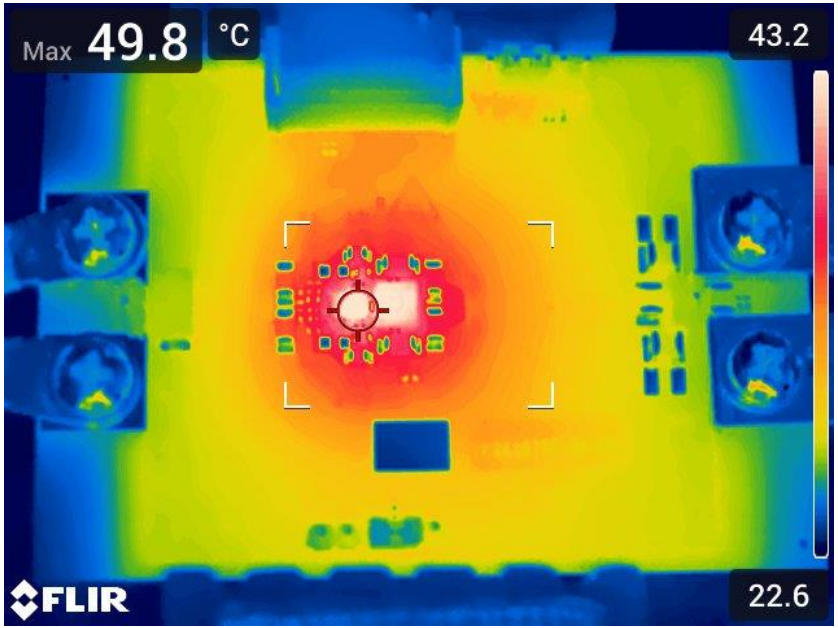
77 mm^2 Total Solution Size

Component count: 8

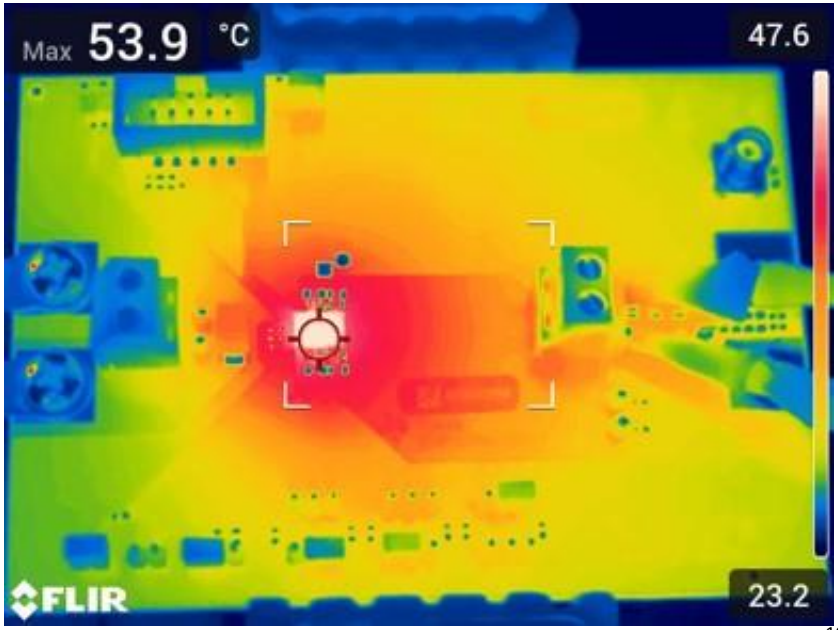
Low temperature rise at full load for both devices

Thermal performance (5 V_{in}, 0.9 V_{out}, 12 A load)

TPS62873-Q1 EVM



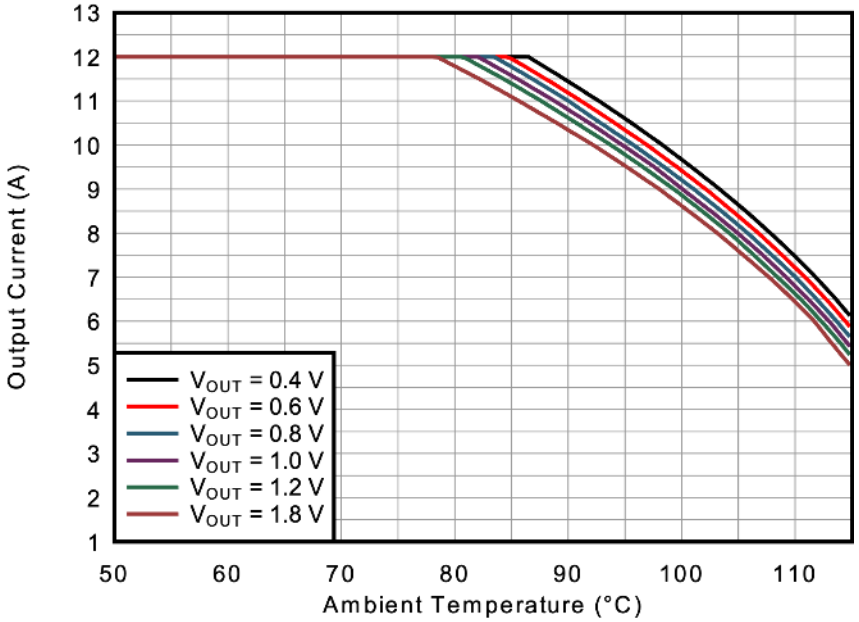
TPSM8287A EVM



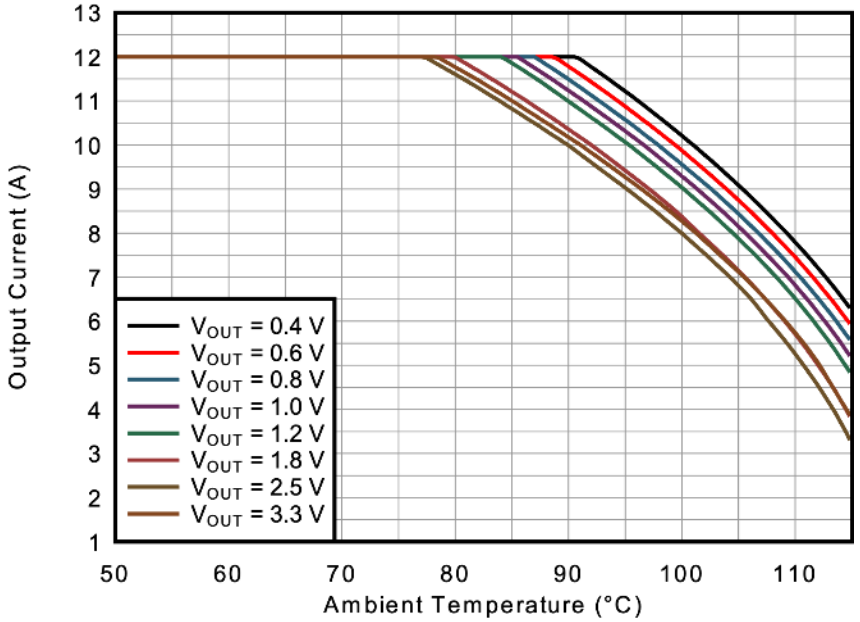
TPSM8287A12BAS | Safe Operating Area (SOA)

No derating up to ~80°C

V_{IN} = 3.3 V



V_{IN} = 5 V



Conclusion

- Enable lower core voltages and increased load current for the latest processors
- Maintain a high voltage accuracy at DC and during load transients
- Efficiency and good thermal performance
- Small total solution size with the optimal amount of output capacitance

Getting started

You can start evaluating this device leveraging the following:

Content type	Content title	Link to content or more details
Product folders	**TPS62873-Q1** and **TPS62873** (6 A/9 A/12 A/15 A) **TPS62876-Q1** (15 A/20 A/25 A/30 A) **TPSM8287A** (6 A/10 A/12 A/15 A) power module	Link Link Link Link
Technical blog content	**How to deliver current beyond 100 A to an ADAS processor**	Link
Processor power trees	**AM68x Processor Power Solutions for Industrial Applications** **MobileyeEyeQ6L – Semi Discrete Power Tree**	Link Link
Application notes	**Operating TPS6287X-Q1 Devices in a Stacked Configuration** **Understanding SOA Curves to Operate at High Output Currents and Temperature**	Link Link

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For more information on the New Product Update series, calendar and archived recordings

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