Webinar

Common mistakes in power supplies using GaN devices - Part 2

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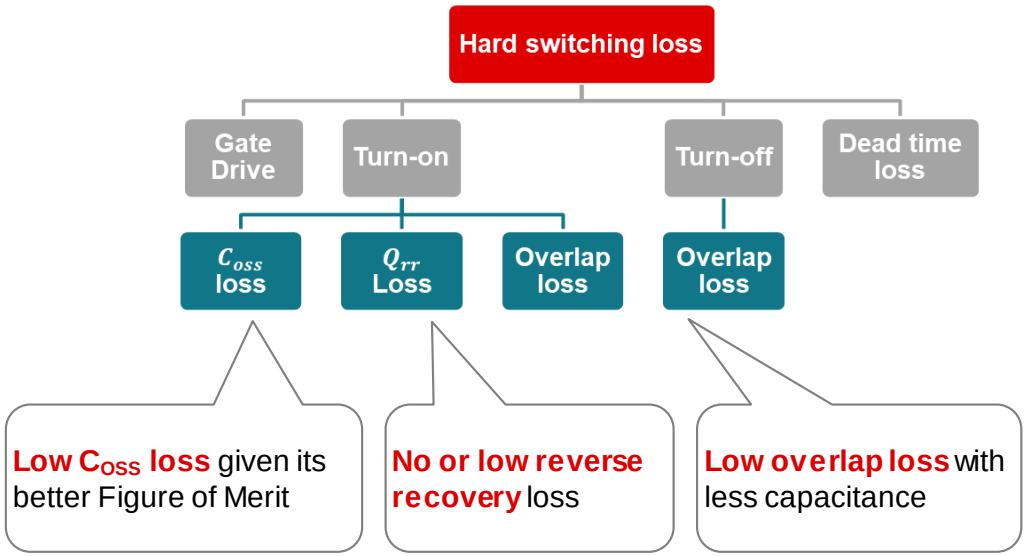
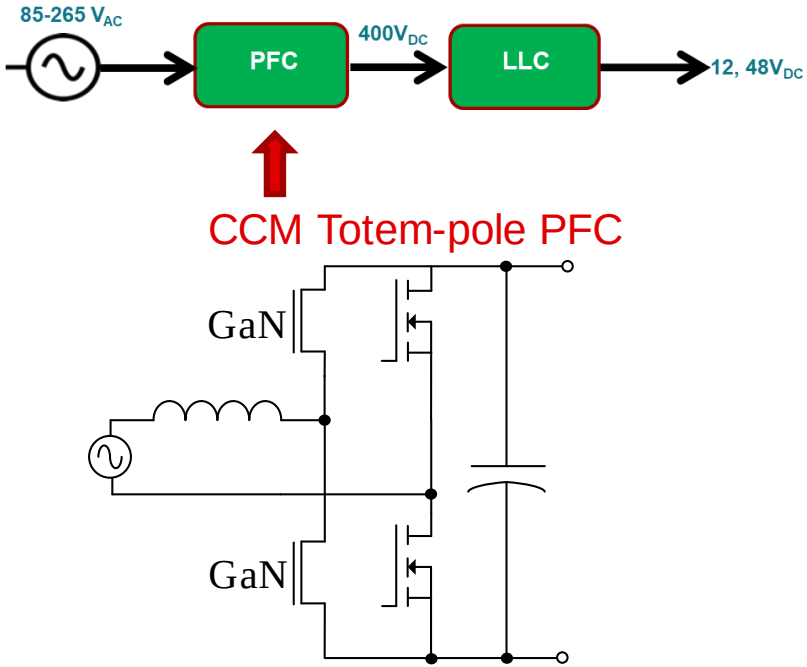
Why wide bandgap device in hard-switching converters?

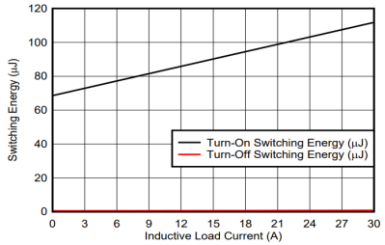
Wide bandgap device benefits





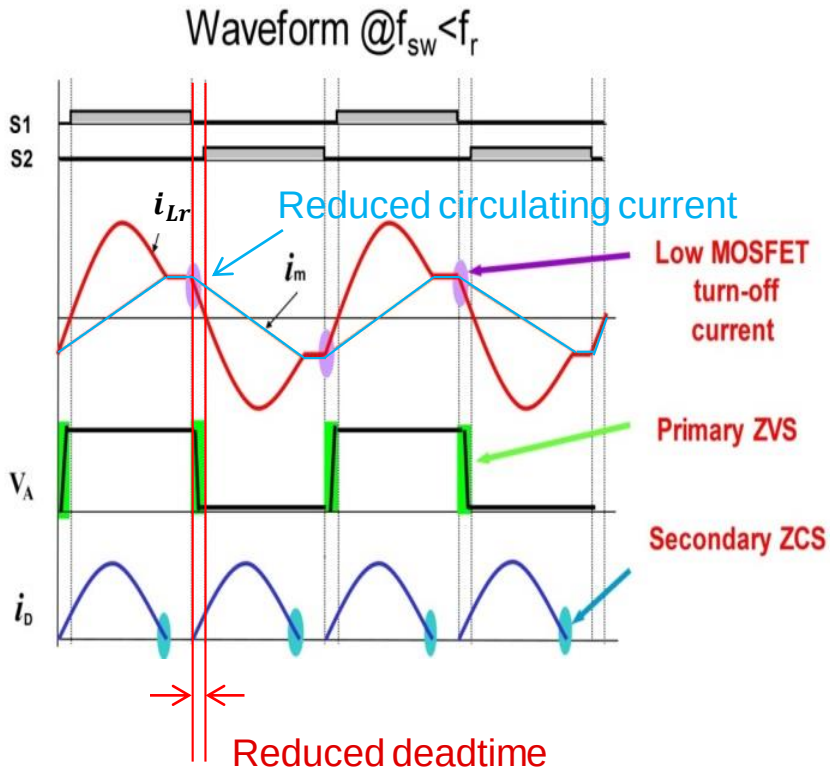
Why wide bandgap device in soft-switching converters?

- **Reduced output capacitance C_{oss}**
  - Reduces dead-time
  - Low transformer magnetizing current to minimize circulating current loss & eddy loss.
- **Reduced turn-off overlap and gate driver losses**



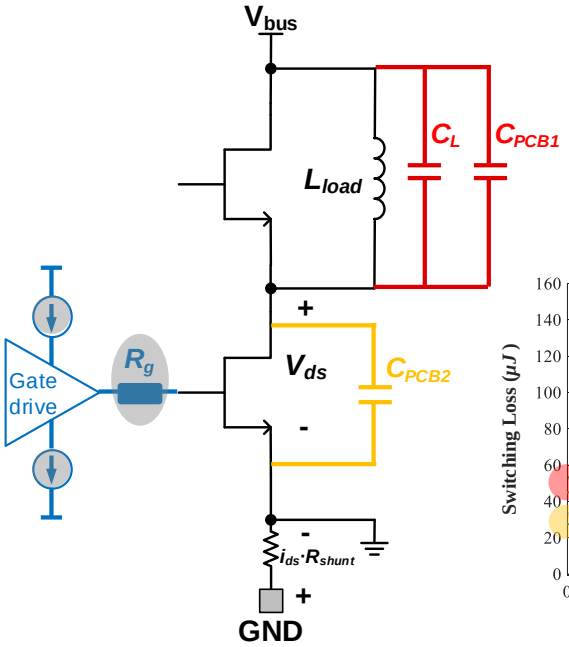
Negligible turn-off loss in TI GaN with gate driver integration

- **High power density in system**
  - GaN enables higher f_{sw} to reduce magnetic components, and enables magnetic integration.

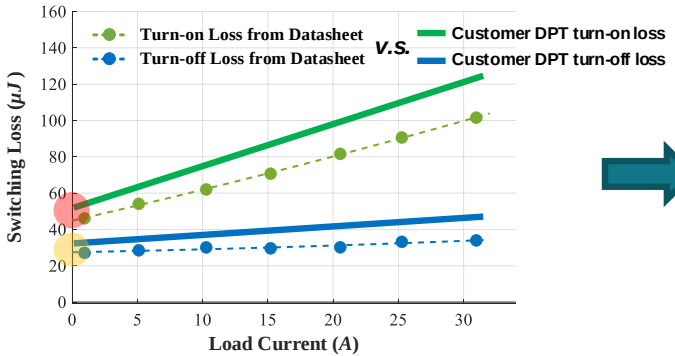


1) Why actual switching loss can be different from datasheet?

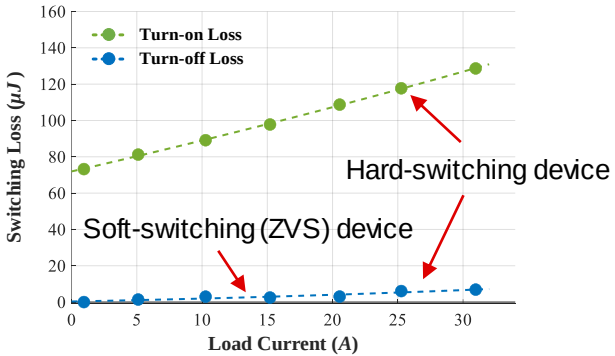
- Parasitic capacitance from load inductor C_L and PCB C_{PCB} leads to additional C_{oss} loss in hard-switching conditions.
- Interpret the datasheet loss correctly to applications
- Gate driver differences:
  - Gate drive strength (source/sink capability), R_g
  - Gate drive layout



Double Pulse Test (DPT)

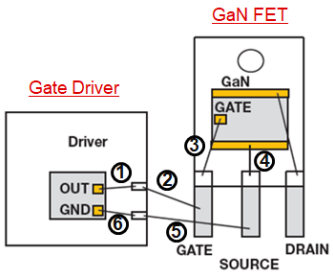


Datasheet Loss



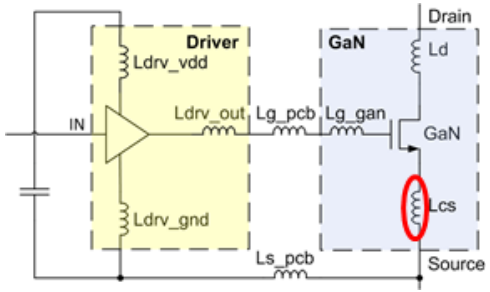
Device Hard-switching Loss

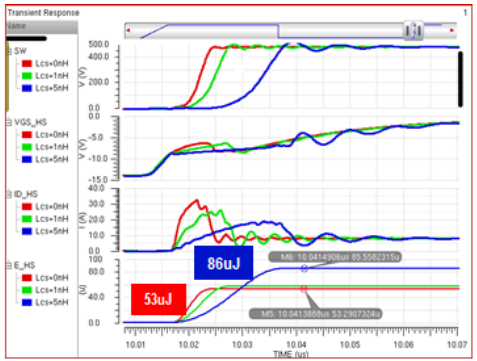
Gate driver layout affects switching loss



- **Common Source Inductance (CSI)**
  - Slows V_{DS} transitions.
  - Higher overlap losses (Hard-Switching).
  - Longer dead-times (Soft-Switching).
- **Gate Loop Inductance**
  - Limit peak gate current: slow down gate drive and induce high overlap losses in hard switching.
  - Gate overstress reliability risk.
  - Miller shoot-through risk.

Common Source Inductance Effect

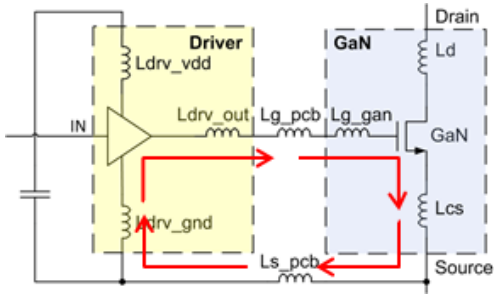


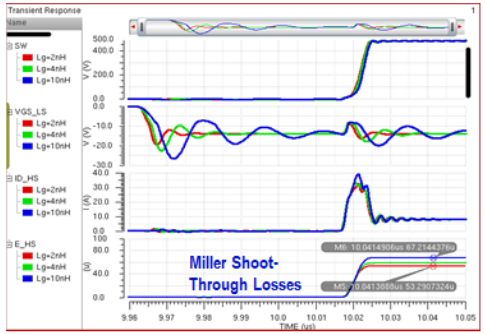


High-side turn on versus common-source inductance:
red = 0 nH, green = 1 nH, blue = 5 nH

Limits peak I_{DS}, De-biases V_{GS}

Gate Loop Inductance Effect





Low-side hold-off versus gate-loop inductance
red = 2 nH, green = 4 nH, blue = 10 nH

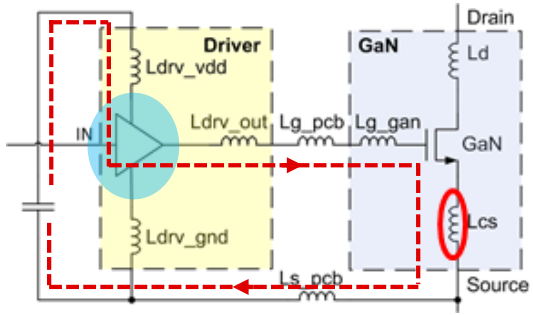
Limits peak I_{GATE} & slows down dV_{DS}/dt
Causes V_{GS} ringing & Miller shoot-through

Gate drive optimizations

- **Discrete Layout in PCB**

  Reduce cross-talk: gate drivers with active miller clamping is preferred for high *dv/dt* operation.

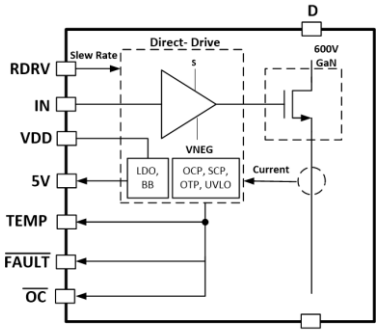
  Reduce gate loop inductance: Place bypass cap closer and use vertical loop in PCB.

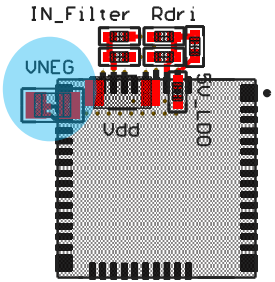


Reduce L_{cs}: Kelvin source connection for gate drive loop

- **Gate Drive Integration**

  Gate driver integration benefits:
  - The gate loop inductance in between the driver and GaN is minimized.
  - Gate drive strength and noise immunity are better controlled.





Layout: external bypass capacitor needs to be placed close to the driver supply.

LMG342x / LMG352x

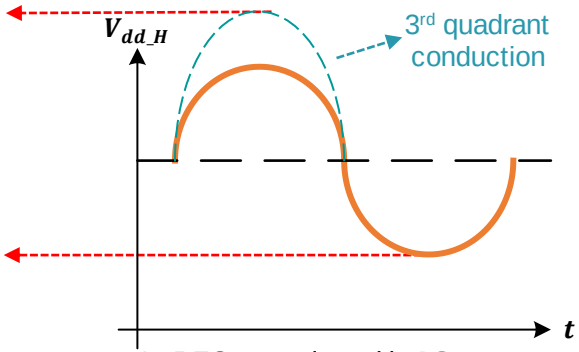
2) Why bootstrap needs proper designs in WBG devices?

- **Challenges in Bootstrap Circuit in GaN / SiC**

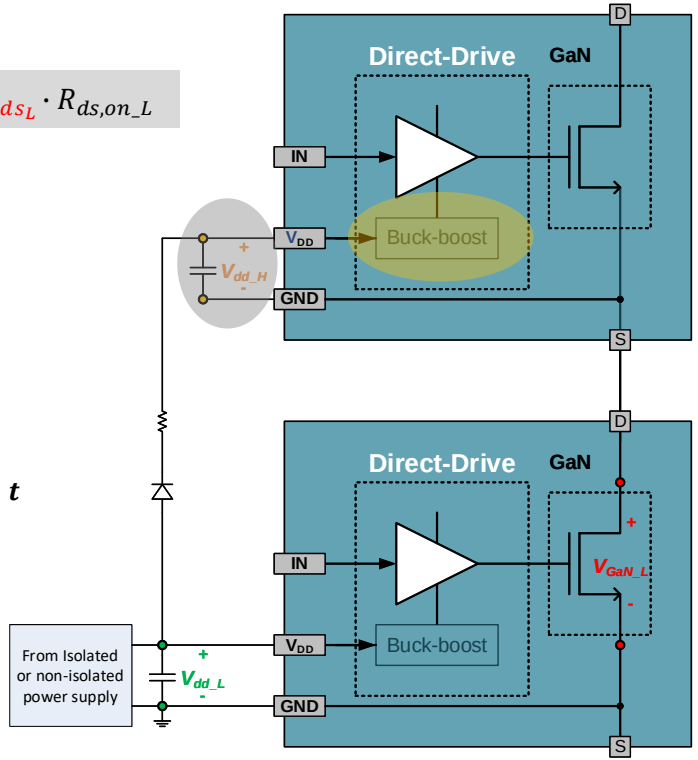
$$V_{dd\_H} \approx V_{dd_L} - V_{diode} - V_{GaN\_L} \approx V_{dd\_L} - V_{diode} - I_{ds_L} \cdot R_{ds,on\_L}$$

The peak drive voltage can exceed the maximum V_{gs} rating in GaN devices.

The valley drive voltage can affect the on-resistance and switching speed of high-side devices.



In PFC operation with **AC** current, V_{dd_H} varies with peak and valleys.

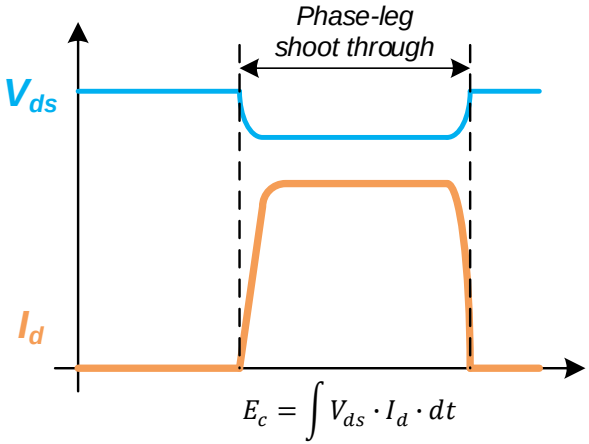


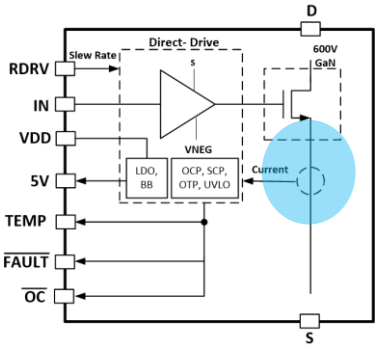
- **Solutions:**
  - Add pre-regulation circuits (e.g. buck-boost converter) such that the output for drive voltage is stable.

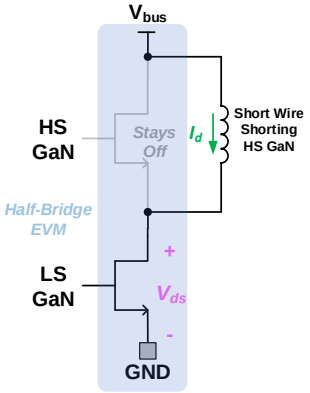
3) Why fast SCP is needed in WBG device?

- During short circuit, device is dissipating more energy and cause over-heating.
- SiC / GaN has **smaller chip size**, thus shorter short-circuit withstand time with less thermal capacity.

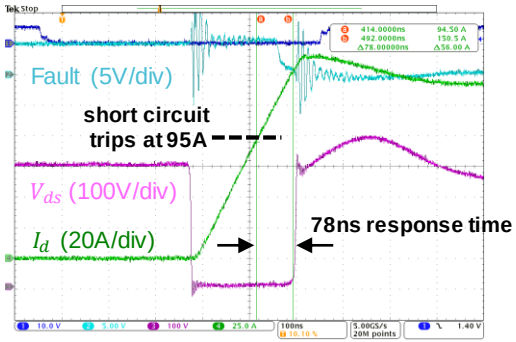
- **Integrated Short Circuit Protection**
  - Provides fast response time with accurate tripping points.
  - No external components.







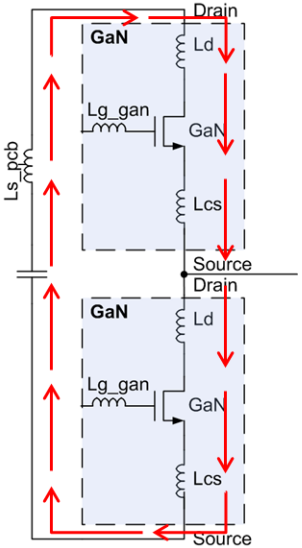
Short Circuit Test Diagram

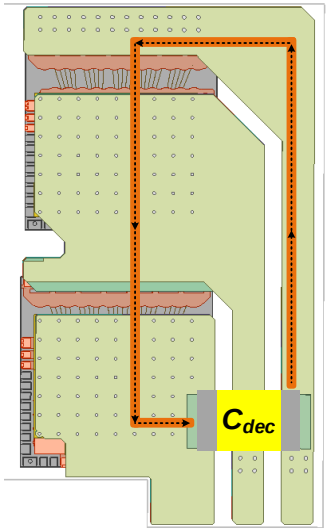


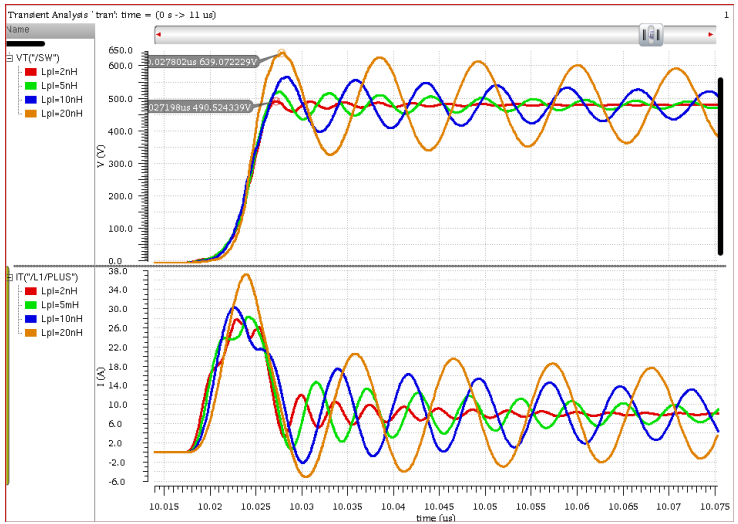
Short Circuit Test at 400V

4) Why power loop layout is critical?

- **Large Power Loop Inductance will**
  - Increase ringing and cause EMI concerns
  - Increase voltage spikes
  - Induce noises causing signal integrity issue



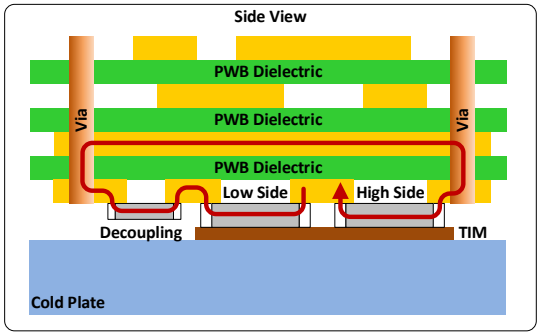


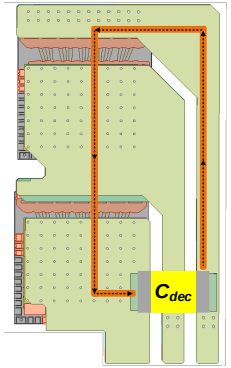


V_{SW} ringing versus power loop inductance
red = 2nH, green = 5nH, blue = 10nH, orange = 20nH

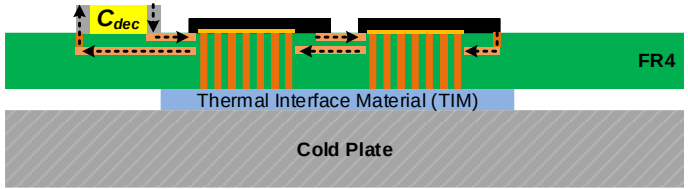
Good practice for power loop layout

- **Good Practice Procedures**
  - Place GaN devices and decoupling capacitors close together.
  - Use multiple ceramic decoupling capacitors with low-inductance.
  - Vertical loop: use wide return path in the **adjacent layer** for inductance cancellation.



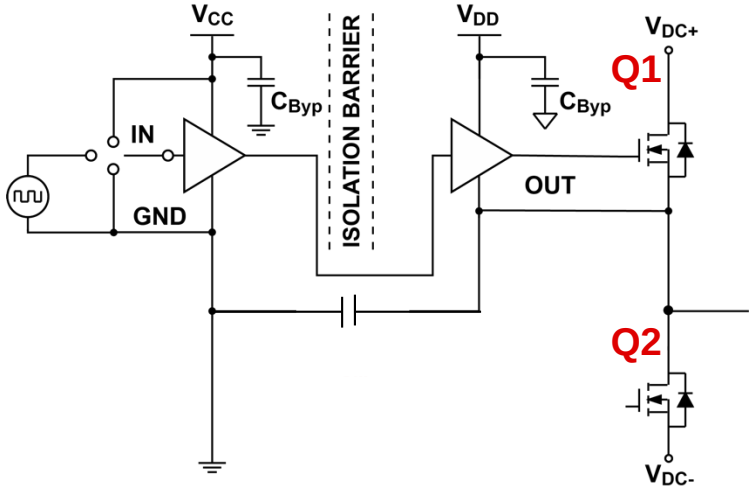


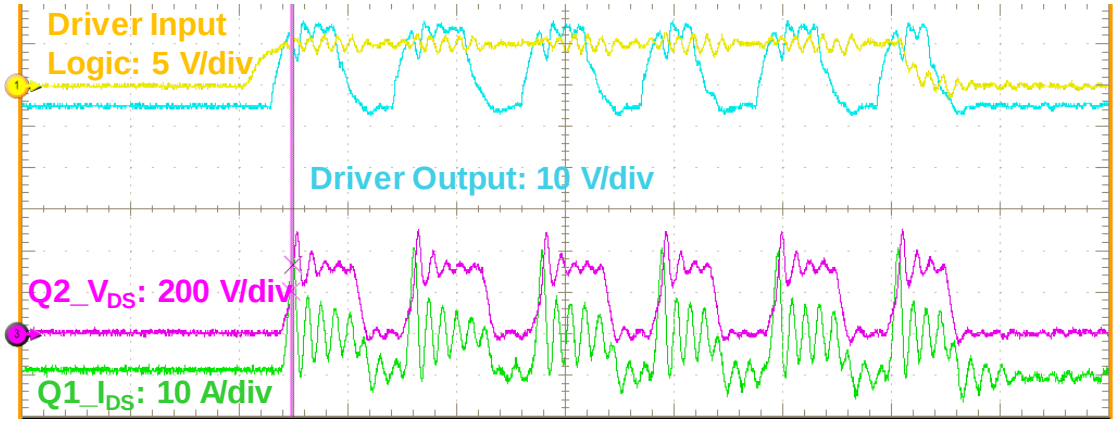
L_{ds} = 12.7 nH



L_{ds} = 2.0 nH

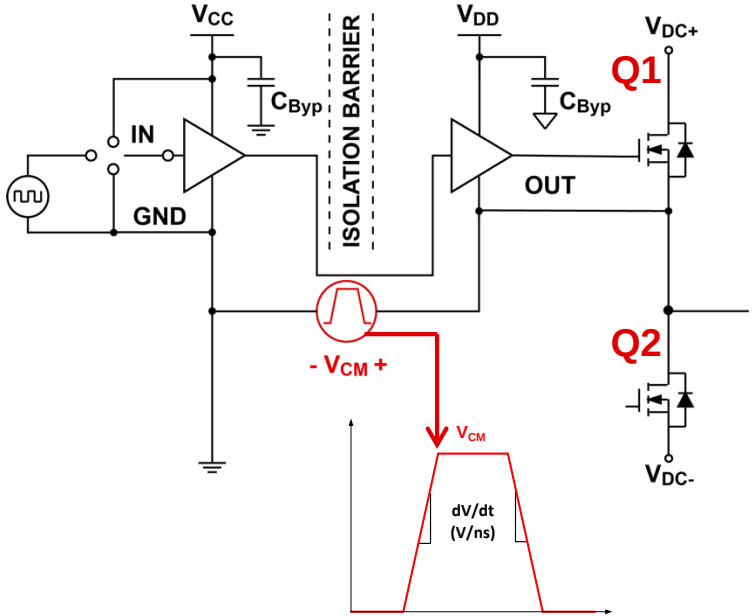
5) Why driver output doesn't follow input?



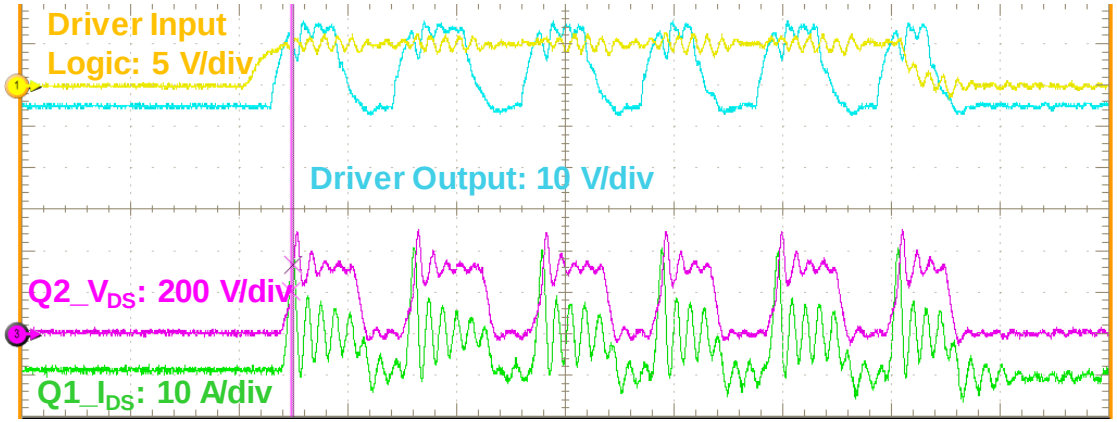


5) Isolated driver doesn't have enough CMTI capability

- **Without good common mode transient immunity (CMTI), parasitic noise currents could cause malfunction of the driver which includes missing pulse, excessive propagation delay, high or low error or output latch**



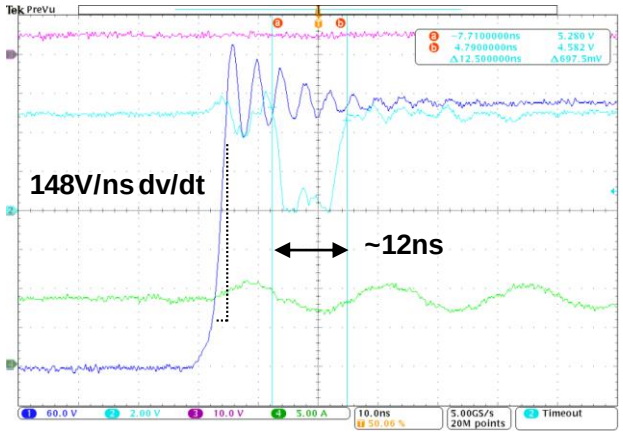
CMTI Failure Example



Time: 100 ns/div

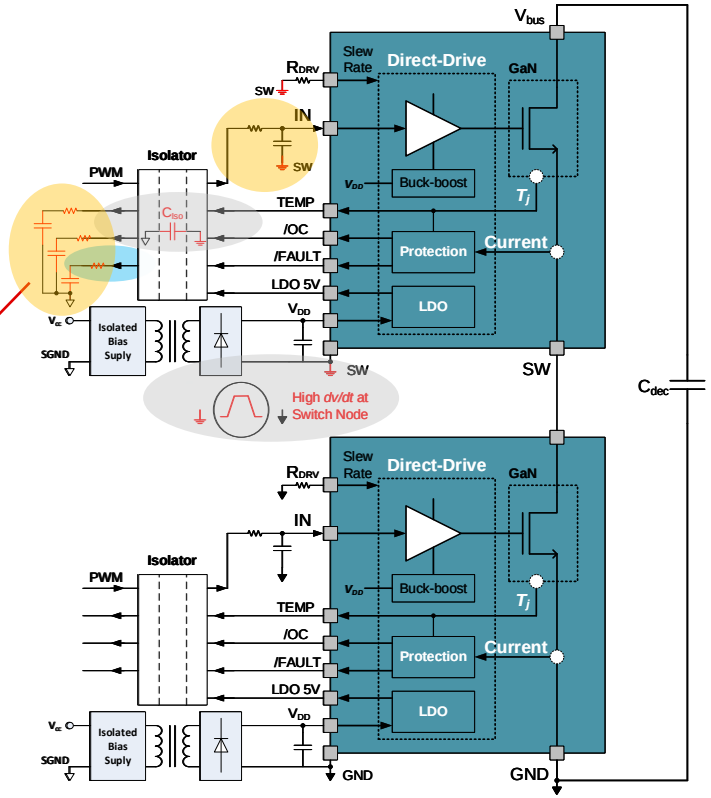
6) Why a false signal on isolator output?

- The isolator's insufficient CMTI is causing the glitch at isolator output.
- **Solution**
  - Choose higher CMTI isolator
  - Isolator with default low output is preferred
  - An RC filter is recommend on the **high-side isolator's output**



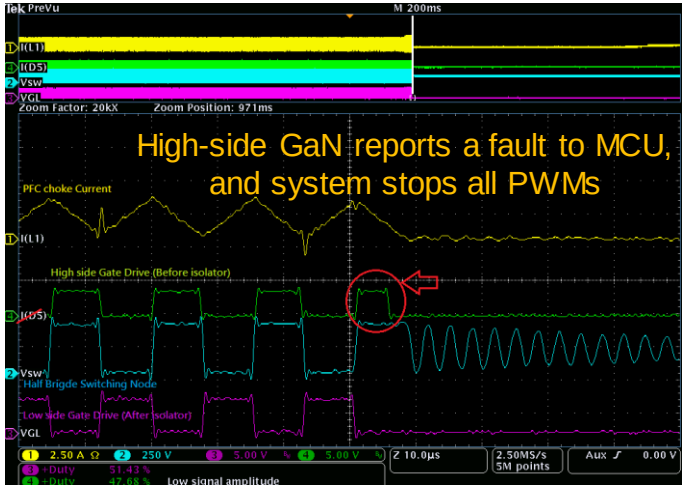
V_{ds} (60V/div)

HS Fault after Isolator (2V/div)

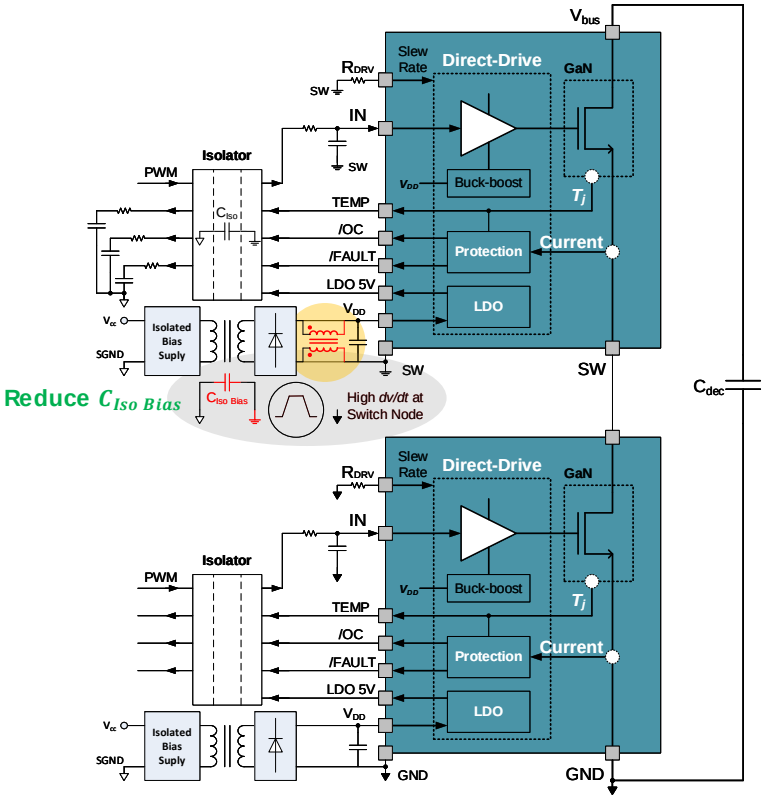


7) Why CMTI is critical for high-side isolated bias supply?

- Large $C_{Iso\ Bias}$ induces common-mode noise to signal ground and affects signals like fault feedback or PWMs.
- **Solutions:**
  - Low coupling capacitance in the transformer and PCB layout.
  - Add common mode choke.

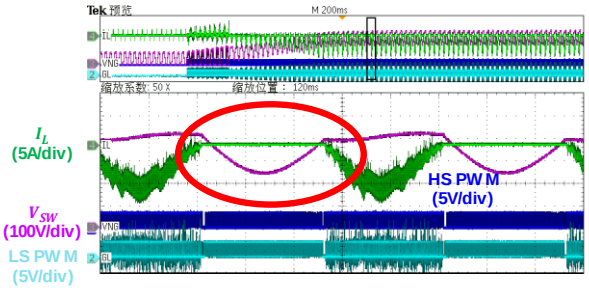


system stops switching at high dv/dt

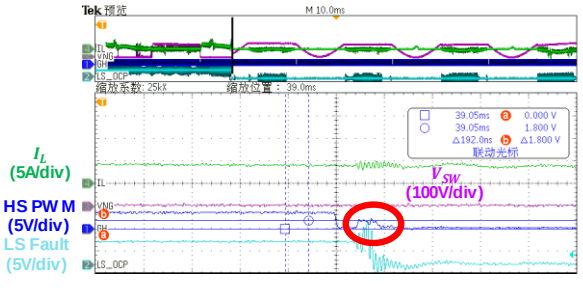


8) Why system cannot start at high *dv/dt*?

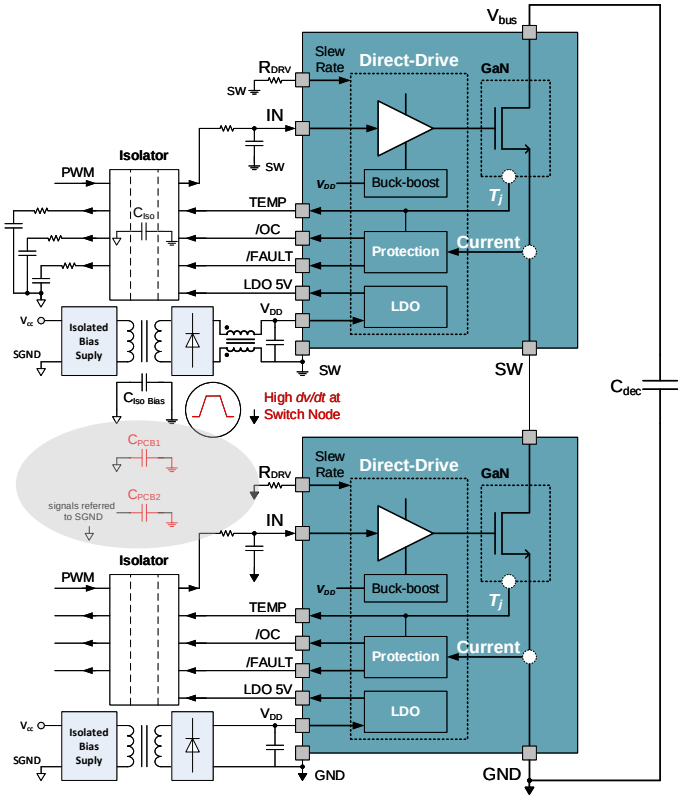
- **Root cause:** the switch node has overlap with the **control ground** and signals leading to capacitive coupling noises.



- No current in positive AC cycle
- LS GaN triggered fault

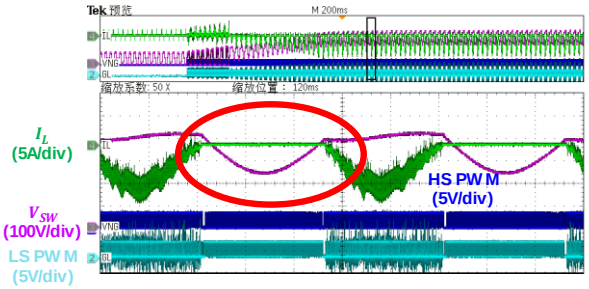


- When LS GaN is turning on, HS PWM has a 1.8V noise causing shoot-through.



Check switch node coupling

- **Root cause:** the switch node has overlap with the **control ground** and signals leading to capacitive coupling.
- **Solution:** avoid signal tracing above or below the switch node plan unless the signals are referring to switch-node.



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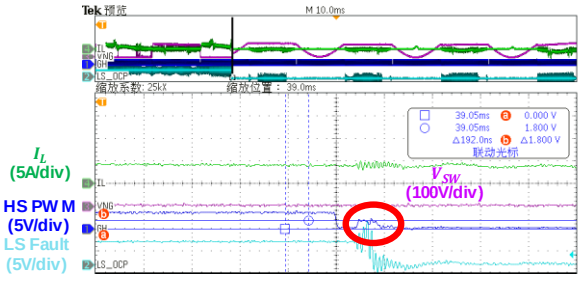

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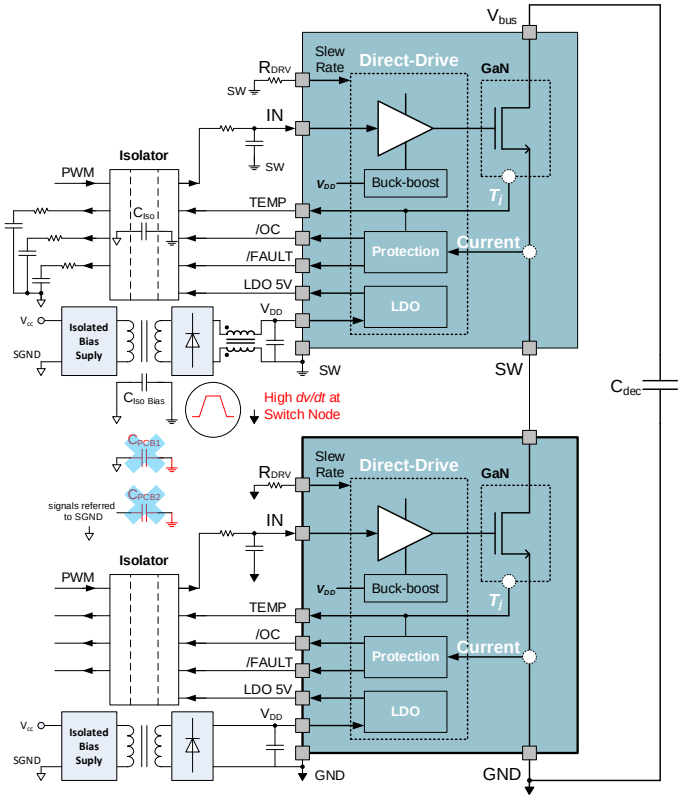

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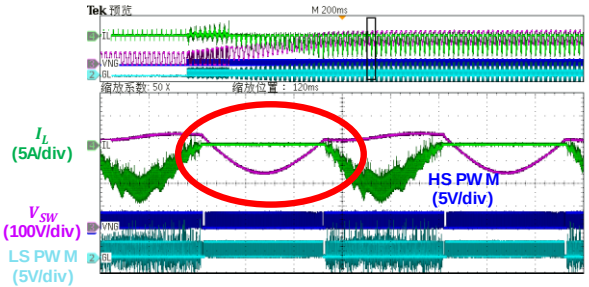

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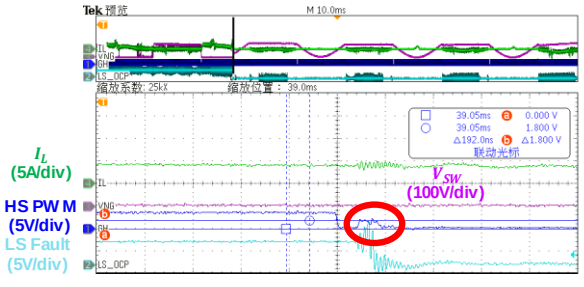
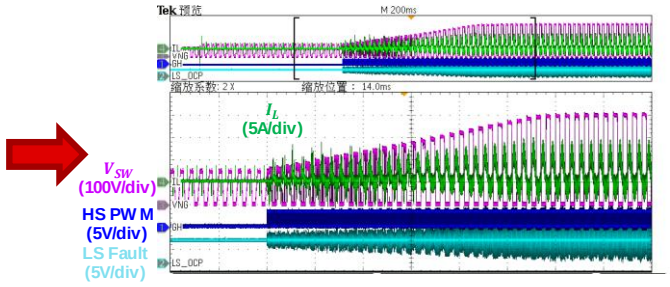


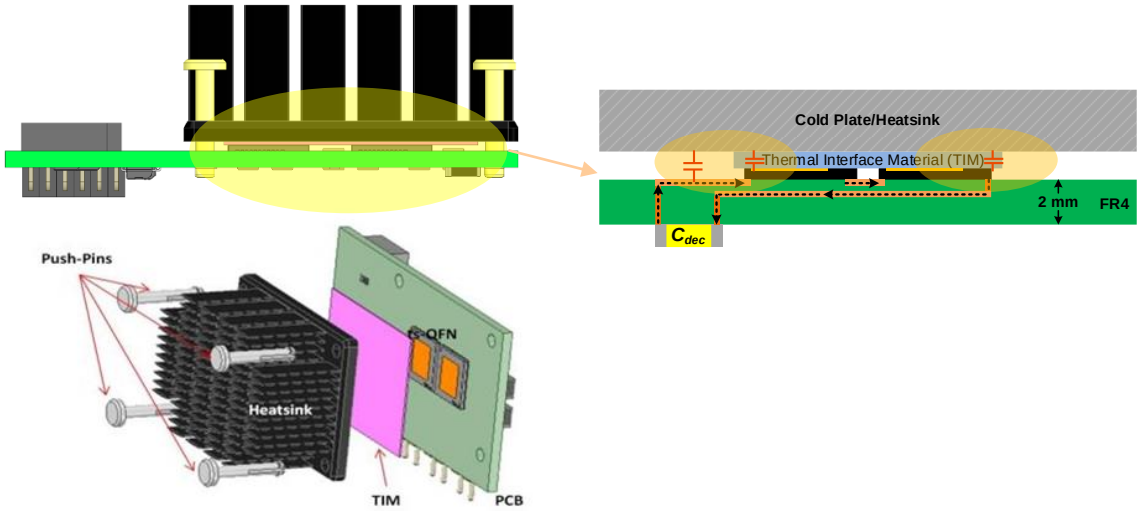
- When LS GaN is turning on, HS PWM has a 1.8V noise causing shoot-through.

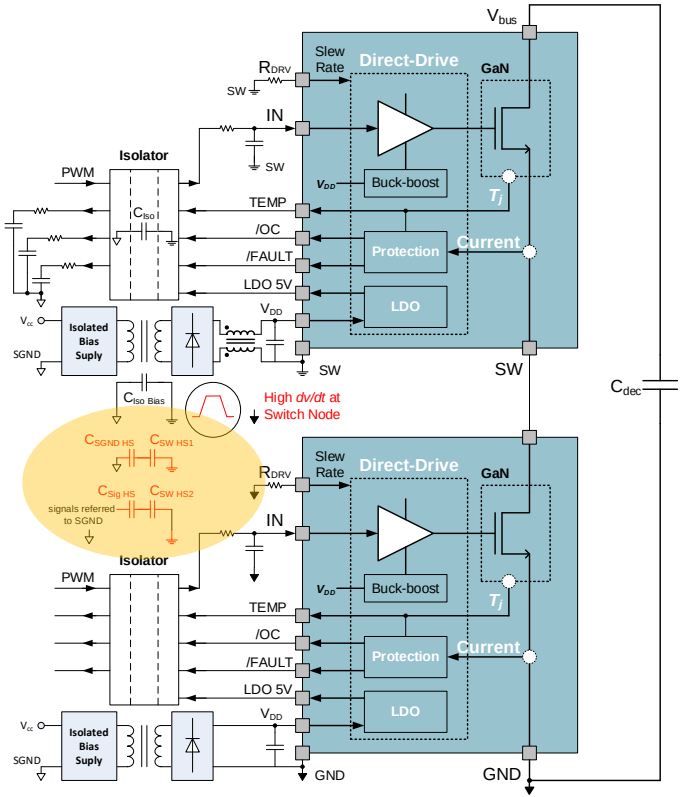


- Rework the board and remove the noise coupling from switch node.
- Modified their layout and solved the problem.

9) Why to avoid noise coupling to and from cooling plane?

- **Noise coupling through cooling:**
  - Most GaN / SiC devices' exposed thermal pad is electrically connected to device's drain or source.
  - Capacitive coupling exists between the switch-node and signal ground or signals.

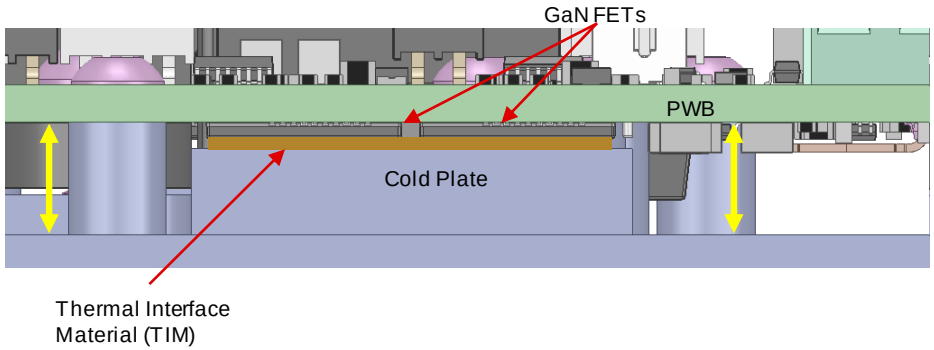




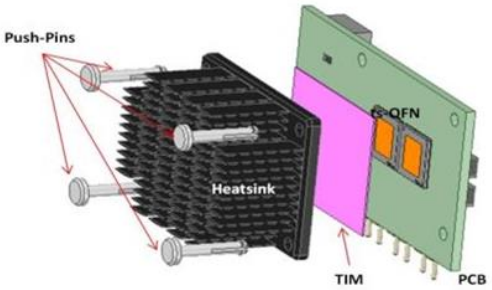
Ways to reduce noise coupling to cooling plane

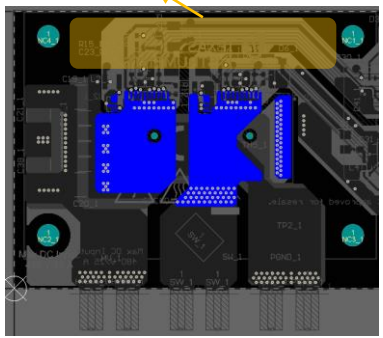
- Minimize the **traces** and **vias** in adjacent layers to cooling plane.
- Increase distance to cooling plane in certain area to reduce coupling capacitance.

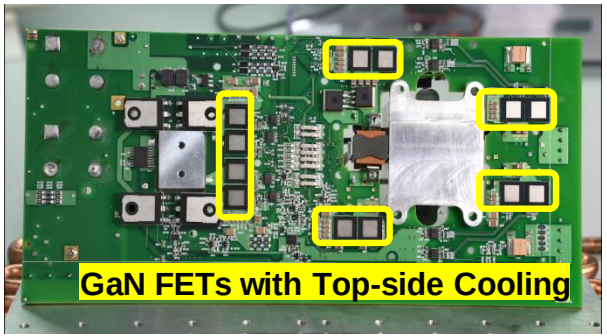
$$C = \frac{\varepsilon \cdot A}{d}$$



most traces in inner layers



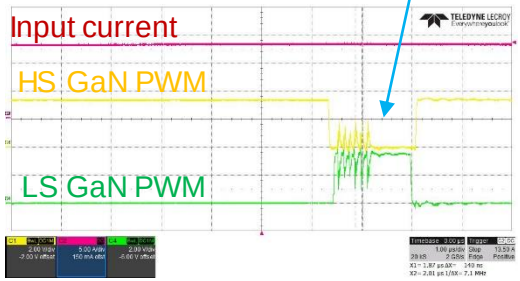




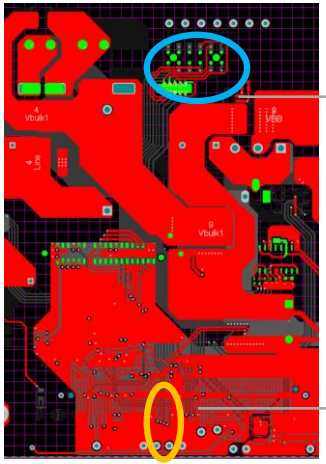
10) Why PWM signals are noisy at high dv/dt?

- **Issue:** PWM signals from the controller have large noises at high *dv/dt* operations.

No shielding on the PWM traces from controller to GaN card: high *dv/dt* and *di/dt* noises are coupled to PWMs

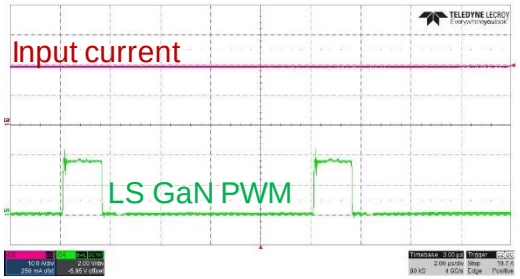


Noise Issue at 100V/ns, 380V



PWM signals from C2000

- **PCB trace is cut**
- **Shielded wire is used**

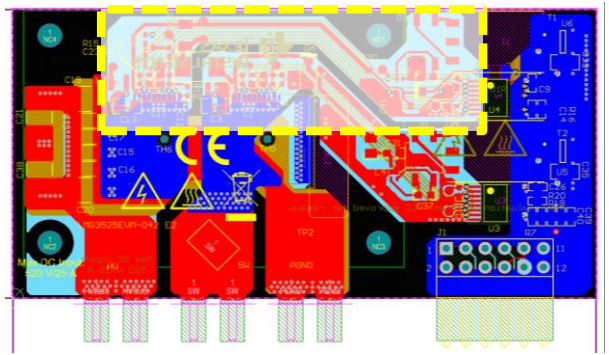


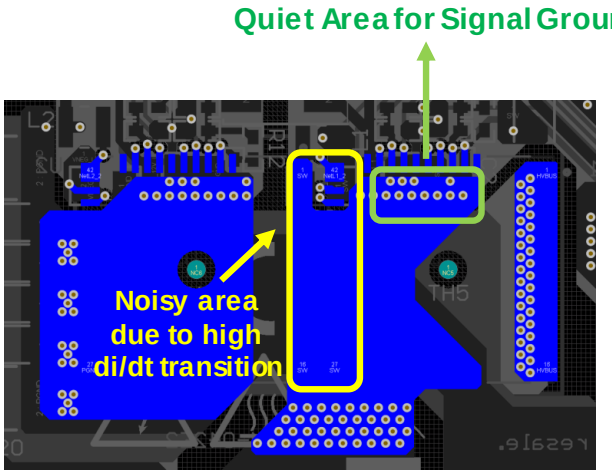
Operate Properly at 100V/ns, 380V

Good practices to maintain signals integrity

- **Signal Shielding:** all signals need to be shielded by its reference ground. Shielding is recommended for both the controller's outputs and the isolator outputs.
- **Kelvin Signal Connection:**
  - Avoid the noise area where high transient power passes through due to PCB trace impedance.
  - The quiet area with significantly less power transition is used for signal ground.

Signals traces with Ground Shielding





Summary: design guidelines with WBG devices

- **Gate driver**
  - Optimize gate loop layout
  - For bootstrap operation, add pre-regulations for drive voltage
  - Fast short circuit protection
- **Power loop**
  - Reduce power loop inductance for EMI and noise immunity improvement
- **CMTI in high *dv/dt* operation**
  - Good CMTI performance in isolator / isolated gate driver, and isolated bias supply
  - Additional RC filter can help on glitch noises
- **Noise coupling**
  - Avoid switch-node coupling to signals unless the signals are referred to switch-node
  - Minimize capacitive coupling to cooling plane
  - Provide good shielding to signals

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