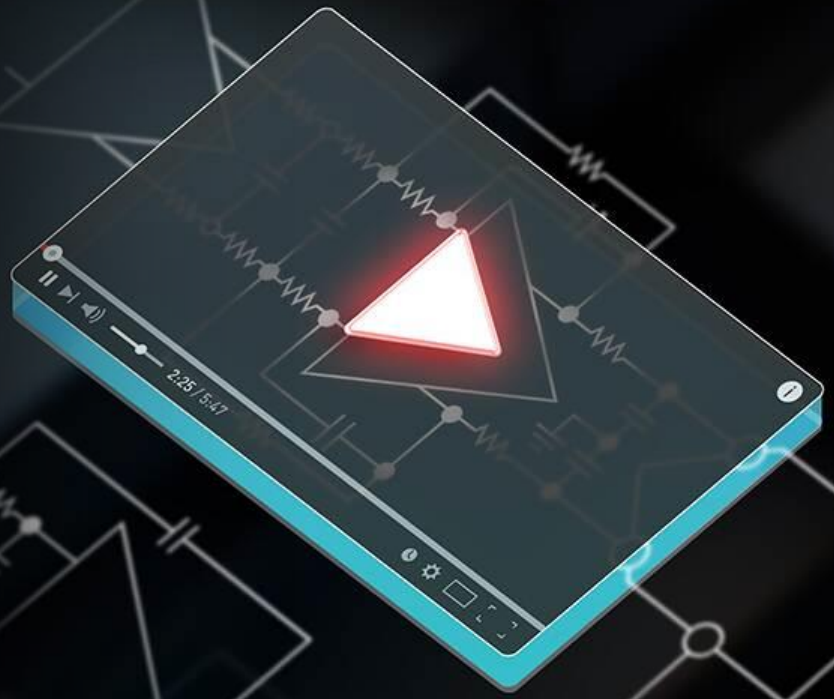
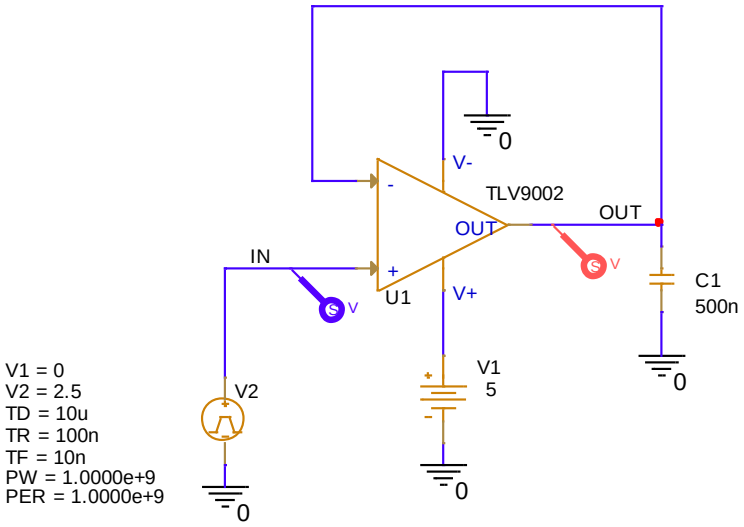
TI Precision Labs Seminar

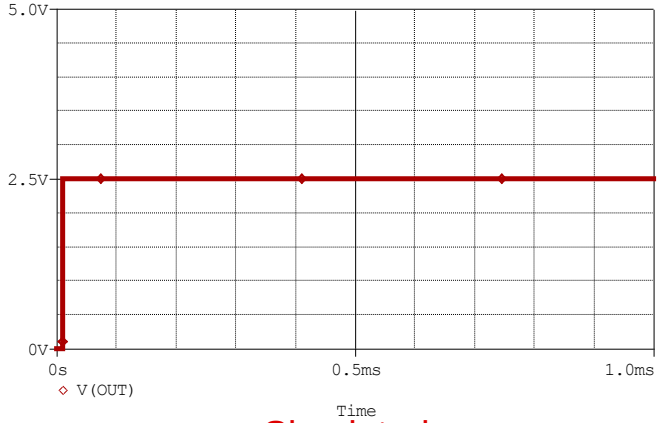
Circuit stability analysis and compensation schemes



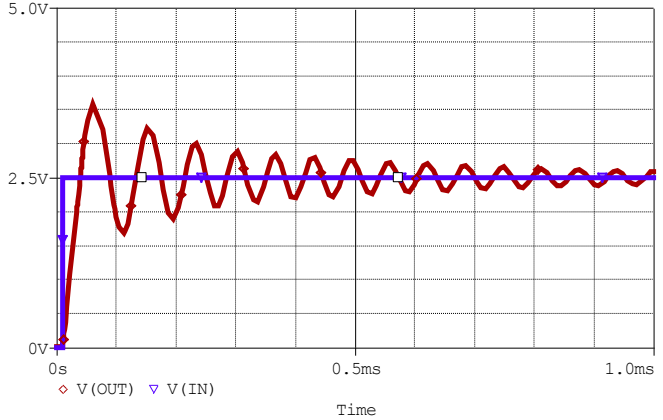
Op amp stability issue



Desired=2.5V

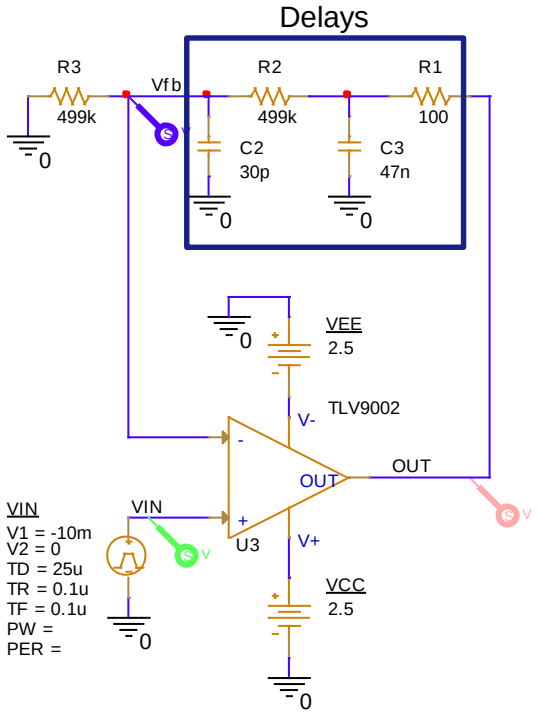


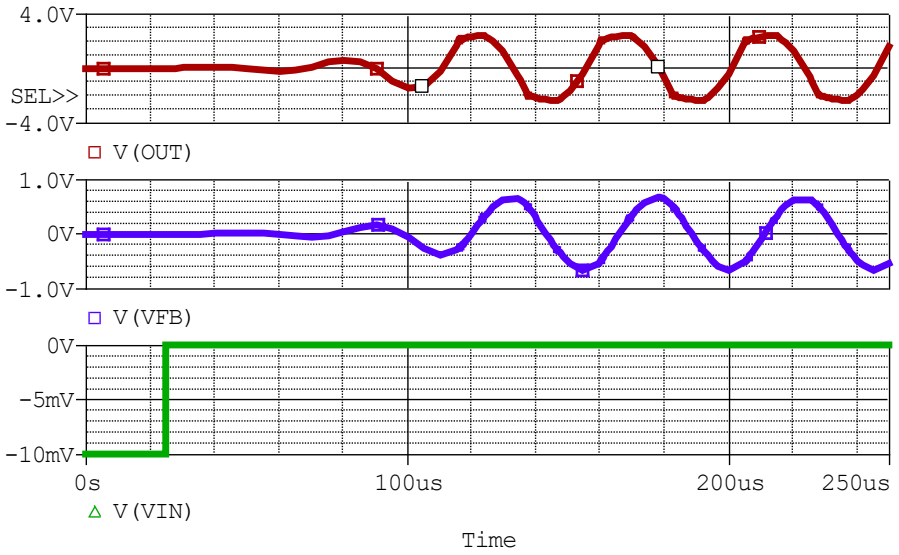
Simulated



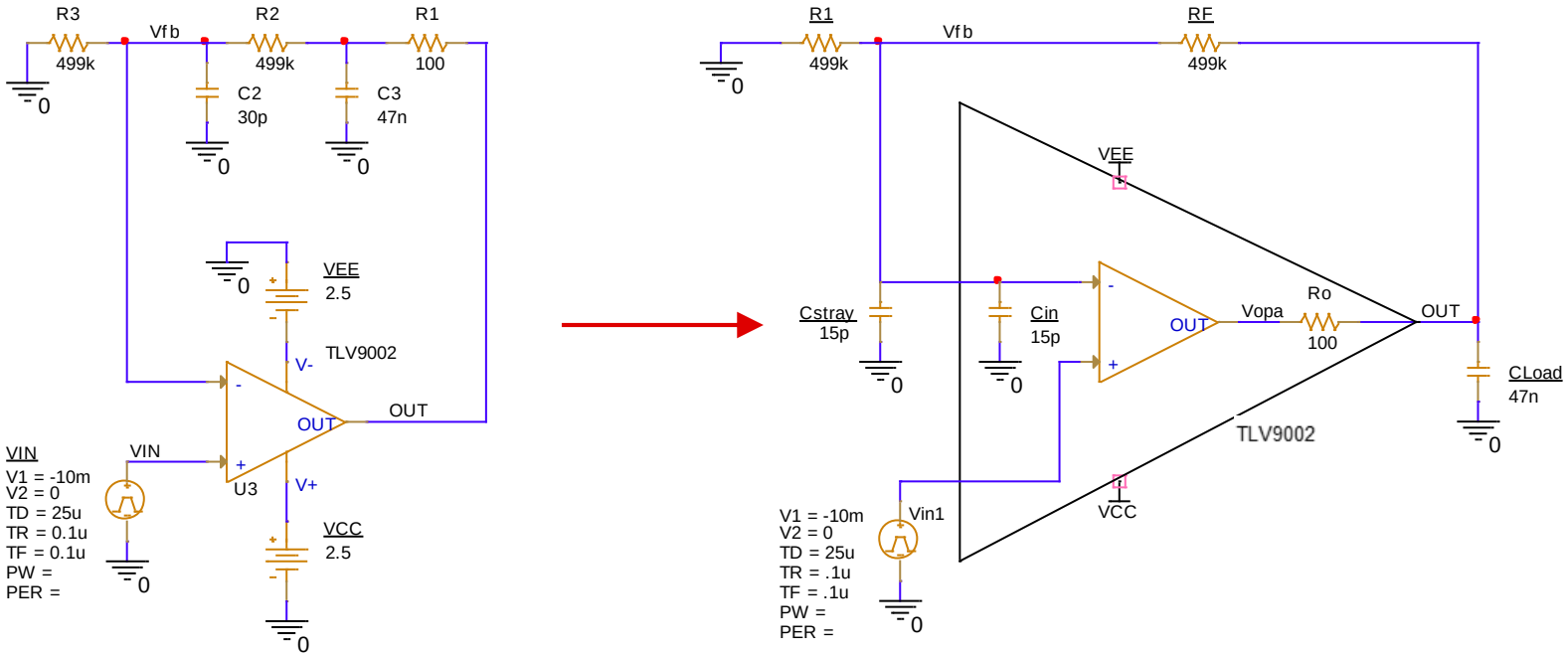
Simplified cause of op amp stability issues

Issues happen because of too much delay from output to feedback.





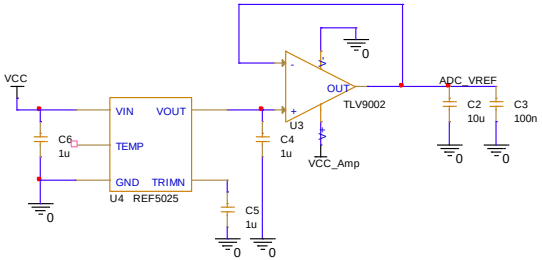
Delay happens in many circuits



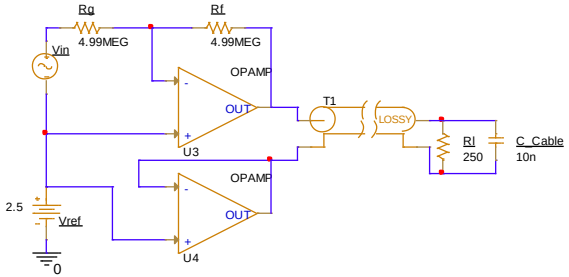
Circuits with possible stability issues

Output capacitive loads

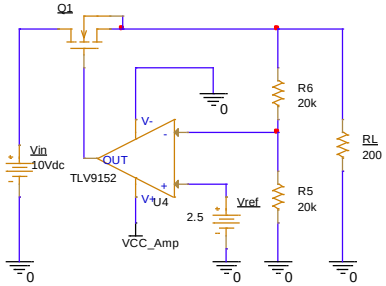
Reference buffers



Cable/shield drive

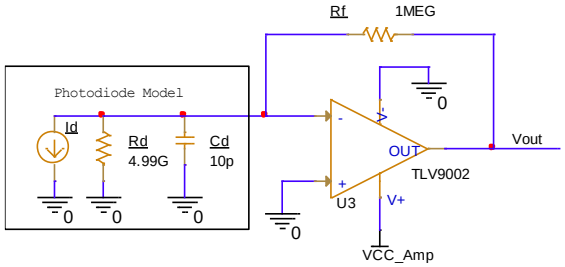


MOSFET gate drive

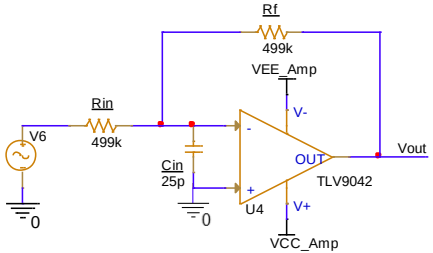


Input capacitance and large value resistors

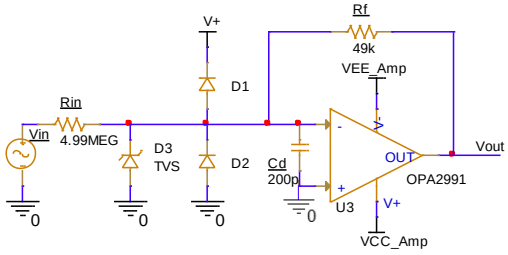
Transimpedance amplifiers



Large value resistors for low-power circuits



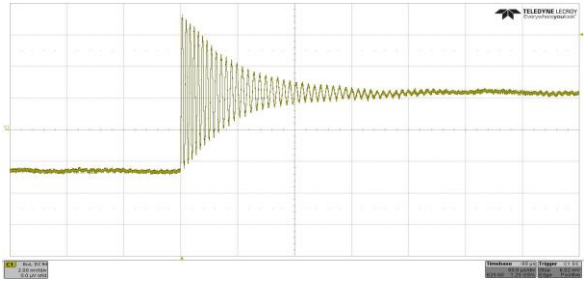
Transient suppression



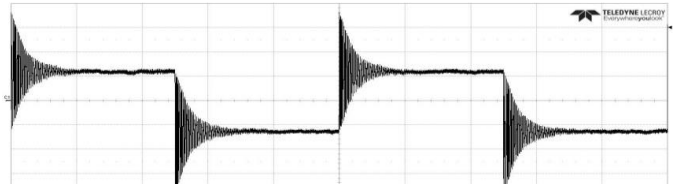
Identify stability issues in the lab

- **Oscilloscope/fgen – time domain analysis**:
  - Oscillations
  - Overshoot and ringing
  - Unstable DC voltages
  - High distortion

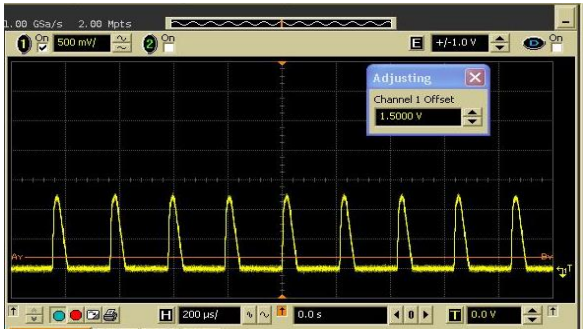
Output response to step input

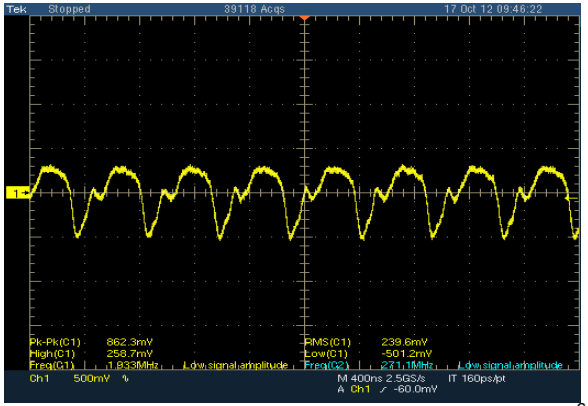


Output response to square wave input



Sustained output oscillation with DC input



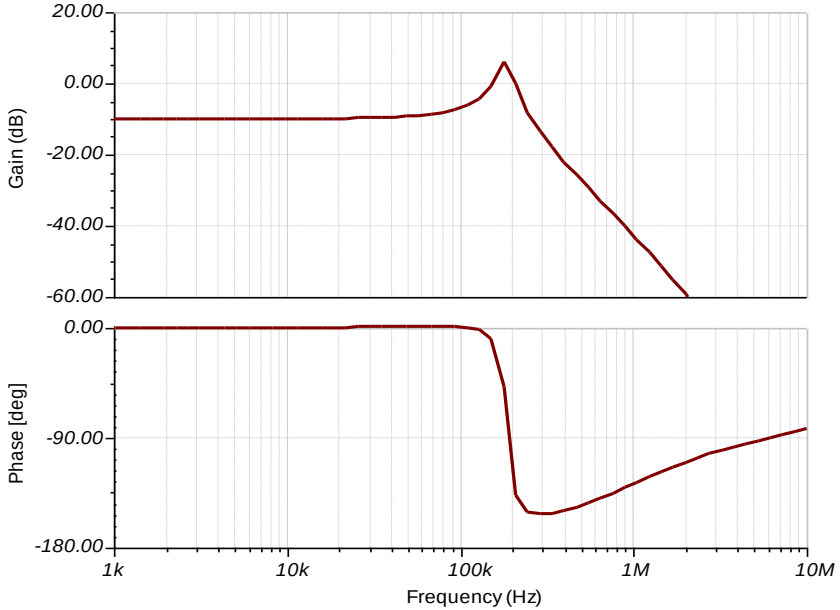


Identify stability issues in the lab

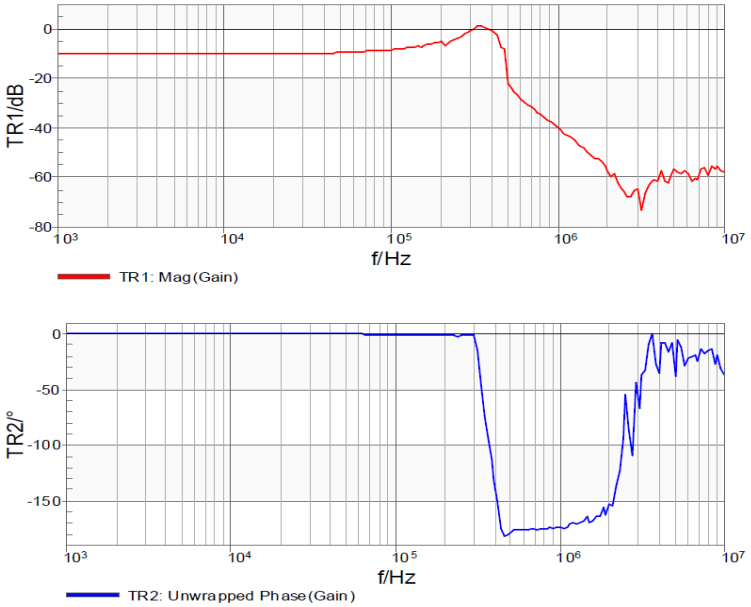
- **Gain/phase analyzer - Frequency domain:**

  - Peaking, unexpected gains, rapid phase shifts

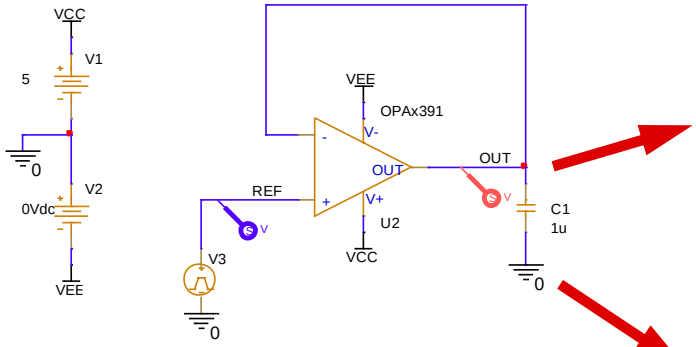
Simulated

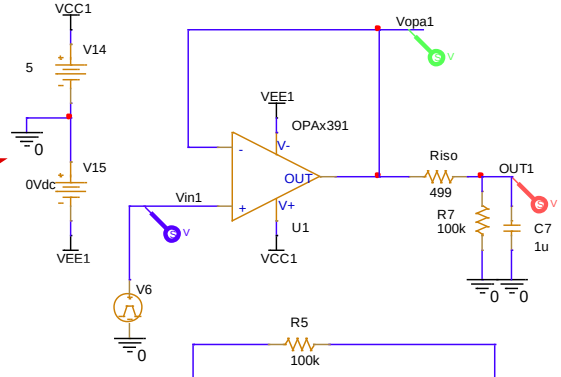


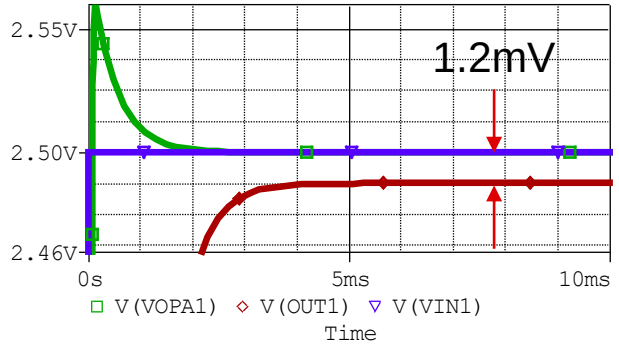
Measured

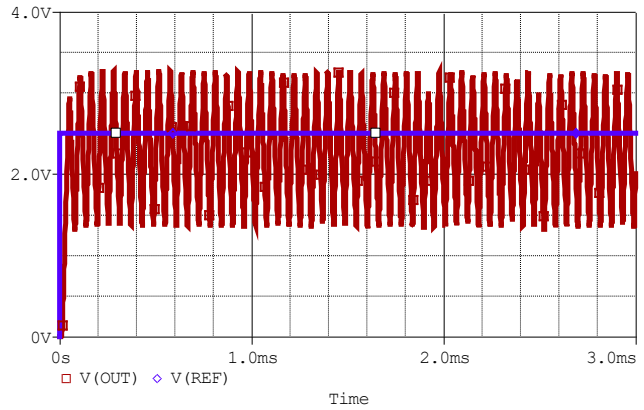


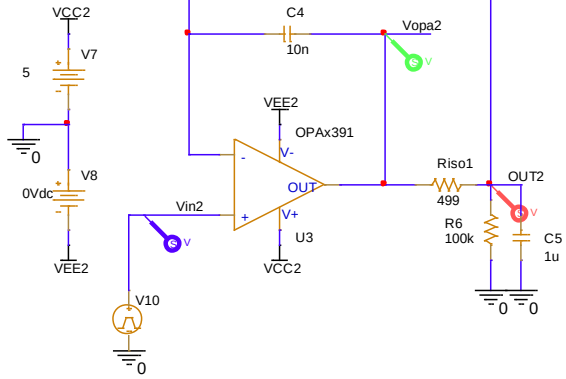
Solving op amp stability issues



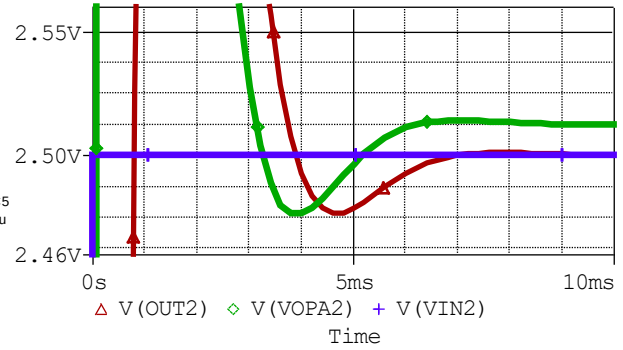




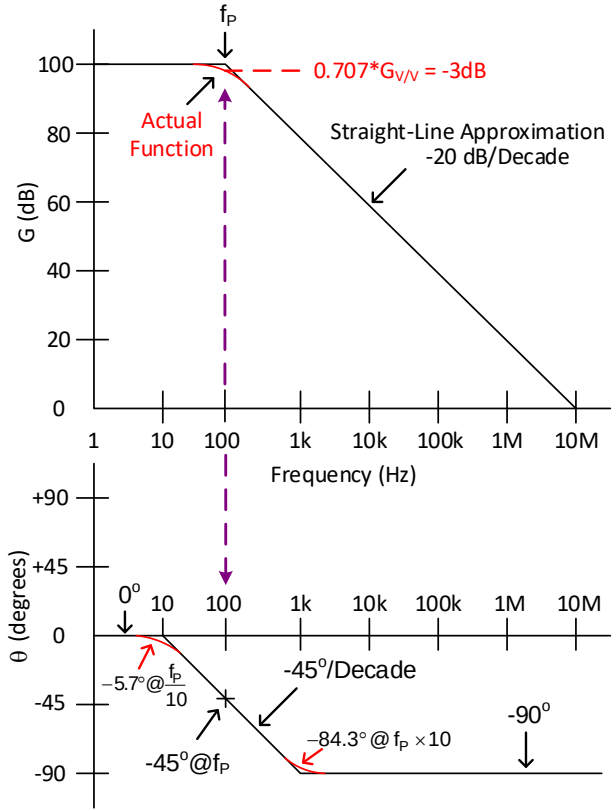




OPA391 $V_{os(typ)}$ = 10µV



Bode plots - pole



$$G_{V/V} = \frac{Vout}{V_{in}} = \frac{G_{DC}}{\mathrm{j}\left(\frac{f}{f_p}\right) + 1}$$ As a complex number

$$G_{V/V} = \frac{V_{out}}{V_{in}} = \frac{G_{DC}}{\sqrt{\left(\frac{f}{f_p}\right)^2 + 1}}$$ Magnitude

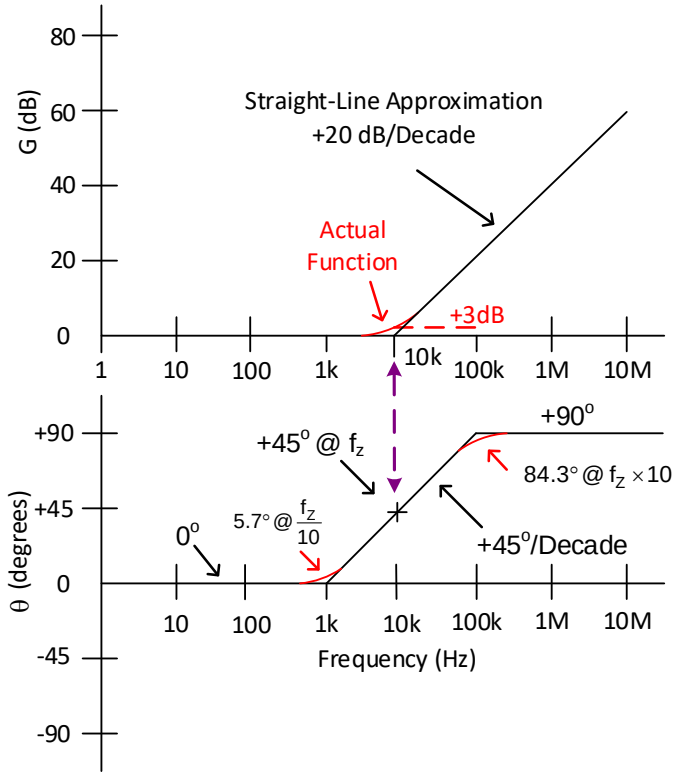
$$\Theta = -\tan^{-1}\left(\frac{f}{f_p}\right)$$ Phase

$$G_{dB} = 20 \times \log_{10} G_{V/V}$$ Magnitude in dB

Pole location = f_p (cutoff freq)

	Magnitude	Phase
$f << f_p$	G_{DC}	0˚
$f < 0.1f_p$		-45˚/decade
$f = f_p$	-3dB	-45˚
$f > 10f_p$	-20dB/decade	-45˚/decade
$f >> f_p$		-90˚

Bode plots – zero



$$G_{V/V} = \frac{V_{out}}{V_{in}} = G_{DC}\left[j\left(\frac{f}{f_z}\right) + 1\right]$$ As a complex number

$$G_{V/V} = \frac{V_{out}}{V_{in}} = G_{DC}\sqrt{\left(\frac{f}{f_z}\right)^2 + 1}$$ Magnitude

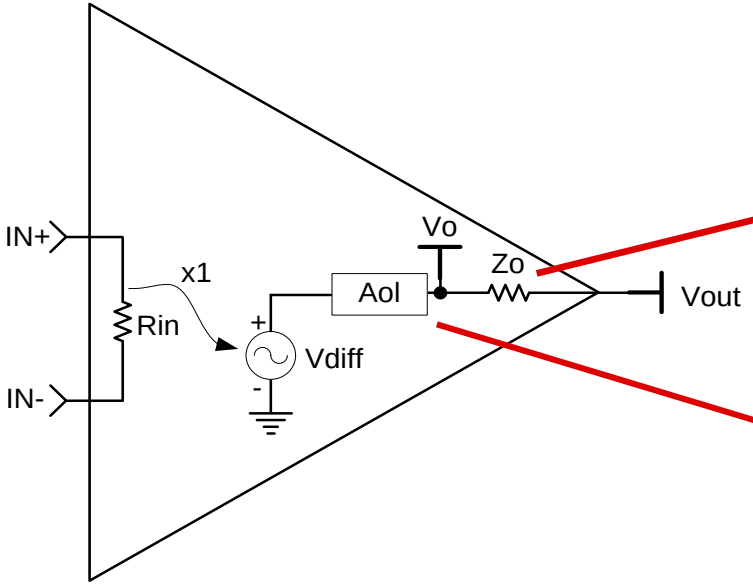
$$\Theta = \tan^{-1}\left(\frac{f}{f_z}\right)$$ Phase

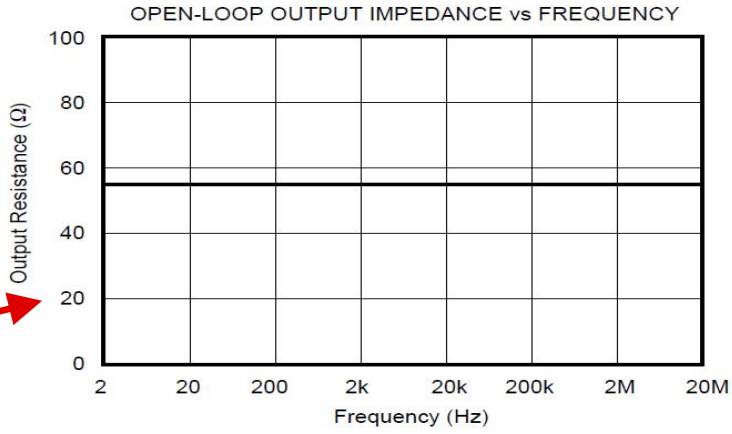
$$G_{dB} = 20 \times \log_{10} G_{V/V}$$ Magnitude in dB

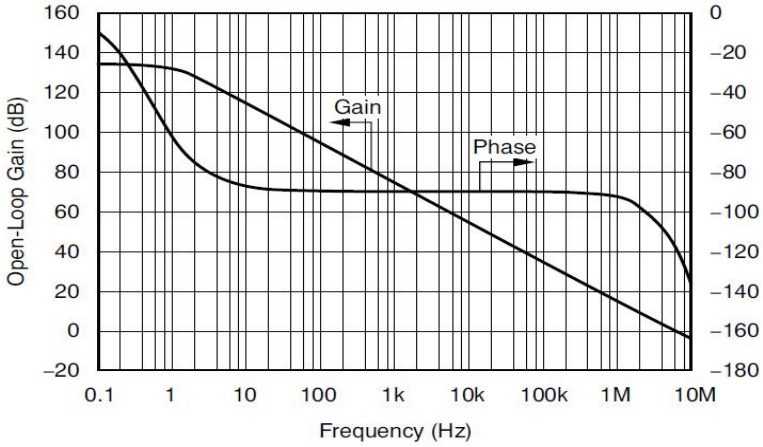
Zero location = f_z

	Magnitude	Phase
$f << f_z$	0dB	0˚
$f < 0.1f_z$		+45˚/decade
$f = f_z$	3dB	45˚
$f > 10f_z$	+20dB/decade	+45˚/decade
$f >> f_z$		90˚

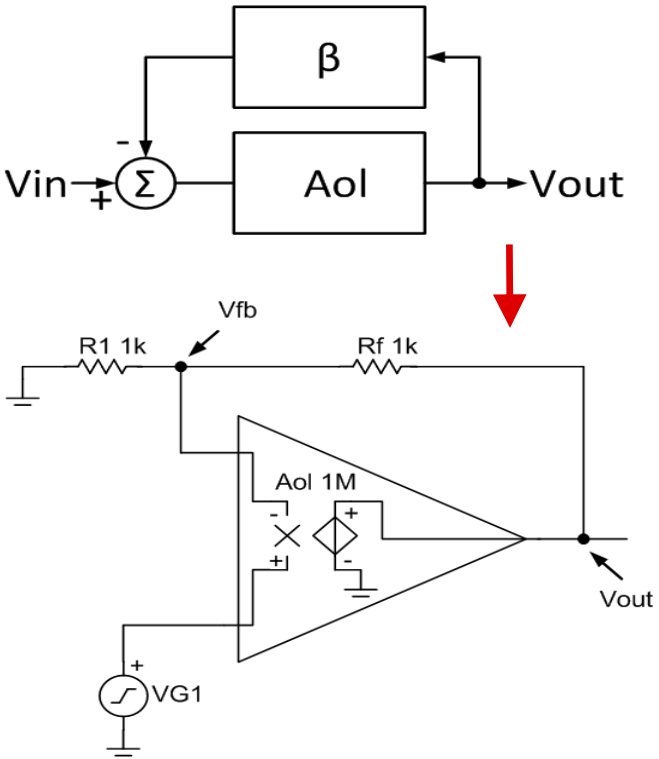
Op amp open loop model







Op amp closed loop model



A_{ol} = Open Loop Gain

β = Feedback Factor = $\frac{V_{fb}}{V_{out}} = \frac{R_1}{R_1+R_f}$

A_{cl} = Closed Loop Gain = $\frac{A_{ol}}{1+A_{ol}\beta}$

$A_{ol}\beta$ = Loop Gain

$$A_{cl} = \lim_{A_{ol}\beta\to\infty}\left(\frac{A_{ol}}{1+A_{ol}\beta}\right) = \frac{1}{\beta} = 1+\frac{R_f}{R_1}$$

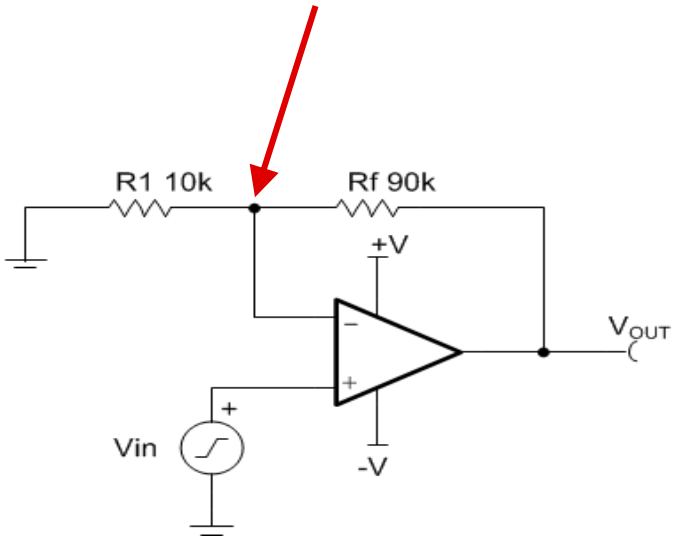
Closed loop gain ≈ 1/β . G = -1 op amp has β = ½ or 1/β = 2. This is why G = -1 has noise gain = +2 and closed BW of G=+2.

When is an amplifier unstable?

$$\mathbf{A_{CL}} = \frac{\mathbf{A_{OL}}}{\mathbf{1 + A_{OL}\beta}}$$

- A circuit is unstable when $A_{OL}\beta = -1$
- $A_{OL}\beta = -1$ sets the denominator of $A_{CL} = 0$
- $A_{OL}\beta = -1$ when $A_{OL}\beta(dB) = 0dB$ and phase shift($A_{OL}\beta$) = 180°
  - Phase shift is relative to the DC phase

$A_{OL}\beta = -1$ when the phase at V_{FB} has shifted 180º relative to Vin

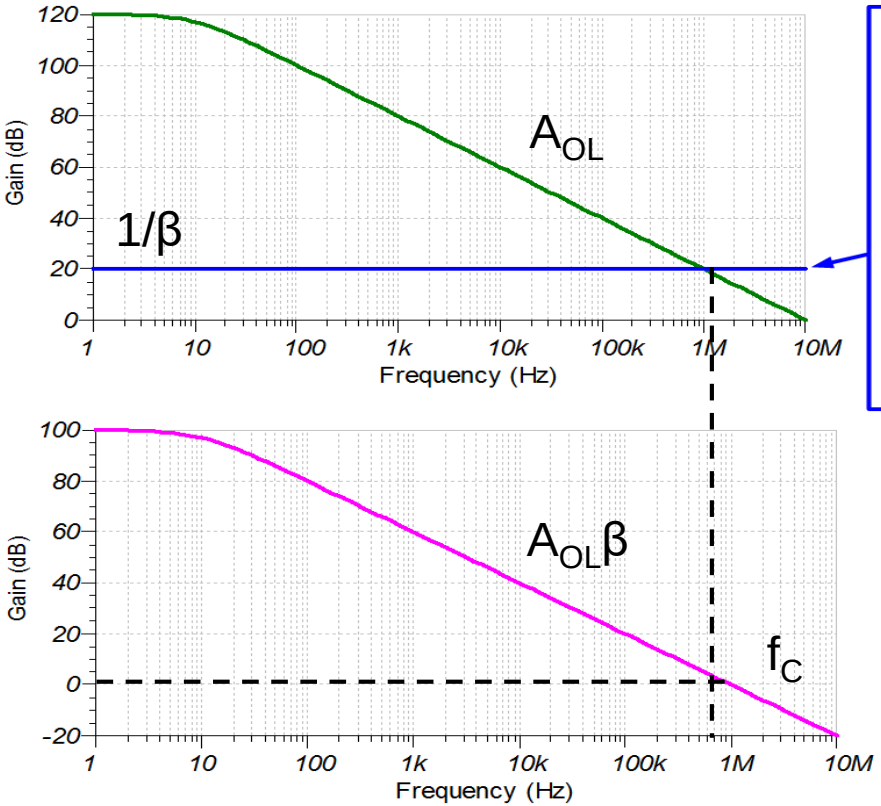


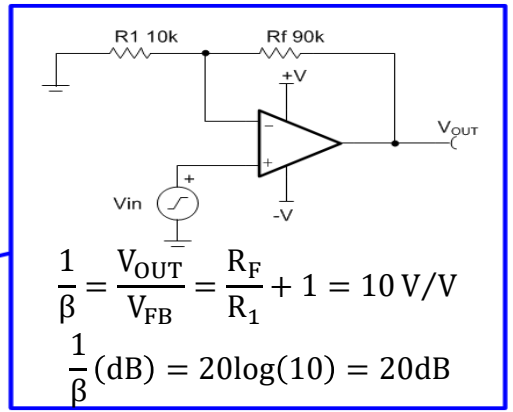
Phase margin (PM)

How close the system is to a 180° phase shift in $A_{OL}\beta$

- PM = Phase($A_{OL}\beta$) when Gain($A_{OL}\beta$) = 0dB
- Ex: 10° phase margin = 170° phase shift in $A_{OL}\beta$

Loop gain magnitude – $A_{OL}\beta$





$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

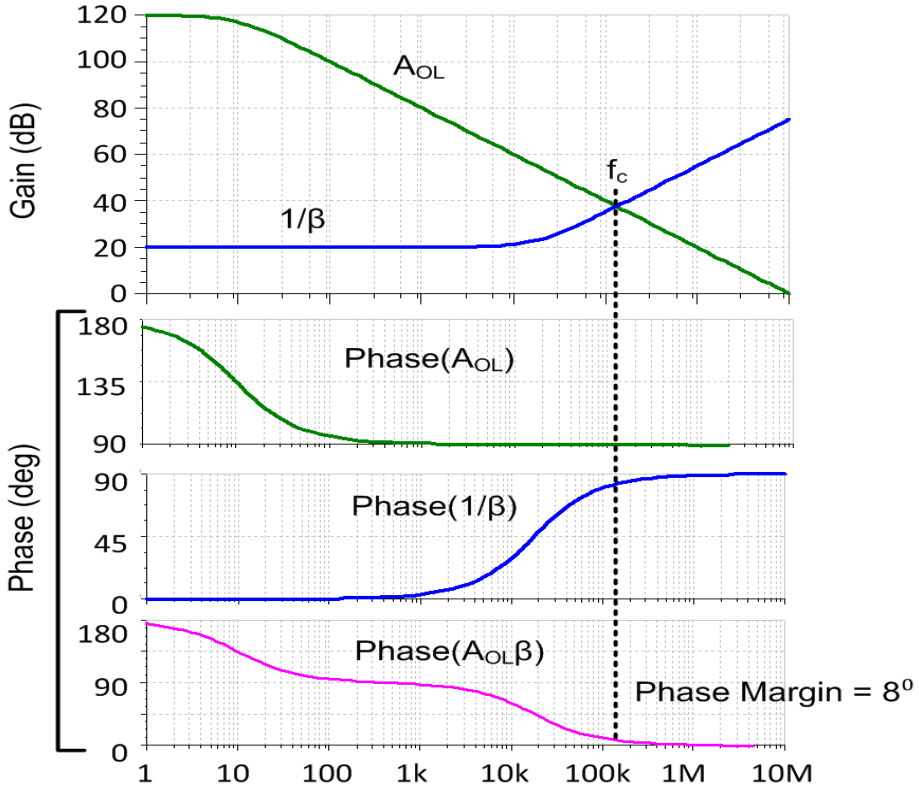
Loop gain in dB:

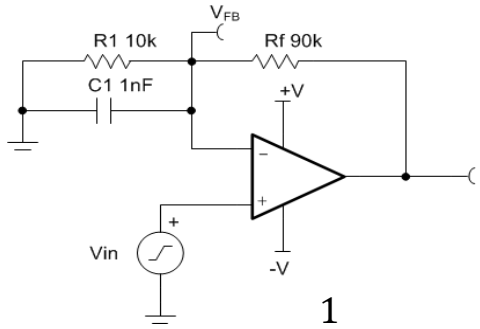
$$20\log(A_{OL}\beta) = 20\log(A_{OL}) - 20\log\left(\frac{1}{\beta}\right)$$

$$A_{OL}\beta(dB) = A_{OL}(dB) - \frac{1}{\beta}(dB)$$

Note: $A_{OL}\beta(dB) = 0dB$ when A_{OL} and $\frac{1}{\beta}$ intersect

Loop gain phase – phase($A_{OL}\beta$)



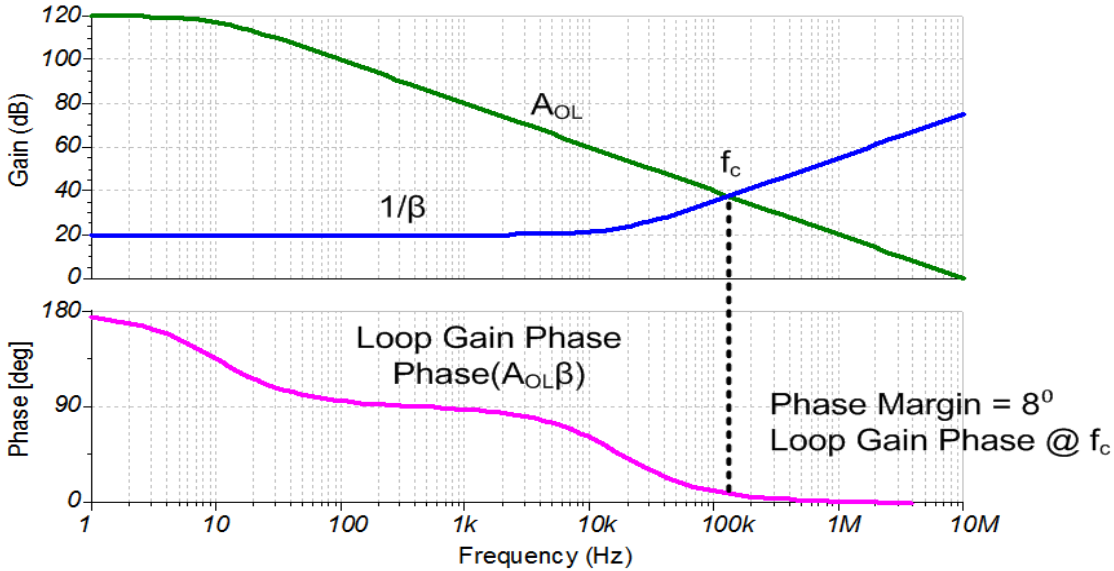


C1 introduces a zero in $\frac{1}{\beta}$

$$\frac{1}{\beta} = \frac{Z_f}{Z_1} + 1$$

At DC the capacitor is open, so gain = 10V/V. At high frequency, the capacitor causes Z_1 to decrease so gain increases by +20dB/decade

Phase margin



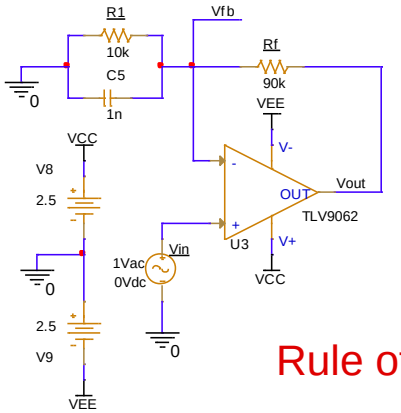
Rule of thumb:

Phase margin > 45° is required for optimal stability.

Phase margin < 45° is considered “marginally stable.”

This does not ensure a robust design over process variation.

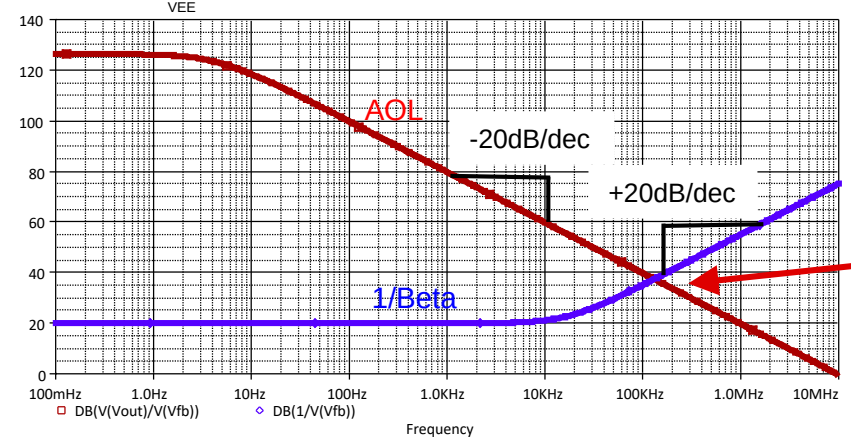
Rate of closure – unstable example



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = 10\left(\frac{f}{f_C} + 1\right)$$

1/β(dB) = 20dB at DC, then increases by +20dB/decade after the zero frequency

Rule of thumb: rate of closure = 20dB is required for optimal stability

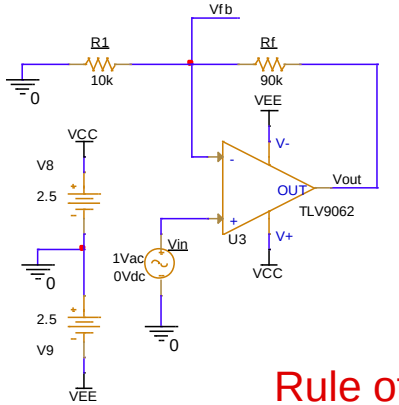


$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20\text{dB} - (+20\text{dB})| = 40\text{dB}$$

Unstable because rate of closure > 20dB

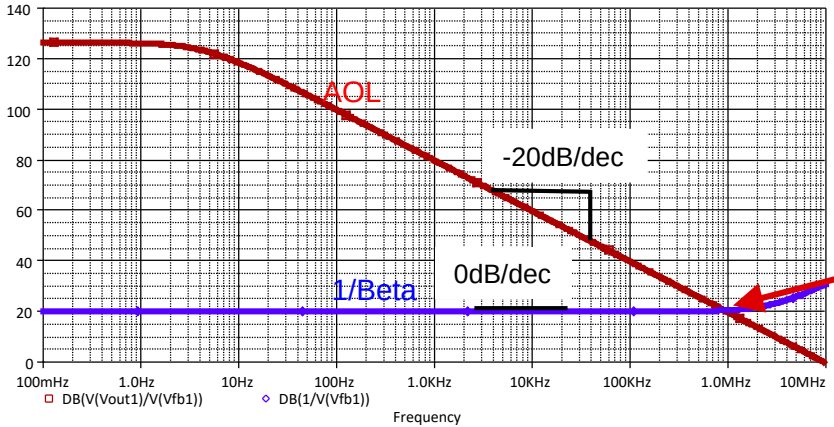
Rate of closure – stable example



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20\log(10) = 20dB$$

Rule of thumb: rate of closure = 20dB is required for optimal stability

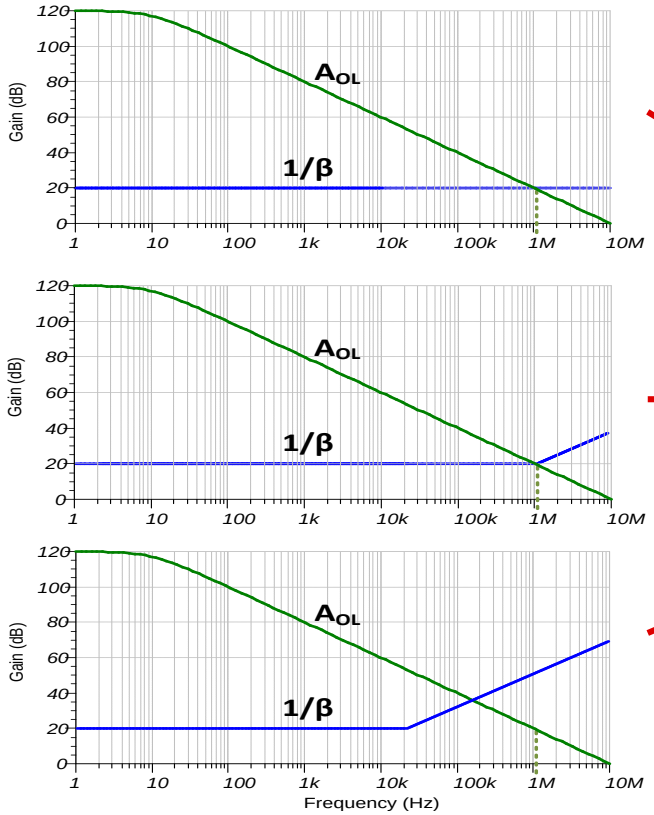


$$\text{Rate of Closure} = \left|\text{Slope}(A_{OL}) - \text{Slope}\left(\frac{1}{\beta}\right)\right|$$

$$\text{Rate of Closure} = |-20dB - 0dB| = 20dB$$

Stable because rate of closure = 20dB

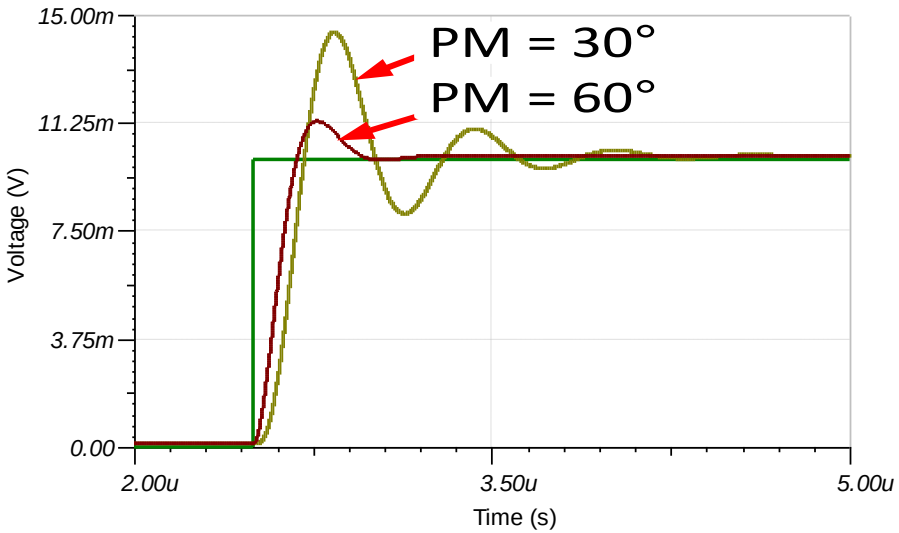
Rate of closure (ROC) and phase margin

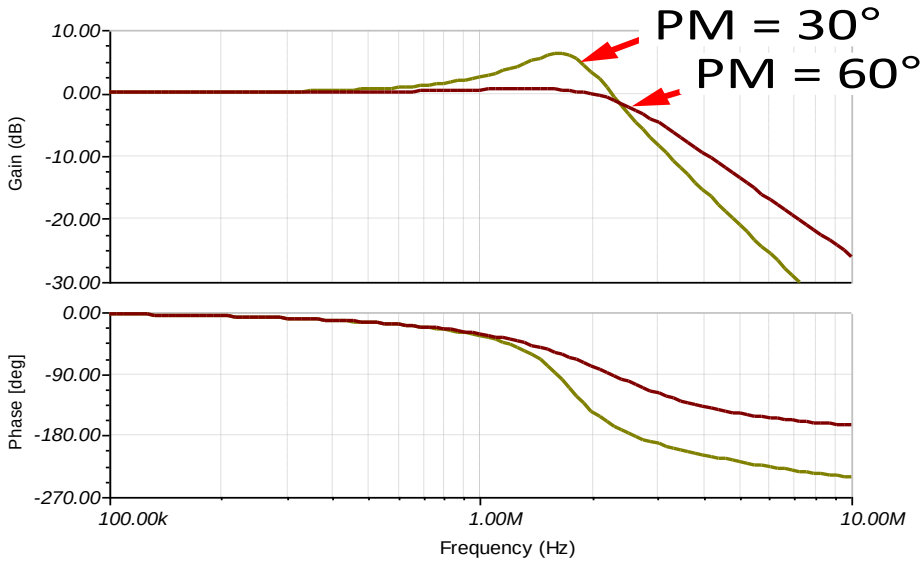


ROC (dB/decade)	Phase margin (°)
20	45 < PM < 90
20 < ROC < 40	45
40	0 < PM < 45

Indirect loop gain phase margin measurements

Phase margin can be measured indirectly on closed-loop circuits

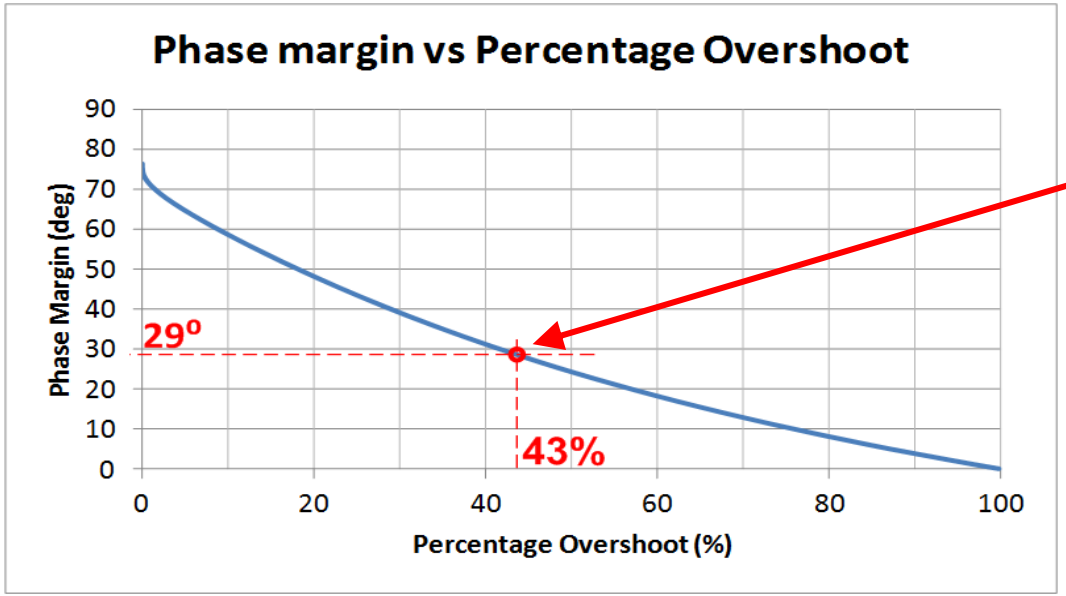


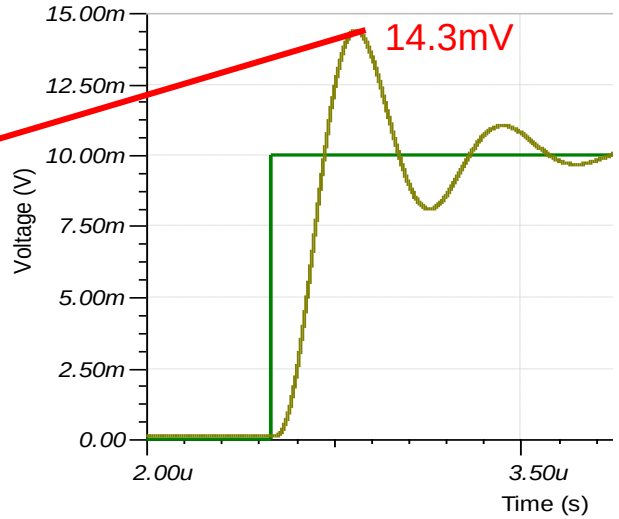


Time domain → percent overshoot

AC gain/phase → AC peaking

Indirect loop gain phase margin measurements

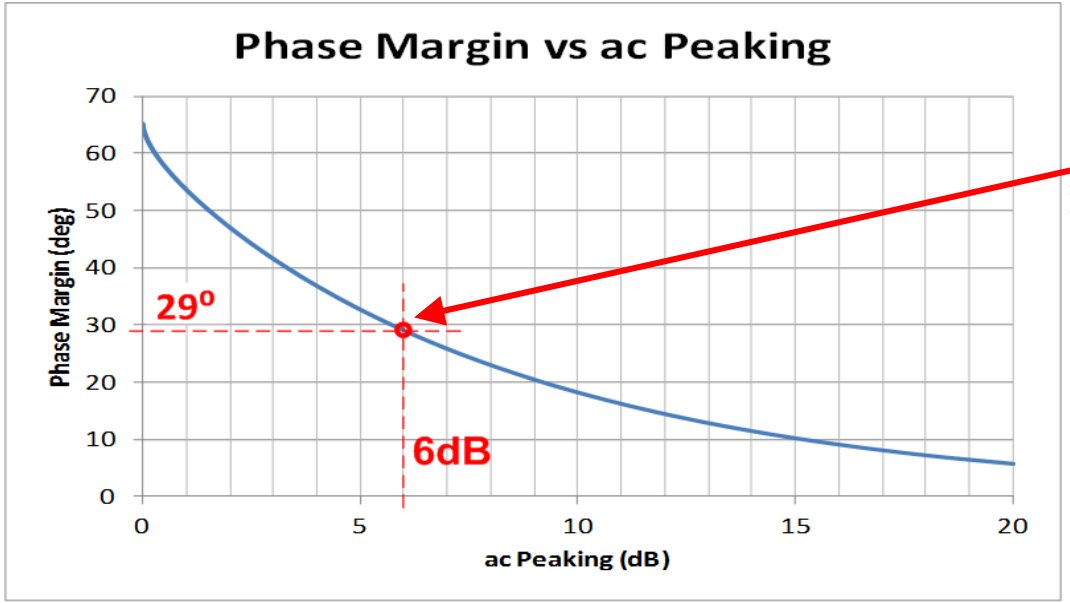


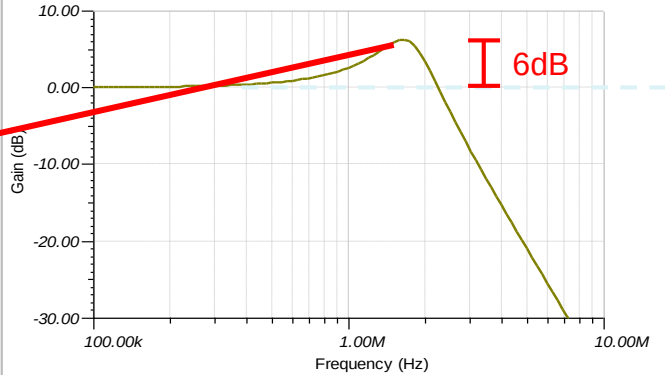


$$\%\text{Overshoot} = \left(\frac{14.3\text{mV} - 10\text{mV}}{10\text{mV}}\right) * 100\% = 43\%$$

43% overshoot → 29° phase margin

Indirect loop gain phase margin measurements



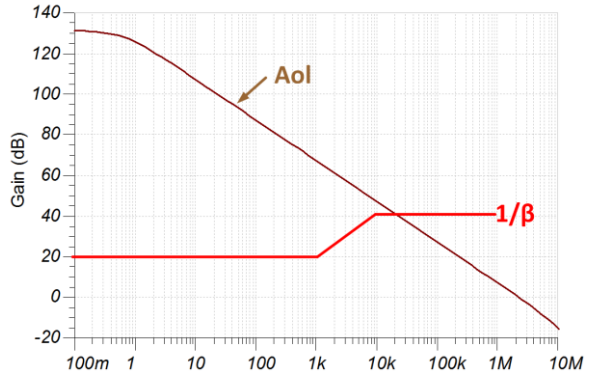


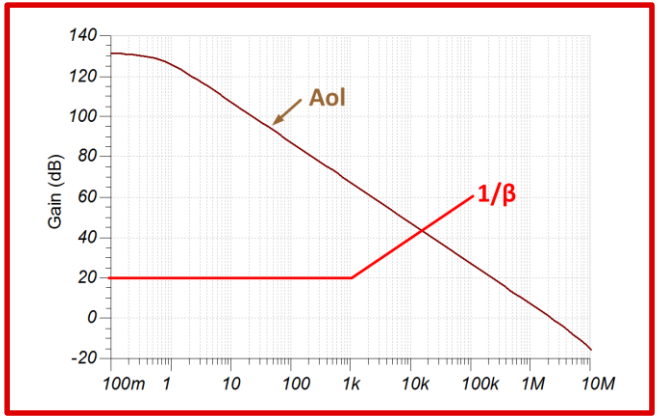
$$\text{AC peaking} = 6\text{dB} - 0\text{dB} = 6\text{dB}$$

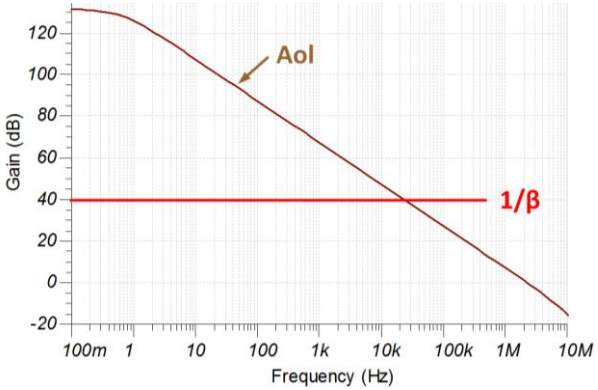
6dB AC peaking → 29° phase margin

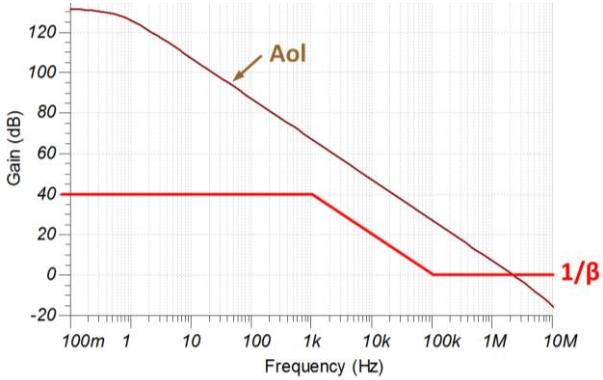
Quiz

Which **one** of these A_{OL} and 1/β curves is **unstable**?



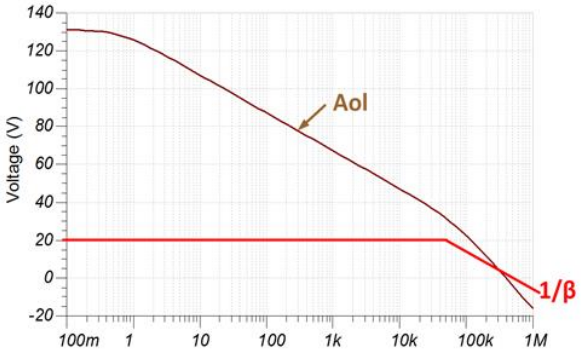


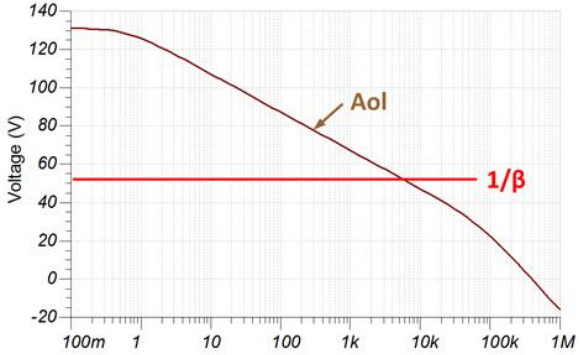


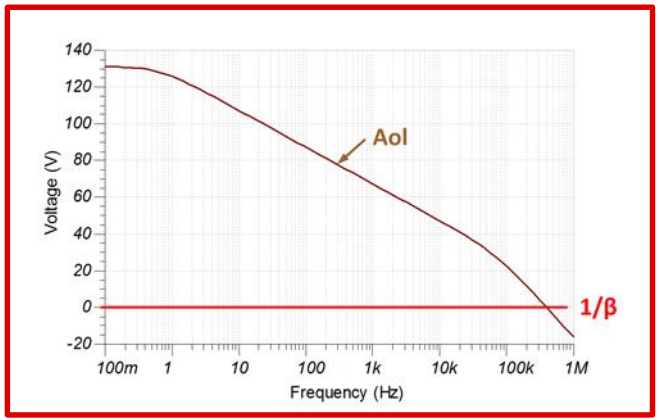


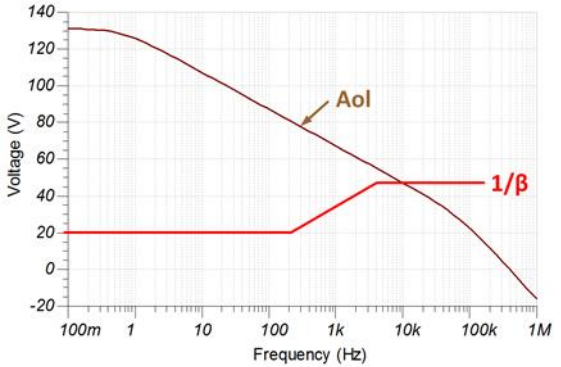
Quiz

Which **one** of these A_{OL} and 1/β curves is **un**stable?



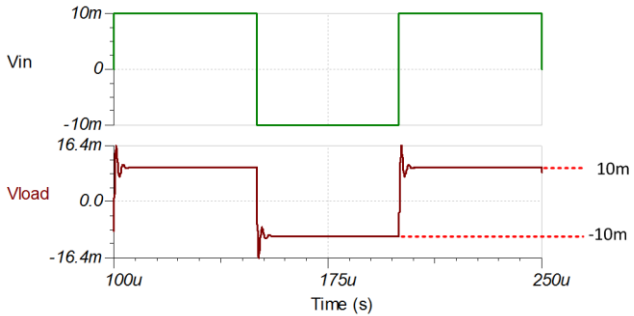




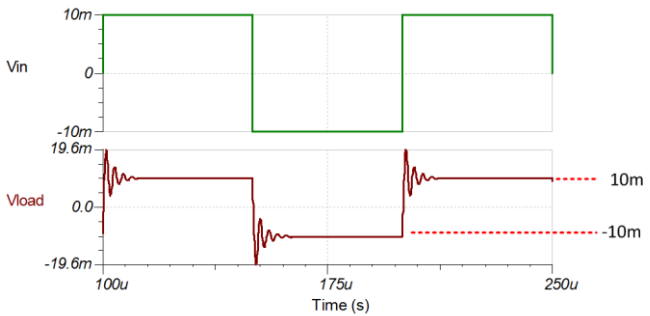


Quiz

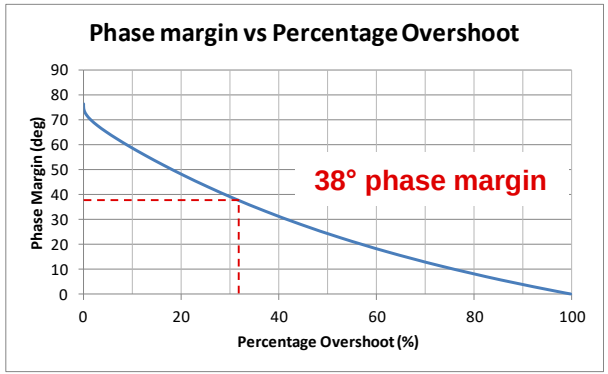
Find the phase margin of each system according to the % overshoot.

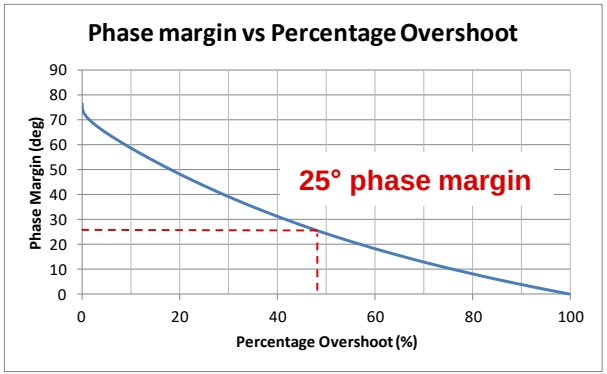


$$\%\text{Overshoot} = \left(\frac{16.4\text{mV} - 10\text{mV}}{20\text{mV}}\right) * 100\% = \mathbf{32\%}$$



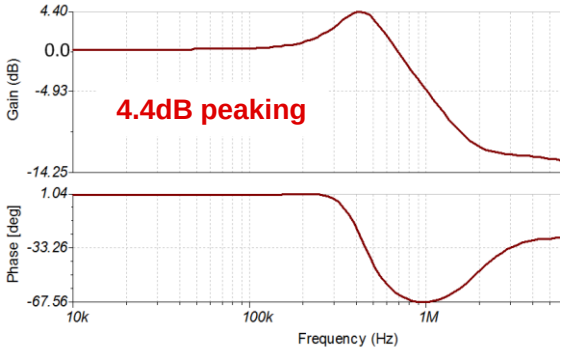
$$\%\text{Overshoot} = \left(\frac{19.6\text{mV} - 10\text{mV}}{20\text{mV}}\right) * 100\% = \mathbf{48\%}$$

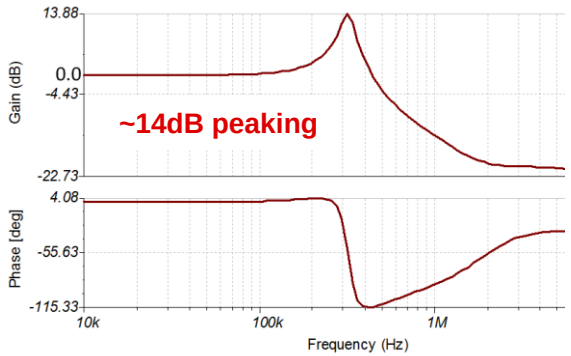


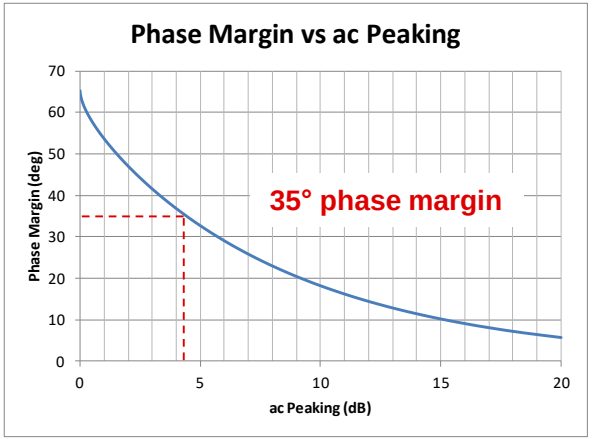


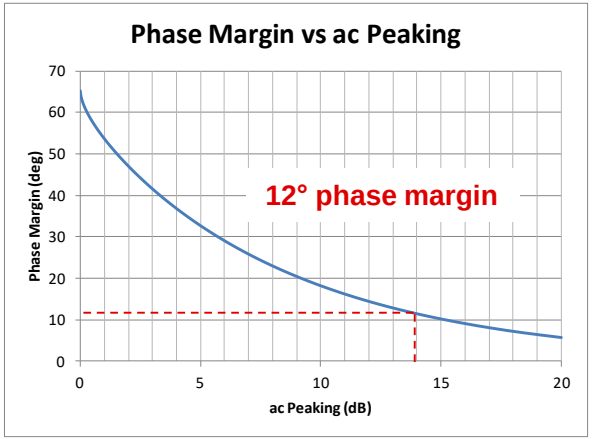
Quiz

Find the phase margin of each system according to the AC peaking.



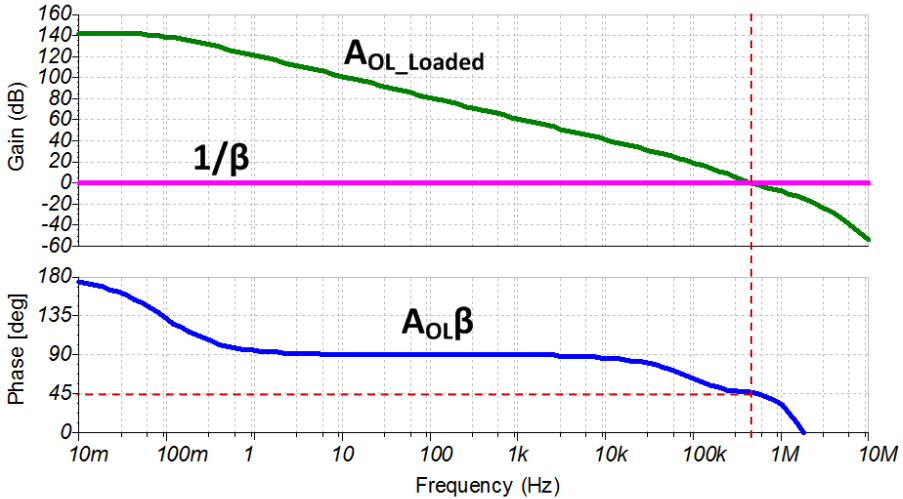




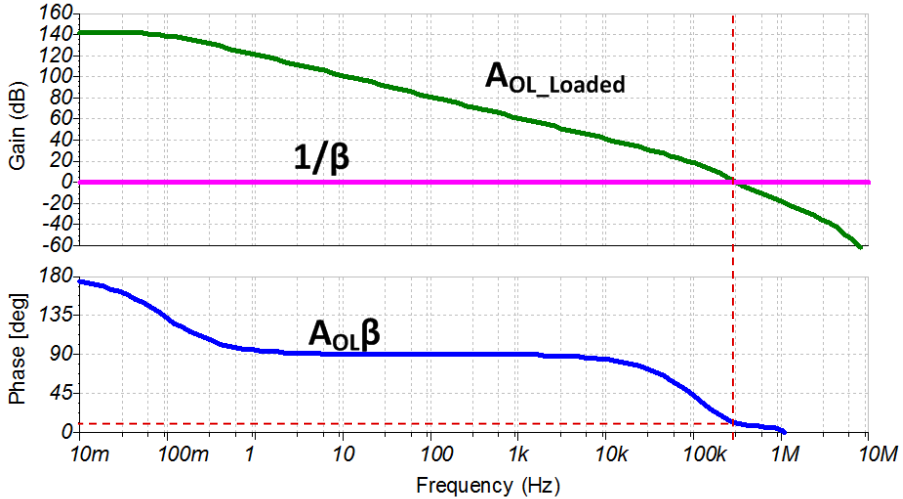


Quiz

Find the phase margin of each system according to the Bode plot.



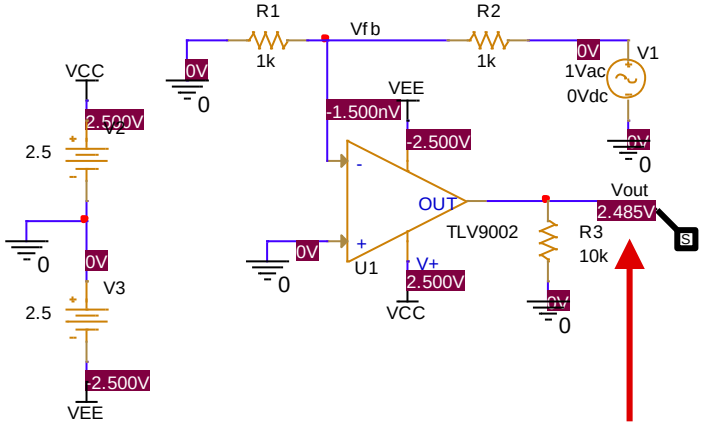
45° phase margin



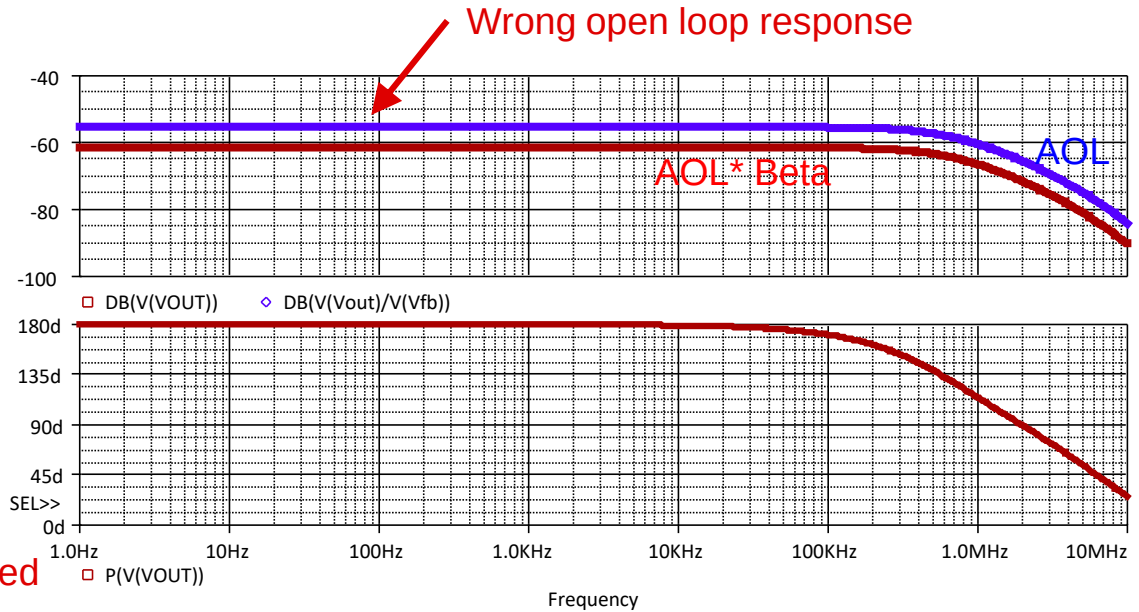
~15° phase margin

Simulating open-loop circuits

No DC biasing produces erroneous results

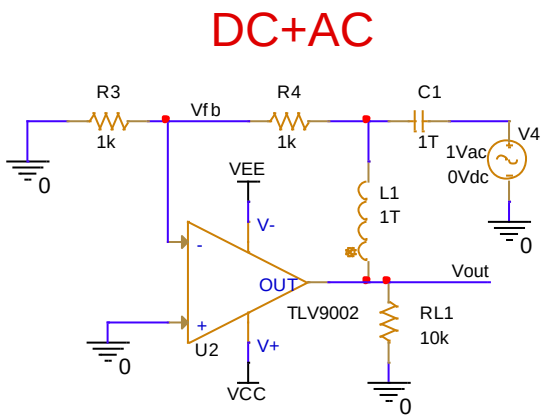


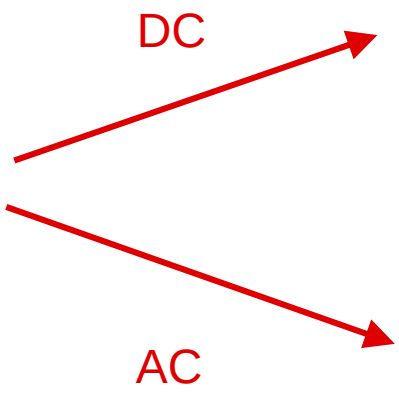
Output saturated

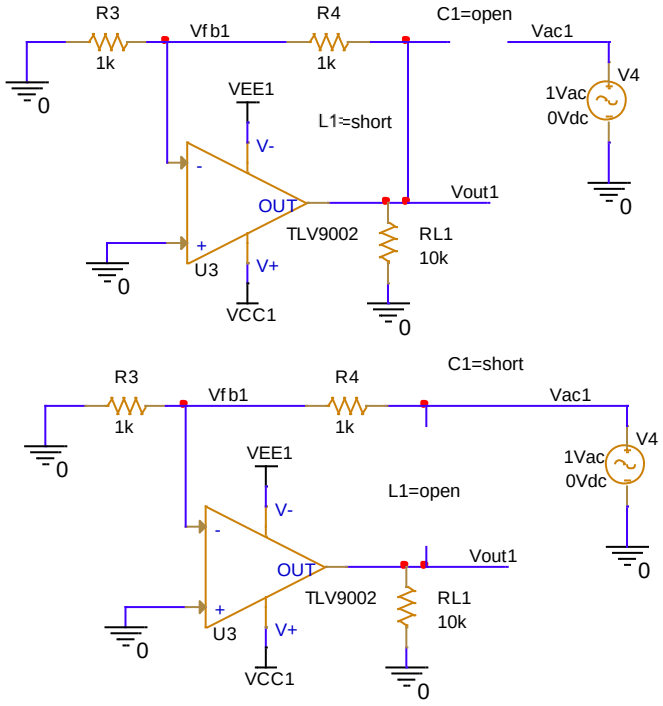


Simulating open-loop circuits

DC: closed loop needed for SPICE operation
AC: open loop needed for stability analysis

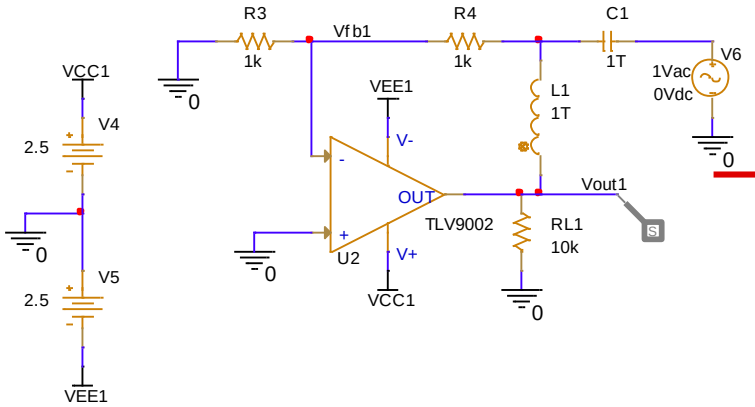


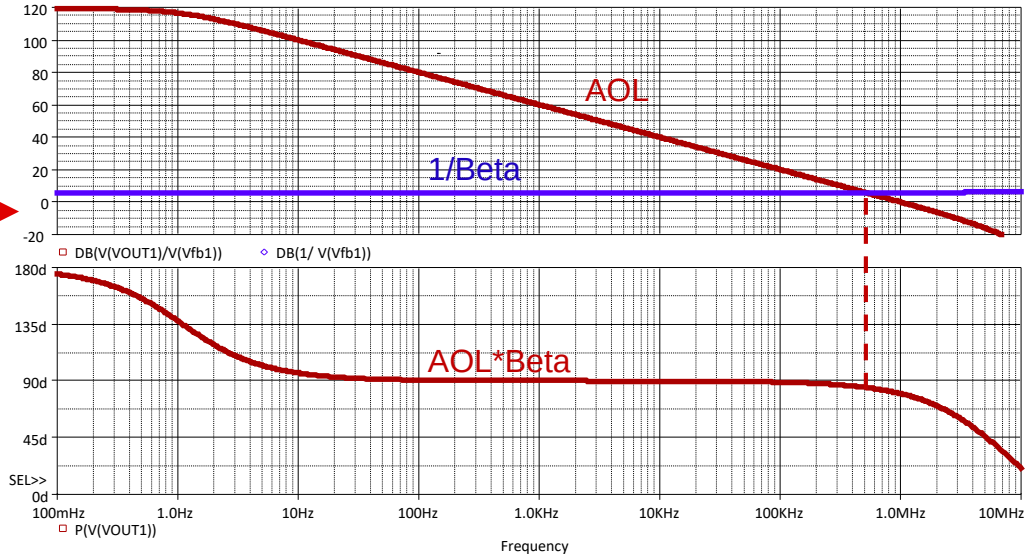




Standard open-loop SPICE configuration

We need an open-loop circuit (no feedback) to generate open-loop gain ($\mathbf{A_{OL}}$), **1/β**, and loop gain ($\mathbf{A_{OL}\beta}$) curves





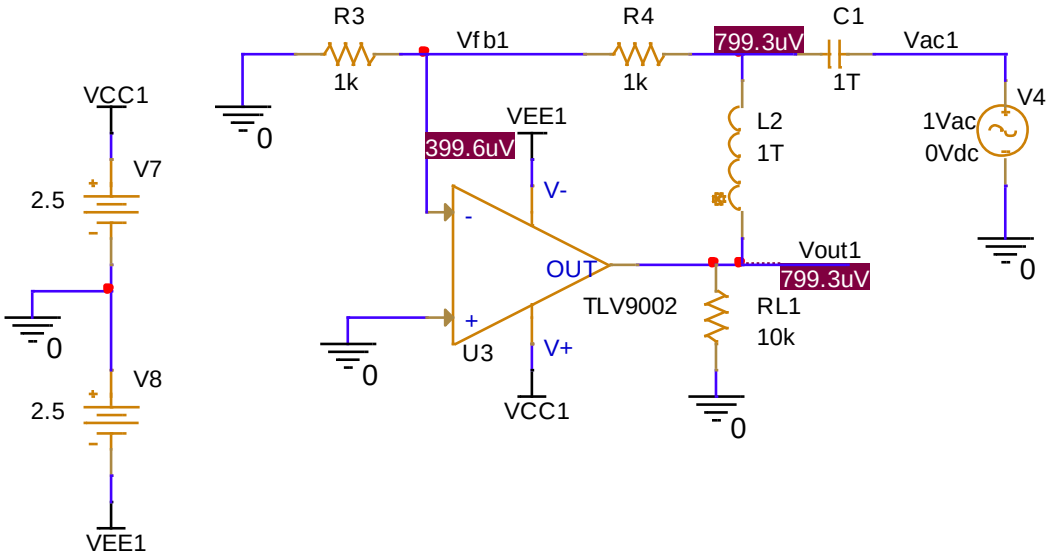
A_{OL_LOADED} = Vo / Vfb

1/β = 1 / Vfb

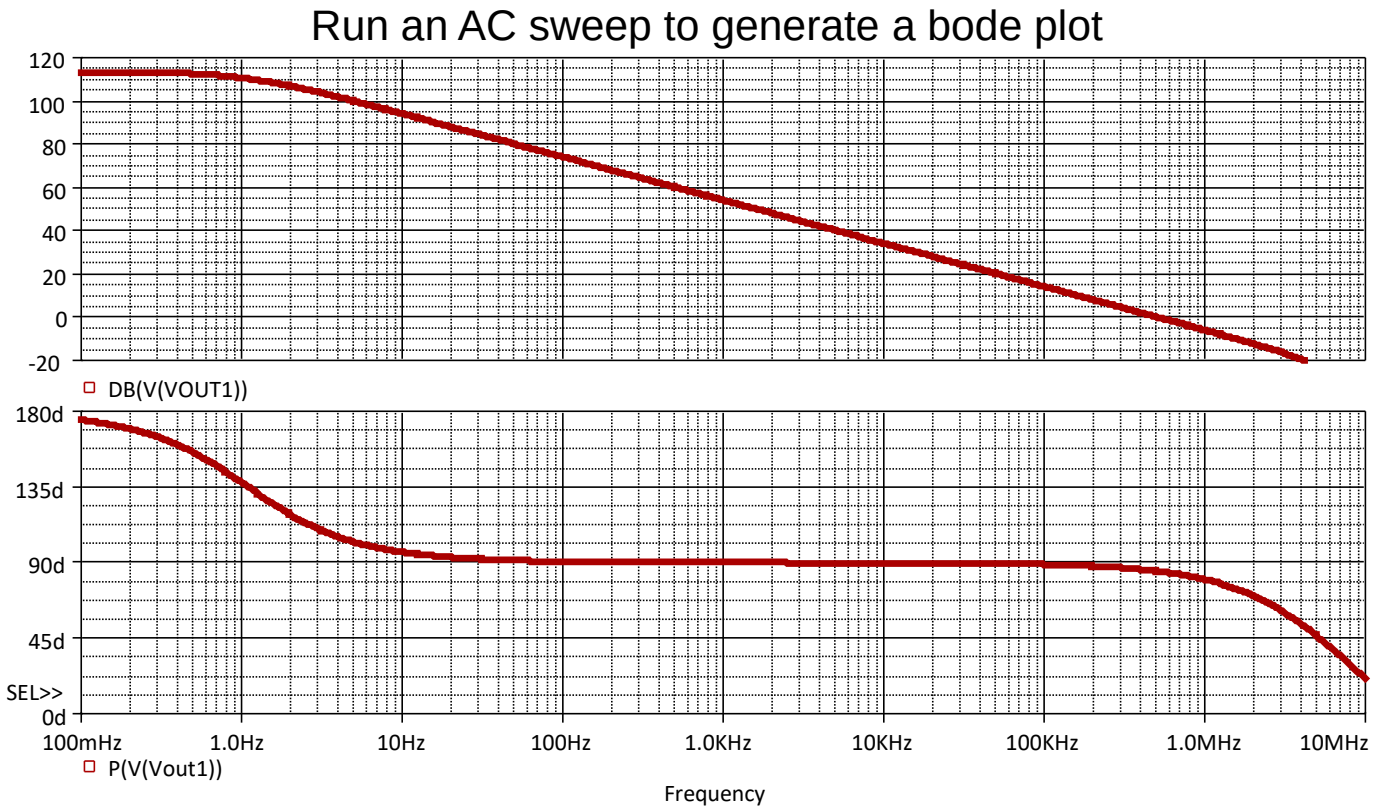
$A_{OL}\beta$ = Vo

Check DC operating point

Run DC-Bias Simulation Profile → Enable Bias Voltage Display



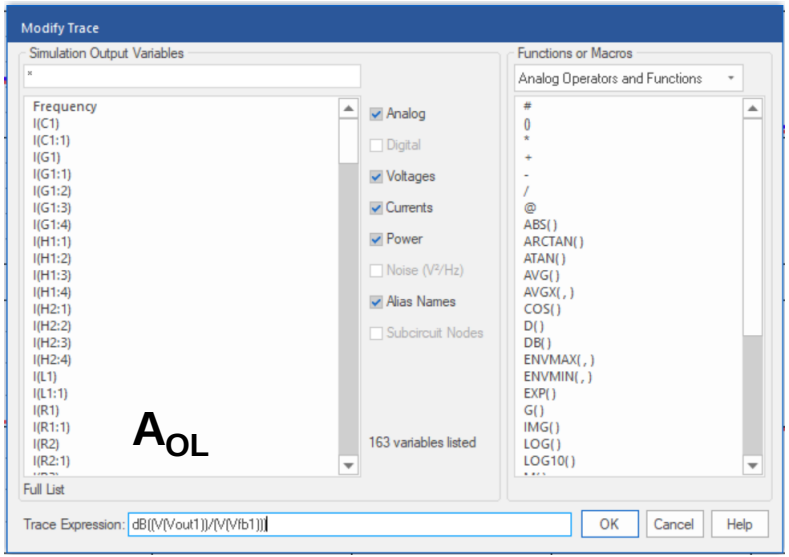
Generating open-loop curves

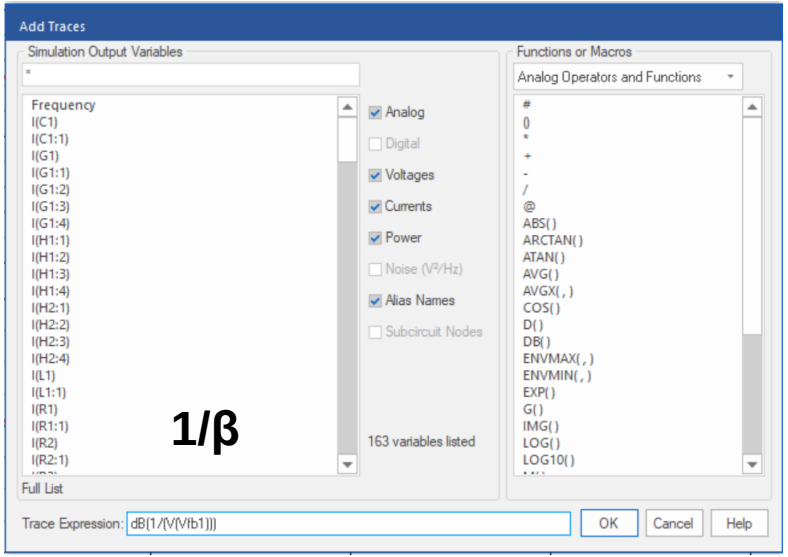


Generating open-loop curves

Perform math on the existing curves to create the new curves:

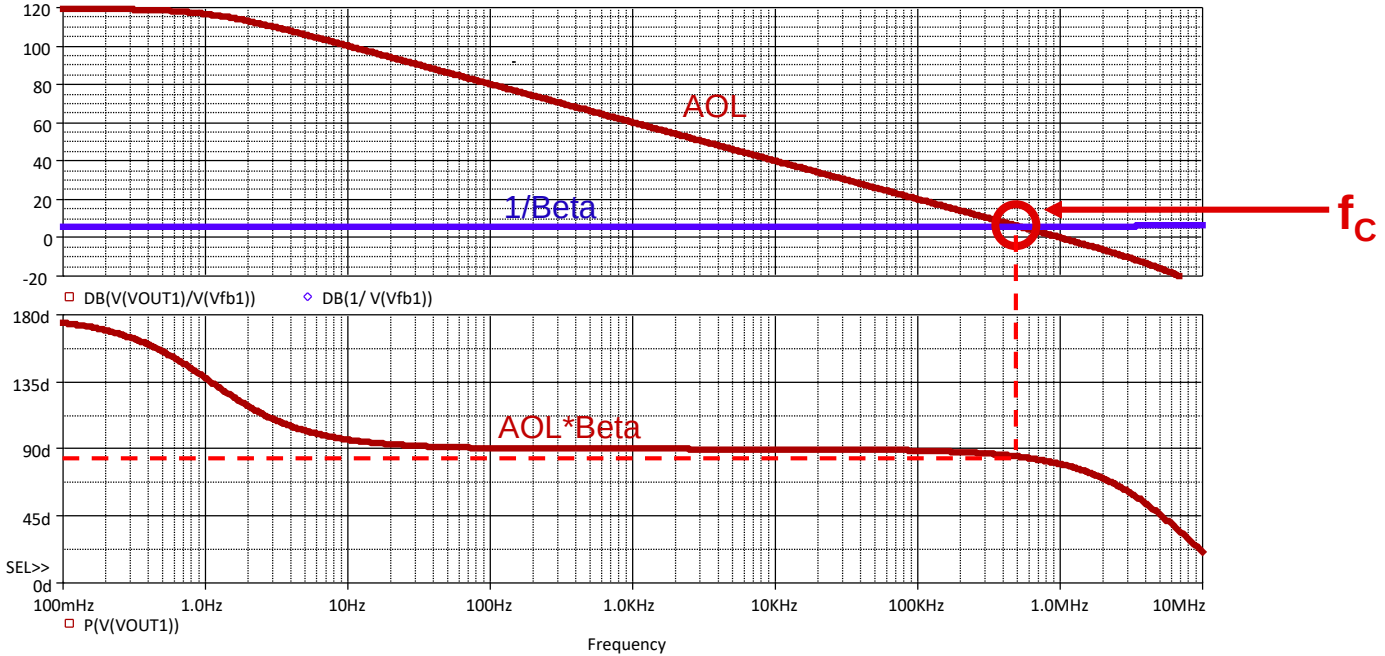
$$A_{OL} = \frac{V_{out}}{V_{fb}} \qquad \frac{1}{\beta} = \frac{V_{ac}}{V_{fb}} = \frac{1}{V_{fb}} \qquad A_{OL}\beta = Vout$$





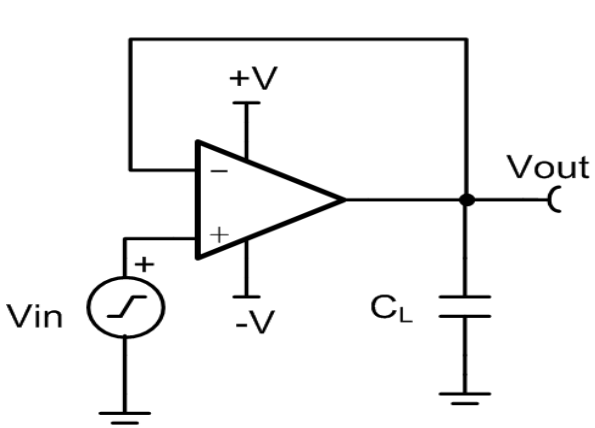
Generating open-loop curves

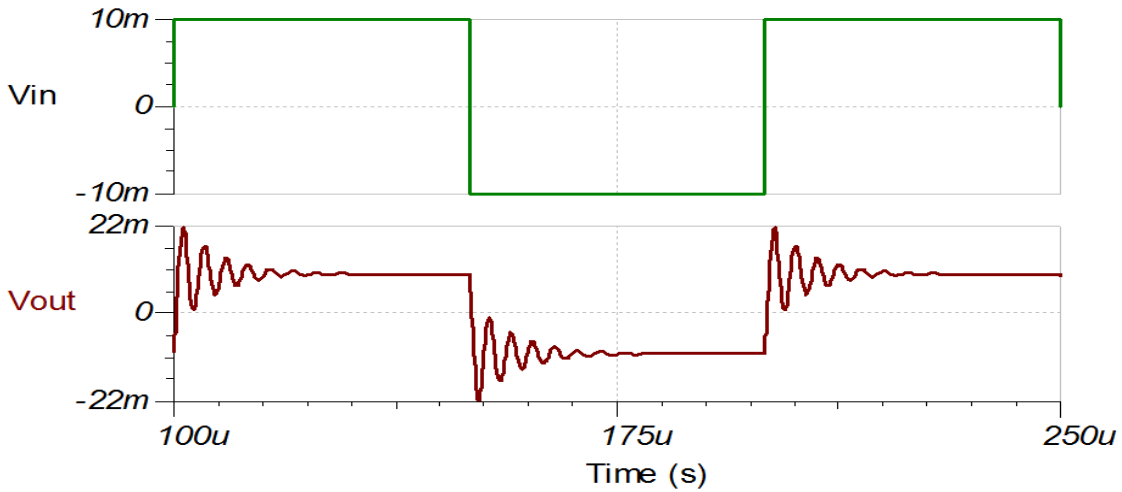
Use a cursor to determine the frequency where Aol intersects 1/Beta, f_C, then use a cursor to observe the phase of Aol*Beta at f_C.



Phase margin = Aol*β Phase @ f_C

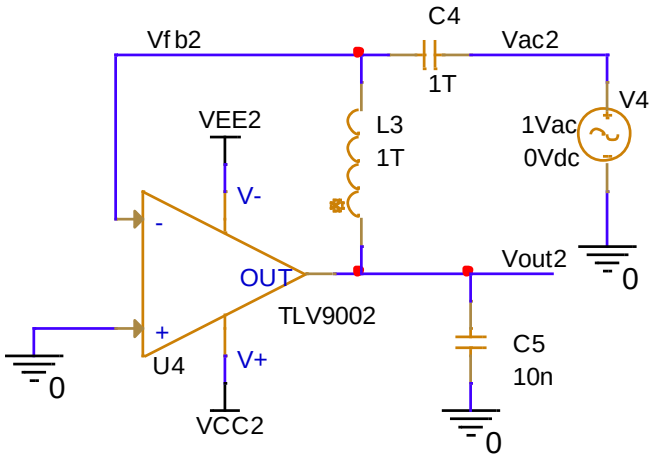
Why do capacitive loads cause instability?

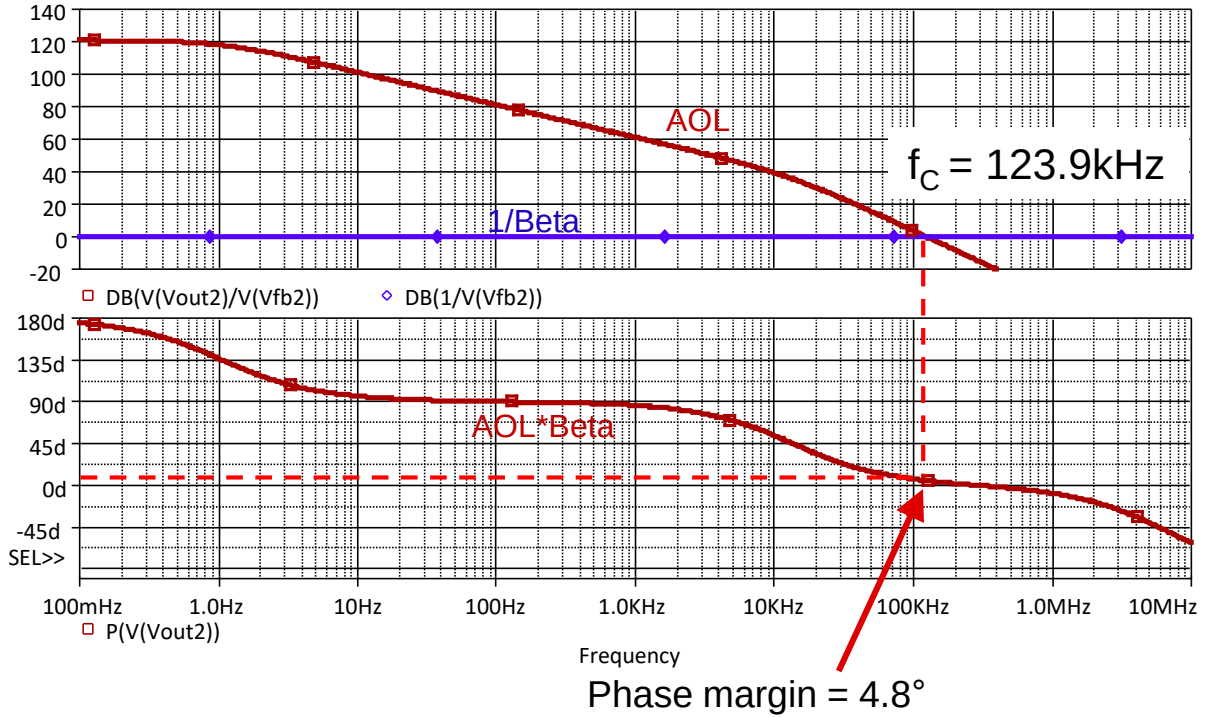




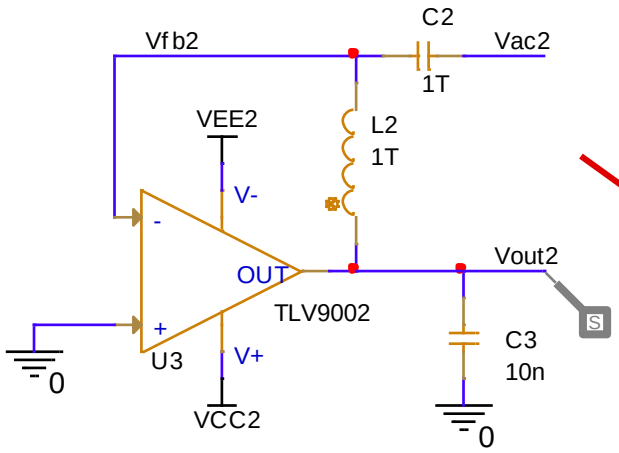
Simulate the effects of output capacitance

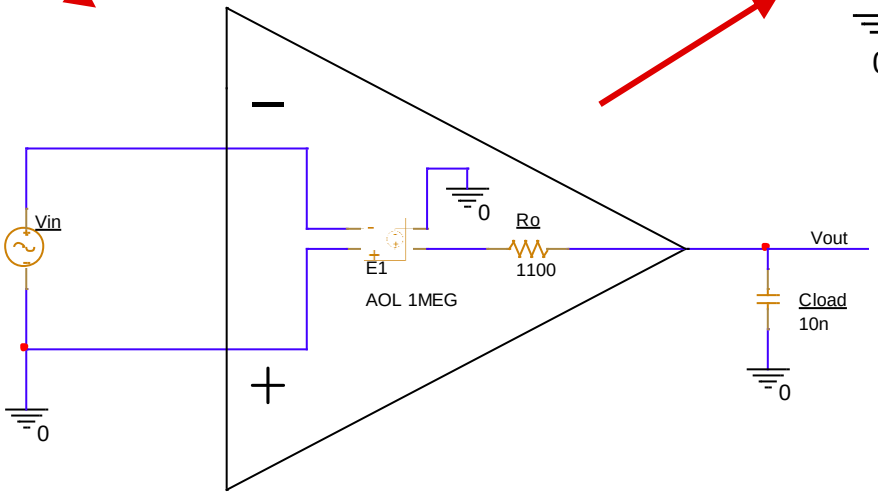
Run open-loop analysis on buffer circuit with capacitive load

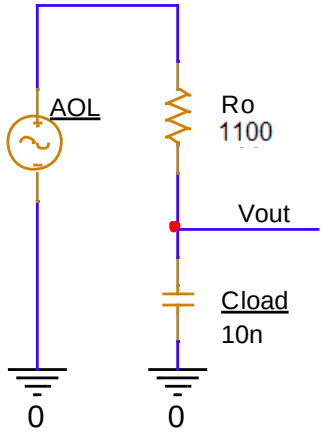




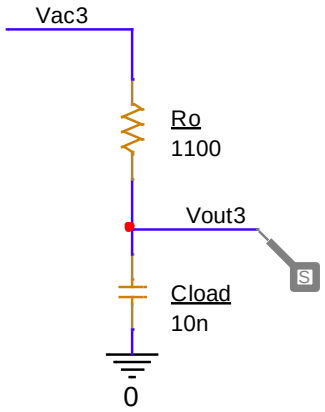
Capacitive loads – stability theory

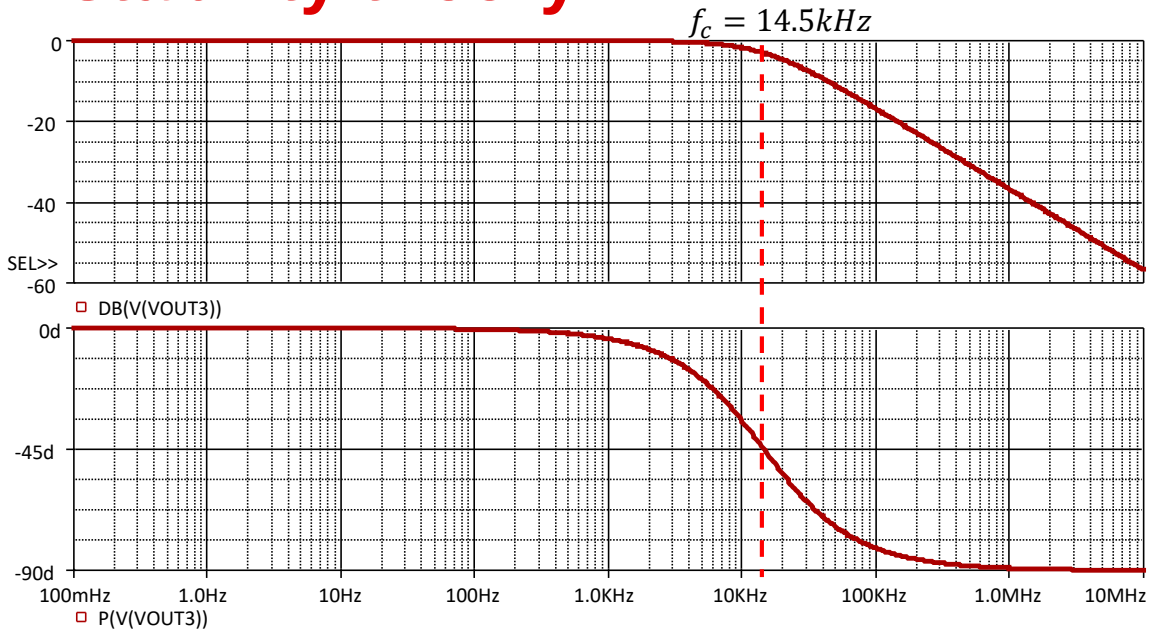






Capacitive loads – stability theory



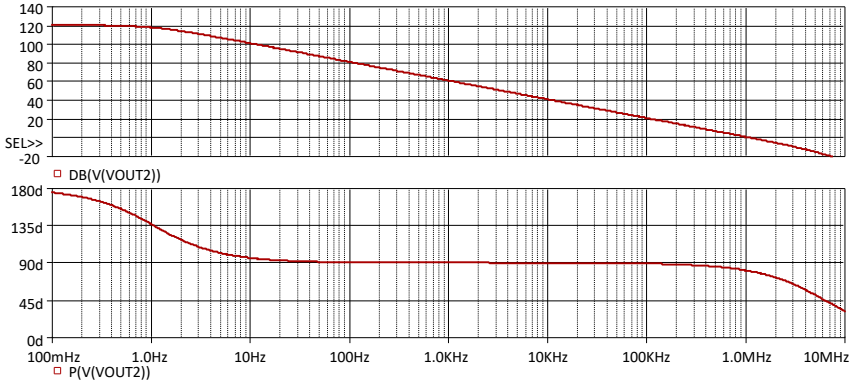


Transfer function: $$\frac{V_o}{V_{in}}(s) = \frac{1}{1 + s * Ro * C_{LOAD}}$$

Pole equation: $$f_{POLE} = \frac{1}{2 * \pi * Ro * C_{LOAD}}$$

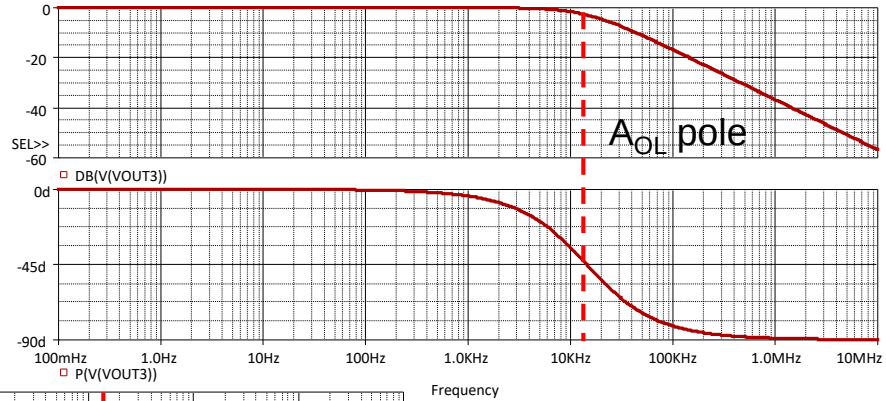
Capacitive loads – stability theory

A_{OL} (from data sheet)

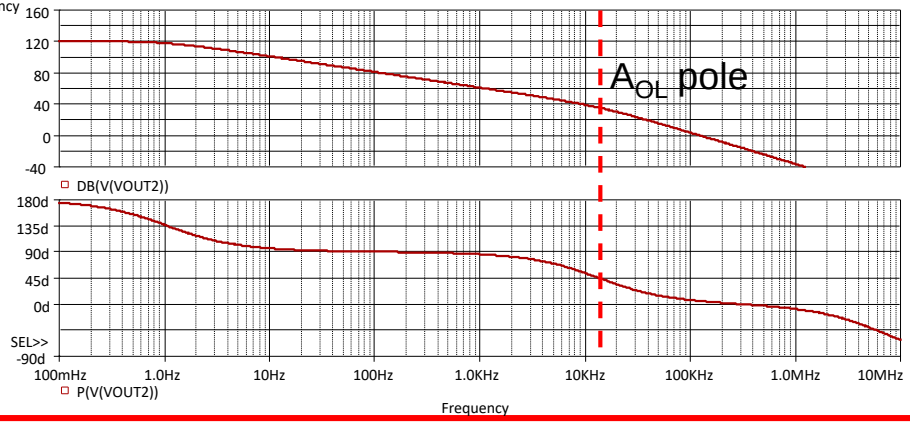


X

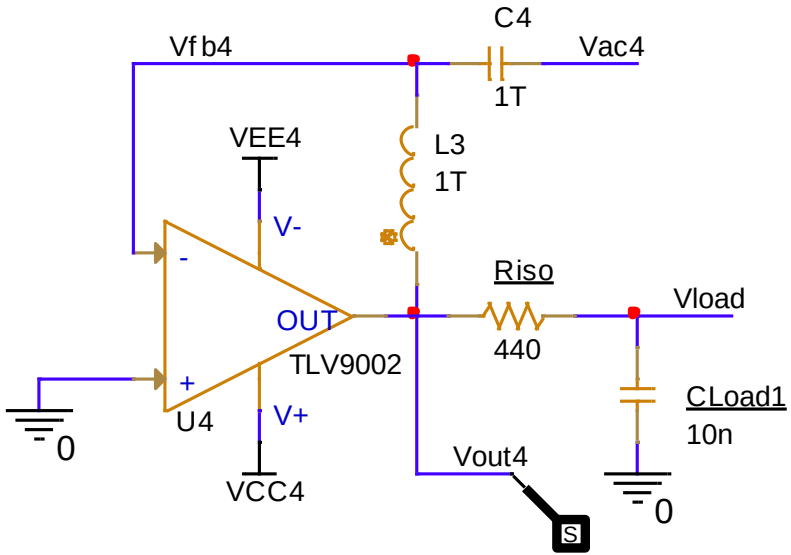
A_{OL} load



Loaded A_{OL} =

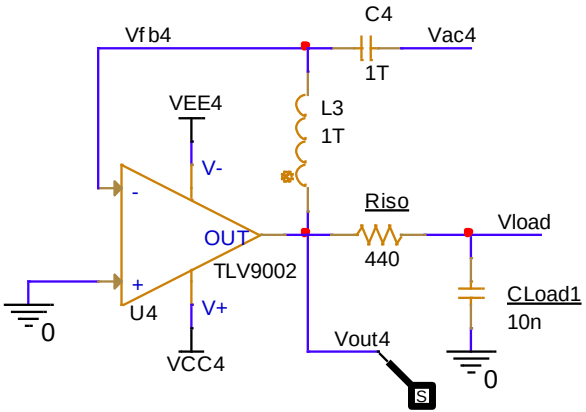


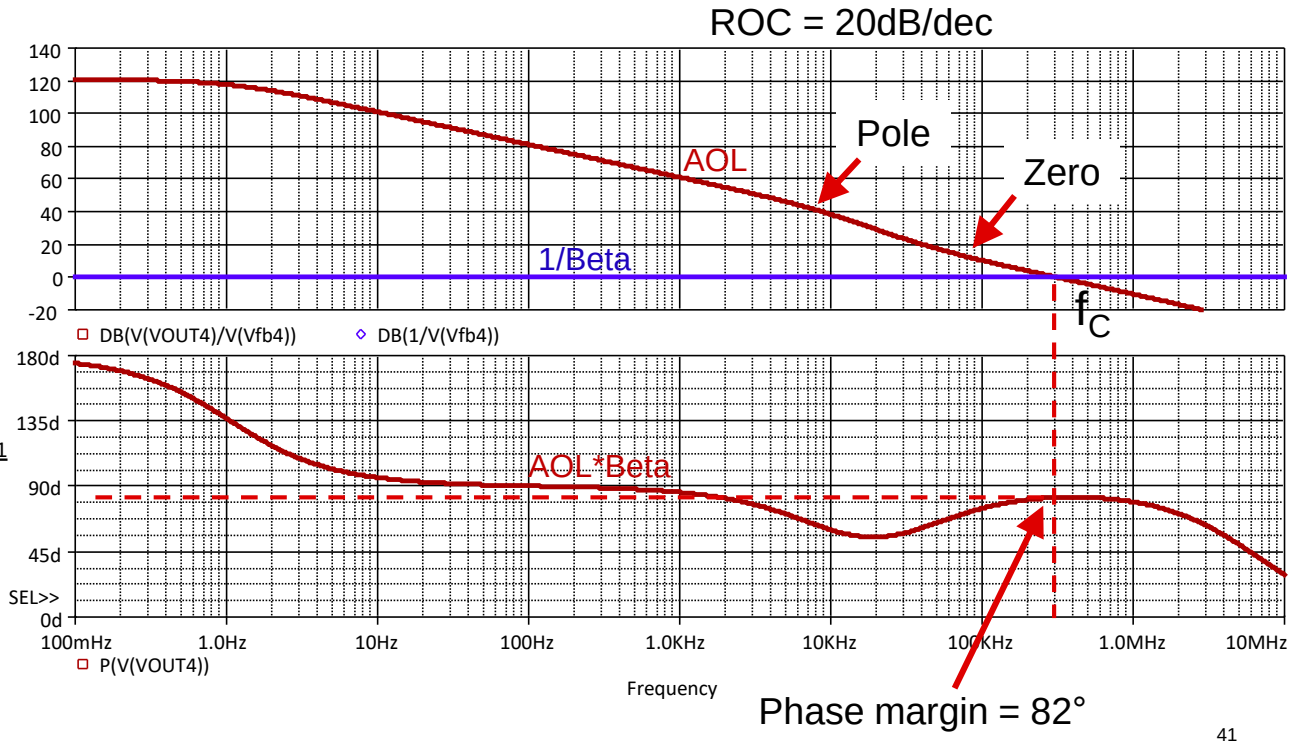
Compensation method 1: R_{ISO}



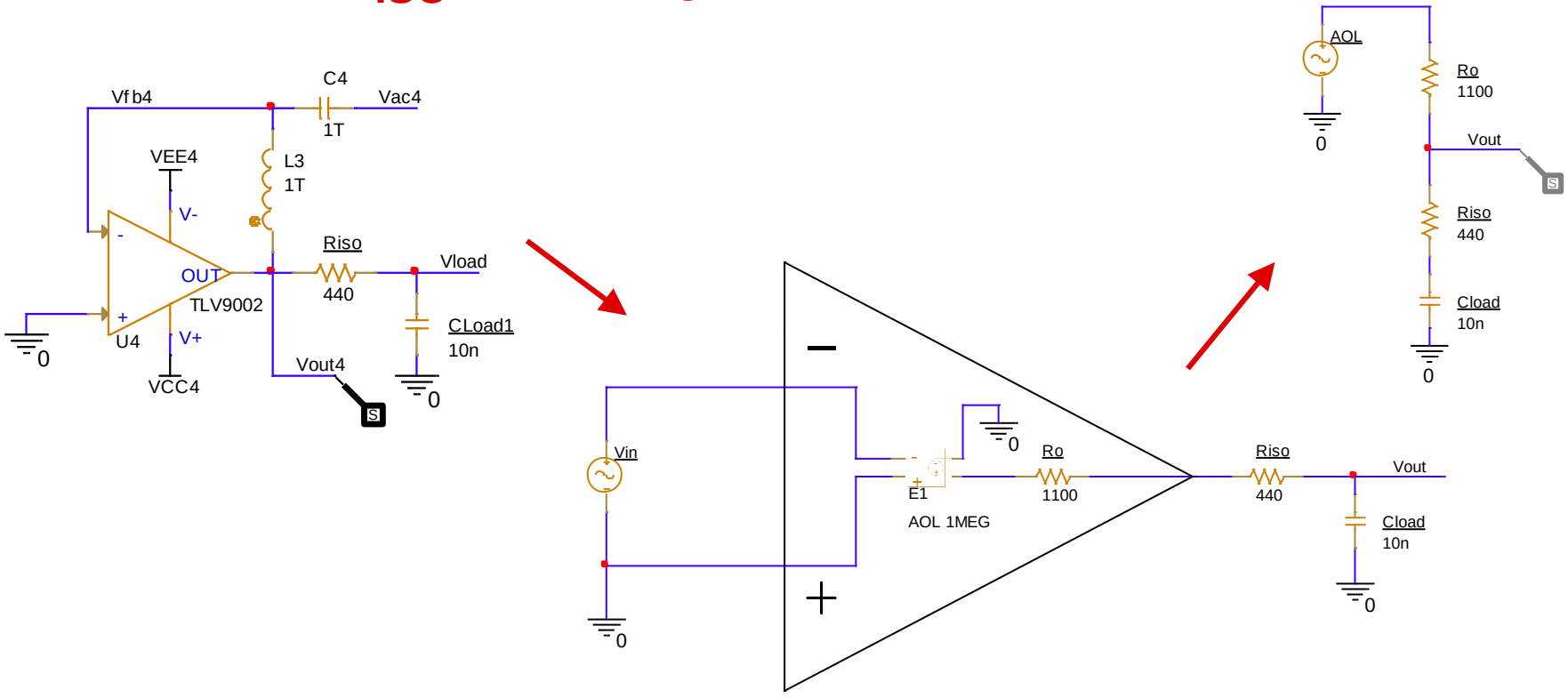
Method 1: R_{ISO} – results

Theory: Adds a zero to cancel the pole in loaded A_{OL}

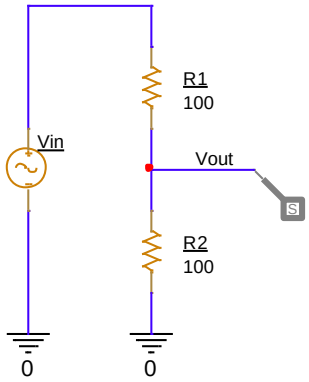




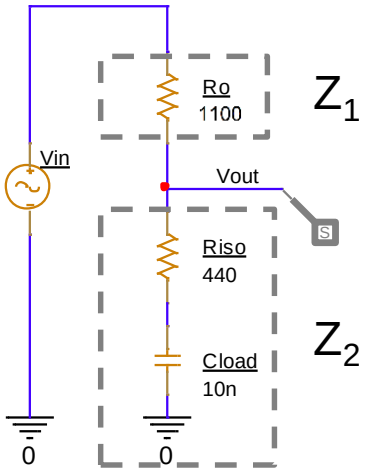
Method 1: R_{ISO} – theory



Resistor divider analogy



$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_2 + R_1}$$



$$\frac{V_{out}}{V_{in}} = \frac{Z_2}{Z_2 + Z_1}$$

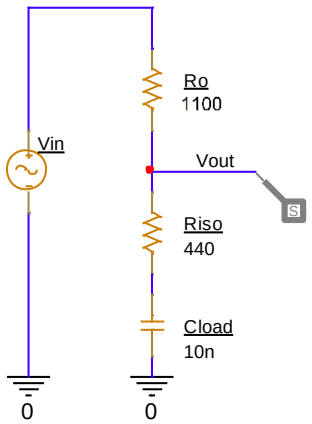
$$\frac{V_{out}}{V_{in}} = \frac{R_{ISO} + \frac{1}{s * C_{LOAD}}}{\left(R_{ISO} + \frac{1}{s * C_{LOAD}}\right) + R_O}$$

$$\frac{V_{out}}{V_{in}} = \frac{1 + s * R_{ISO} * C_{LOAD}}{1 + s * (R_{ISO} + R_O) * C_{LOAD}}$$

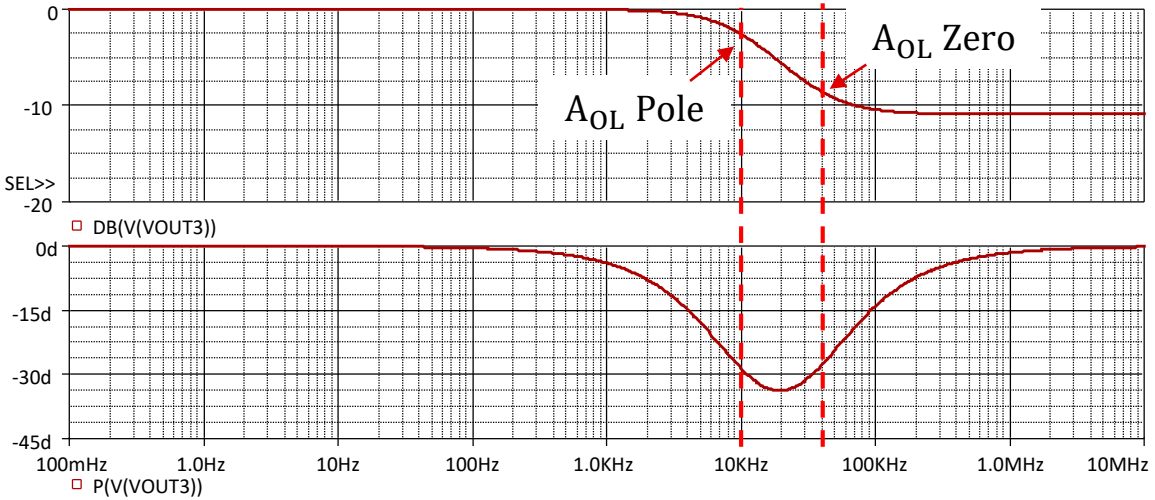
Zero: R_{ISO} & C_{LOAD}

Pole: R_O, R_{ISO}, and C_{LOAD}

Method 1: R_{ISO} – theory



Vin = datasheet Aol



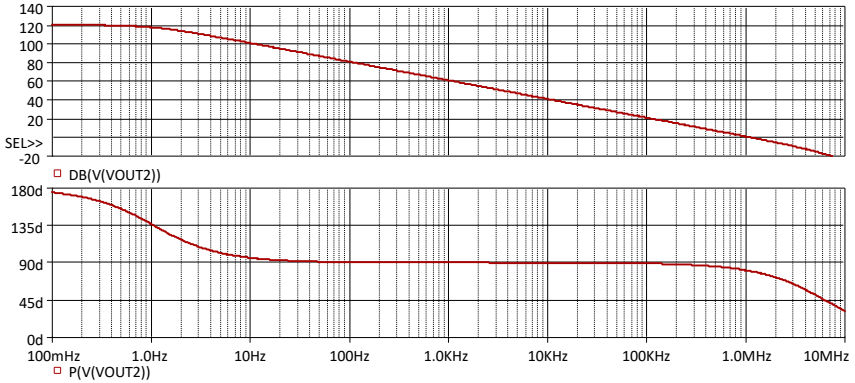
Transfer function: $$\frac{V_o}{V_{in}}(s) = \frac{1 + s * R_{ISO} * C_{LOAD}}{1 + s * (R_O + R_{ISO}) * C_{LOAD}}$$

Zero equation: $$f_{ZERO} = \frac{1}{2 * \pi * R_{ISO} * C_{LOAD}}$$

Pole equation: $$f_{POLE} = \frac{1}{2 * \pi * (R_O + R_{ISO}) * C_{LOAD}}$$

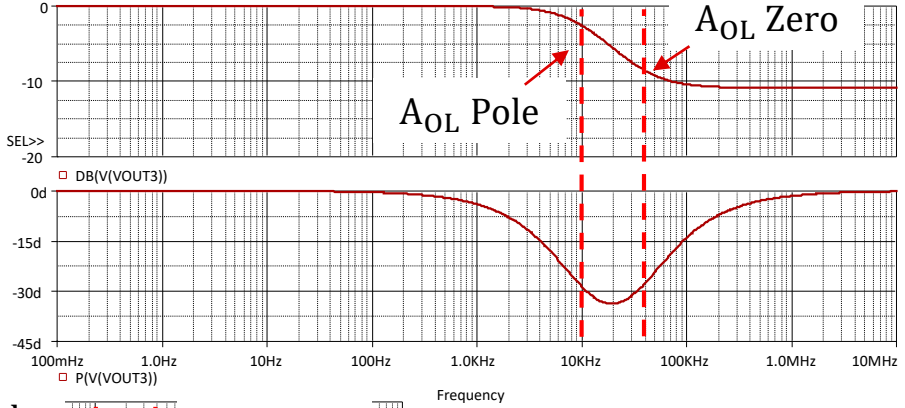
Method 1: R_{ISO} – theory

A_{OL} (from data sheet)

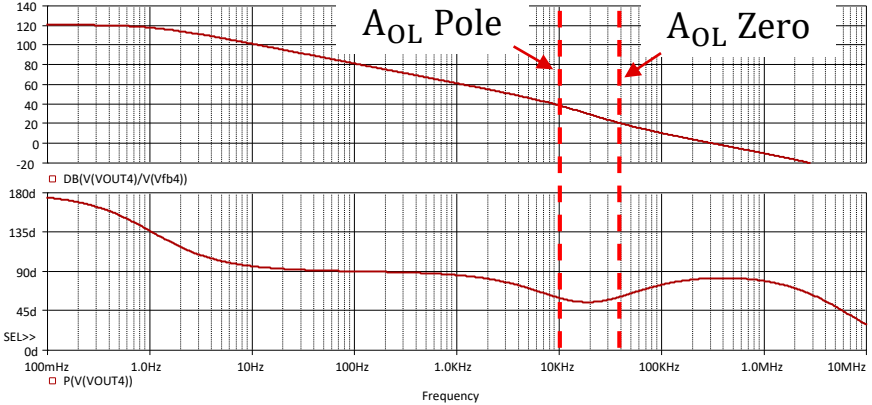


X

A_{OL} load



Loaded A_{OL} =



Method 1: R_{ISO} – design

Design steps:

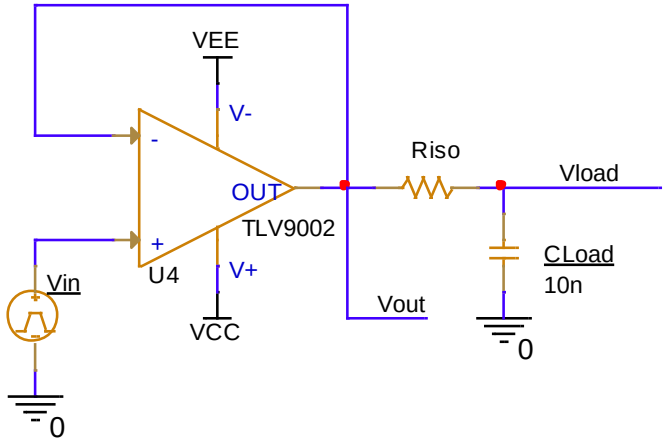
1.) Find the zero frequency, f_{ZERO}, where A_{OL_Loaded} = 20dB
2.) Calculate Riso to set the zero at f_{ZERO}
This will yield between 60° and 90° degrees of phase margin

R_{ISO} equation:

$$R_{iso} = \frac{1}{2 * \pi * f_{ZERO} * C_{LOAD}}$$

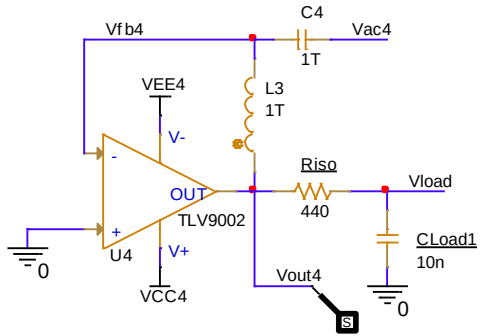
$$R_{iso} = \frac{1}{2 * \pi * 36kHz * 10nF}$$

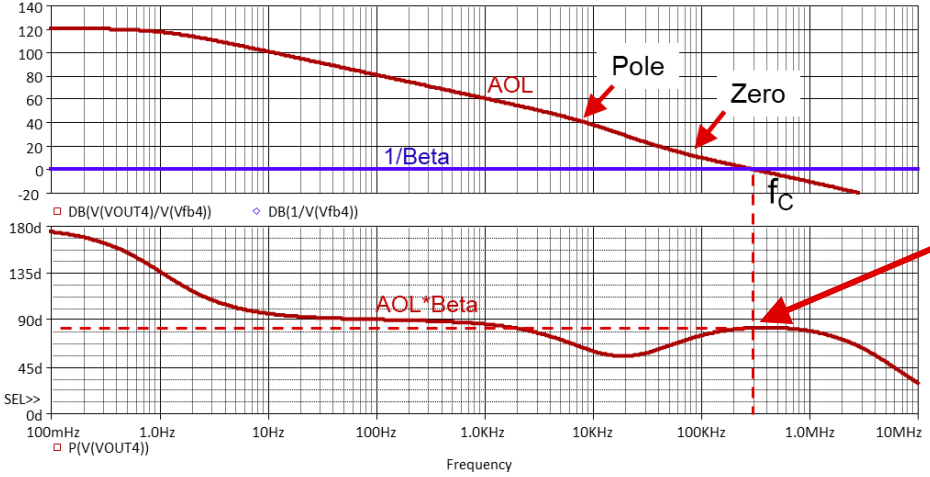
$$R_{iso} = \mathbf{442\Omega} \rightarrow R_{iso} = 440\Omega \text{ (Standard Value)}$$



Note: Goal is to cancel pole due to Cload & Ro.

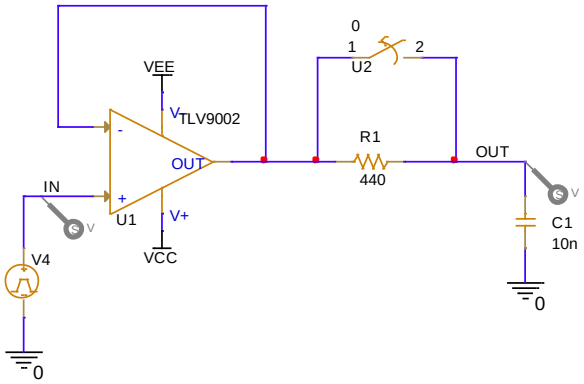
Method 1: R_{ISO} – AC results

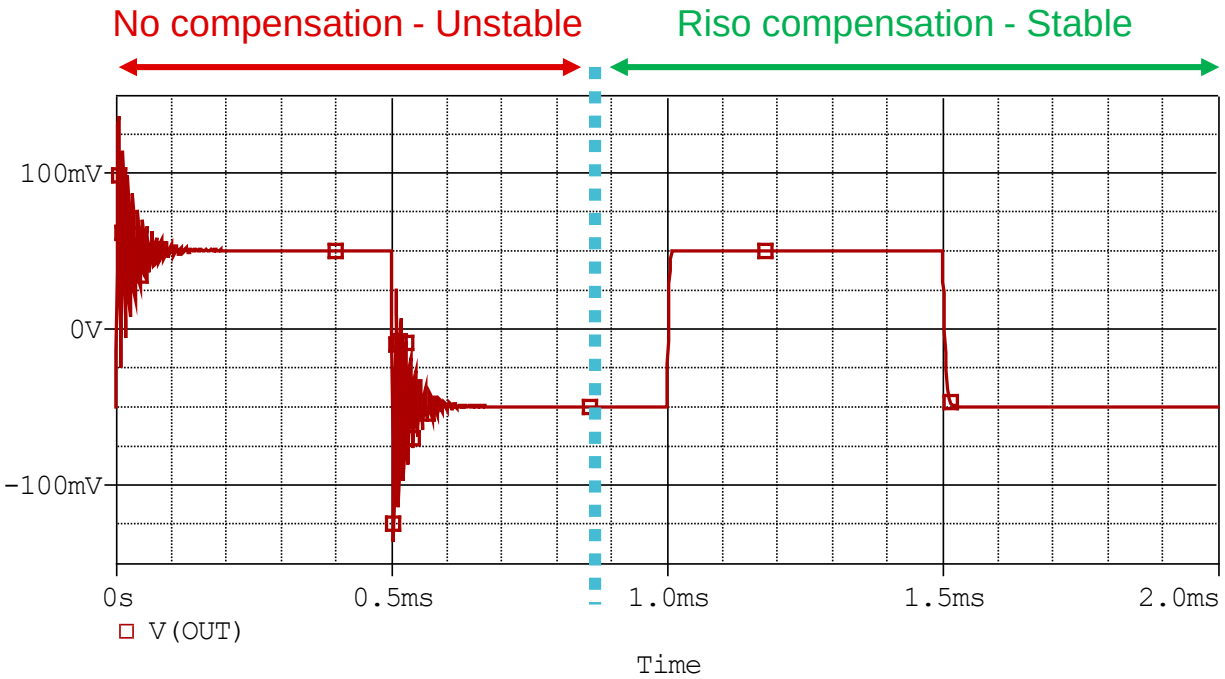




Phase margin = 82°

Unstable vs. stable transient results

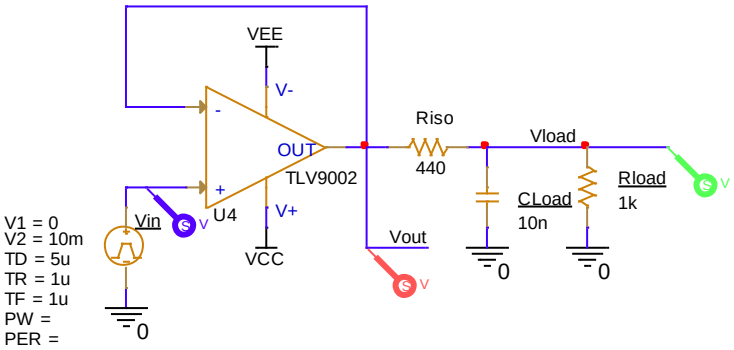


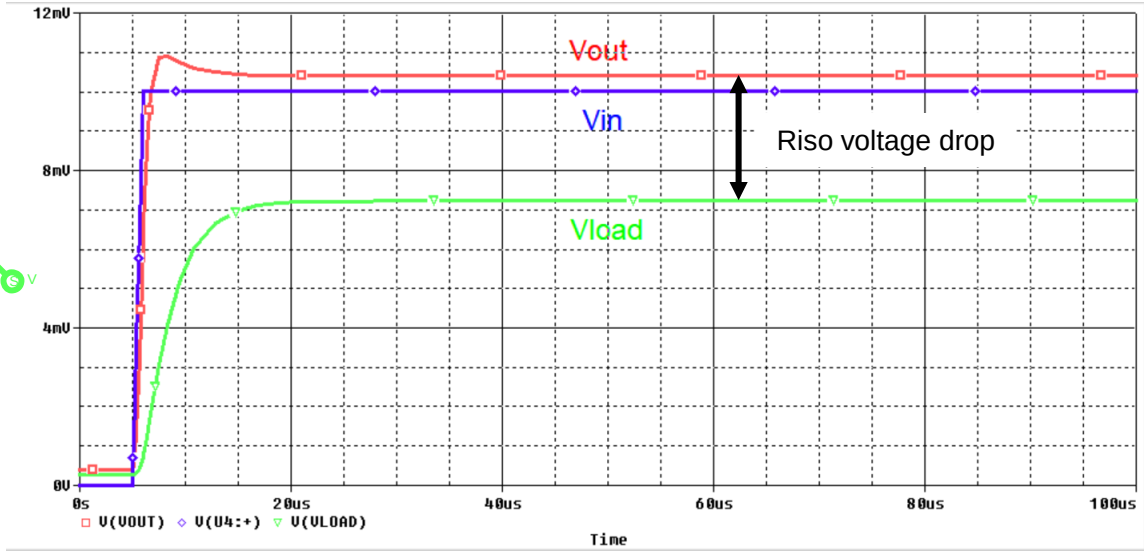


Method 1: R_{ISO} – disadvantage

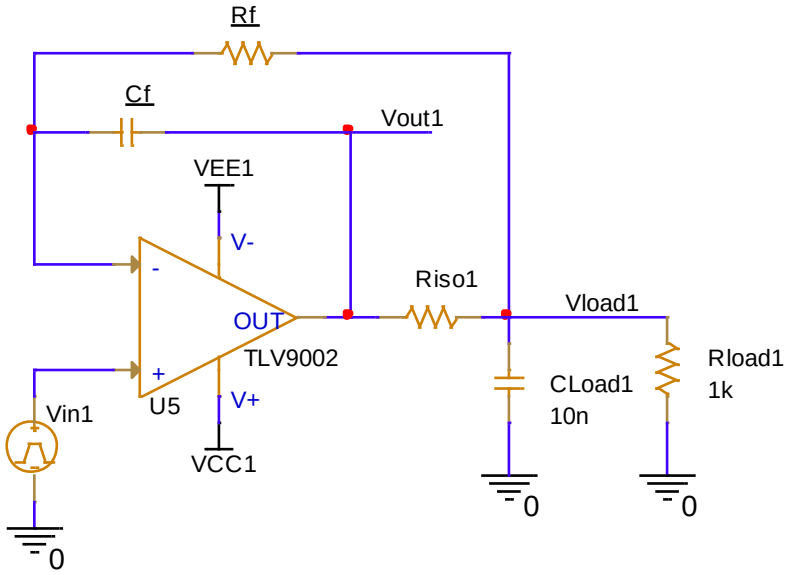
Disadvantage:

Voltage drop across R_{ISO} may not be acceptable for certain applications.





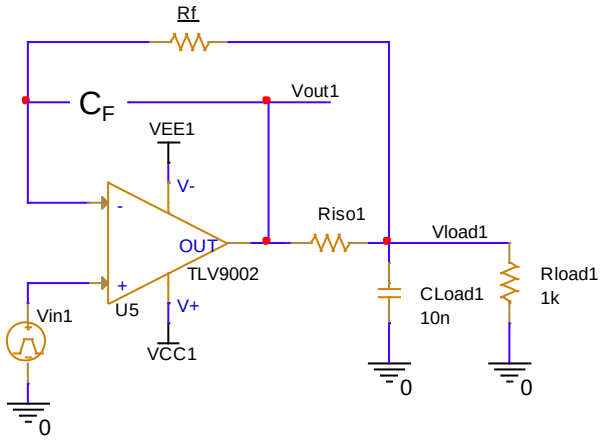
Method 2: R_{ISO} + dual feedback



Method 2: R_{ISO} + dual feedback – theory

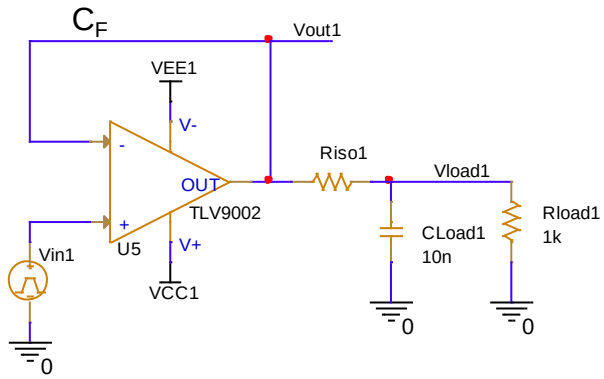
DC circuit

C_F: Open
R_F: Closes the feedback around R_{ISO}
$V_{LOAD} = V_{IN}$



AC circuit

C_F: Short
R_F >> Z_{CF}, therefore R_F is effectively open
Behaves like R_{ISO} circuit



Method 2: R_{ISO} + dual feedback - design

Design steps:

1. Set R_{ISO} using method 1: R_{ISO} techniques

   $R_{ISO} = 440\Omega$

2. Set R_F: $R_F \geq (R_{ISO} * 100)$

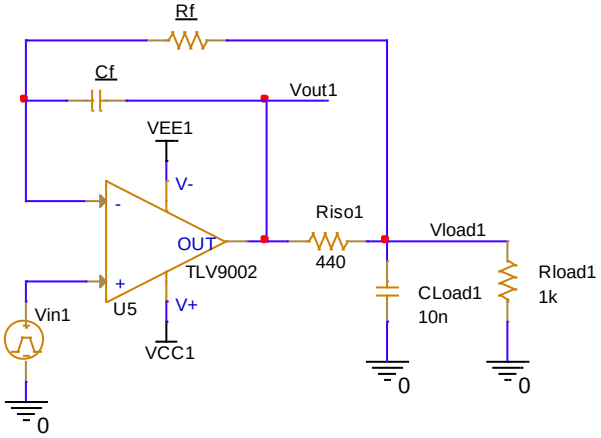
   $R_F \geq R_{ISO} * 100$

   $R_F \geq 44k\Omega \rightarrow R_F = 49.9k$ (Standard Value)

3. Set C_F:

   $$\frac{5 \times R_{iso} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{iso} \times C_L}{R_F}$$

   $440pF \leq C_F \leq 881pF \rightarrow C_F = 680pF$

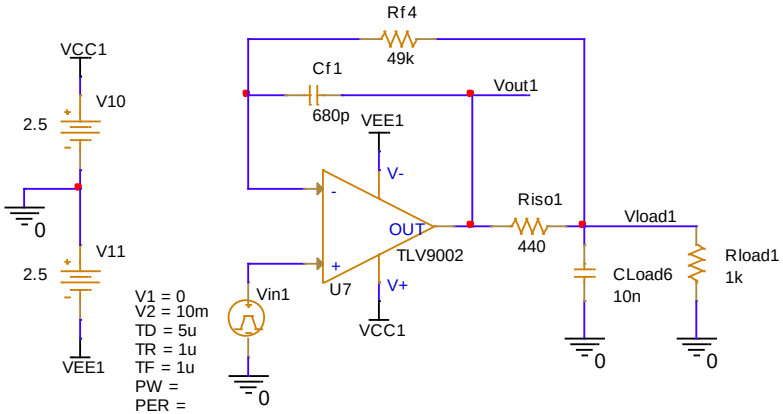


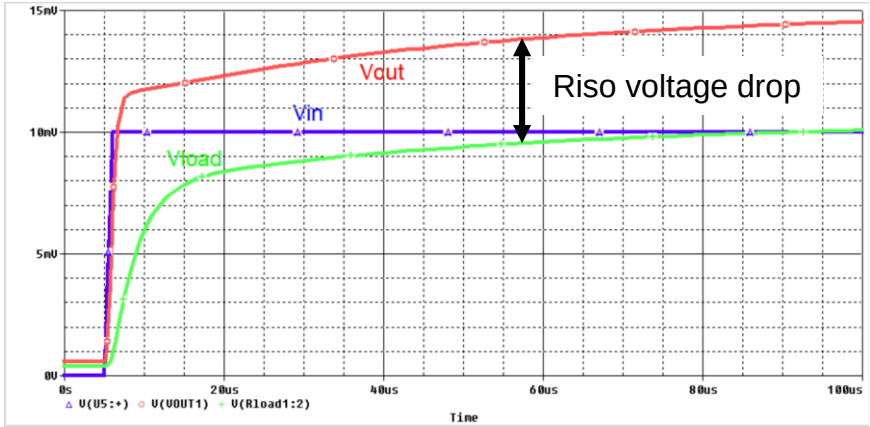
Notes:

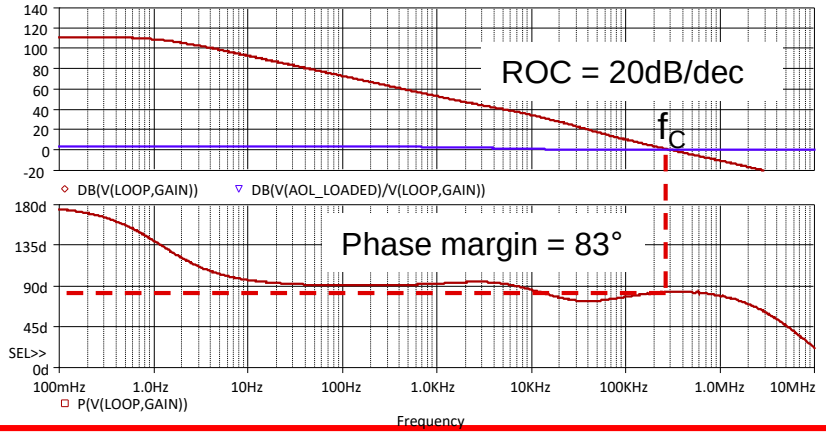
- Rule 3 ensures that the two feedback paths will never create a resonance that would cause instability
- Lower values of C_F = faster settling, higher overshoot

Method 2: R_{ISO} + dual feedback - results

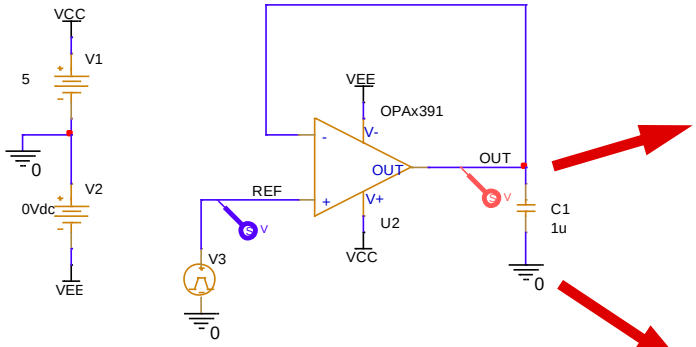
- V_{LOAD} matches V_{IN} – no voltage divider error.
- This topology has some limitations on settling time and capacitive load range

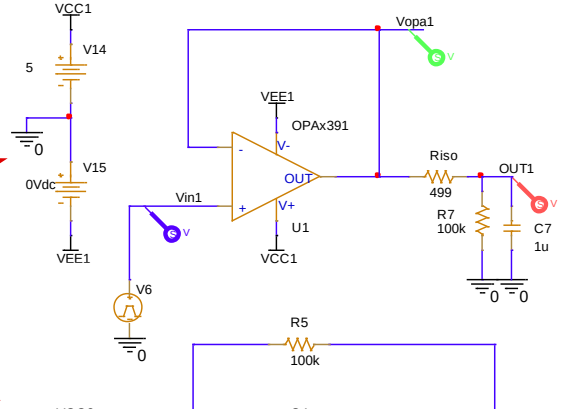


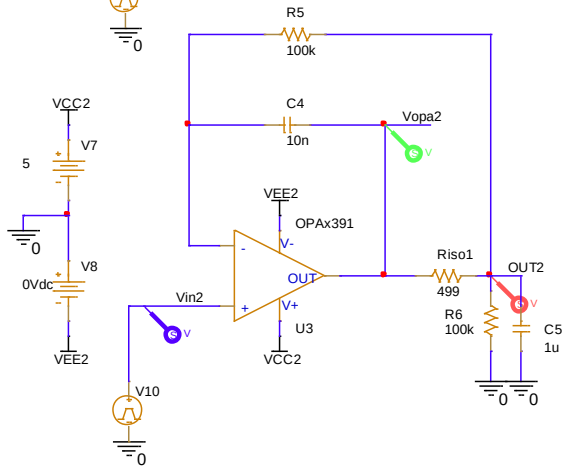


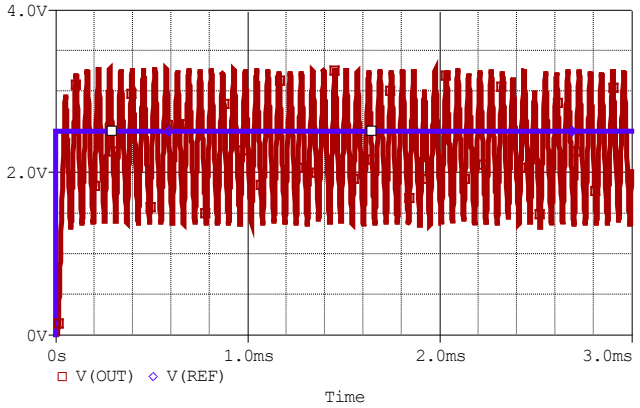


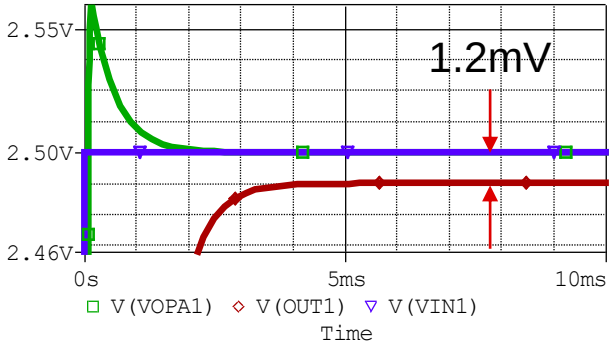
Solving op amp stability issues



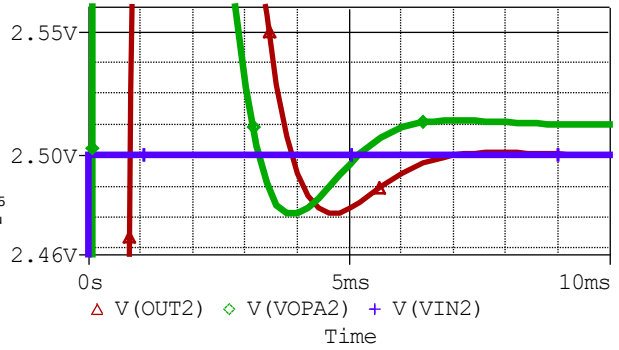








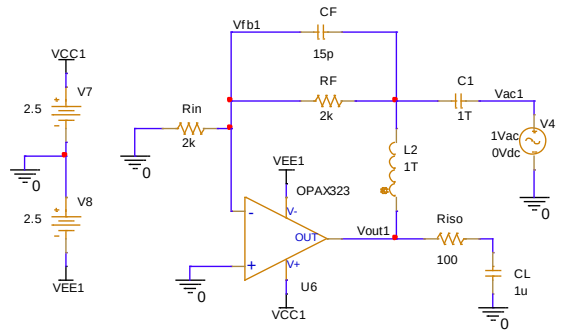
OPA391 $V_{os(typ)}$ = 10µV

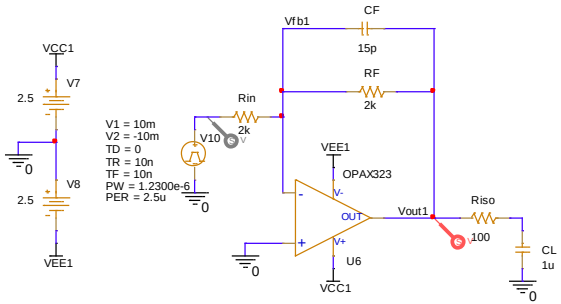


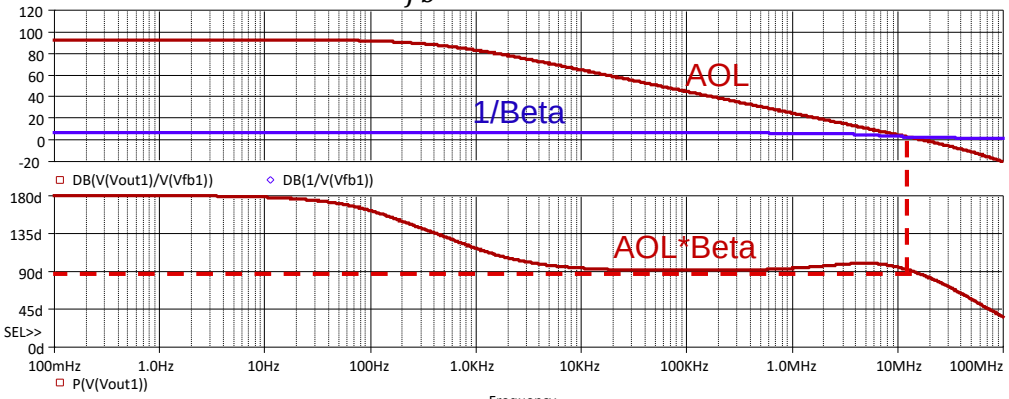
Summary: Method 1 to break the loop

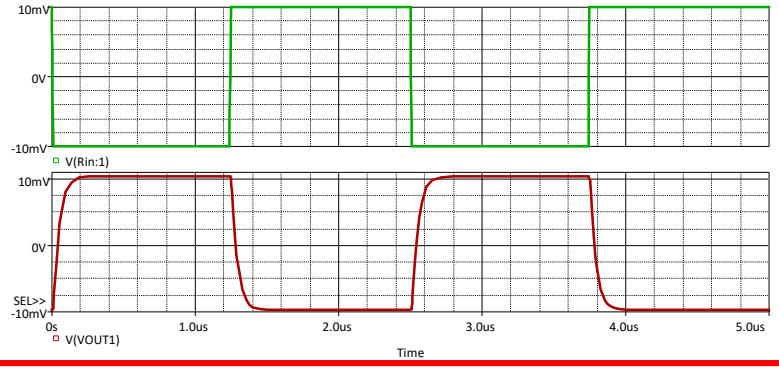
$$A_{OL} = \frac{V_{out}}{V_{fb}} \qquad \frac{1}{\beta} = \frac{V_{ac}}{V_{fb}} = \frac{1}{V_{fb}}$$

$$Loop\ gain = A_{OL}\beta = \frac{V_{out}}{V_{fb}} \times V_{fb} = V_{out}$$

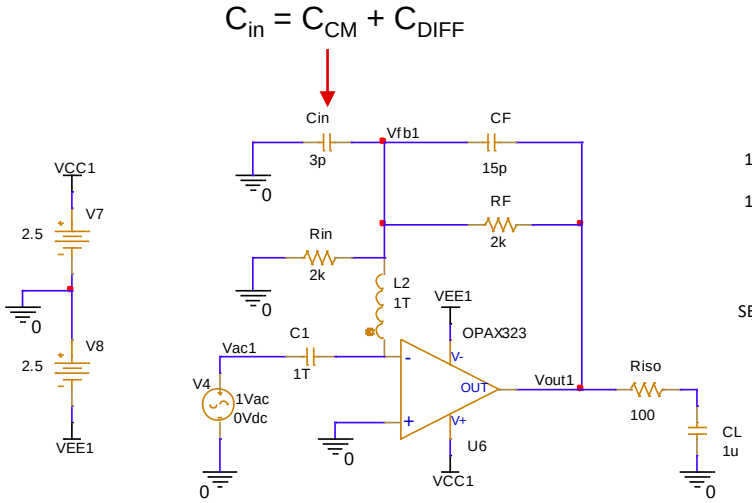


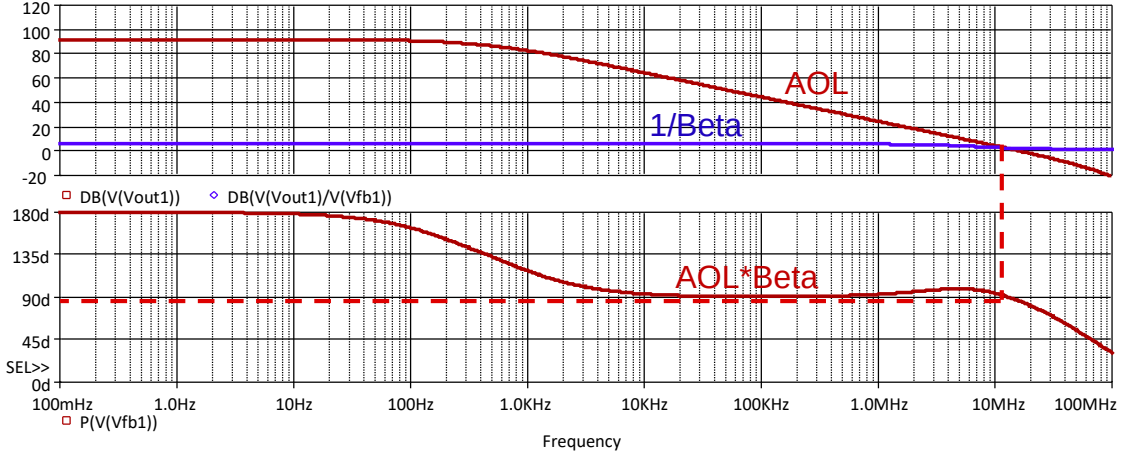






Summary: Method 2 to break the loop



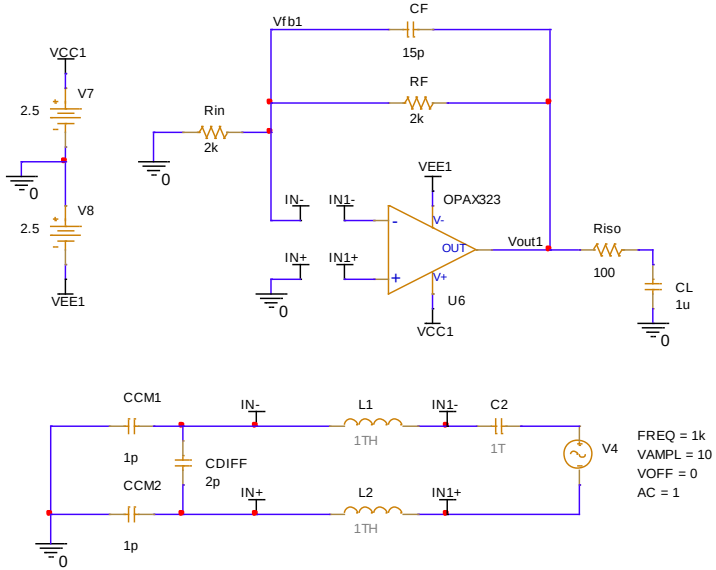


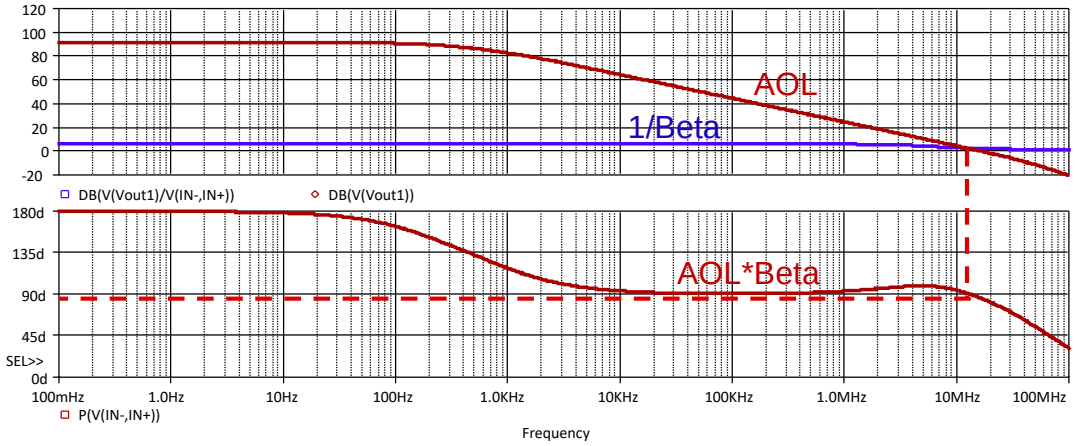
$$A_{OL} = V_{out}$$

$$\frac{1}{\beta} = \frac{V_{out}}{V_{fb}}$$

$$Loop\ gain = A_{OL}\beta = \left(V_{out} \times \left(\frac{V_{fb}}{V_{out}}\right)\right) = V_{fb}$$

Summary: Method 3 to break the loop



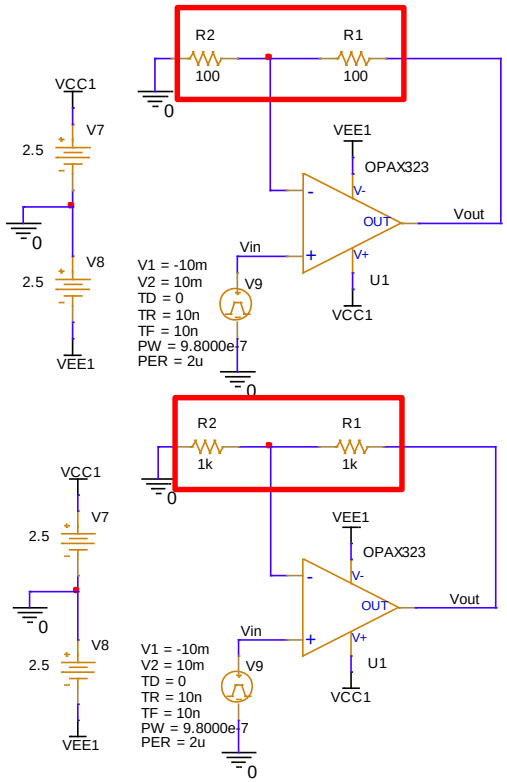


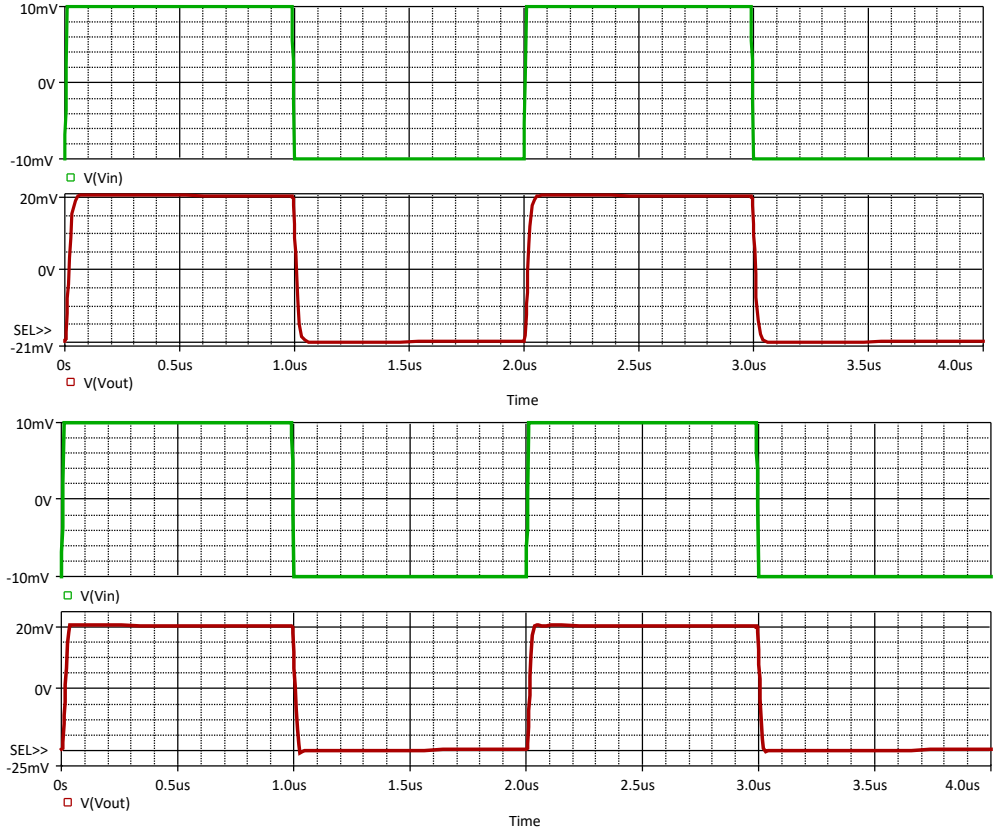
$$A_{OL} = V_{out}$$

$$\frac{1}{\beta} = \frac{V_{out}}{(V_{IN-}) - (V_{IN+})}$$

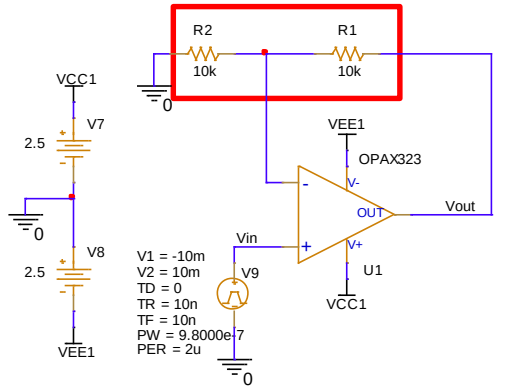
$$Loop\ gain = A_{OL}\beta = (V_{IN-}) - (V_{IN+})$$

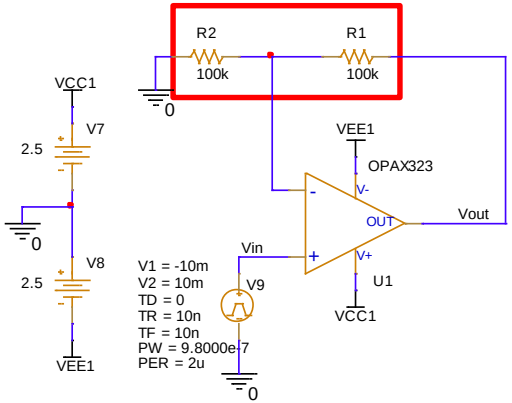
Solving op amp stability

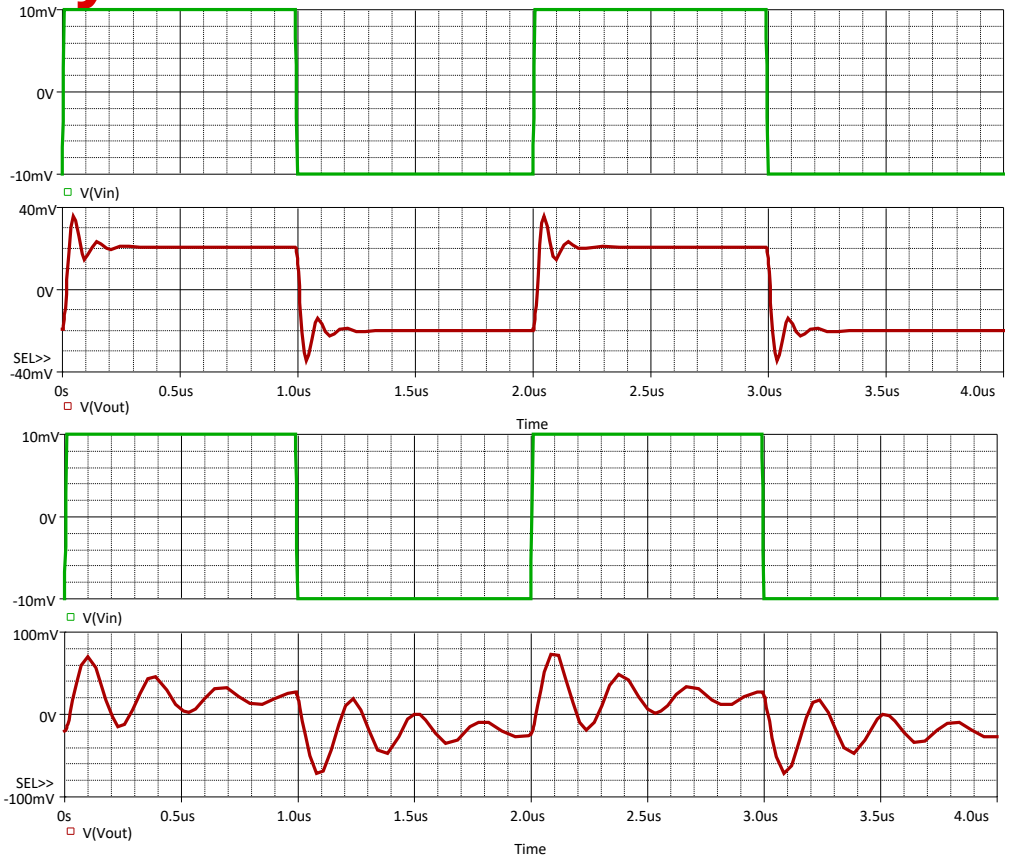




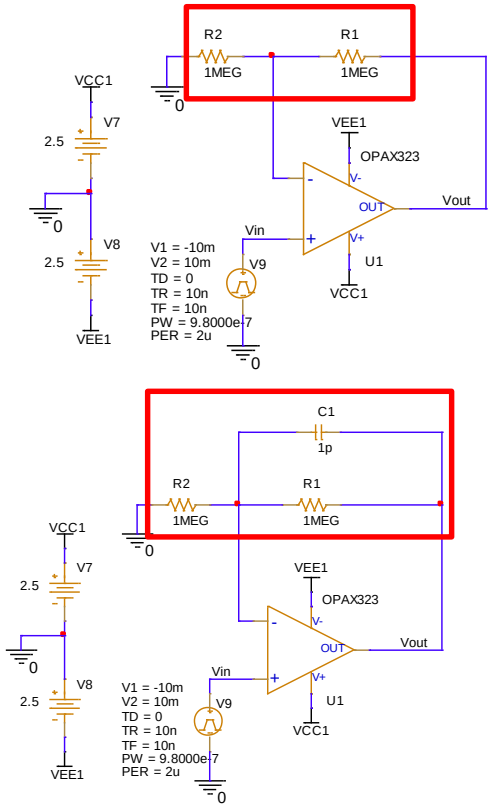
Solving op amp stability

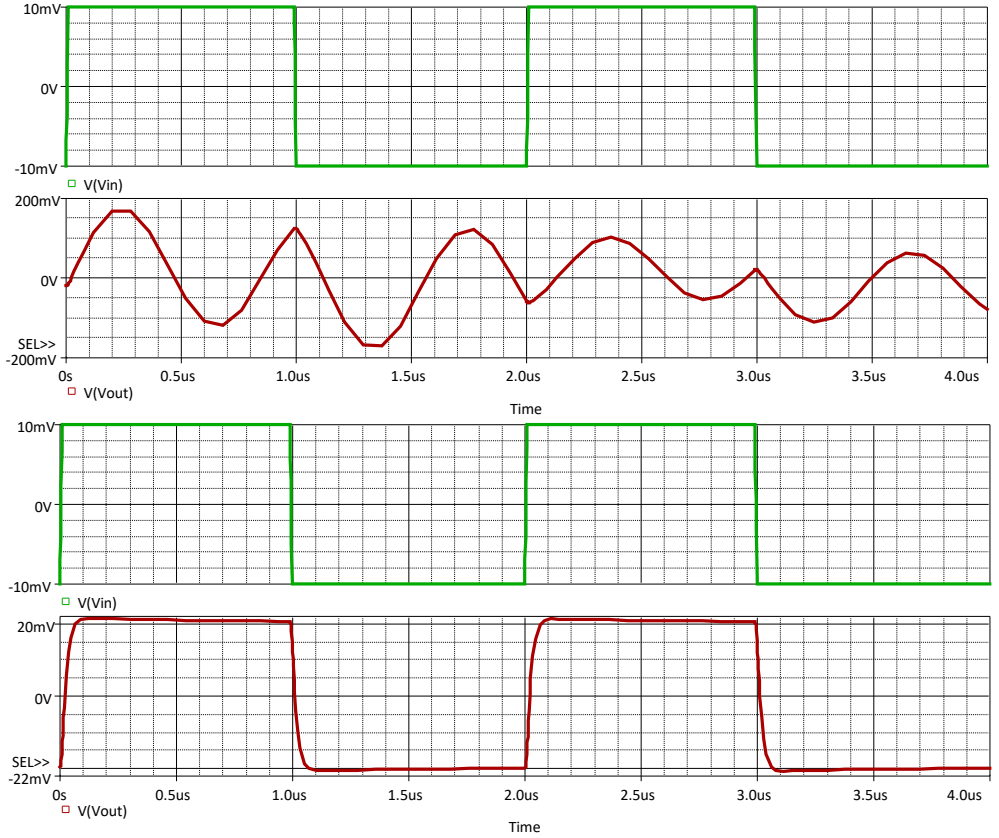






Solving op amp stability





Resources

- TI Precision Labs (TIPL) Op Amps Stability Series
- Analog Engineer's Pocket Reference Guide
- PSpice for TI simulation tool
- TINA-TI simulation tool
- Analog Engineer’s Calculator
- Universal do-it-yourself amplifier circuit evaluation module (DIYAMP-EVM)

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