Common Standard Logic Use Cases

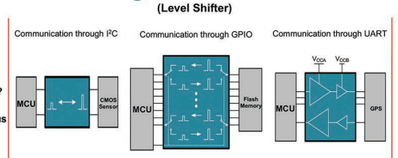
Voltage Level Translation

(Level Shifter)

Does your system have sub-systems communicating between different voltage domains?
Common Interfaces: GPIO, MDIO, PMBus, SDIO,UART, I²C, SPI, SMBus

Why: Translating Different Voltage Levels

Communication through I²C / Communication through GPIO / Communication through UART

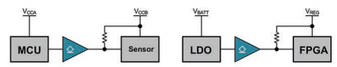


Recommendations:
SN74AXC1T45
LSF0102
TXS0102

Does your system need to isolate different voltage domains?

Why: Isolating Different Power Sources

(Buffer)
Voltage Source Separation



Recommendations:
SN74LVC1G07
SN74LVC07A
SN74LVC1G125

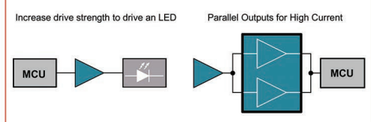
Signal Integrity

(Buffer)

Does your system need to drive a high current peripheral from a low current controller?

Why: Enhancing Drive Strength

Increase drive strength to drive an LED / Parallel Outputs for High Current



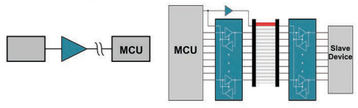
Recommendations:
SN74AUP1G34
SN74LVC2G34

(Transceiver)

Does your system have signals on long traces or high capacitance lines? Or does any output in your system need to drive multiple inputs?

Why: Overcoming high capacitance loads

Redriving Long Traces / Parallel Communications over Lossy Line



Recommendations:
SN74LVC1G34
SN74LVC244A
SN74LVC245A

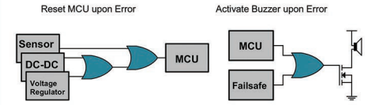
Signal Routing

(Logic Gates)

Does your system have multiple error signals that need to control a single action?

Why: Combining Error Signals

Reset MCU upon Error / Activate Buzzer upon Error

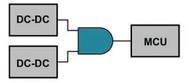


Recommendations:
SN74LVC1G32
SN74AUP1G32

(Logic Gates)
Power Good

Does your system have multiple power rails each with a power good signal?

Why: Combining Power Good



Power Good Options		
Gate to Use	Power Good	Enable Signal
NOR	Active Low	Active High
NAND	Active High	Active Low
AND	Active High	Active High
OR	Active Low	Active Low

Recommendation:
SN74LVC1G08
SN74AUP1G00

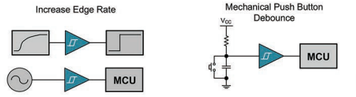
Signal Timing / Noise

(Schmitt Trigger, Logic Gates)

Does your system contain slow or noisy signals?

Why: Correcting Slow/Noisy Signals

Increase Edge Rate / Mechanical Push Button Debounce

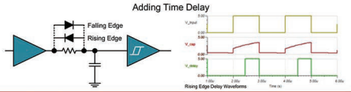


Recommendations:
SN74AUP1G17
SN74LVC2G17

Does your system require a time delay on a control signal?

Why: Adding Time Delay

Adding Time Delay

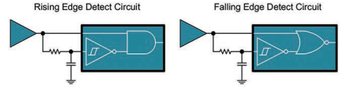


Recommendations:
SN74AUP1G17
SN74LVC2G17

Does your system need to generate a pulse on a rising or falling edge of a signal?

Why: Detecting an Edge

Rising Edge Detect Circuit / Falling Edge Detect Circuit



Recommendations:
SN74LVC1G57
SN74LVC1G58
SN74LVC1G123

How do I narrow down my Logic and Translation selection quickly?

Logic Families

Key Careabouts	Logic Family	Number of Devices	Auto Qual. Devices
CD4 — High Voltage Logic 3-18V	CD4k	111	4
SN74* — 5V TTL TTL-Compatible Inputs 5V	HCT[1]	195	18
Standard Voltage General-Purpose Logic 2-6V	HC[1]	300	48
Standard Voltage Medium Drive (12mA/ch) 2-6V	LV-A	69	16
Low Voltage Up-Translation Capable 1.6-5.5V	LV1T	9	
Low Voltage High Drive (24 mA/ch) 1.65-3.6V	LVC	218	52
Very Low Voltage Ultra-Low Power (0.9 µA) 0.8-3.6V	AUP	63	3
Very Low Voltage High Data Rates (500 Mbps) 0.8-2.7V	AUC	63	

[1] Advanced Version available (i.e. AHCT, AHC) – Improved Drive Strength and Speed

Translation Families

Interface	Recommended Device
1 Bit GPIO	2N7001T or SN74AXC1T45
Clock Signal	SN74AXC1T45
2 Bit GPIO	2N7001T or LSF0102
Reduced Pin Count JTAG	SN74AVC2T45
I2C	TXS0102 or LSF0102
MDIO	TXS0102 or LSF0102
SMBus/PMBus	TXS0102 or LSF0102
IC-USB	SN74AVC2T872 or TXS0202
4 Bit GPIO	SN74AXC4T245 or LSF0204
UART	SN74AXC4T245
SPI	SN74AVC4T774
JTAG	SN74AVC4T774
I2S	SN74AVC4T774
Quad-SPI	TXB0106
SDIO/SD/MMC	TXS0206 or TXS0206-29
8 Bit RMII/RGMII	SN74AXCH8T245
8+ Bit RMII/RGMII	SN74AVCH16T245

Increasing Bit Count: 1, 2, 4, 6, 8+

*All AVC and AXC family part recommendations are for <3.6 V, for up to 5.5V consider LVC Family

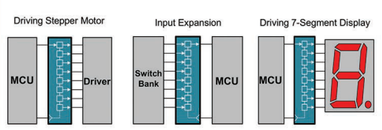
I/O Expansion & Clocking

(Shift Register)

Does your system need more inputs / outputs than the controller has available?

Why: Expanding Number of Inputs or Outputs

Driving Stepper Motor / Input Expansion / Driving 7-Segment Display



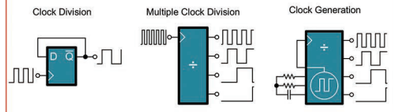
Recommendations:
SN74HC595B
SN74LV164A

(Flip-Flop, Counter)

Does your system need to do clock division?

Why: Dividing a clock signal

Clock Division / Multiple Clock Division / Clock Generation



Recommendations:
SN74AUP1G74 or
SN74LVC2G74 or
SN74HC4060

Visit ti.com/logic-circuit

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265