TPS7A78 120mA スマート AC/DC リニア電圧レギュレータ

1 特長

- 18$V_{AC\ RMS}$ 以上の非絶縁型電源ソリューション
  - 最高 75% の効率
  - スタンバイ時消費電力:15mW (標準値)
  - リニア・ソリューションの 1/4 のサイズのライン電圧降下コンデンサ
- 固定出力電圧で提供
  - 1.3V ～ 5V (50mV 刻み)
- 電源障害検出
- パワー・グッド表示
- 精度：1% (標準値)
- パッケージ
  - 5mm × 6.5mm の HTSSOP-14 (PWP)

2 アプリケーション

- キー・パネル
- ガレージのドア・システム
- 小型家電製品
- 電気メータ
- 煙感知器と熱感知器
- サーモスタット

3 概要

TPS7A78 は、使いやすい非磁気的 AC/DC 変換方式により、電源の総合効率とスタンバイ時電力を改善します。TPS7A78 は、コンデンサ電圧降下アーキテクチャを使用して AC 電源電圧を降圧してから、整流された電圧をアクティブにクランプします。次に、この整流された電圧をアプリケーション固有の動作電圧まで下げてレギュレートします。本デバイスの独自のアーキテクチャを使用すると、スタンバイ時の電力をわずか数十ミリワットに低減できます。TPS7A78 のスイッチト・キャパシタ段は、整流された入力電圧を 4 分の 1 に降圧し出力電流を入力電流の 4 倍に増やすことで、電力損失を減らします。これは、$P_{IN} \cong P_{OUT}$ および $V_{IN} \cong V_{OUT} \times 4$で与えられます。従来型のコンデンサ電圧降下 (キャップドロップ) 段と比較して、この降圧方式では入力電流が減少するため、必要なコンデンサの値を最小化できます。

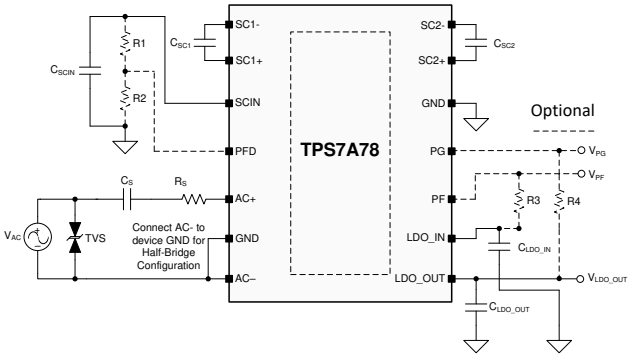
TPS7A78 は外付け磁気部品を必要としないため、磁気に対する耐タンパー性を備えた電源を必要とする電力メータ用途に適しています。この特長により、磁気シールドのコストを最小化しながら IEC 61000-4-8 に簡単に準拠できます。

製品情報(1)

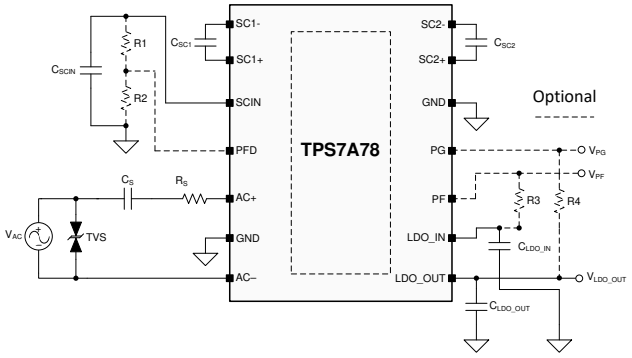
型番	パッケージ	本体サイズ(公称)
TPS7A78	HTSSOP (14)	5.00mm × 6.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ハーフブリッジ構成の標準的な回路図



フルブリッジ構成の標準的な回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2019年3月発行のものから更新 **Page**

- デバイスのステータスを APL から量産データに 変更 ... 1

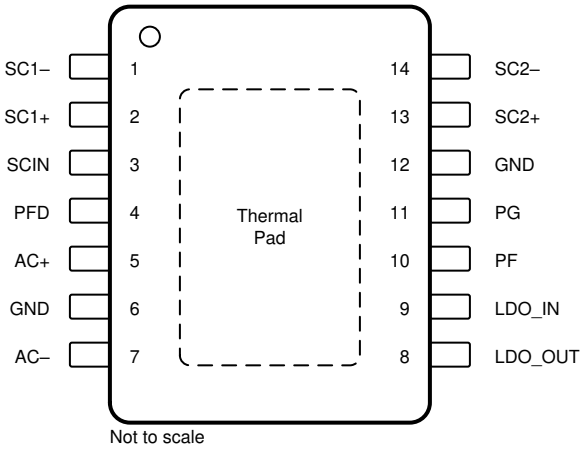
5 概要（続き）

また、TPS7A78 は、電源障害に対して早期アラートを発行し電源が完全に失われる前にシャットダウンできるユーザ・プログラマブルな電源障害検出スレッショルドも備えています。マイクロコントローラのシーケンシングまたはリセット用にパワー・グッド・インジケータ (PG) も備えています。

TPS7A78 は、14 ピンの HTSSOP (PWP) パッケージで供給されます。

6 Pin Configuration and Functions

PWP Package
14-Pin HTSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SC1–	—	Negative terminal of the switched-capacitor, voltage-reduction stage pin. Connect a minimum 1-µF, X5R (or better) dielectric, 16-V-rated capacitor between this pin and the SC1+ pin. Place the capacitor as close to the device as possible; see the *Recommended Operating Conditions* table for details.
2	SC1+	—	Positive terminal of the switched-capacitor, voltage-reduction stage pin. Connect a minimum 1-µF, X5R (or better) dielectric, 16-V-rated capacitor between this pin and the SC1– pin. Place the capacitor as close to the device as possible; see the *Recommended Operating Conditions* table for details.
3	SCIN	—	Rectified DC-voltage pin. Place the capacitor as close to the device as possible; see the *Device Functional Modes* section for the dual-input power-supply capability and the *Calculating the Bulk Capacitor* section for the proper capacitor calculation.
4	PFD	Input	Power-failure detect pin. An analog voltage input compares the reference voltage to a resistor-divided V_{SCIN} voltage to detect a V_{AC} power-failure; see the *Recommended Operating Conditions* table and the *Calculating the PFD Pin Resistor Dividers for Power-Fail Detection* section for details.
5	AC+	Power	AC-supply line or neutral input to the device after the capacitive-drop (cap-drop) capacitor and surge resistor. Either this pin or the AC– pin must have the cap-drop capacitor and surge resistor in series with the line. See the *Full-Bridge (FB) and Half-Bridge (HB) Configurations* section for details.
6	GND	Ground	Ground pin. All device ground pins must be referenced to the same ground. Connect this pin to the thermal pad at the bottom of the device; see the *Layout* section for details.
7	AC–	Power	AC-supply line or neutral input to the device pin after the cap-drop capacitor and surge resistor. Either this pin or the AC+ pin must have the cap-drop capacitor and surge resistor in series with the line. See the *Full-Bridge (FB) and Half-Bridge (HB) Configurations* section for details.
8	LDO_OUT	Output	Regulated DC output pin. Connect a minimum 0.68-µF, X5R (or better) dielectric capacitor between this pin and the device GND pins. Place the capacitor as close to the device as possible; see the *Recommended Operating Conditions* table for the maximum capacitor value.
9	LDO_IN	—	Charge-pump output pin. Connect a minimum 0.68-µF, X5R (or better) dielectric capacitor between this pin and the device GND pins. This pin is internally driven and must not be driven externally. For optimal performance, connect a capacitor that is 10x the value of C_{LDO_OUT} placed as close to the device as possible. See the *Recommended Operating Conditions* table for the maximum capacitor value.
10	PF	Output	Power-fail indicator pin. An open-drain indicator signal indicates if the V_{AC} supply has failed. Pullup this pin through an external resistor to V_{LDO_IN} or to a DC-rail that shares the same GND as the device. The PF pin goes low when V_{PFD} is less than the $V_{IT(PFD,FALLING)}$ threshold, as specified in the *Electrical Characteristics* table. See the *Recommended Operating Conditions* table for proper selection of the pullup resistor.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
11	PG	Output	Power-good indication pin. An open-drain indicator signal indicates if the V_{LDO_OUT} surpassed the $V_{IT(PG,RISING)}$ threshold, as specified in the *Electrical Characteristics* table. Pullup this pin through an external resistor to V_{LDO_OUT} or to a DC rail that shares the same GND as the device. See the *Recommended Operating Conditions* table for proper selection of the pullup resistor.
12	GND	Ground	Ground pin. All device ground pins must be referenced to the same ground. Connect this pin to the thermal pad at the bottom of the device; see the *Layout* section for details.
13	SC2+	—	Positive terminal of the switched-capacitor, voltage-reduction stage pin. Connect a minimum 1-µF, X5R (or a better) dielectric, 10-V-rated capacitor between this pin and the SC2– pin. Place the capacitor as close to the device as possible; see the *Recommended Operating Conditions* table for details.
14	SC2–	—	Negative terminal of the switched-capacitor, voltage-reduction stage pin. Connect a minimum 1-µF, X5R (or a better) dielectric, 10-V-rated capacitor between this pin and the SC2+ pin. Place the capacitor as close to the device as possible; see the *Recommended Operating Conditions* table for details.
Thermal pad		—	Exposed pad of the package. Connect this pad to device ground pins. Connect the thermal pad to a large-area ground plane for best thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Voltage	AC+, AC– (V_{AC} supply mode only)	–1.5	30	V
	SCIN (V_{AC} supply mode only, internally driven)	–1.5	30	
	SCIN (DC supply mode only, voltage directly applied on SCIN pin)	– 0.3	24	
	LDO_OUT	– 0.3	5.5	
	PF, PG	– 0.3	6	
	PFD	–0.3	3	
Current	LDO_OUT pin reverse current(3)		6	mA
	Maximum output	Internally limited		
	I_{PF}, I_{PG}		5	
Temperature	Storage, T_{STG}	– 65	150	℃

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the device GND pins (not Earth GND); see the *Full Bridge (FB) and Half Bridge (HB) Configurations* section for details.
(3) Exceeding the maximum reverse current into the LDO_OUT pin can cause damage to the device; see the *Reverse Current* section for details.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{AC}(2)	Connected via C_S(3) and R_S(3)(4) on either AC+ or AC–	18(5)			V_{RMS}
f_{AC}	Line frequency		50	20,000	Hz
I_{SURGE}	Peak transient current into or out of either the AC+ or AC– pins (during hot plug for ≤ 100 µs)			2.5	A
I_{SHUNT}	AC current during shunt event on either AC+ or AC- pins			200	mA_{RMS}
V_{SCIN}	DC supply mode, voltage applied to the SCIN pin for devices with V_{LDO_OUT} ≤ 3.4 V	17(6)		23	V
C_{SCIN}	Bulk capacitor for V_{AC} supply mode	22			µF
C_{SCIN}	Bulk capacitor for DC-supply mode	1.0			µF
C_{SC1}	Switched-capacitor stage 1	1		4.7(7)	µF
C_{SC2}	Switched-capacitor stage 2	1		4.7(7)	µF
C_{LDO_IN}	LDO_IN capacitor	0.68	10	1000	µF
C_{LDO_OUT}	LDO_OUT capacitor	0.68	1	100	µF
R_1	PFD top resistor divider	0		200	kΩ
R_3 & R_4	Power-good and power-fail pullup resistors	10		100	kΩ
I_{OUT}	Output current	0		120	mA
T_J	Operating junction temperature	–40		125	℃

(1) All voltages are with respect to the device GND pins (not Earth GND); see the *Full Bridge (FB) and Half Bridge (HB) Configurations* section for details.
(2) Theoretically there is no upper limit to the V_{AC} supply voltage because this voltage is dropped across the C_S capacitor; see the *Calculating the Cap-Drop Capacitor* section for details.
(3) The voltage ratings for the cap-drop capacitor C_S and the surge resistor R_S must be able to handle the peak V_{AC} supply voltage; see the *Typical Application* section for details.
(4) The surge resistor R_S is required to limit the inrush current into or out off either AC+ or AC– pins during hot-plug or surge current events; see the *Calculating the Surge Resistor* section for details.
(5) Only available for devices with ≤ 3.3-V output voltage options.
(6) DC-supply mode is also availabe for 3.6-V devices but with a minmum required V_{SCIN} supply voltage of 18 V.
(7) A 16 V or higher voltage rating is recommended for the C_{SC1} capacitor, and a 10 V or higher voltage rating is recommeded for the C_{SC2} capacitor.

7.4 Thermal Information

THERMAL METRIC(1)(2)		TPS7A78 PWP (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Thermal metrics were modeled on a JEDEC Hi-K board in order to provide a standardized layout and measurement technique for comparison purposes.The *An empirical analysis of the impact of board layout on LDO thermal performance* application report goes into detail on how board layout impacts the thermal performance of linear regulators.

7.5 Electrical Characteristics

V_{SCIN} [1] = 4 ($V_{LDO\_OUT\ (nom)}$ + 0.6 V) + 1 V or 17 V (whichever is greater), C_{SCIN} = 10 µF, C_{S1} = 1.0 µF, C_{S2} = 2.2 µF , C_{LDO_IN} = 10 µF, C_{LDO_OUT} = 1.0 µF, and I_{OUT} = 1 mA (unless otherwise noted);typical values are at T_J = 25°C [2]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO_SCIN}	UVLO_SCIN threshold rising	V_{SCIN} rising, $V_{LDO\_OUT(nom)}$ ≤ 3.4 V	17			V
$V_{UVLO\_LDO\_IN}$	UVLO_LDO_IN threshold rising	V_{SCIN} rising	3.9			V
	UVLO_LDO_IN threshold falling	V_{SCIN} falling			3.5	V
$\Delta V_{LDO\_OUT(\Delta IOUT)}$	Load regulation	0 mA ≤ I_{OUT} ≤ 120 mA			0.21	mV/mA
V_{LDO_OUT}	Output voltage accuracy	V_{SCIN} [1][3] = 4 ($V_{LDO\_OUT\ (nom)}$ + 0.6 V) + 3 V, 0 mA ≤ I_{OUT} ≤ 120 mA	–2	1	2	%
I_{CL}	Output current limit	V_{LDO_OUT} = 0.9 x $V_{LDO\_OUT(nom)}$	145	215	300	mA
I_{DD_SCIN}	SCIN pin quiescent current	$V_{LDO\_OUT(nom)}$ = 3.3 V, I_{OUT} = 0 mA, no R_3, R_4		280		µA
V_{Ripple}	Output voltage ripple	V_{AC} = 120 V, 60 Hz, FB, C_S = 1.0 µF, C_{SCIN} = 180 µF, $V_{LDO\_OUT(nom)}$ = 5 V, I_{OUT} = 10 mA, scope BW = 10 MHz		3		mV
$V_{IT(PFD,RISING)}$	PFD pin rising threshold	V_{PFD} rising, R_4 = 100 kΩ	1.24		1.42	V
$V_{IT(PFD,FALLING)}$	PFD pin falling threshold	V_{PFD} falling, R_4 = 100 kΩ	1.17		1.25	
$V_{HYS(PFD)}$	PFD pin hysteresis			110		mV
$V_{IT(PG,RISING)}$	PG pin rising threshold	R_3 = 100 kΩ, V_{SCIN} rising	90.16	92	93.84	%V_{LDO_OUT}
$V_{IT(PG,FALLING)}$	PG pin falling threshold	R_3 = 100 kΩ	88.5	90	91.5	
$V_{HYS(PG)}$	PG pin hysteresis			2		
$V_{OL(PF),(PG)}$	PF and PG pins low-level ouput voltage	$I_{PF,PG}$ = 500 µA			0.2	V
$I_{LKG(PF),(PG)}$	PF and PG pins open-drain leakage current	$V_{PF,PG}$ = 5 V			50	nA
$T_{SD(Shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		162		℃
$T_{SD(Reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		135		

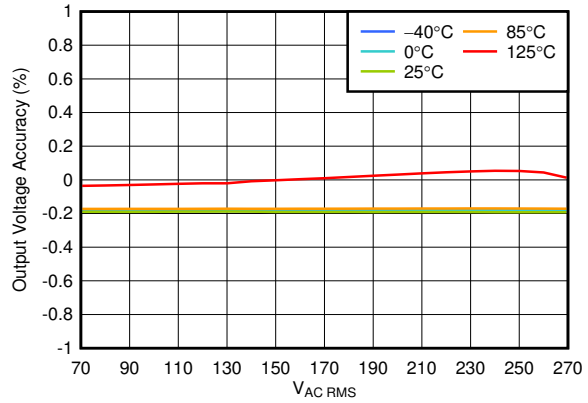
(1) For V_{LDO_OUT} > 4.4 V, V_{SCIN} is limited to 24 V for testing purposes only.
(2) Electrcial characteristic data tested in DC supply mode equivalent to V_{SCIN} voltage under AC supply mode.
(3) V_{SCIN} ≥ 19 V.

7.6 Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{PF(HL)}$	PF pin going from high to low		1		µs
$t_{PG(LH)}$	PG pin going from low to high		1		µs
f_{SC}	Switched capacitor stage operating frequency		200		kHz

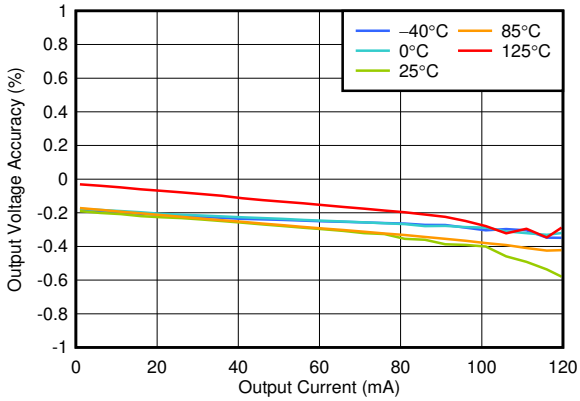
7.7 Typical Characteristics

at operating temperature T_J = 25°C, V_{AC} supply = 120 V_{RMS} per 60 Hz, full-bridge (FB) bridge configuration, C_S = 1.0 µF, C_{SCIN} = 220 µF, C_{SC1} = 1.0 µF, C_{SC2} = 2.2 µF, C_{LDO_IN} = 10 µF, C_{LDO_OUT} = 1.0 µF, and I_{OUT} = 1 mA (unless otherwise noted)



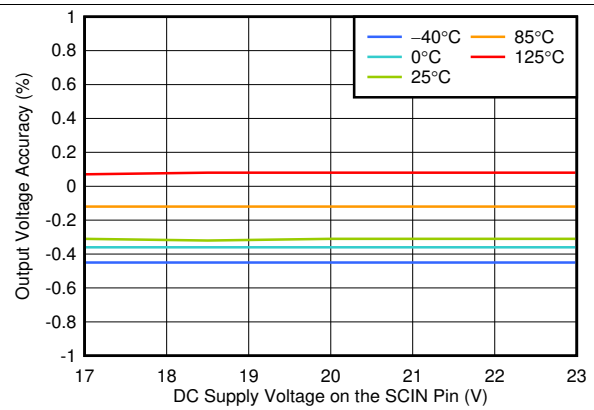
V_{AC} = 70 V_{RMS} to 270 V_{RMS}, V_{LDO_OUT} = 5.0 V

図 1. V_{LDO_OUT} Accuracy vs V_{AC} Supply



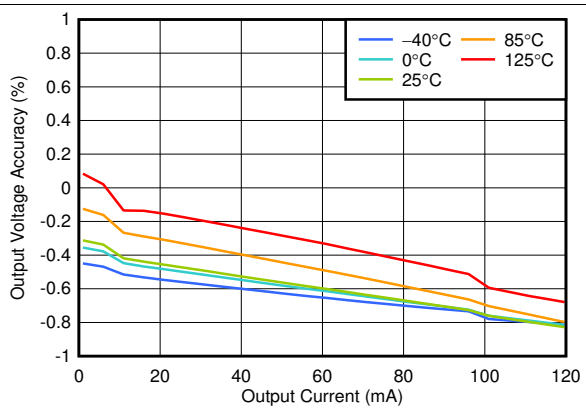
V_{LDO_OUT} = 5.0 V, I_{OUT} = 0 mA to 120 mA

図 2. V_{LDO_OUT} Accuracy vs I_{OUT}



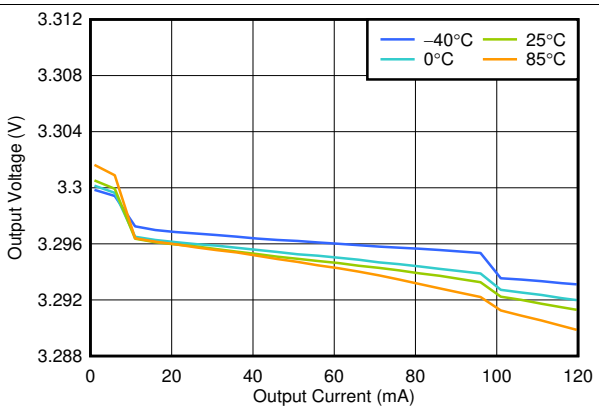
V_{SCIN} = 17 V, V_{LDO_OUT} ≤ 3.4 V

図 3. V_{LDO_OUT} Accuracy vs DC Supply on the SCIN Pin



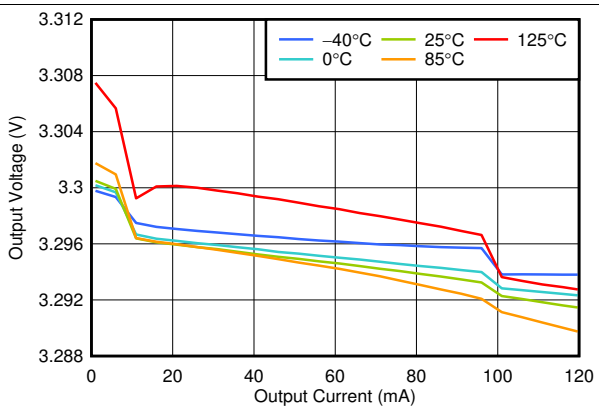
V_{SCIN} = 19 V, V_{LDO_OUT} ≤ 3.4 V

図 4. V_{LDO_OUT} Accuracy vs I_{OUT} DC Supply on the SCIN Pin



V_{SCIN} = 17 V, V_{LDO_OUT} = 3.3 V

図 5. V_{LDO_OUT} vs I_{OUT} DC Supply on the SCIN Pin



V_{SCIN} = 19 V, V_{LDO_OUT} = 3.3 V

図 6. V_{LDO_OUT} vs I_{OUT} DC Supply on the SCIN Pin

Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{AC} supply = 120 V_{RMS} per 60 Hz, full-bridge (FB) bridge configuration, C_S = 1.0 µF, C_{SCIN} = 220 µF, C_{SC1} = 1.0 µF, C_{SC2} = 2.2 µF, C_{LDO_IN} = 10 µF, C_{LDO_OUT} = 1.0 µF, and I_{OUT} = 1 mA (unless otherwise noted)

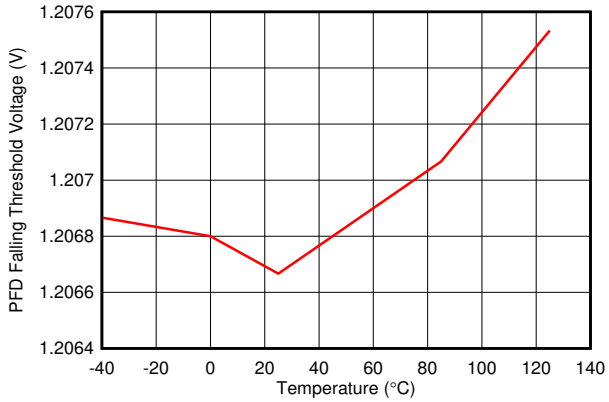


図 7. $V_{IT(PFD,FALLING)}$ Threshold vs Temperature

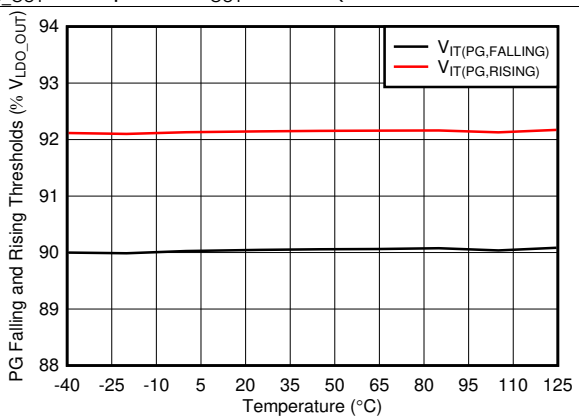
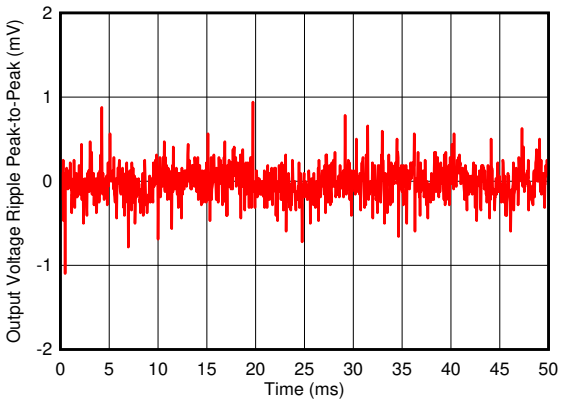
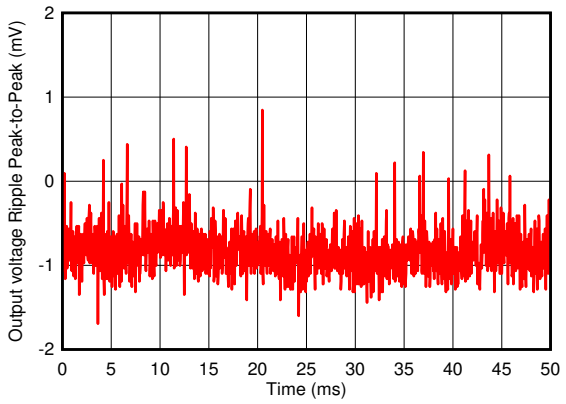


図 8. $V_{IT(PG,FALLING)}$ and $V_{IT(PG,RISING)}$ Thresholds vs Temperature



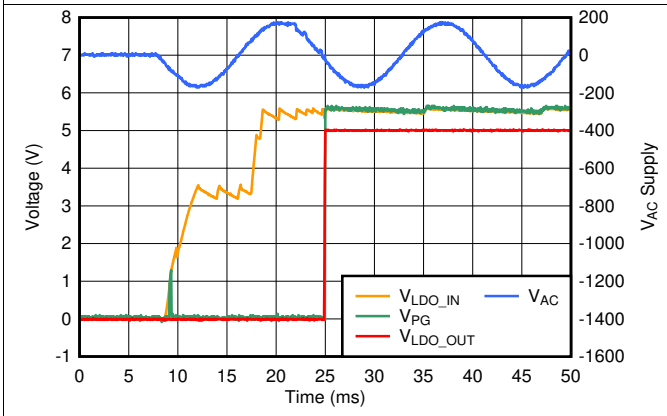
FB configuration, scope bandwidth = 10 MHz,
I_{OUT} = 1 mA

図 9. V_{LDO_OUT} Ripple for FB Configuration



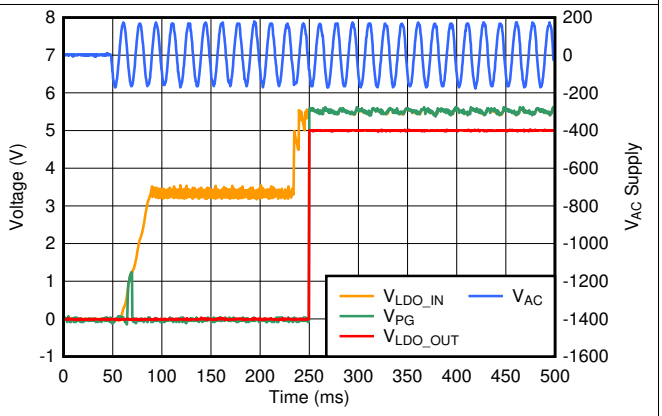
FB configuration, scope bandwidth = 10 MHz,
I_{OUT} = 120 mA

図 10. V_{LDO_OUT} Ripple for FB Configuration



C_S = 2.2 µF, C_{SCIN} = 22 µF, C_{LDO_IN} = 1.0 µF, I_{OUT} = 10 mA

図 11. Fast Startup With Larger Than the Required Cap-Drop Capacitor for 10-mA I_{OUT}

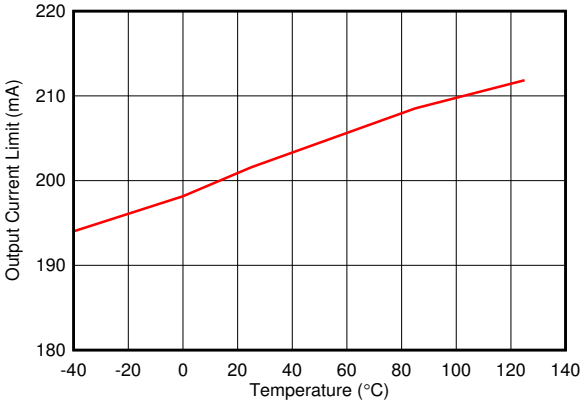


C_S = 100 nF, C_{SCIN} = 22 µF, C_{LDO_IN} = 1.0 µF, I_{OUT} = 10 mA

図 12. Slow Startup With the Minimum Required Cap-Drop Capacitor for 10-mA I_{OUT}

Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{AC} supply = 120 V_{RMS} per 60 Hz, full-bridge (FB) bridge configuration, C_S = 1.0 µF, C_{SCIN} = 220 µF, C_{SC1} = 1.0 µF, C_{SC2} = 2.2 µF, C_{LDO_IN} = 10 µF, C_{LDO_OUT} = 1.0 µF, and I_{OUT} = 1 mA (unless otherwise noted)



V_{SCIN} = 19 V, V_{LDO_OUT} ≤ 3.4 V

図 13. I_{OUT} Current Limit

8 Detailed Description

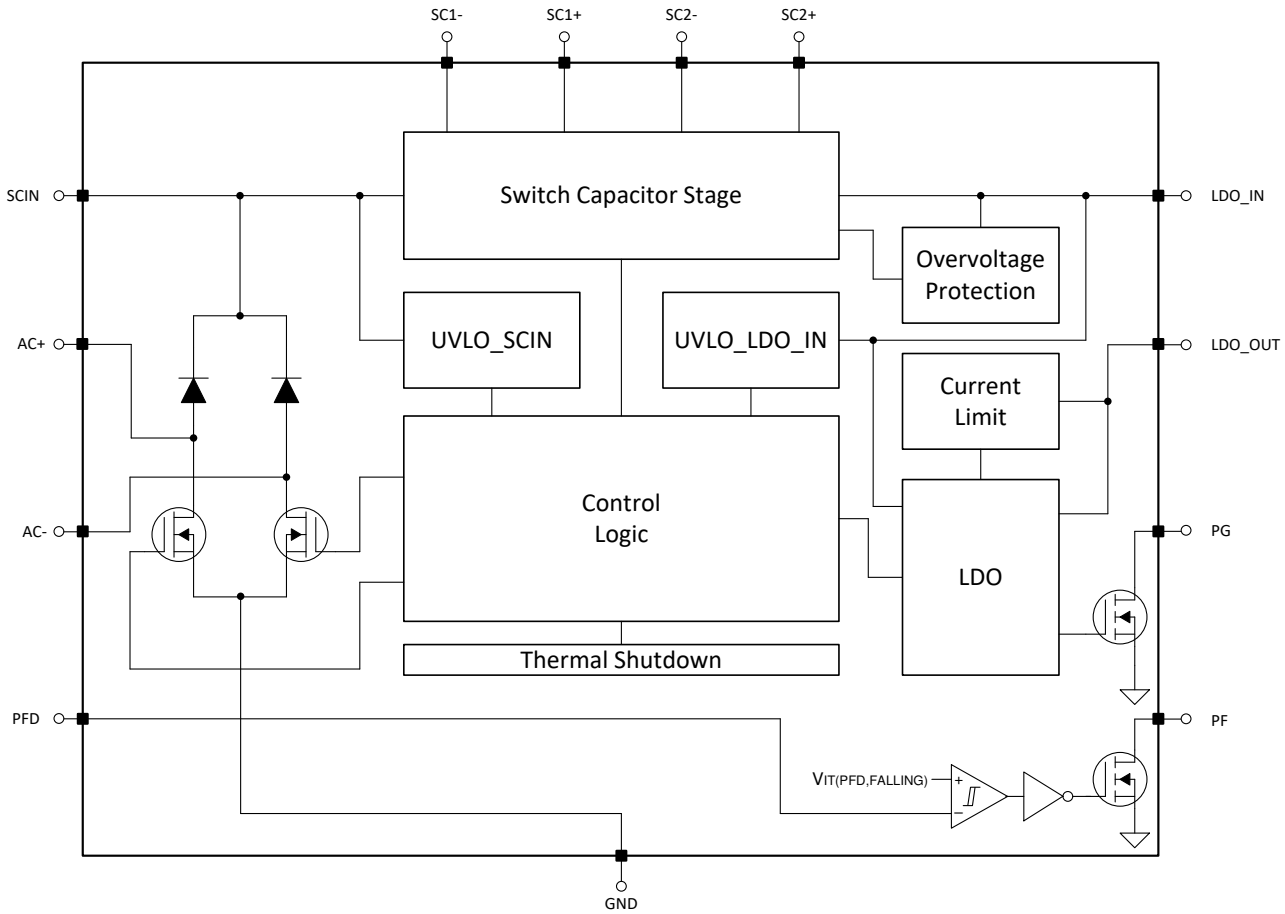
8.1 Overview

The TPS7A78 features an internally controlled, active bridge rectifier that can be configured either as full bridge (FB) or a half bridge (HB), a 4:1 switched-capacitor stage (charge pump), an internally controlled low-dropout (LDO) linear-voltage regulator, as well as current-limit, thermal-shutdown, programmable power-fail detection, and power-good detection.

The TPS7A78 is a non-isolated, smart linear-voltage regulator that uses an external high-voltage, capacitor-drop (cap-drop) capacitor (C_S) and an internally controlled, active bridge-rectifier to create a regulated DC output voltage. The device incorporates a switched-capacitor charge pump stage that transforms the voltage and current characteristics of the rectifier stage to the voltage and current needs of the LDO stage, providing a 4-times reduction in input power for a given load power. This feature also reduces the size of the required C_S by a factor of 4. The external surge resistor R_S is used to limit the inrush-current to the device. Unlike typical AC-to-DC power solutions, the TPS7A78 does not require external magnetic components, thus making the device an excellent choice for electricity-metering applications by improving tamper resistance. This unique design allows the TPS7A78 to reduce standby power to approximately 15 mW for light-load applications while maintaining high efficiency.

For applications with output voltages of 3.6 V or less, the TPS7A78 can be powered from a DC supply connected directly to the SCIN pin. This supply mode can provide DC-only operation or DC-powered backup in case of AC supply failure. When a DC supply is used to power the device, the internally controlled dropout voltage regulation is affected as explained in the *Dropout Voltage Regulation* section. The AC+ and AC– pins must be grounded when only a DC power source is used.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Active Bridge Control

The TPS7A78 has an internally controlled, actively clamped, full-bridge rectifier between the AC+ and AC– pins that requires one of these pins to be connected in series with the high-voltage capacitor C_S and the surge resistor R_S. The active clamp for the bridge is designed to stabilize the rectified DC voltage at the SCIN pin to optimize performance given the LDO output voltage. The clamp circulates any excess AC charging current from the cap-drop capacitor C_S and surge resistor R_S through the AC+ or the AC– pins to the GND pins when the SCIN pin voltage surpasses its UVLO_SCIN rising threshold during startup. The clamp maintains the SCIN pin voltage higher than this threshold to support the targeted output voltage. This excess AC charging current is also referred to as the shunt current, I_{SHUNT}; see the *Standby Power and Output Efficiency* section for details on the shunt current.

A DC supply can also be used to provide power directly to the SCIN pin, which completely bypasses the bridge active-clamp circuit; see 表 1 for details on the DC supply mode.

8.3.2 Full-Bridge (FB) and Half-Bridge (HB) Configurations

The TPS7A78 can be configured to operate either in full-bridge (FB) or half-bridge (HB) configurations. HB configuration ties the AC input pin without the series C_S and R_S components to the device GND pins. See *図 14* and 図 15 for the HB and FB configurations.

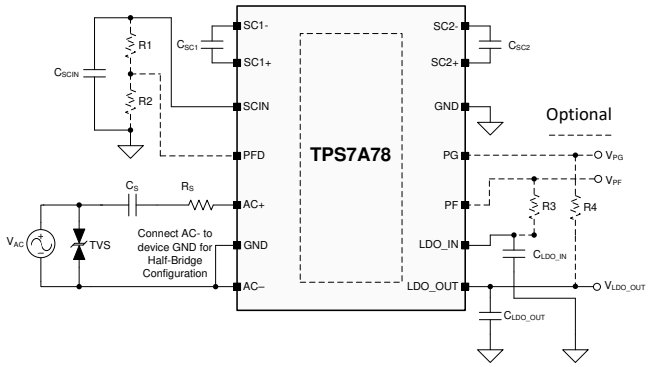


図 14. Typical Schematic Half-Bridge Configuration

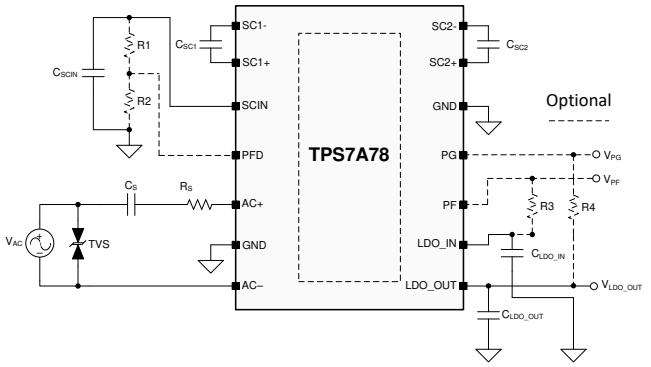


図 15. Typical Schematic Full-Bridge Configuration

注

When FB configuration is used, do not tie the device GNDs to earth GND neither schematically nor accidentally via an earth-grounded oscilloscope or measurement equipment because the device GNDs and earth GND are at different voltage potentials. Doing so and can cause damage to the device and external equipment. Tying the device GND pins to earth GND when FB configuration is used is only acceptable if a second surge resistor R_S is used on the AC input pin side without the series C_S and first R_S, as illustrated in 図 16 with floating device GND pins and 図 17 with non-floating (earth grounded) device GND pins.

Feature Description (continued)

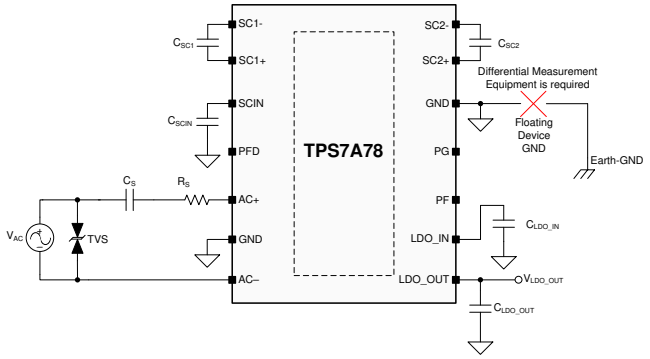


図 16. Full-Bridge Floating Device GND

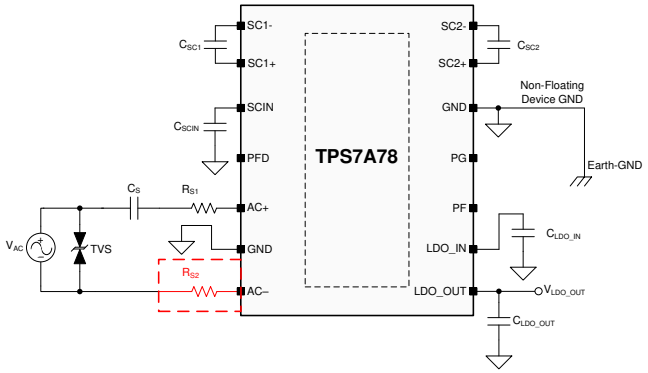


図 17. Full-Bridge Non-Floating Device GND

8.3.3 4:1 Switched-Capacitor Voltage Reduction

The TPS7A78 uses a switched-capacitor charge pump to reduce the rectified DC voltage at the SCIN pin by four times, providing the LDO block with an input voltage above its dropout voltage that is then regulated to the target output voltage. The DC voltage at the SCIN pin can be provided either by the active clamp for the bridge rectifying the input V_{AC} supply or by a direct DC supply connection to the SCIN pin.

8.3.4 Undervoltage Lockout Circuits (V_{UVLO_SCIN}) and ($V_{UVLO\_LDO\_IN}$)

The TPS7A78 incorporates two undervoltage lockout (UVLO) circuits; the UVLO_SCIN circuit and the UVLO_LDO_IN circuit. UVLO_SCIN is used to make sure that the active clamp for the bridge has charged the C_{SCIN} capacitor to a voltage level that surpasses the UVLO_SCIN rising threshold to start the switched-capacitor stage. The UVLO_SCIN rising threshold voltage is a function of the LDO output voltage, $V_{LDO\_OUT(nom)}$, as indicated in the *Electrical Characteristics* table.

The UVLO_LDO_IN circuit is used to ensure that the switched-capacitor stage has charged the C_{LDO_IN} capacitor to a voltage level that surpasses the UVLO_LDO_IN rising threshold to enable the LDO circuit to begin regulation at the specified LDO output voltage. See the *Startup Behavior* section for details.

注

The LDO_IN pin must not be driven externally and must not be used as a supply rail to an external load.

8.3.5 Dropout Voltage Regulation

This LDO functional block follows the conventional definition of dropout voltage (V_{DO}) between V_{LDO_IN} and V_{LDO_OUT}. However, the supply mode can have an effect on the dropout voltage.

When the AC input is used as the supply, a fixed dropout (V_{DO}) of 600 mV (typical) between V_{LDO_IN} and V_{LDO_OUT} is maintained for output voltages between 5.0 V and 3.4 V. For output voltages below 3.4 V, the V_{LDO_IN} voltage is maintained at 4.0 V regardless of the output voltage.

A DC supply via the SCIN pin can only be used for output voltages of 3.6 V or less. Under a load condition approaching maximum output current and at high ambient temperature, the LDO can be driven into dropout; see the *Switched-Capacitor Stage Output Impedance* section for details.

8.3.6 Current Limit

The LDO block has an internal current-limit circuit that protects the output during overcurrent events or short-circuit faults. The current-limit circuit limits the output current to (I_{CL}), as specified in the *Electrical Characteristics* table.

Feature Description (continued)

When in current limit, the output voltage cannot be regulated and the device heats up because of the increase in power dissipation. When in current limit, the LDO pass transistor dissipates power equal to $V_{DO} \times I_{CL}$, where V_{DO} is equal in the worst case to V_{LDO_IN}. The heat generated when operating at current limit, in conjunction with the ambient temperature, can trigger the internal thermal shutdown. During thermal shutdown, both V_{LDO_OUT} and the switched-capacitor stage are shut down to prevent further heating; see the *Load Transient* section for more details.

8.3.7 Programmable Power-Fail Detection

The TPS7A78 can monitor the rectified DC voltage at the SCIN pin to provide the application with an early warning via the power-fail (PF) pin if the main power fails. An external resistor-divider network connected to the VSCIN pin provides the input to the power-fail detect (PFD) analog input pin to monitor for an AC line supply failure. When the AC supply falls below its minimum level programmed by the resistor divider R_1 and R_2, as illustrated in 図 14 and in 図 15, the PF output is pulled low. If this feature is not used, omit R_1 and R_2 and connect PFD and PF pins to the device GND pins reference.

注

The PFD pin can also be used to monitor another DC rail within the application to provide an early warning via the PF pin. However, this DC rail must share the same GND reference with the TPS7A78 GND and the absolute maximum voltage of the PF pin must not be exceeded.

8.3.8 Power-Good (PG) Detection

The power-good (PG) circuit monitors the V_{LDO_OUT} voltage to indicate the status of the LDO output voltage. PG is pulled low until V_{LDO_OUT} reaches its proper regulate voltage level, then PG is released and allowed to be pulled high. If V_{LDO_OUT} falls below the $V_{IT(PG\_FALLING)}$ threshold, PG is asserted low to indicate the LDO output voltage is not in regulation. PG pin low assertion can happen during an overcurrent event or a short-circuit fault.

PG can be used to release the reset pin of a microcontroller. The PG pin must be pulled up to a DC rail such as V_{LDO_OUT}.

Use the recommended pullup resistor value specified in the *Electrical Characteristics* table for the PG pin. The functionality of the power-good detection pin has no effect on the internal control logic other than to indicate the state of the output voltage. If this function is not used, connect the PG pin to the device GND pins reference.

注

An external DC rail can also be used to pull up the PG pin signal via a pullup resistor only when the external DC rail shares the same reference GND with the TPS7A78 GND and the absolute maximum voltage of the PG pin is not exceeded.

8.3.9 Thermal Shutdown

A thermal shutdown protection circuit is included to disable V_{LDO_OUT} and to stop the switched-capacitor stage from switching when the junction temperature T_J of the pass-transistor rises to $T_{SD(SHUTDOWN)}$. Thermal shutdown hysteresis assures that the device resets, resumes normal operation, and that V_{LDO_OUT} turns back on when T_J falls to $T_{SD(RESET)}$. Based on the thermal time constant of the die and the device startup time, the device output can cycle on and off until power dissipation is reduced and the junction temperature remains below $T_{SD(RESET)}$.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operating above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

8.4 Device Functional Modes

The unique features of the TPS7A78, along with its dual-input power-supply capability, enables the device to be used in a vast array applications. 表 1 gives a general overview of the conditions that lead to different modes of operation, given that the requirements in the *Typical Application* section are met.

表 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	DEVICE POWER-SUPPLY	I_{OUT}	T_J
Normal operation	V_{AC} supply(1) / DC supply(2)	$I_{OUT} < I_{CL}$ used in the *Calculating the Cap-Drop Capacitor C_S* section	$T_J < T_{SD\ (Shutdown)}$
Dropout mode(3)	C_S or C_{SCIN} capacitors are not sufficient to support I_{OUT} (V_{AC} supply)	$I_{OUT} < I_{CL}$ used in the *Calculating the Cap-Drop Capacitor C_S* section	$T_J < T_{SD\ (Shutdown)}$
	$V_{SCIN} \le V_{UVLO\ SCIN}$ rising threshold and $V_{LDO\_IN} > V_{UVLO\ LDO\_IN}$ rising threshold (DC supply)(4)	$I_{OUT} < I_{CL}$ used in the *Calculating the Cap-Drop Capacitor C_S* section	$T_J < T_{SD\ (Shutdown)}$
Disabled mode(5)	$V_{LDO\_IN} < V_{UVLO\ LDO\_IN}$ falling threshold (V_{AC} supply)	Not applicable	$T_J > T_{SD\ (Shutdown)}$
	$V_{LDO\_IN} < V_{UVLO\ LDO\_IN}$ falling threshold (DC supply)		

(1) The device can function with the V_{AC} supply down to 18 V_{RMS}; see the *Typical Application* section for details.
(2) The DC supply applied on the SCIN pin must be bounded by the $V_{SCIN\ (MAX)} > V_{SCIN} > V_{UVLO\_SCIN}$ (RISING) threshold as specified in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.
(3) The device can be in dropout when powered by V_{AC} or DC supplies; see the *Dropout Voltage Regulation* section for details.
(4) This condition applies after device has started up.
(5) Any true condition disables the device V_{LDO_OUT} and stops the switched-capacitor stage from switching; see the *Disabled Mode* section for details.

8.4.1 Normal Operation

The device is mainly designed to be powered by the AC supply; however, a DC supply can also be used to power the TPS7A78. See the *Active Bridge Control* and *Application and Implementation* sections for proper operation.

8.4.2 Dropout Mode

During dropout mode and when V_{LDO_OUT} tracks V_{LDO_IN}, the transient performance becomes significantly degraded because the pass-transistor is operating in the ohmic or triode region.

8.4.3 Disabled Mode

There is no disable pin and disable mode simply means that the output, V_{LDO_OUT}, is turned off and the switched capacitor (see the *4:1 Switched-Capacitor Voltage Reduction* section) is not switching. However, when V_{SCIN} is less than the V_{UVLO_SCIN} rising threshold and V_{LDO_IN} is greater than the $V_{UVLO\_LDO\_IN}$ falling threshold, the internal blocks resume normal operation when either the AC or the DC supply is restored.

注

When the device is in disabled mode and powered by an AC supply, the bridge active control (see the *Active Bridge Control* section) continues to run until the AC supply powers off.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7A78 is a non-isolated smart AC/DC linear-voltage regulator capable of providing a maximum 120-mA load current; see 図 14 and 図 15 for the HB and FB configurations, respectively.

Being highly customizable, the TPS7A78 can be used in many low-power AC-to-DC or DC-to-DC applications, such as electricity meters, appliances, and thermostat controls. 図 18 shows an example configuration for a single-phase AC supply.

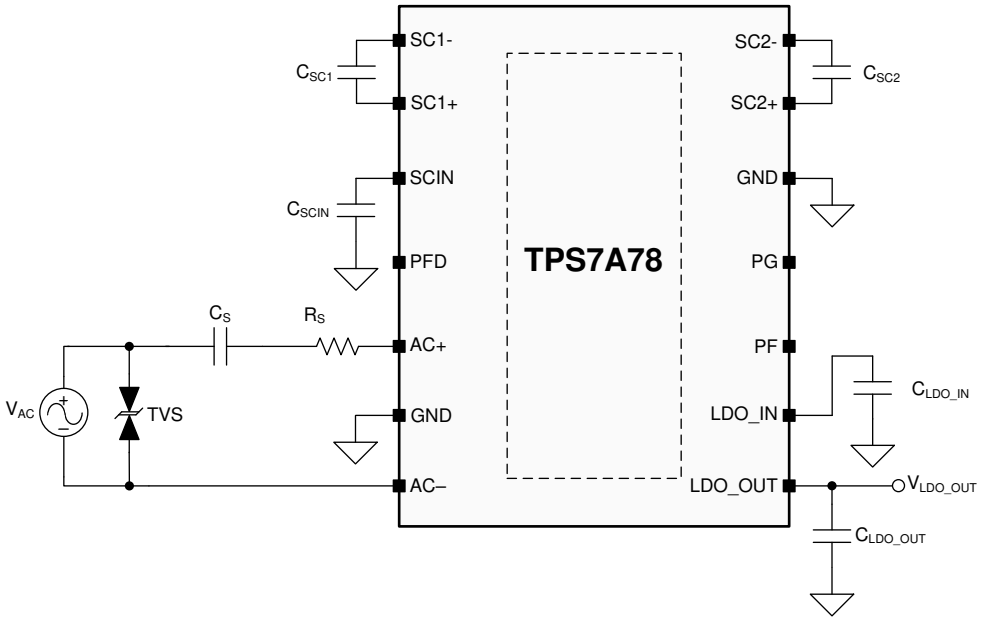


図 18. Implementation Example for the TPS7A78 Single-Phase AC Supply

9.1.1 Recommended Capacitor Types

The choice of capacitor types is flexible as long as the minimum derated capacitor values and capacitor voltage ratings are met.

Based on the system design requirements, TI recommends that greater than the minimum capacitor values and voltage ratings, as well as better than minimum-required dielectric materials for all device capacitors, be specified to ensure optimal performance. Chose the correct high-voltage, safety-rated cap-drop capacitor, C_S, as required by the application. Regardless of the capacitor types selected, the effective capacitance varies with operating voltage, temperature, and time. Follow the manufacturer recommendations for component derating.

9.1.2 Input and Output Capacitors Requirements

All the capacitors illustrated in 図 14 or 図 15 are required for proper operation. The value of C_S required to support the application current is obtained from the *Calculating the Cap-Drop Capacitor C_S* section. The chosen C_S capacitor must tolerate the peak V_{AC} supply voltage of the application and meet the required safety requirements.

Application Information (continued)

Choosing an a larger value of the C_S capacitor than required has an adverse effect on the standby power consumption; however, capacitance reduction over long-term service is inevitable and must be considered when selecting the value of C_S. A ceramic capacitor can be used as C_S in designs for lower AC supply voltages, but the capacitor voltage rating must be appropriate to the application.

For switching capacitors C_{SC1} and C_{SC2}, select the minimum-required capacitor values and voltage ratings specified in the *Recommended Operating Conditions* table. Using too large of a capacitor for the switching capacitors is not recommended because a large capacitor lengthens the start-up time and load transient recovery time of the entire solution. Keep the switching capacitors as close to the device as possible to eliminate any unwanted trace inductance.

For the bulk capacitor C_{SCIN}, use the minimum required capacitor value obtained from the *Calculating the Bulk Capacitor C_{SCIN}* section and increase that value based on the expected capacitor degradation resulting from aging and operating conditions. Accounting for capacitor degradation is especially important if a relatively low life expectancy of the capacitor is expected when an electrolytic capacitor is used. If the application requires an extended hold-up time, the values of the C_{SCIN} or C_{LDO_IN} capacitors can be increased as long as the maximum capacitor values specified in the *Recommended Operating Conditions* table are not exceeded. Using a significantly larger values of C_{SCIN} or C_{LDO_IN} has an adverse effect on the startup time of the solution.

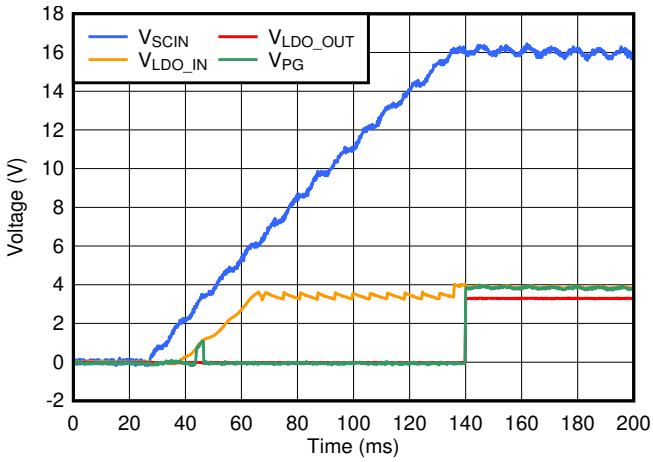
For the C_{LDO_OUT} capacitor, maintain a 10:1 ratio between C_{LDO_IN} and C_{LDO_OUT} for applications using the maximum load current. For lesser load currents, the minimum required C_{LDO_OUT} and C_{LDOU_IN} capacitors are sufficient. For optimum performance, place all capacitors as close as possible to the device.

9.1.3 Startup Behavior

The device startup time is dependent on the circuit topology (FB versus HB configuration), AC supply voltage and frequency, input capacitors values, and output voltage. The FB configuration has a faster startup time compared to the HB configuration. Having a larger than minimum C_S capacitor value shortens the startup time without exceeding the maximum I_{SHUNT} current specified in the *Recommended Operating Conditions* table. However, startup behavior depends on which C_{SCIN} and C_{LDO_IN} capacitor values are used. 図 19 illustrates the startup behavior with the minimum required C_{SCIN} capacitor and a typical C_{LDO_IN} capacitor to support 30 mA of load current with the FB configuration. 図 20 illustrates the startup behavior with the minimum required C_{SCIN} capacitor and a large C_{LDO_IN} capacitor in the same configuration.

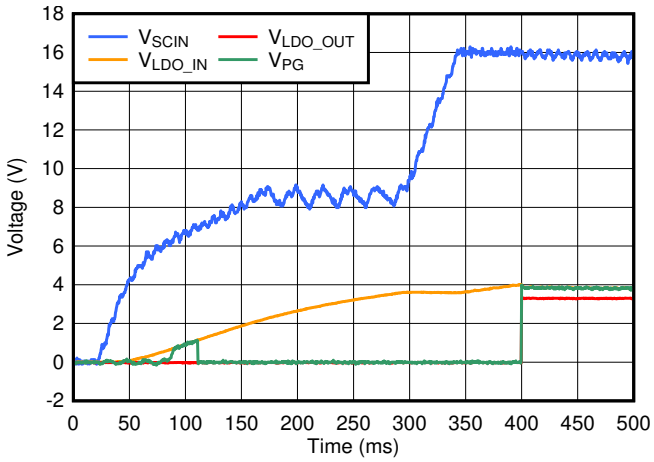
Although the load current has no effect on startup time or startup behavior, the bulk capacitor C_{SCIN} and input capacitor C_{LDO_IN} have a significant effect on the time and behavior; see 図 19 and 図 20. For some applications, larger C_{SCIN} or C_{LDO_IN} capacitors are used to hold-up the output voltage on for a longer period of time after the input collapses.

Application Information (continued)



V_{AC} = 120 V_{RMS} at 60 Hz, FB, C_S = 220 nF,
V_{LDO_OUT} = 3.3 V, C_{SCIN} = 47 µF, C_{LDO_IN} = 1 µF, I_{OUT} = 30 mA

図 19. Startup Behavior With a Minimum C_{SCIN} Capacitor and a Typical C_{LDO_IN} Capacitor for a 30-mA Load



V_{AC} = 120 V_{RMS} at 60 Hz, FB, C_S = 220 nF,
V_{LDO_OUT} = 3.3 V, C_{SCIN} = 47 µF, C_{LDO_IN} = 330 µF,
I_{OUT} = 30 mA

図 20. Startup Behavior With a Minimum C_{SCIN} Capacitor and a Large C_{LDO_IN} Capacitor for a 30-mA Load

9.1.4 Load Transient

A load-transient event can trigger the internal overcharge protection circuit on the LDO_IN pin. This condition prevents C_{LDO_IN} from overcharging when a heavy load is abruptly removed. The overvoltage protection circuit engages and prevents the switched capacitors from switching until the excess charge on C_{LDO_IN} is discharged into the load. This protection behavior occurs most often during heavy load-transient events on devices with higher output voltages. The value of the C_{LDO_IN} capacitor and the load current determine how long the overvoltage protection circuit remains engaged. 図 21 shows the overvoltage protection circuit behavior after the load is removed without tripping the PG signal.

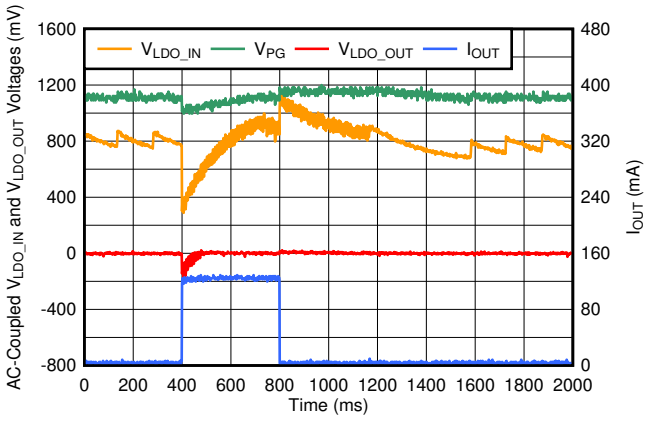
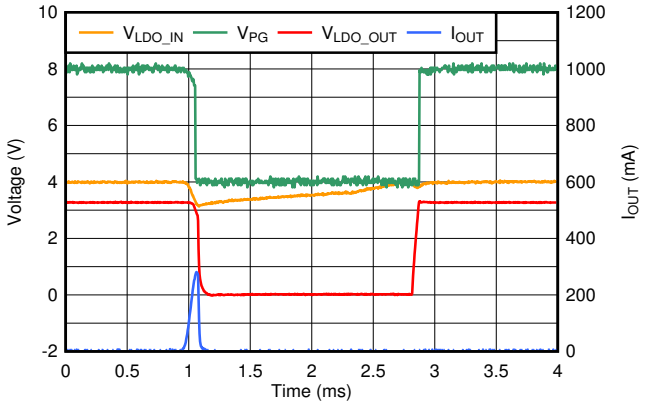


図 21. Overvoltage Protection Circuit Behavior for a 5.0-V Output Voltage Device During Load Transient

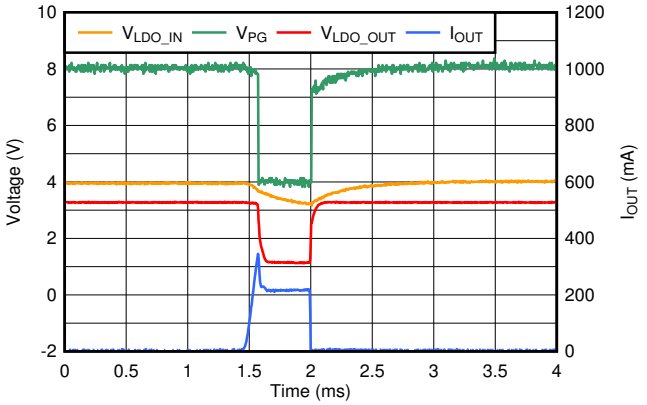
As illustrated in 図 22, a load-transient event that exceeds the maximum output current can disable the output when the heavy load pulls down the V_{LDO_IN} voltage below the $V_{UVLO\_LDO\_IN}$ falling threshold. If the application is prone to heavy load-transient events as illustrated in 図 22, increase the C_{LDO_IN} capacitor value as necessary. However, as illustrated in 図 20, too large of a C_{LDO_IN} leads to a longer startup time.

Application Information (continued)



V_{AC} = 120 V_{RMS} at 60 Hz, FB, C_{LDO_IN} = 10 µF, V_{LDO_OUT} = 3.3 V, I_{OUT} = 1 mA to 600 mA, current slew = 1 A/µs

図 22. Heavy Load-Transient Event Triggering a Restart



V_{AC} = 120 V_{RMS} at 60 Hz, FB, C_{LDO_IN} = 56 µF, V_{LDO_OUT} = 3.3 V, I_{OUT} = 1 mA to 600 mA, current slew = 1 A/µs

図 23. Heavy Load-Transient Event Without Triggering a Restart

9.1.5 Standby Power and Output Efficiency

The AC input current cannot be directly calculated because of the active bridge control; see the *Active Bridge Control* section. The AC input current through the AC+ and AC– pins is a combination of two current components, as shown in 図 24: I_{SHUNT} and I_{PEAK}. The I_{SHUNT} current component is identified by its wave profile because this component is the AC charging current supplied by the cap-drop capacitor C_S. The I_{PEAK} current component is identified by its instantaneous peak current profile.

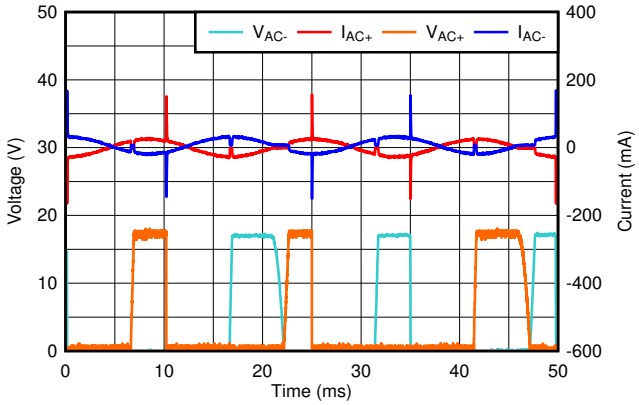


図 24. The Device V_{AC} Input Current With its Two Components

式 1 calculates the shunt current I_{SHUNT}, and 式 2 calculates the peak current I_{PEAK}.

$$I_{SHUNT} = V_{AC\ (MAX)} / XC_S = V_{AC\ (MAX)} \times 2 \times \pi \times f \times C_S \quad (1)$$

$$I_{PEAK} = V_{SCIN} / R_S \quad (2)$$

$$V_{SCIN} = 4 \times (V_{LDO\_OUT\ (nom)} + 0.6\ V)$$

where

- $V_{AC\ (MAX)}$ is the maximum V_{AC} supply RMS voltage
- XC_S is the impedance of the standard C_S capacitor to be used in the application
- V_{SCIN} is the rectified DC voltage on the SCIN pin
- R_S is the standard R_S resistor to be used in the application (3)

Application Information (continued)

The frequency of the shunt activity is uncorrelated to the AC input frequency. Therefore, the standby power must be measured with a power analyzer. Fortunately, using a power analyzer is relatively simple and the measurement setup shown in 図 25 and 図 26 can be used to measure the standby power and the output efficiency.

If the application has an upstream current-limit circuit that limits any high-transient input currents, such as surge or hot-plug currents, the requirement for the surge resistor R_S can be relaxed. The input transient current-limit circuit allows the R_S resistor to be removed, thus significantly improving the standby power and output efficiency because no power loss is dissipated in R_S.

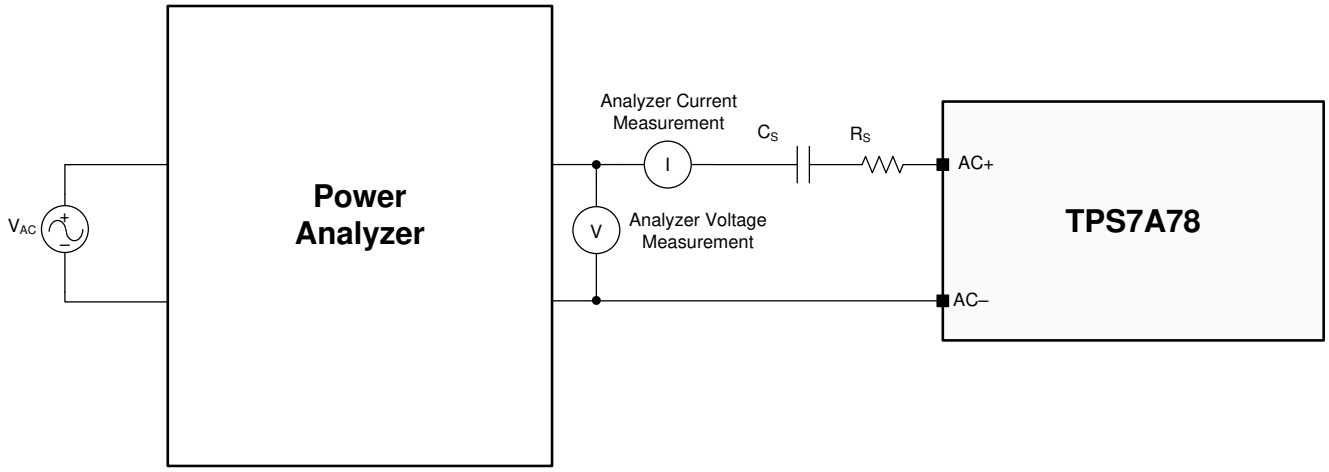


図 25. Standby Power and Output Efficiency Measurement Setup

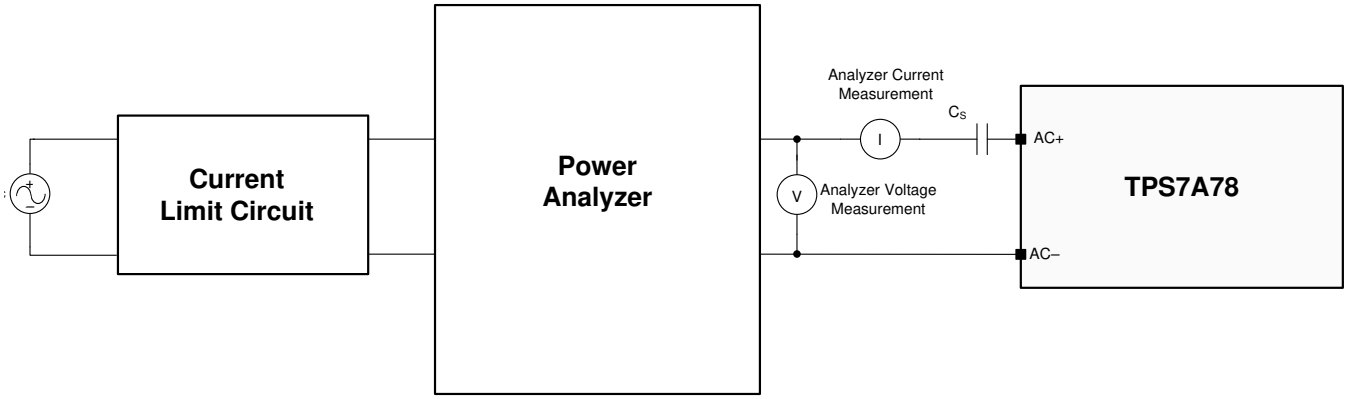
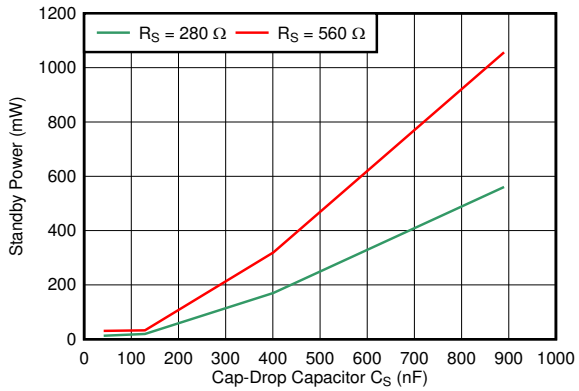


図 26. Standby Power and Output Efficiency Measurement Setup With an Upstream Current-Limit Circuit

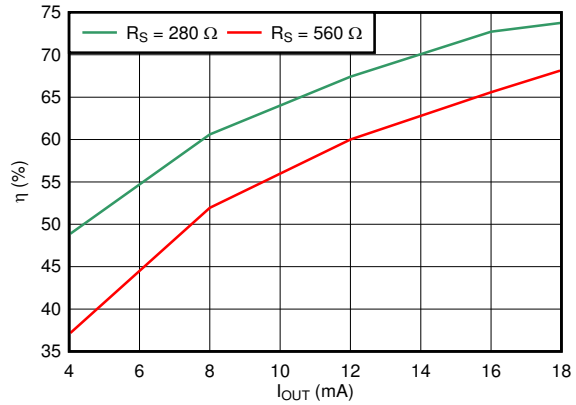
Application Information (continued)

The standby power and output efficiency measurements shown in 図 27 to 図 29 were created with the measurement setup in 図 25.



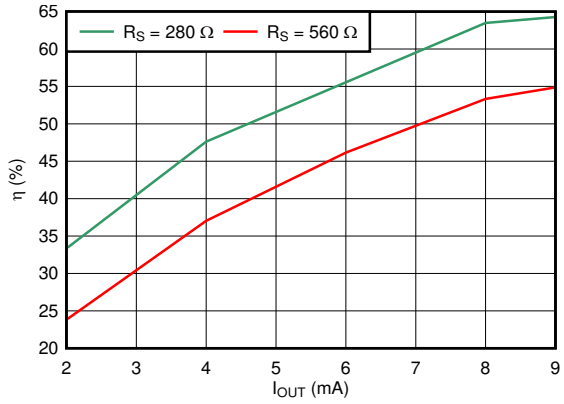
V_{AC} = 120 V_{RMS} at 60 Hz, FB, V_{LDO_OUT} = 5.0 V, I_{OUT} = 0 mA

図 27. Standby Power vs Cap-Drop Capacitor (C_S)



V_{AC} = 120 V_{RMS} at 60 Hz, FB, C_S = 150 nF, V_{LDO_OUT} = 5.0 V

図 28. Efficiency vs I_{OUT} FB Configuration



V_{AC} = 120 V_{RMS} at 60 Hz, HB, C_S = 150 nF, V_{LDO_OUT} = 5.0 V

図 29. Efficiency vs I_{OUT} HB Configuration

9.1.6 Reverse Current

Excessive reverse current can damage the TPS7A78. Reverse current flows through the intrinsic body diode of the pass-transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are:

- If the device has a large C_{LDO_OUT} and the input supply collapses with little or no load current
- The LDO_OUT pin is biased when the input supply is not present
- The LDO_OUT pin is biased above the voltage of the LDO_IN pin

If reverse current flow is expected in the application, external protection is recommended to provide protect. Reverse current is not limited within the device, so external limiting is required, as illustrated in 図 30 and 図 31, if extended reverse-voltage operation is anticipated.

Application Information (continued)

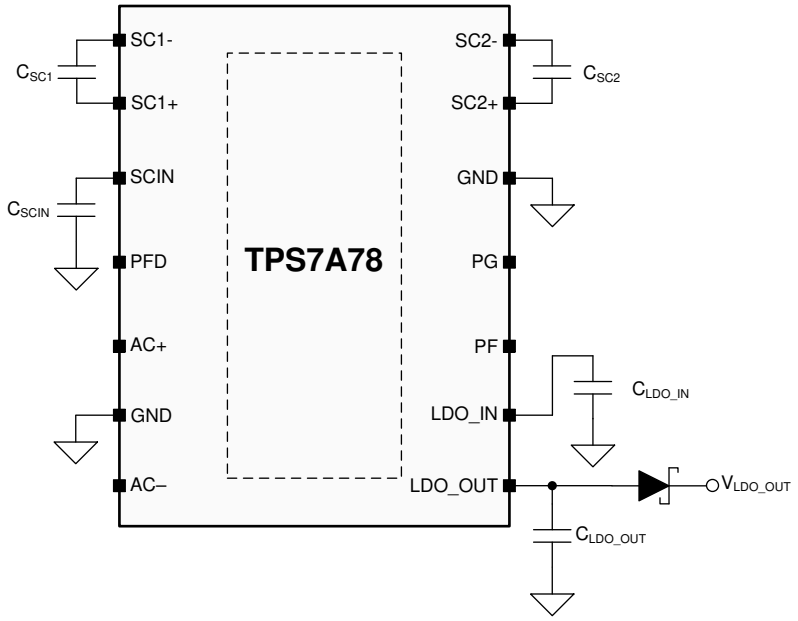


図 30. Example Circuit for Reverse Current Protection Using a Schottky Diode

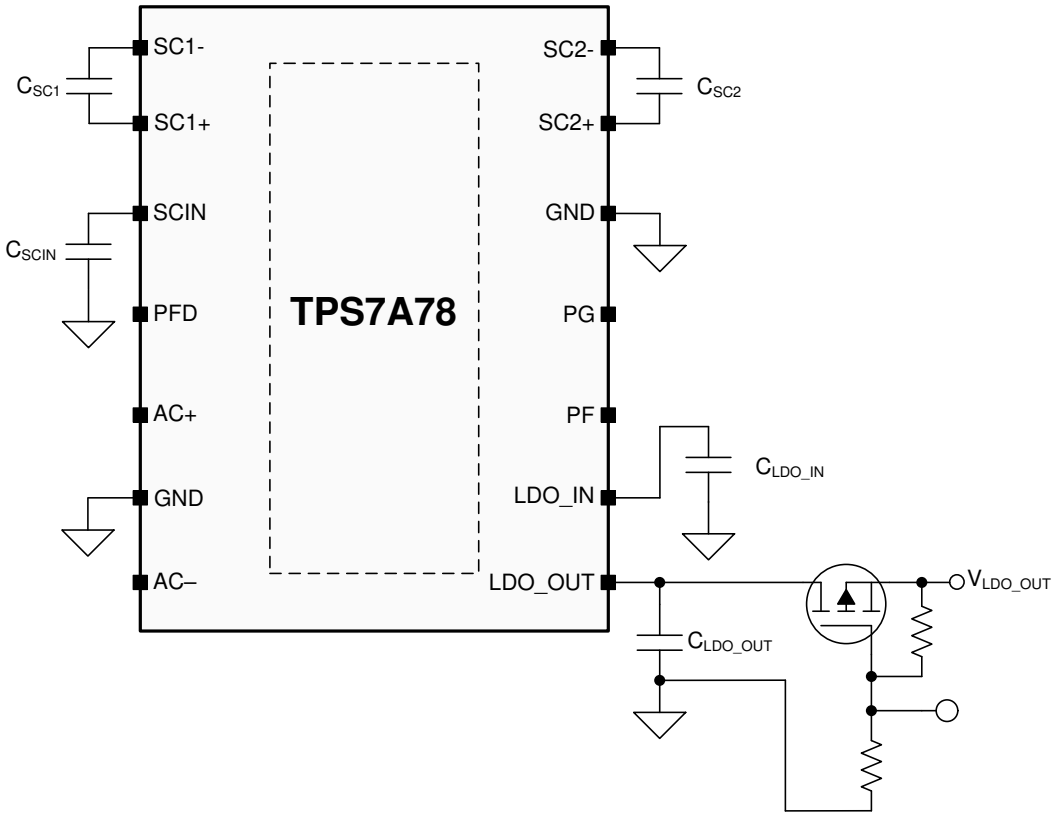


図 31. Example Circuit for Reverse Current Protection Using a P-Channel FET

Application Information (continued)

9.1.7 Switched-Capacitor Stage Output Impedance

To ensure a low output impedance of the device switched-capacitor stage (charge pump), connect a 1-µF X5R or a better dielectric capacitor in parallel with the bulk capacitor C_{SCIN}. 図 32 shows the switched-capacitor stage output impedance versus temperature at the maximum output current of 120 mA. When a DC supply power source is used to power the device under heavy loading conditions close to the maximum current rating at high temperature, the load can run the LDO into dropout because of the degradation in the charge pump output impedance. To enhance performance with a DC supply, apply the DC supply voltage to the SCIN pin equal to 4 (VLDO_OUT (nom) + 0.6 V) + 2 V to ensure optimal performance. See 図 5 and 図 6 for a 3.3-V output voltage example.

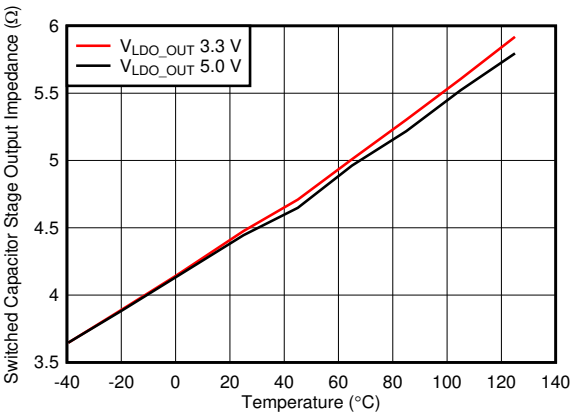


図 32. Switched-Capacitor Stage Output Impedance vs Temperature at a 120-mA Load Current

9.1.8 Power Dissipation (P_D)

To ensure proper thermal design, the printed circuit board (PCB) area around the TPS7A78 must include a minimal of heat-generating devices to avoid added thermal stress. The three internal sources that dissipate power are: the bridge rectifier conduction losses, the switched-capacitor stage, and the LDO. For devices with an output voltage greater 3.3 V, the maximum power dissipation under a maximum load current of 120 mA is estimated to be between 160 mW and 190 mW, assuming a nominal C_S capacitor value for the given load current. For applications with less than a 3.3-V output , the power dissipated in the LDO is the dominant power and can be calculated using 式 4 because the dropout voltage between V_{LDO_IN} and V_{LDO_OUT} can be as high as 2.7 V for the 1.3-V output option. See the *Dropout Voltage Regulation* section for details on dropout voltage.

$$P_{D\_LDO} = (V_{LDO\_IN} - V_{LDO\_OUT}) \times I_{OUT} \quad (4)$$

The higher dropout for less than 2.0-V output voltage options may run the device into thermal limitations at the startup ramp for higher temperatures, especially with the large LDO_OUT pin capacitor or when close to the maximum load. The thermal pad under the TPS7A78 must contain an array of filled vias that conduct heat to additional copper planes for increased heat dissipation. The amount of thermal dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to 式 5, power dissipation and junction temperature are determined by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package as well as the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance, but not indicative of performance in any particular implementation.

Application Information (continued)

9.1.9 Estimating Junction Temperature

The JEDEC standard recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J). As described in the *Semiconductor and IC Package Thermal Metrics* application report, use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. As described in the *Semiconductor and IC Package Thermal Metrics* application report, use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to estimate the junction temperature.

$$T_J = T_T + \psi JT \times P_{D\_Total} \quad (6)$$

where

- P_{D_Total} is the total dissipated power in the device
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi JB \times P_D \quad (7)$$

where

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report.

9.2 Typical Application

This section demonstrates the design process for a typical application of the TPS7A78, including the calculation of the values of the external components required for proper operation. 図 33 shows an optimized electricity meter application using an HB configuration. For this design, the AC supply line voltage is referenced to the TPS7A78 GND pins to share the same GND as the system microcontroller.

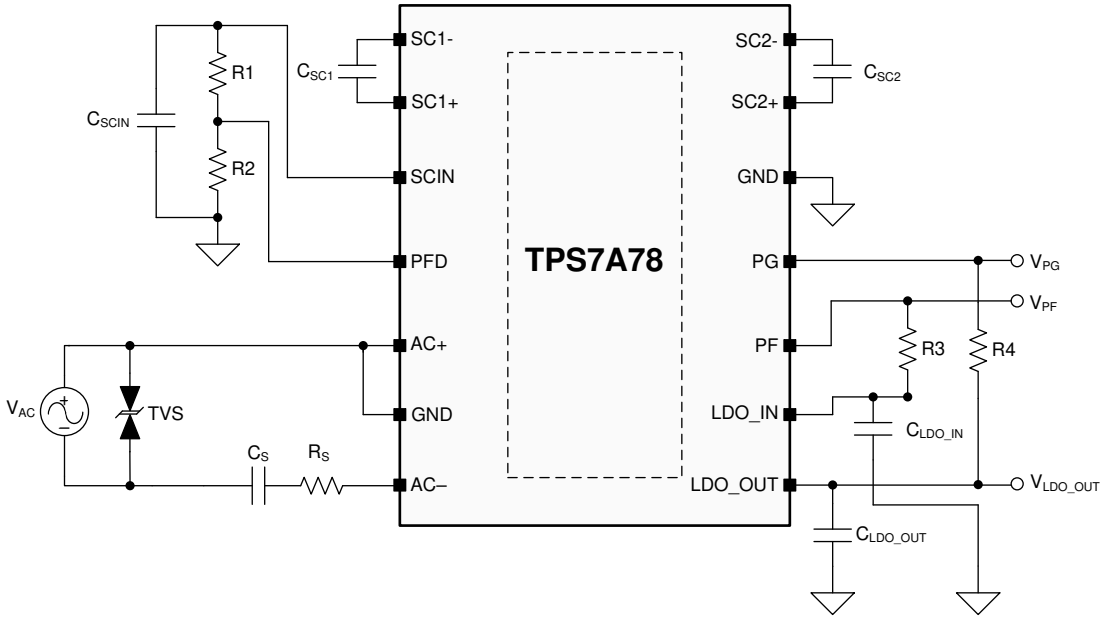


図 33. Example for a Single-Phase Electricity Meter Configuration

Typical Application (continued)

9.2.1 Design Requirements

表 2 summarizes the design requirement for this example.

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
V_{AC} supply voltage	85 $V_{AC\ RMS}$ to 265 $V_{AC\ RMS}$
V_{AC} supply frequency	50 Hz (±3 Hz)
Bridge configuration	HB, AC+ pin is tied to the device GND pins
Device GND pins reference	Floating device GND, AC supply line voltage is referenced to the device GND pins
Output voltage	3.3 V
Output current	12 mA
Electrical fast transient immunity (EFT)	(IEC 61000-4-4) level 2 (1 kV)

9.2.2 Detailed Design Procedure

This section discusses how to calculate the external components required for this design example.

9.2.2.1 Calculating the Cap-Drop Capacitor C_S

Use 式 8 to calculate the minimum required cap-drop capacitance needed to support the application current. For common application conditions, 表 3 can be used to select the minimum standard cap-drop capacitor required to support the application current. However, neither 式 8 nor 表 3 account for capacitance derating under biasing voltage and operating temperature conditions. Follow the manufacturer recommendation and guidelines on capacitor derating and degradation to ensure the minimum-required capacitance needed for the application under various operating conditions. Do not use a load current less than 10 mA to calculate the C_S capacitor because the device current is a larger fraction of the load current. 式 8 and 表 3 can also be used to calculate the value of C_S depending on the application $V_{AC\ (MIN)}$ voltage and frequency and then use the highest value for the application.

$$C_S = I_{OUT} / (16 \times f \times [\sqrt{2} \times V_{AC\ (MIN)} - 4 \times (V_{LDO\_OUT\ (nom)} + 0.6\ V)]) \quad (8)$$

where

- the C_S value is the minimum cap-drop capacitance value in farads needed to support I_{OUT}
- I_{OUT} is the application nominal load current, but the application peak current must be considered if this current cannot be supported by the LDO output capacitor
- V_{LDO_OUT} is the targeted LDO output voltage
- $V_{AC\ (MIN)}$ is the minimum RMS V_{AC} supply voltage
- f is the minimum V_{AC} line frequency

表 3. The Minimum Required Cap-Drop Capacitor C_S

$V_{AC\ (MIN)}$ (f)	I_{OUT} (mA)	C_S FOR FB (nF)	C_S FOR HB (nF)
120 (60)	10	100	220
	30	330	470
	60	560	1000
	90	820	1500
	120	1000	2200
240 (50)	10	47	100
	30	150	330
	60	330	560
	90	470	820
	120	560	1200

The capacitance value of C_S from 式 8 is for the FB configuration. For the HB configuration, double the calculated capacitance value, then approximate the value up to the nearest standard capacitor value after taking capacitance degradation into account. Similarly, the capacitor value of C_S from 表 3 represents the minimum required capacitor value and is already approximated to the nearest standard value but capacitor degradation is not accounted for.

9.2.2.1.1 C_S Calculations for the Typical Design

式 8 yields a capacitance value of 153 nF, as given by 式 9, which results from the $V_{AC\ (MIN)}$ voltage and frequency of this application. This value is for the FB configuration. For the HB configuration, doubling the calculated capacitance value yields 306 nF, and approximate this value up to the nearest standard capacitor value, which yields a C_S value of 330 nF.

$$C_S = (0.012\ ) / (16 \times 47 \times [\sqrt{2} \times 85 - 4(3.3 + 0.6)]) = 153\ n\ F \quad (9)$$

As mentioned in the *Calculating the Cap-Drop Capacitor C_S* and *Input and Output Capacitors Requirements* sections, capacitance loss under long-term service is inevitable and must be considered in the design. Follow the manufacturer recommendations and guidelines for capacitor derating and degradation over time.

9.2.2.2 Calculating the Surge Resistor R_S

The device requires a surge resistor or resistors in series with the AC+ and or AC– pins, depending configuration; see the *Full-Bridge (FB) and Half-Bridge (HB) Configurations* section for details. The purpose of the surge resistor is to limit the hot-plug AC current into the AC+ and AC– pins when the AC supply voltage is applied. 式 10 calculates the value of the minimum surge resistor $R_{S\ (MIN)}$ required for the application.

$$R_{S\ (MIN)} = V_{AC\ (PEAK)} / I_{Surge\ (MAX)}$$

where

- $V_{AC\ (PEAK)}$ is the peak V_{AC} supply voltage for the application
- $I_{Surge\ (MAX)}$ is the maximum V_{AC} current into or out of out the AC+ or AC– pins for a duration of ≤100 µs, as specified in the *Recommended Operating Conditions* table. (10)

If the solution requires the use of a transient voltage surge suppressor (TVS) or a metal-oxide varistor (MOV), then use the maximum clamping voltage of the TVS or MOV instead of the peak V_{AC} voltage in 式 10. After calculating $R_{S\ (MIN)}$, select the next-higher standard resistor value.

9.2.2.2.1 R_S Calculations for the Typical Design

The peak AC supply voltage for this example is equal to 375 V ($\sqrt{2}$ × 265) and the electrical fast transient immunity (EFT) requirement is given as 1 kV. Thus, a TVS with a maximum clamping voltage of 1000 V can be used. 式 11 shows the calculated $R_{S\ (MIN)}$ value.

$$R_{S\ (MIN)} = 1000 / 2.5 = 400\ \Omega \quad (11)$$

Because both the device I_{PEAK} current and the device maximum I_{SHUNT} current flow through R_S, the power rating of R_S must be able to handle these currents values. See the *Checking for the Device Maximum I_{SHUNT} Current* section for the I_{SHUNT} current calculation and R_S power rating for this application.

If the application already has an upstream hot-plug current-limit circuit, then the requirement for the surge resistor can be relaxed to significantly improve the solution standby-power; see the *Standby Power and Output Efficiency* section for details.

9.2.2.3 Checking for the Device Maximum I_{SHUNT} Current

After determining the cap-drop capacitor value, a check must be performed to confirm that the maximum I_{SHUNT} current specified in the *Recommended Operating Conditions* table is not exceeded by the standard capacitor value of C_S. Other factors that affect the I_{SHUNT} current are the maximum AC supply RMS voltage and the maximum line frequency.

9.2.2.3.1 I_{SHUNT} Calculations for the Typical Design

Given the maximum AC supply voltage and the minimum frequency for this application example, the calculated I_{SHUNT} current using 式 1 from the *Standby Power and Output Efficiency* section yields:

$$I_{SHUNT} = 265 \times 2 \times \pi \times 53 \times 330 \times 10^{-9} = 0.02912 \text{ A} \quad (12)$$

注

The *Recommended Operating Conditions* table does not specify the maximum AC voltage that can be used because the maximum V_{AC} voltage is bound by the maximum I_{SHUNT} current and the availability of the high-voltage cap-drop capacitor.

The RMS power given in 式 13 and the peak power given in 式 14 must be used to determine the power rating of the surge resistor R_S.

$$P_{RMS} = (I_{SHUNT})^2 \times R_S \quad (13)$$

$$P_{PEAK} = [I_{SHUNT} \times R_S + 4(V_{LDO\_OUT\ (nom)} + 0.6\ V)]^2 / R_S \quad (14)$$

Using 式 13 and 式 14 yields the following R_S power ratings:

$$P_{RMS} = (0.02912)^2 \times 400 = 0.34 \text{ W} \quad (15)$$

$$P_{PEAK} = [0.02912 \times 400 + 4(3.3 + 0.6)]^2 / 400 = 1.86 \text{ W} \quad (16)$$

Use the power rating resulting from 式 14 because this equation yields a higher power requirement. Furthermore, additional margin is always a good design practice.

9.2.2.4 Calculating the Bulk Capacitor C_{SCIN}

The TPS7A78 uses a bulk capacitor C_{SCIN} to smooth the rectified DC voltage ripple on the SCIN pin and to supply charge to the switched capacitor stage; see the *4:1 Switched-Capacitor Voltage Reduction* section. The C_{SCIN} capacitor also functions as a charge reservoir to hold-up the device output voltage for a period of time if the supply collapses. The minimum value of the C_{SCIN} capacitor required can be calculated using 式 17 through 式 20, however these equations make the following assumptions to simplify the C_{SCIN} capacitor calculation:

- The AC supply frequency is within ±5% of the nominal standard frequencies of 50 Hz and 60 Hz
- The voltage ripple on the SCIN pin is around from 0.5 V to 0.8 V.
- The AC impedance of the cap-drop capacitor C_S is at least ten times lower than that of the bulk capacitor C_{SCIN} and the surge resistor R_S

Use 式 17 for the FB 60-Hz V_{AC} supply and 式 18 for the HB 60-Hz V_{AC} supply.

$$C_{SCIN} = 0.0014 \times I_{OUT} \quad (17)$$

$$C_{SCIN} = 0.0035 \times I_{OUT} \quad (18)$$

Use 式 19 for the FB 50-Hz V_{AC} supply and 式 20 for the HB 50-Hz V_{AC} supply.

$$C_{SCIN} = 0.0017 \times I_{OUT} \quad (19)$$

$$C_{SCIN} = 0.0041 \times I_{OUT}$$

where

- I_{OUT} is the application load current (20)

The calculated C_{SCIN} capacitor from 式 17 through 式 20 represents the minimum value required for the application example. However, 式 17 through 式 20 do not account for capacitance derating for all operating conditions. Follow the manufacturer recommendation and guidelines to ensure the minimum required capacitance needed for the application. See the *Input and Output Capacitors Requirements* section for more details.

9.2.2.4.1 C_{SCIN} Calculations for the Typical Design

式 21 shows the use of 式 20 to calculate the C_{SCIN} capacitor value for the requirements of this application example.

$$C_{SCIN} = 0.0041 \times 0.012 = 49.2\ \mu F \quad (21)$$

The calculated C_{SCIN} capacitor from the equations in the *Calculating the Bulk Capacitor C_{SCIN}* section represents the minimum value required for the respective device configuration. Choose the nearest standard capacitor value; see the *Input and Output Capacitors Requirements* section for more details.

9.2.2.5 Calculating the PFD Pin Resistor Dividers for a Power-Fail Detection

Using the device power-fail detection feature is optional as indicated in *図 14* and 図 15. The PFD pin is an analog voltage input to an internal comparator that drives the open-drain PF output. The resistor divider consisting of R_1 and R_2 can be used to set the minimum V_{SCIN} voltage that triggers the PF output. Regardless of whether an AC or DC supply is used, the PF output triggers when the supply fails to maintain the V_{SCIN} voltage above $V_{SCIN\ (MIN)}$. 式 22 gives the calculation of the $R_1 – R_2$ resistor divider that sets the PF pin trigger point.

$V_{IT(PFD,FALLING)}$ threshold = ($V_{SCIN\ (MIN)}$ – V_{ripple} on the SCIN pin) × [R_2 / (R_1+ R_2)]

where

- V_{Ripple} is the peak-to-peak voltage ripple on the SCIN pin and is in the range of 0.5 V to 0.8 V (22)

式 23 calculates the $V_{SCIN\ (MIN)}$ voltage.

$$V_{SCIN\ (MIN)} = 4\ (V_{LDO\_OUT\ (nom)} + 0.6\ V) – 1.5\ V \quad (23)$$

Set R_1 as close as possible to the maximum value specified in the *Recommended Operating Conditions* table. This high R_1 value limits the power used by the resistors, then calculates the value of R_2. Choose the closest standard resistor value for R_2. Optionally, because the PFD pin is a high-impedance node, add a 10-pF capacitor in parallel with the R_2 resistors to reduce noise coupling into V_{PFD}.

Pull up the PF pin to a DC rail, such as V_{LDO_IN}, so that a microcontroller can monitor the PF signal as an early power-fail warning to trigger the switch to a backup power solution or to perform a controlled system shutdown. Pulling up the PF pin to V_{LDO_IN} rather than V_{LDO_OUT} ensures that the PF signal is continuously monitored even if V_{LDO_OUT} is down because of a load-transient event or a short-circuit fault.

注

An external DC rail can also be used to pullup the PF pin signal via a pullup resistor only if the external DC rail shares a common ground with the device GND pins and the absolute maximum of the PF pin voltage is not exceeded.

9.2.2.5.1 PFD Pin Resistor Divider Calculations for the Typical Design

Using 式 23 and then solving 式 22 for R_2 yields an R_2 value of 18.3 kΩ.

$$V_{SCIN\ (MIN)} = 4\ (3.3 + 0.6) – 1.5\ V = 14.1\ V \quad (24)$$

$$R_2 = (V_{IT(PFD,FALLING)} \times R_1) / (V_{SCIN\ (MIN)} – V_{ripple}\ \text{on the SCIN pin} – V_{IT(PFD,FALLING)}) \quad (25)$$

$$R_2 = (1.17 \times 200) / (14.1 – 0.5 – 1.17) \quad (26)$$

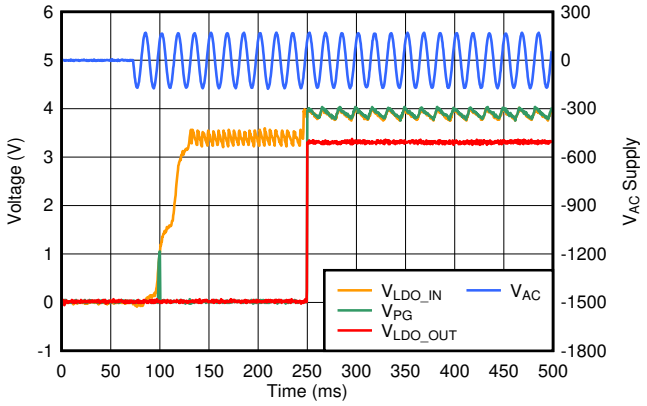
9.2.2.6 Summary of the Typical Application Design Components

表 4 summarizes the component values chosen through the design process for this application example.

表 4. Typical Application Design Example Components

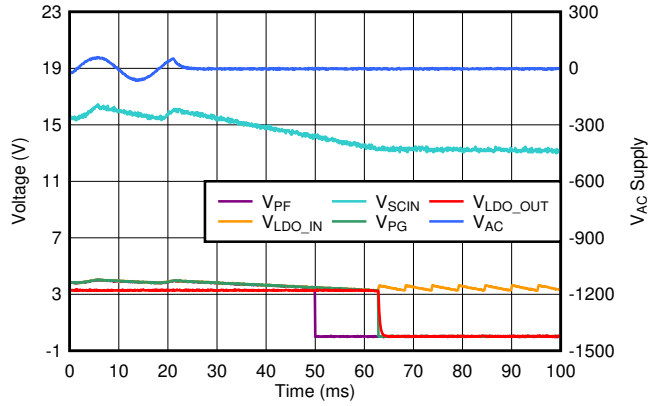
COMPONENT	CALCULATED VALUE
C_S	330 nF, capacitance loss under long-term service is inevitable and must be considered in the design.
R_S	400 Ω, see the *Checking for the Device Maximum I_{SHUNT} Current* section for the R_S power-rating calculation.
C_{SCIN}	47 µF, approximate the 49.2-µF capacitor value resulting from the *Calculating the Bulk Capacitor C_{SCIN}* section.
C_{SC1}	1 µF, select the minimum capacitor value specified in the *Recommended Operating Conditions* table.
C_{SC2}	1 µF, select the minimum capacitor value specified in the *Recommended Operating Conditions* table.
C_{LDO_IN}	1 µF, select the typical capacitor value specified in the *Recommended Operating Conditions* table.
C_{LDO_OUT}	1 µF, select the typical capacitor value specified in the *Recommended Operating Conditions* table.
R_1	200 kΩ, select the maximum resistor value specified in the *Recommended Operating Conditions* table.
R_2	18.7 kΩ, approximate the 18.3-kΩ resistor value from the *PFD Pin Resistor Divider Calculations for the Typical Design* section.
R_3 and R_4	100 kΩ, select the maximum resistor values specified in the *Recommended Operating Conditions* table.

9.2.3 Application Curves



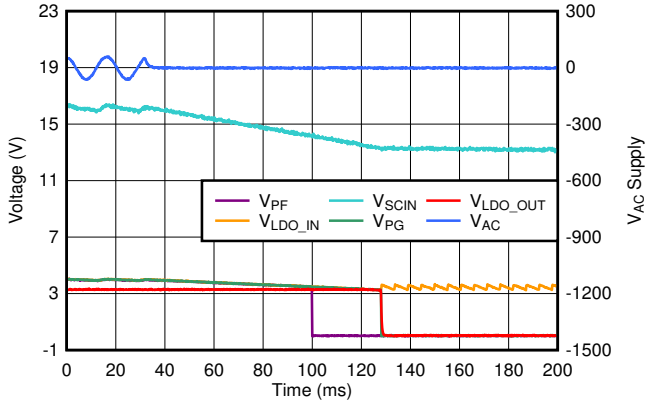
C_S = 330 nF, C_{SCIN} = 47 µF, C_{SC1} = C_{SC2} = 1.0 µF,
C_{LDO_IN} = C_{LDO_OUT} = 1.0 µF, I_{OUT} = 12 mA

図 34. Startup Time



C_S = 330 nF, C_{SCIN} = 47 µF, C_{SC1} = C_{SC2} = 1.0 µF,
C_{LDO_IN} = C_{LDO_OUT} = 1.0 µF, I_{OUT} = 12 mA

図 35. Shutdown Hold-Up Time With a 47-µF C_{SCIN} Capacitor



C_S = 330 nF, C_{SCIN} = 120 µF, C_{SC1} = C_{SC2} = 1.0 µF,
C_{LDO_IN} = C_{LDO_OUT} = 1.0 µF, I_{OUT} = 12 mA

図 36. Shutdown Hold-Up Time With a 120-µF C_{SCIN} Capacitor

10 Power Supply Recommendations

The TPS7A78 is designed primarily to operate from an AC supply voltage ≥ 18 V_{AC} and an input line frequency up to 20 kHz. To ensure that the output voltage is well regulated and that dynamic performance is optimum, the procedures and examples in the *Typical Application* section must be followed.

The TPS7A78 can also operate from a DC supply voltage from 17 V to 23 V depending on the output voltage. To ensure proper operation and ensure that the DC output voltage is well regulated, the DC supply voltage applied to the SCIN pin must be well regulated and greater than or equal to the minimum V_{UVLO_SCIN} rising threshold specified in the *Electrical Characteristics* table.

11 Layout

11.1 Layout Guidelines

- Place the input and output capacitors as close to the TPS7A78 as possible
- Place the PFD resistor divider, if used, away from the AC+, AC– pins, and the switched-capacitor stage pins; if not used, tie the PFD pin to the common ground with the device GND pins
- Pull up the PG pin, if used, to the LDO_OUT pin via a pullup resistor; otherwise, tie the PG pin to the common ground with the device GND pins
- Pull up the PF pin, if used, to the LDO_IN pin via a pullup resistor; otherwise, tie the PF pin to the common ground with the device GND pins
- Follow the recommended creepage distance between the AC+ and AC– pin traces, and between these traces and other circuit traces
- Tie the AC+ and AC– pins to the device GND pins if only the DC input supply is used
- Place thermal vias around the device to distribute heat

11.2 Layout Example

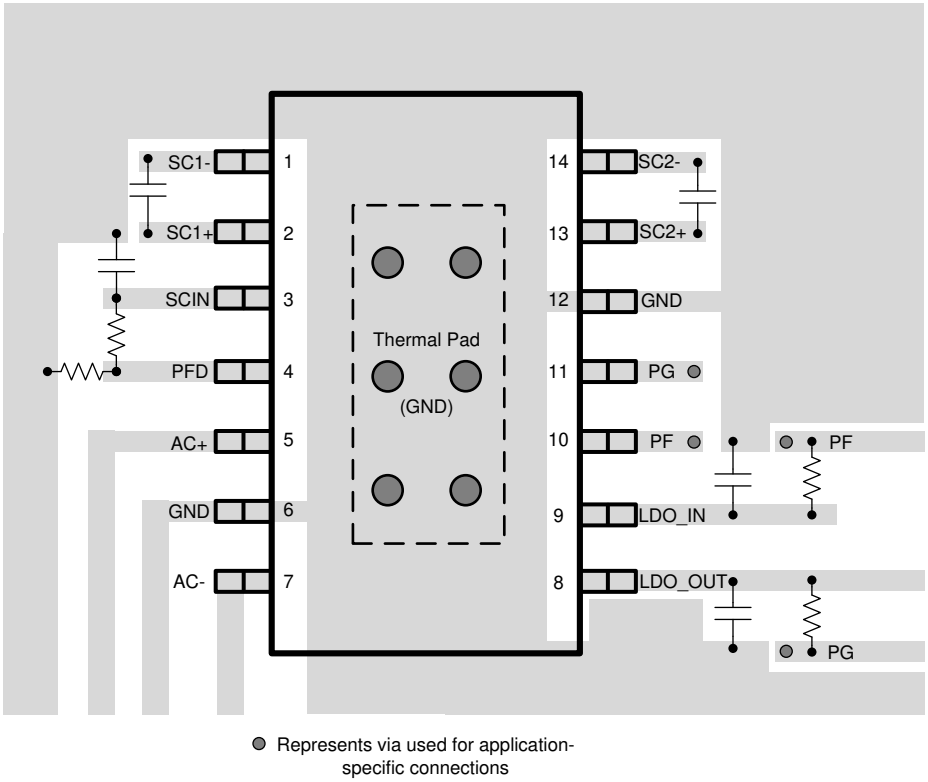


図 37. Example Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 評価基板

TPS7A78 を使用する回路の性能の初期評価に役立てるため、評価基板 (EVM) を利用可能です。*TPS7A78EVM-011 評価基板のユーザー・ガイド*は、テキサス・インスツルメンツの Web サイトのプロダクト・フォルダから請求するか、TI eStore から直接お求めになれます。

12.1.1.2 SIMPLIS モデル

このデバイス用の SIMPLIS モデルは、*ツールとソフトウェア*タブのTPS7A78 プロダクト・フォルダで提供しています。

12.1.2 デバイスの項目表記

表 5. デバイスの項目表記(1)(2)

製品名	V_{LDO_OUT}
TPS7A78**xx(x)yyyz**	**xx(x)** は公称出力電圧です。出力電圧の分解能が 50mV の場合、注文番号に 2 桁が使用されます。それ以外の場合は 3 桁が使用されます (例:33 = 3.3V、135 = 1.35V)。 **yyy**はパッケージ指定子です。 **z**はパッケージ数量です。Rは数量の大きいリール、Tは数量の小さいリールです。

(1) 最新のパッケージと発注情報については、このデータシートの末尾にある「パッケージ・オプション」の付録を参照するか、www.ti.comにあるデバイスの製品フォルダをご覧ください。
(2) 出力電圧は、1.3V から 5.0V まで、50mV 刻みで設定できます。詳細と在庫については、工場にお問い合わせください。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『TPS7A78EVM-011 Evaluation module』*ユーザー・ガイド (英語)
- テキサス・インスツルメンツ、*『One-Phase Shunt Electricity Meter Reference Design Using Standalone ADCs』*デザイン・ガイド (英語)
- テキサス・インスツルメンツ、*『Off-Line (Non-Isolated) AC/DC Power Supply Architectures Reference Design for Grid Applications』*デザイン・ガイド (英語)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 商標

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12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A7833PWPR	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7833
TPS7A7833PWPR.A	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7833
TPS7A7833PWPT	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7833
TPS7A7833PWPT.A	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7833
TPS7A7836PWPR	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7836
TPS7A7836PWPR.A	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7836
TPS7A7836PWPT	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7836
TPS7A7836PWPT.A	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7836
TPS7A7850PWPR	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7850
TPS7A7850PWPR.A	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7850
TPS7A7850PWPT	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7850
TPS7A7850PWPT.A	Active	Production	HTSSOP (PWP) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	S7A7850

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

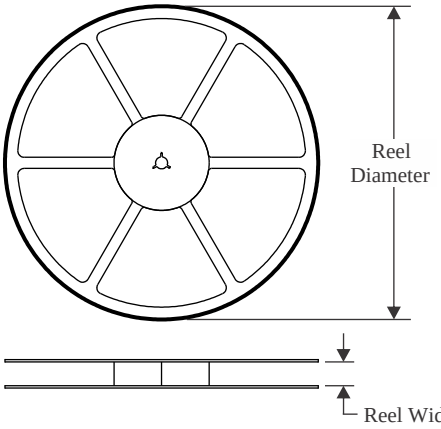
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

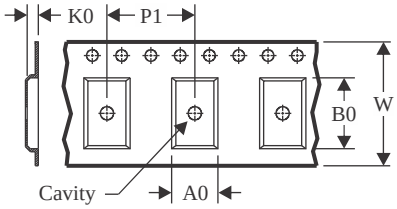
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

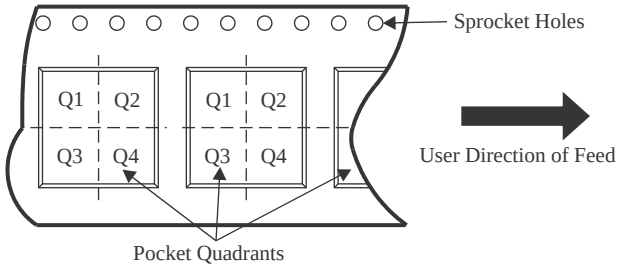


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

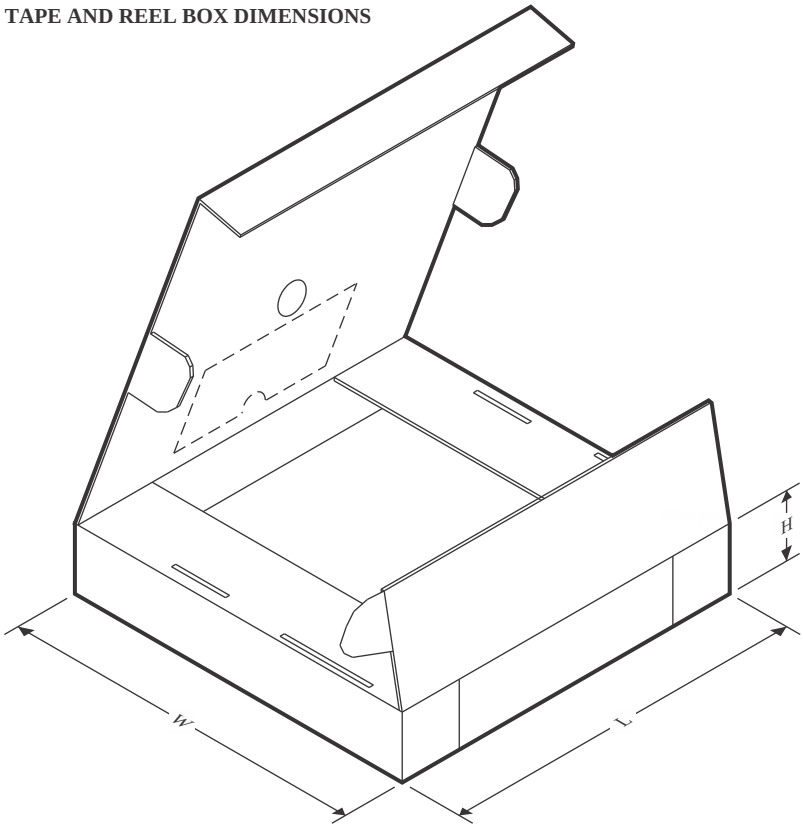
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7833PWPR	HTSSOP	PWP	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A7833PWPT	HTSSOP	PWP	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A7836PWPR	HTSSOP	PWP	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A7836PWPT	HTSSOP	PWP	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A7850PWPR	HTSSOP	PWP	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7A7850PWPT	HTSSOP	PWP	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7833PWPR	HTSSOP	PWP	14	3000	353.0	353.0	32.0
TPS7A7833PWPT	HTSSOP	PWP	14	250	353.0	353.0	32.0
TPS7A7836PWPR	HTSSOP	PWP	14	3000	353.0	353.0	32.0
TPS7A7836PWPT	HTSSOP	PWP	14	250	353.0	353.0	32.0
TPS7A7850PWPR	HTSSOP	PWP	14	3000	353.0	353.0	32.0
TPS7A7850PWPT	HTSSOP	PWP	14	250	353.0	353.0	32.0

GENERIC PACKAGE VIEW

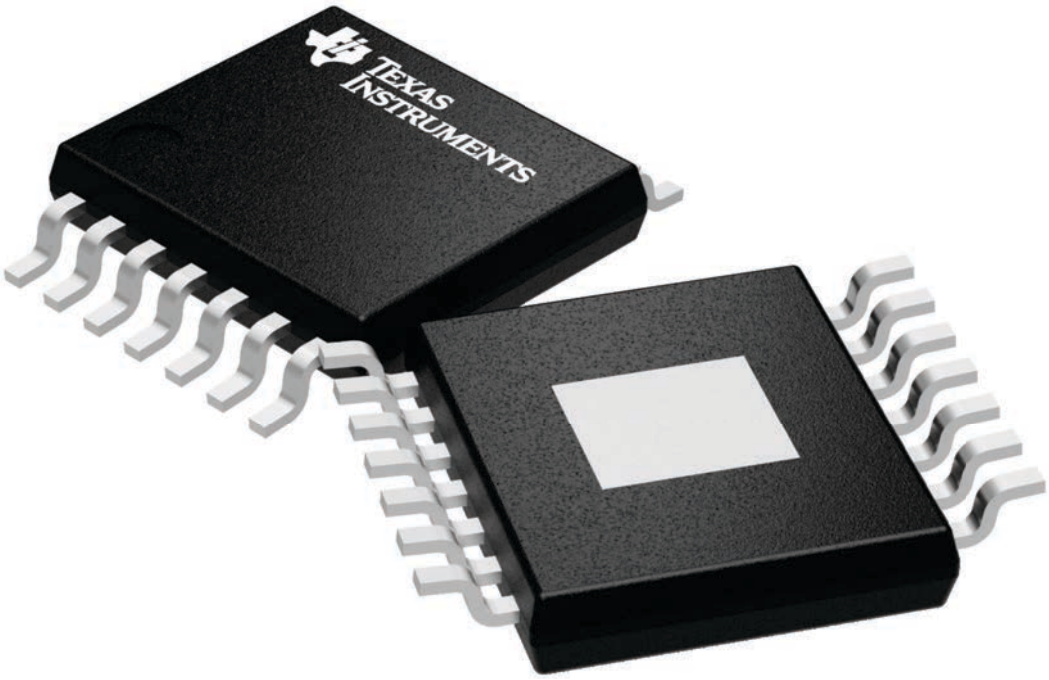
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



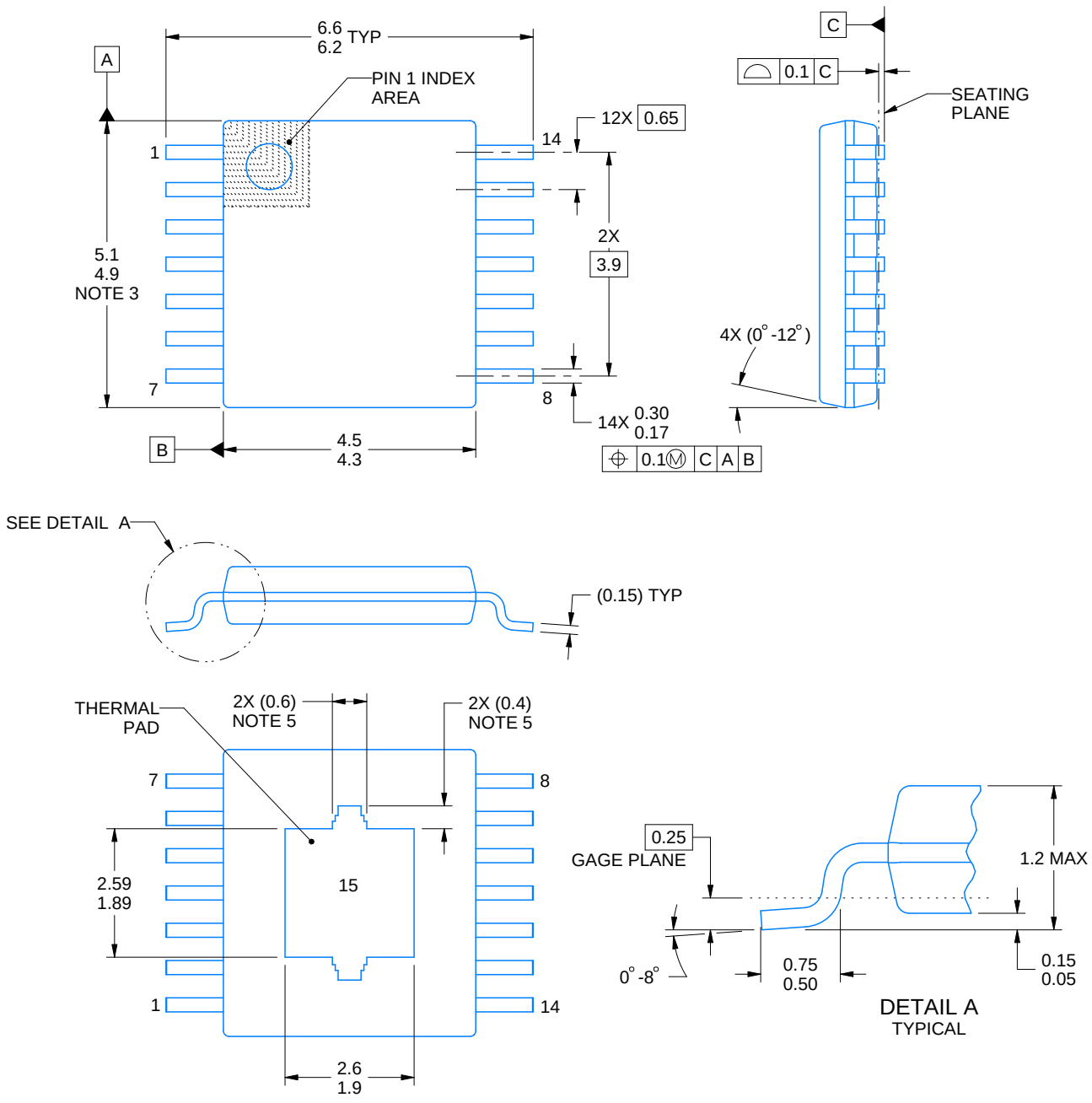
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

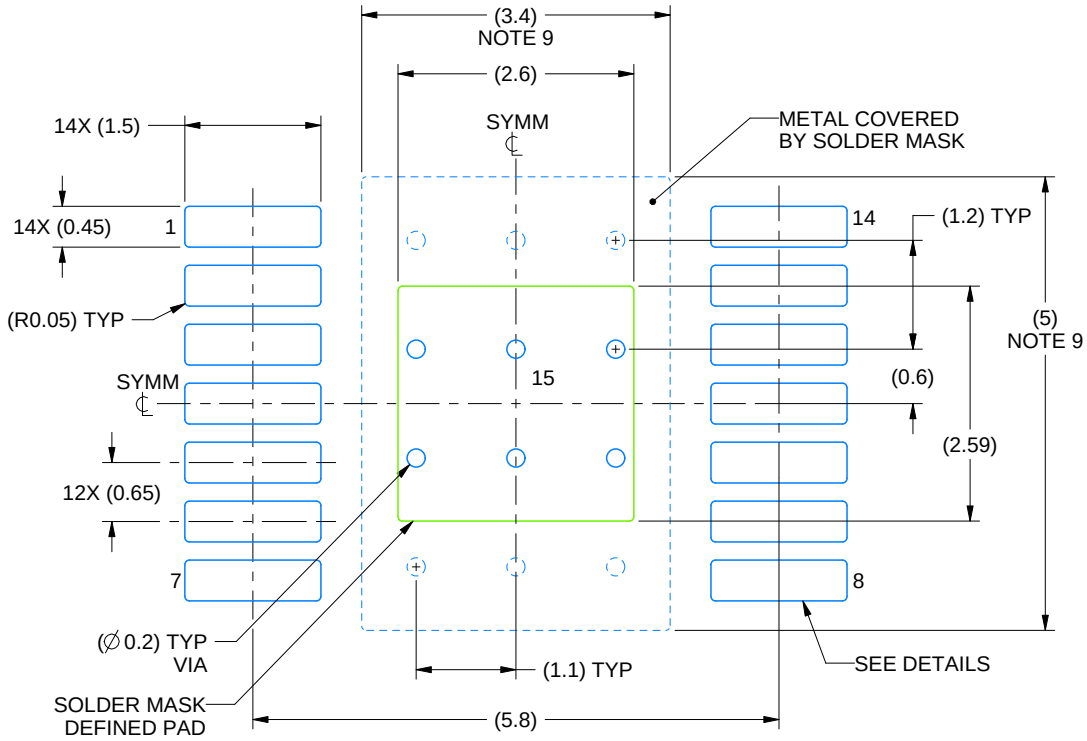
SMALL OUTLINE PACKAGE



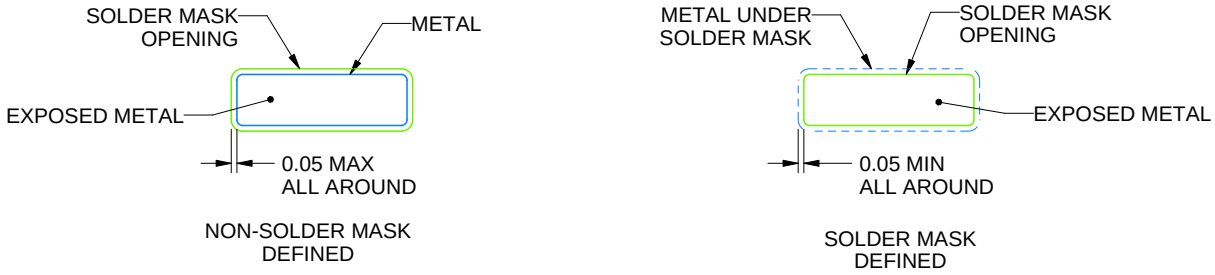
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

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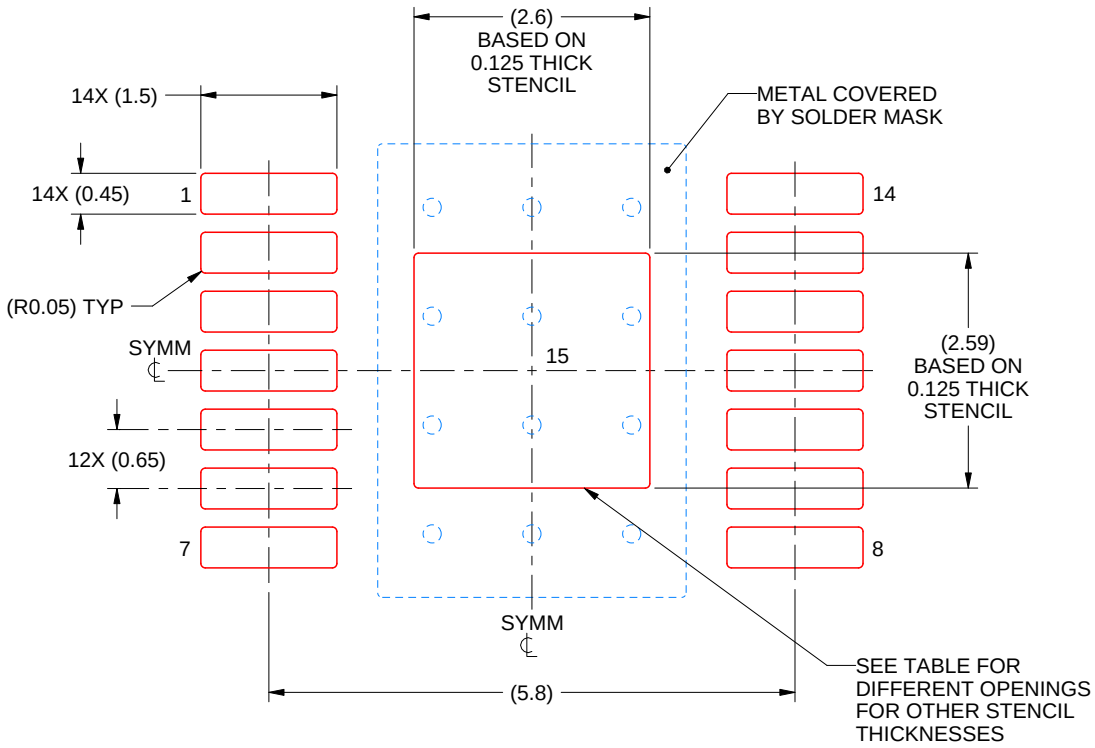
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月