参考資料

デザイン・ガイド:TIDA-060030
車載用 12V～24V エンジン負荷インターフェイスのリファレンス・デザイン

概要

このリファレンス・デザインは、ガソリンおよびディーゼル・エンジン・プラットフォームのソレノイド負荷 (例:車載用ソレノイド、双方向ブラシ付き / ブラシレス DC モータ、単方向ブラシ付き DC モータ、リレー) に接続できる独立した FET 機能を備えた 3 相ハーフ H ブリッジ・モータ・ドライブです。このリファレンス・デザインで使用している DRV8343-Q1 モータ・ドライバは、デバイスあたり最大 6 つの独立した負荷をサポートしており、あらゆるアーキテクチャの負荷出力構成に対応できます。このリファレンス・デザインは、DRV8343-Q1 の多用途性を示すために、プッシュプル構成によるソレノイド、ハイサイドおよびローサイド・ゲート・ドライバによるソレノイド、独立したハイサイドおよびローサイド負荷という 4 種類の出力を備えています。これらの負荷は、TMS320F28035 C2000 車載用高効率 32 ビット・マクロコントローラにより個別に駆動されます。

リソース

TIDA-060030	デザイン・フォルダ
DRV8343-Q1	プロダクト・フォルダ
LMR36006-Q1	プロダクト・フォルダ
TPS7B81-Q1	プロダクト・フォルダ
TMS320F28035	プロダクト・フォルダ

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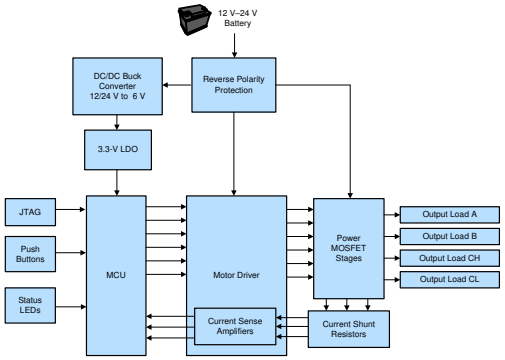
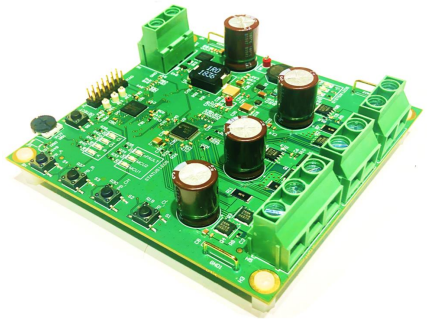
- 12V または 24V 車載システムをサポート
- 動作電圧範囲:5.5V～40V (連続)、最大 60V の過渡耐性
- ピーク電流 20A の負荷駆動能力
- 4 種類の負荷構成で最大 6 つのエンジン負荷を個別に制御
- 小さな基板サイズのソリューション (16 平方インチ未満)
- 一連の保護および診断機能
- AEC-Q100 グレード 1 認定済み

アプリケーション

- 12V および 24V 車載用モータ制御
- BLDC および BDC モータ・モジュール
- ファンと送風機
- 燃料および水ポンプ
- ソレノイド駆動
  - ガソリン・エンジン
  - ディーゼル・エンジン
  - ガソリン / ディーゼル・プラットフォーム

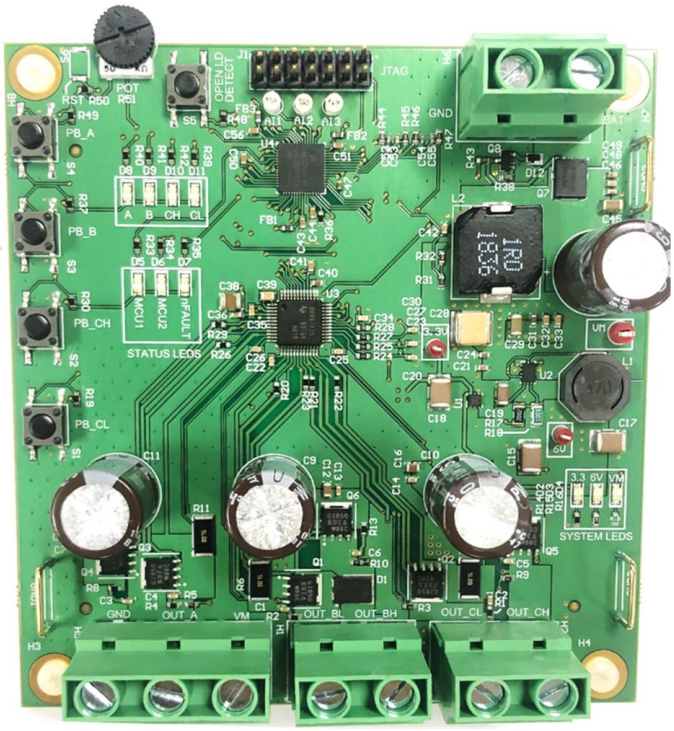




1 System Description

The TIDA-060030 is an example of a system used to drive independent loads for automotive applications such as solenoids, relays, and unidirectional BDC motors. The intent is to drive loads that are found in Engine Control Units (ECUs). Internal Combustion Engines (ICE) will be the largest market for ECUs until the emergence of Hybrid Electric Vehicles, and engine platforms can require up to as many as 60 general-purpose outputs. Some examples of possible output loads are starter relays, canister purge valves, and wastegate solenoids. These outputs are often driven thousands of times per second to maintain engine efficiency and performance. The DRV8343-Q1 device is a motor gate driver that can independently drive loads by individually driving the high-side and low-side MOSFETs, allowing up to 6 independent loads (high-side and low-side from each phase) to be driven. The TIDA-060030 is designed so that a variety of engine loads can be driven from the DRV8343-Q1: phase A drives a unidirectional BDC motor, phase B drives a solenoid with high- and low-side drivers, and phase C separates the high-side and low-side loads to drive two independent solenoids. The reference design is powered from an automotive 12-V or 24-V battery and supports a wide input voltage range of 5.5 V–40 V.

図 1. TIDA-060030 Top View



1.1 Key System Specifications

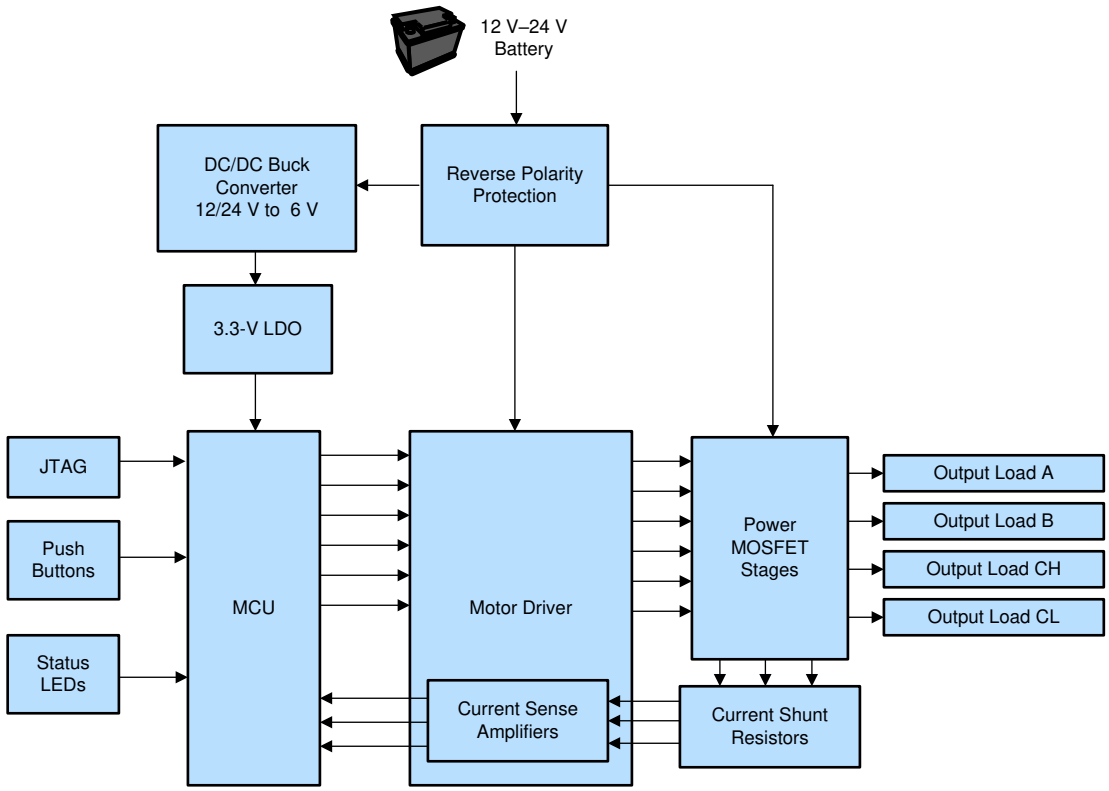
表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
System Input						
V_{IN}	Input voltage	VBAT input	5.5	12 or 24	40	V
V_{OUT}	Phase output voltage	VM	5.5	12 or 24	40	V
I_{IN}	Input current	VBAT input current	0	-	20	A
I_{OUT}	Output current	Should be less than I_{IN}	0	-	20	A
f_{PWM}	PWM frequency		15	-	50	kHz
V_{BUCK}	Buck converter output voltage	LMR36006-Q1 output voltage	-	6	-	V
I_{BUCK}	Buck output current	LMR36006-Q1 output current	-	600	-	mA
V_{LDO}	LDO output voltage	TPS7B81-Q1 output voltage	-	3.3	-	V
I_{LDO}	LDO output current	TPS7B81-Q1 output current	-	150	-	mA

2 System Overview

2.1 Block Diagram

図 2. TIDA-060030 Block Diagram



2.2 Design Considerations

This design is created with the following considerations in mind:

- Hardware demonstration of the capabilities of the DRV8343S-Q1 device to actuate engine loads using independent MOSFET mode
- 5.5-V to 40-V operating range for 12-V or 24-V automotive systems
- Components rated at least 10-A current to support typical solenoid loads
- IC components with AEC-Q100 temperature grade 1 (–40°C ≤ T_A ≤ 125°C)
- Protection circuits, diagnostics, and fault reporting
- Small size complete gate driver and MCU solution (less than 16 sq. in.)

2.3 Highlighted Products

This design uses the following TI products:

- The DRV8343-Q1 is an automotive 3-phase half-bridge gate driver with independent MOSFET control that drives loads of up to 50-V continuous and 60-V transient. In this design, the DRV8343S-Q1 device is used to communicate with the MCU using SPI. It also includes three internal Current Shunt Amplifiers (CSAs) for solenoid current measurement.
- The LMR36006-Q1 is an automotive 4.2-V to 60-V, 0.6-A synchronous step-down buck converter with

adjustable output voltage.

- The TPS7B81-Q1 is an automotive 3.3-V, 150-mA LDO that serves as input voltage for the MCU.
- The TMS320F28035 is a TI C2000 real-time high-efficiency, 32-bit CPU optimized for processing, sensing, and actuation to improve closed-loop performance. It runs up to 60 MHz and has up to 45 programmable GPIO pins, SPI modules, ePWM modules, and ADC modules that are beneficial to this reference design.

2.3.1 DRV8343S-Q1

The DRV8343S-Q1 is an independent half-bridge gate driver with dedicated source (SHx) and drain (DLx) pins to support independent MOSFET control. It supports 5.5-V to 60-V continuous input supply and is intended for 12-V or 24-V automotive systems. It is featured in the TIDA-060030 to demonstrate independent MOSFET mode and actuate up to 6 solenoid loads quickly and independently. The DRV8343S-Q1 incorporates an integrated charge pump output to drive reverse polarity detection, includes protection and diagnostic features, and is AEC-Q100 temperature Grade 1 qualified. Ideally this design is to target ECUs to control relays, valves, brushed-DC motors, and solenoids found inside of gasoline and diesel engines.

2.3.2 LMR36006-Q1

The LMR36006-Q1 is a synchronous, step-down DC/DC converter intended for automotive applications. It supports a wide input voltage range of 4.2-V to 60-V and up to 600 mA of output current, includes protection features such as thermal shutdown, input undervoltage lockout, and short-circuit protection, and is AEC-Q100 temperature Grade 1 qualified. Passive components are selected using TI's WEBENCH® Power Designer to step supply voltage down to 6-V and give extra headroom voltage to increase LDO efficiency.

2.3.3 TPS7B81-Q1

The TPS7B81-Q1 is an automotive low-dropout linear regulator with a wide input voltage range of 3-V to 40-V and maximum output current of 150 mA. It steps the 6-V input voltage into a fixed 3.3-V output voltage for the TMS320F28035 C2000 MCU. It includes integrated fault protections such as thermal shutdown, short-circuit, and overcurrent protection. It is also AEC-Q100 temperature Grade 1 qualified.

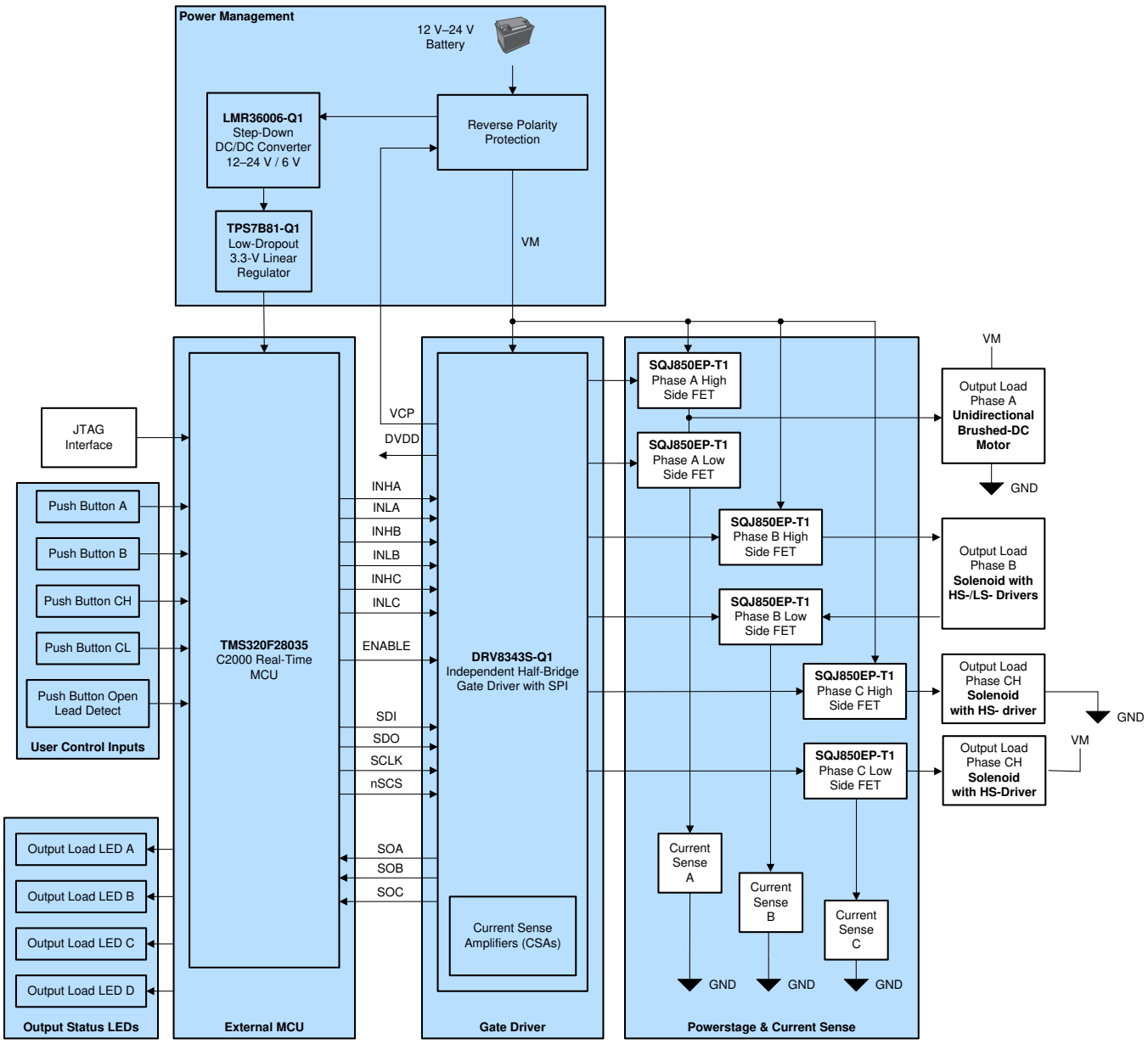
2.3.4 TMS320F28035

The TMS320F28035 is a high-efficiency 32-bit CPU that is part of TI's C2000 family. It comes in a 56-pin RSH VQFN package and is AEC-Q100 temperature Grade 1 qualified for automotive applications. The TMS320F28035 requires a single 3.3-V supply powered from the LDO and has up to 45 individually programmable, multiplexed GPIO pins. It supports control peripherals such as ePWM, ADC, an on-chip temperature sensor, and comparators suitable for motor drive applications. It also incorporates serial port communication peripherals, including:

- One Serial Communications Interface (SCI) Universal Asynchronous Receiver, and Transmitter (UART) Module
- Two Serial Peripheral Interface (SPI) Modules
- One Inter-Integrated-Circuit (I2C) Module
- One Local Interconnect Network (LIN) Module
- One Enhanced Controller Area Network (eCAN) Module

2.4 System Design Theory

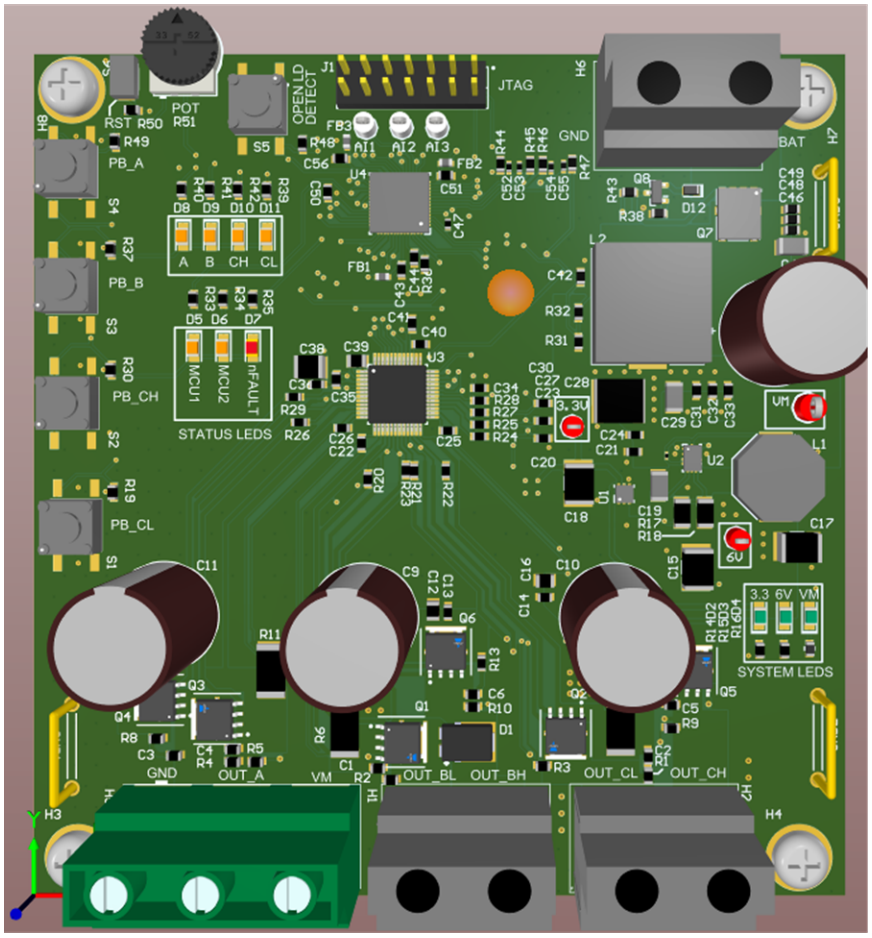
図 3. TIDA-060030 Detailed Block Diagram



2.4.1 Printed Circuit Board (PCB) and Form Factor

- Compatible with C2000 MCU, programmable with JTAG interface
- Optimized size for potential in-application use
- Sufficient size for high current and thermal dissipation
- Organized layout to demonstrate PCB flow

図 4. TIDA-060030 PCB Render



2.4.2 Overall Considerations for Component Selection

Components selected are based on the performance requirements of the expected applications. The main priority for component selection is automotive qualification using AEC-Q100 active components, AEC-Q101 discrete components, and AEC-Q200 passive components.

Capacitors are X7R grade (−55°C to +125°C) or higher, with size and value selected for the expected extremes of operation conditions. The voltage rating of the capacitors should be greater than the maximum voltage they could experience, and 2 × the typical operating voltage to avoid DC bias effects. The amount of output capacitance used depends on output ripple and transient response requirements, and many equations and tools are available online to help estimate these values.

For improved accuracy, feedback resistor dividers should use components with 1% or better tolerance. Resistance tolerance in this design was selected to reduce the total amount of BOM line items. In the design considerations, it is noted where 5% or 10% precision resistors can be used to reduce the cost of a specific individual resistor. Using less precise resistors for cost reasons should be weighed against reducing the amount of BOM line items and ordering in higher volumes to reduce total BOM cost.

Zero-Ohm (0-Ω) resistors are used at the input and output of several of the circuit sections for testing purposes only, and could be removed, if needed, in a production board design.

2.5 Power Management

2.5.1 VBAT Input Protection and Pi Filter

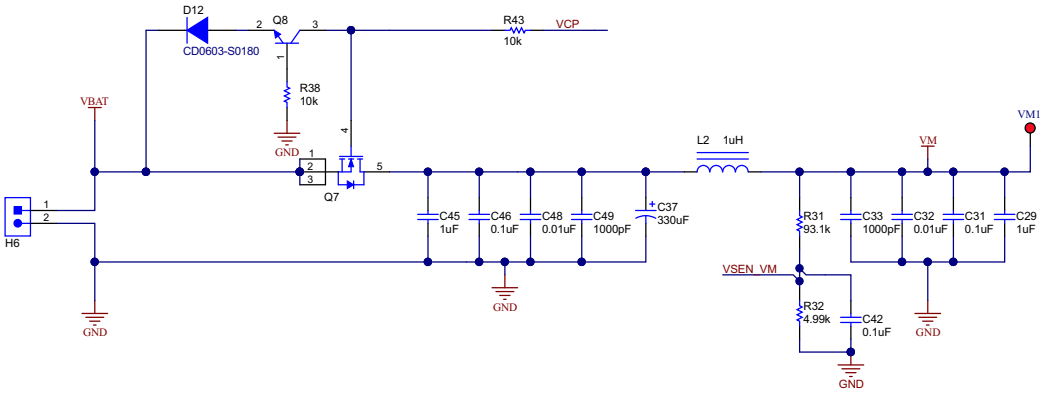
Reverse battery protection is required in nearly every electronic subsystem of a vehicle, both by OEM standards, as well as ISO 16750-2, an international standard pertaining to supply quality.

This implementation uses a power NMOS and an NPN bipolar junction transistor (BJT) to achieve reverse battery protection. If the battery is connected in reverse, the body diode of the NMOS will not conduct current nor turn the NMOS on, thereby protecting the system from the reverse polarity condition. When the battery is connected correctly, the circuit permits current to flow with very little power lost because of the low $R_{DS(on)}$ of the NMOS.

This technique is particularly well-suited for motor drive applications. The DRV8343S-Q1 includes integrated charge pump devices, which can support the required overdrive voltage for the NMOS gate without the need for additional external circuitry. For more background information on reverse polarity protection, see the Protecting automotive motor-drive systems from reverse polarity conditions application report.

After passing the reverse polarity circuit, the power supply uses a set of capacitors and inductors to form a “pi” filter. This removes unwanted AC components on the supply line. Due to the bidirectional format of the pi filter, incoming transients are blocked from entering the board, and any switching noise or clock noise generated on the board is blocked from propagating into the rest of the voltage.

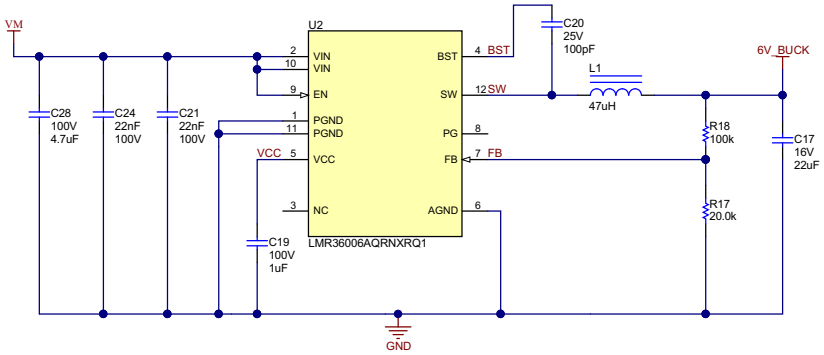
図 5. Reverse Polarity Protection for VBAT and Pi Filter



2.5.2 Buck Converter

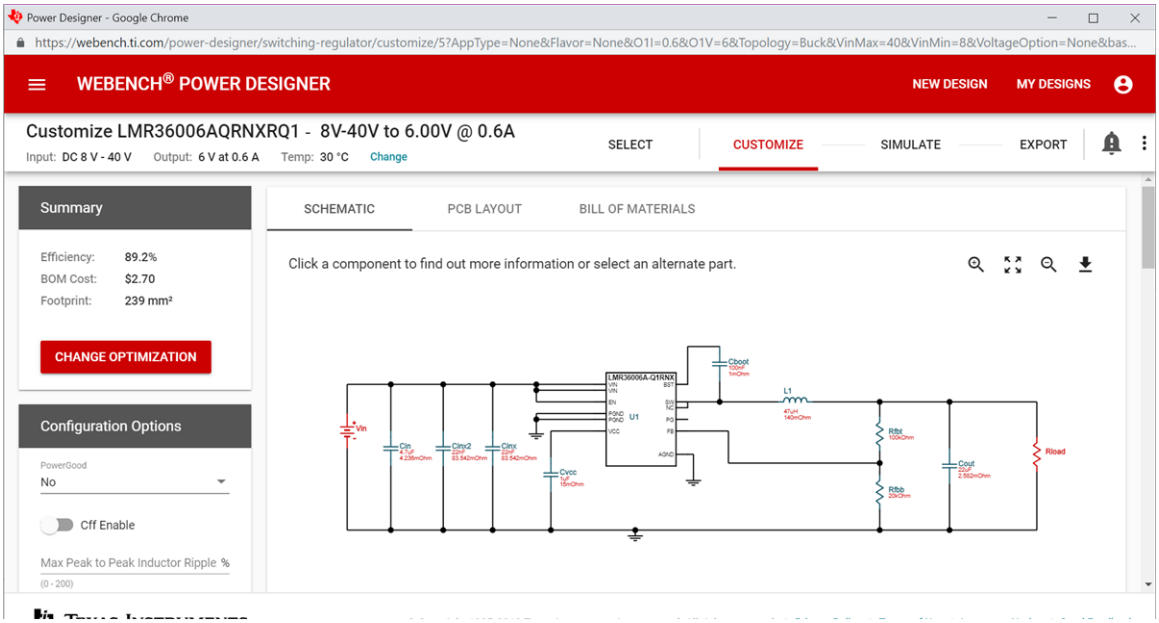
The TIDA-060030 uses an LMR36006-Q1 synchronous, step-down buck converter to step down the input supply voltage to a 6-V signal. This buck converter is designed for automotive applications and is AEC-Q100 temperate Grade 1 qualified. After stepping down the input supply voltage, that signal is input into the LDO stage to provide high efficiency and minimal power losses.

図 6. LMR36006-Q1 Automotive Buck Converter to Step 24-V Down to 6-V



For buck external component selection, Texas Instruments' WEBENCH® Power Designer specifies the correct values based on user input specifications. The tool is found on the LMR36006-Q1 product page on TI.com. A WEBENCH simulation was run for the maximum input voltage the tool allowed (8 V–40 V), 0.6-A max current, and ambient temperature.

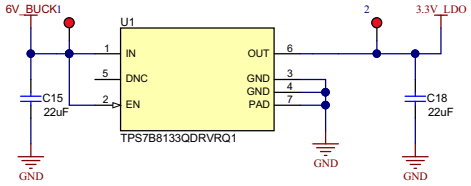
図 7. WEBENCH® Power Designer Tool for LMR36006-Q1



2.5.3 3.3-V Linear Dropout Regulator

The 6-V signal is fed into the TPS7B81-Q1 to provide the 3.3-V supply needed to bias the TMS320F28035 MCU and logic-level components. The TPS7B81-Q1 is a small, efficient solution intended for automotive applications. It has a maximum output current of 150 mA and operates over a wide junction temperature range of –40°C to 150°C. It also has low quiescent current I_Q of 300 nA to conserve energy and extend battery lifetime. TI recommends using a low-equivalent series resistance (ESR) ceramic capacitor with an X5R- or X7R-type dielectric. In the TIDA-060030, 22-µF ceramic capacitors are used for the input and output to counteract reactive input sources and improve transient response, input ripple rejection, and PSRR.

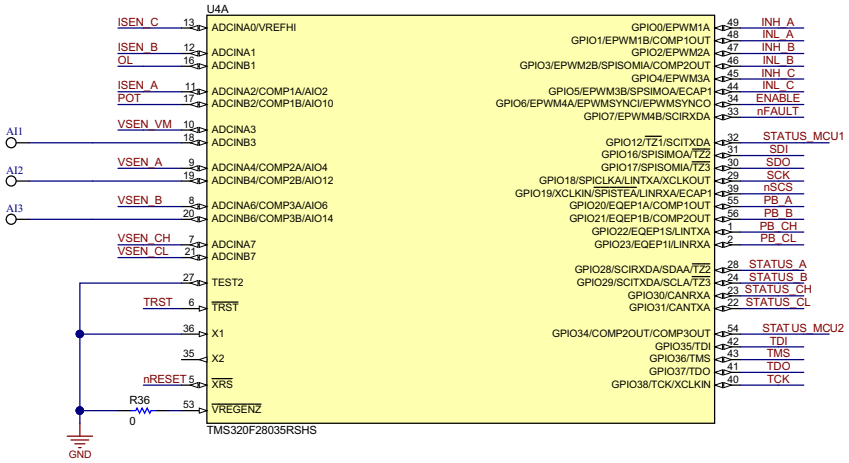
図 8. TPS7B81-Q1 3.3-V Automotive LDO



2.6 Microcontroller

The TMS320F28035 serves as the external MCU for the TIDA-060030 design to receive pushbutton inputs, send input signals to the gate driver, set fault configurations, diagnose faults, and calculate voltage and current feedback from the phase nodes. An SPI is used to set configurations and receive fault diagnostics with the DRV8343S-Q1. ePWM modules are used to receive control signals from the pushbutton inputs, and general purpose I/O pins send the logic-level signals to the motor driver and status LEDs. The ADC modules convert voltages from the phase nodes and SOx pins to respectively translate voltages and currents from the system.

図 9. TMS320F28035 Automotive C2000 Microcontroller



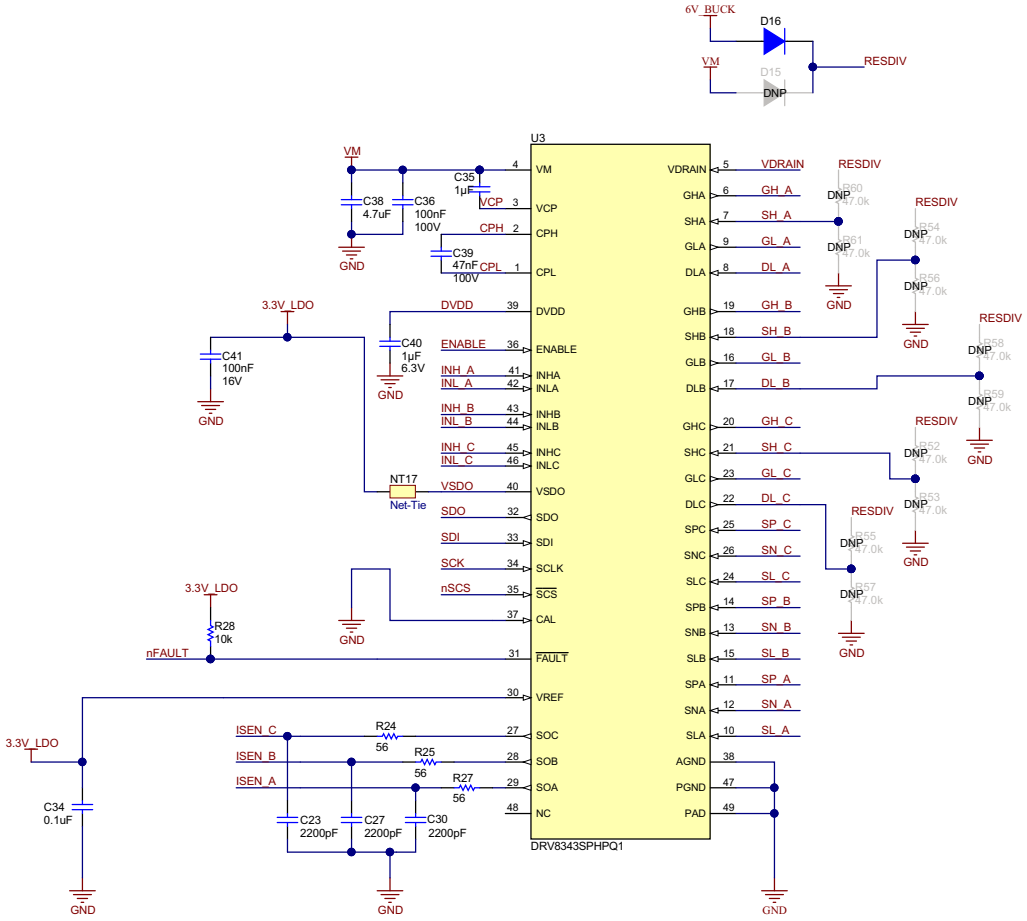
2.7 Motor Driver

The DRV8343S-Q1 is an SPI-configurable motor driver that can drive independent loads using independent MOSFET mode. The device has dedicated source (SHx), drain (DLx), and gate driver pins (GHx/GLx) that can independently drive a variety of output loads such as unidirectional BDC motors, solenoids, BDC motors, or 3-phase BLDC motors. Unlike other 3-phase gate drivers, the DRV8343x-Q1 device includes dedicated drain pins (DLx) that supports independent solenoid drive.

In the TIDA-060030 design, the system is designed to drive four distinct outputs to show device capability. Phase A drives a unidirectional BDC motor by connecting one output to phase A and connecting the other motor output to VM or GND, depending on the direction of the motor. Phase B drives a solenoid using both high-side and low-side FETs for added protection such as short-to-battery or short-to-ground detection. Phase C separates the high-side and low-side FETs to drive two separate solenoid loads, CH and CL. The DRV8343S-Q1 device also includes a charge pump output used to drive the reverse polarity protection MOSFET.

To control the driver outputs, the DRV8343S-Q1 uses SPI bits PWM_MODE to support various system configuration of output loads. The TIDA-060030 design uses independent half bridges for phases A and B and independent MOSFET mode for phase C (100b in PWM_MODE) to control the four output loads. For more information of the register map and fault information, see the *DRV8343-Q1 12-V / 24-V Automotive Gate Driver Unit (GDU) with Independent Half Bridge Control and Three Integrated Current Sense Amplifiers Data Sheet*.

図 10. DRV8343S-Q1 Independent Half-Bridge Gate Driver



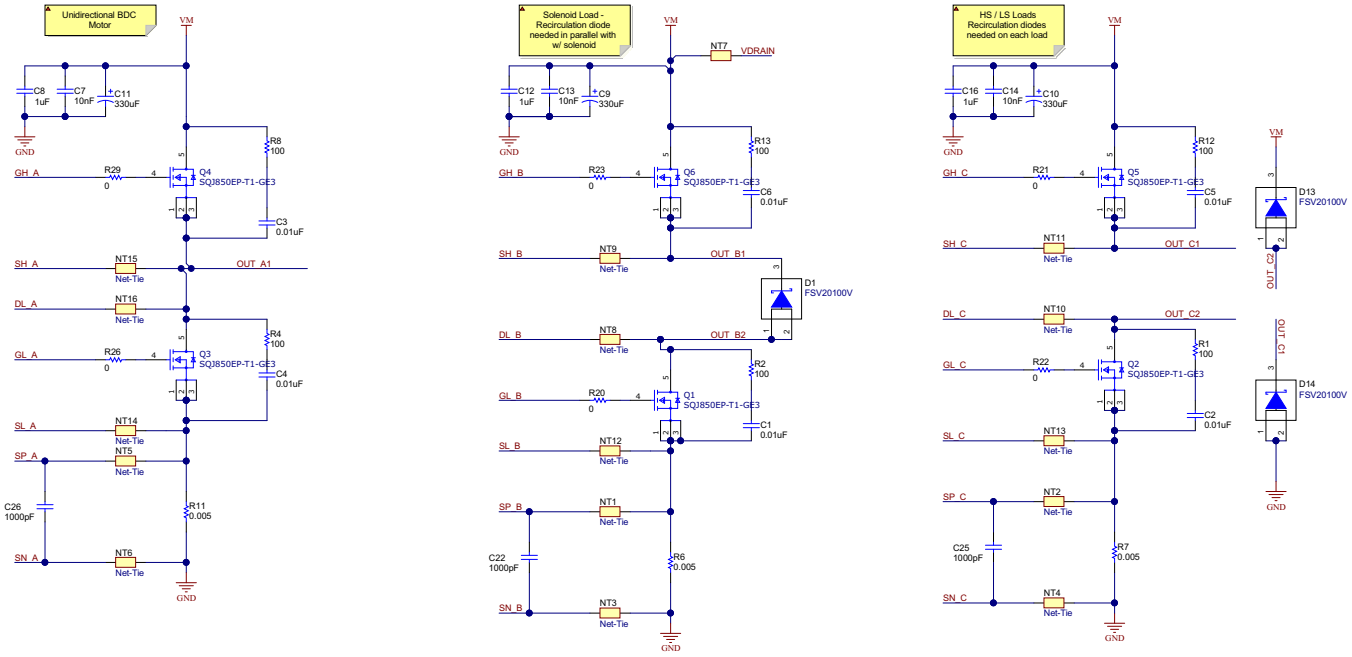
2.8 Power MOSFETs and Output Stage

External Vishay SQJ850EP power MOSFETs and Fairchild FSV20100V recirculation diodes are used for the power output stage. The external MOSFETs are rated for 60-V absolute maximum and peak current of 24-A. For phases B, C high-side, and C low-side, recirculation diodes are implemented to recirculate and dissipate current through the solenoid load when FETs are turned off. The recirculation diodes are rated for 20-A, 100-V as extra headroom for any transient voltages in the system.

The output stage is designed for four different load configurations. Phase A uses both the high-side and low-side driver in a push-pull configuration for the load. One end is connected to the half-bridge and the other end is connected to VM or GND to recirculate current. This configuration provides short-to-battery or short-to-ground detection and is suited for high-speed operations. Phase B uses the high-side and low-side driver in an half-bridge configuration. This allows for both short-to-battery and short-to-ground protection but requires a recirculation diode in the scenario that both drivers are turned off. Phase C splits the half-bridge into a high-side and low-side driver to drive two solenoid loads. Each driver requires a recirculation diode and provides limited protection when driven independently.

To explain how loads are connected to each output phase, see 3.1.1.3.

図 11. TIDA-060030 Power Stage for Phases A, B, C High-Side, and C Low-Side



2.9 Current Feedback

External shunt resistors are used to measure the current going through the phase node. The SPx and SNx pins measure the high- and low-side voltages of the resistor. Those voltages are fed to the Current Sense Amplifiers (CSAs) integrated in the DRV8343S-Q1 to calculate the sense current of that phase through the shunt resistor. That current is sent as a voltage through its respective SOx pin back to the TMS320F28035 device, which is read by an ADC pin.

Because the large currents in the power stage flow through the sense resistor, the selected resistor value must be small to keep the power dissipation at a minimum. For high current systems, the resistor value is usually in mΩ. In the TIDA-060030 design, up to 20 A of current can sink through the 5-mΩ sense resistor R11. This dissipates 2 W of power through that resistor. Increasing the resistor value can improve the signal-to-noise ratio but will also increase the power dissipation.

One important factor to consider is that current cannot be measured through the high-side FET of phase C. This is because shunt resistors need to be placed near ground, and CH does not have any connections to ground.

図 12. Current Sense Voltages From the SOx Pins of the DRV8343-Q1 to the MCU

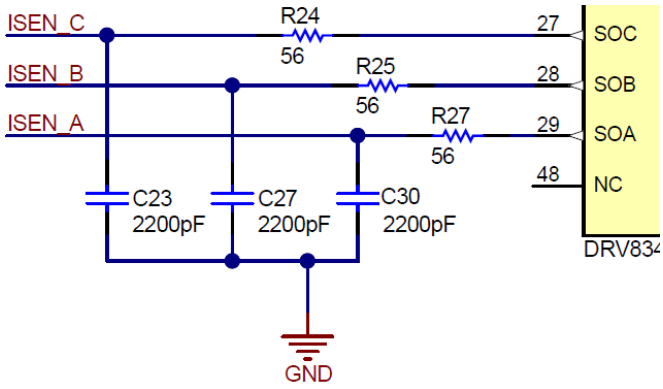
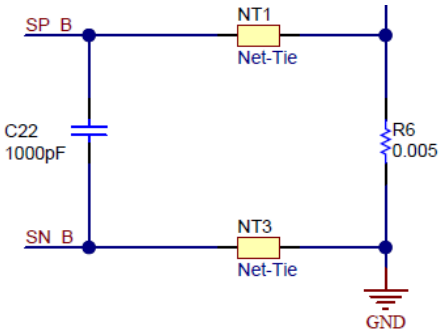


図 13. Voltages SPx and SNx Across the Current Shunt Resistor are fed to the Internal Current Sense Amplifier (CSA)

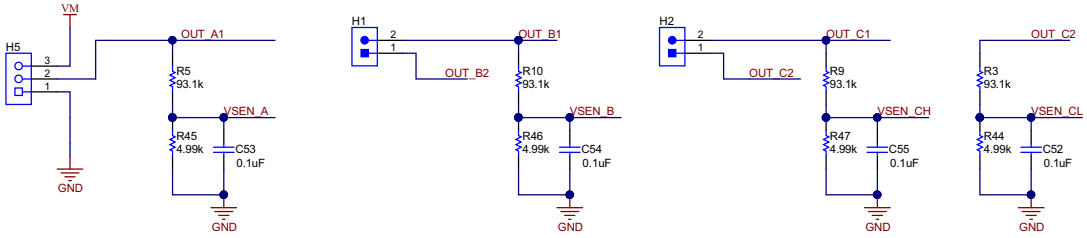


2.10 Voltage Feedback

A resistor divider is used to step down the output and supply voltages to logic-level voltages read by the ADC module of the TMS320F28035. The same voltage divider circuit is used on all output loads: phase A, B, C high-side, and C low-side. In the TIDA-060030, the resistor values used for the voltage divider are 93.1 kΩ for the high resistor and 4.99 kΩ for the low resistor. These values are specifically chosen to step down a full-load output voltage signal to a full-scale ADC logic-level signal.

It is imperative that these resistors are precise with 1% or better tolerance to obtain accurate measurements of feedback voltage.

図 14. Voltage Feedback for VM, Phase A, Phase B, Phase CH, and Phase CL



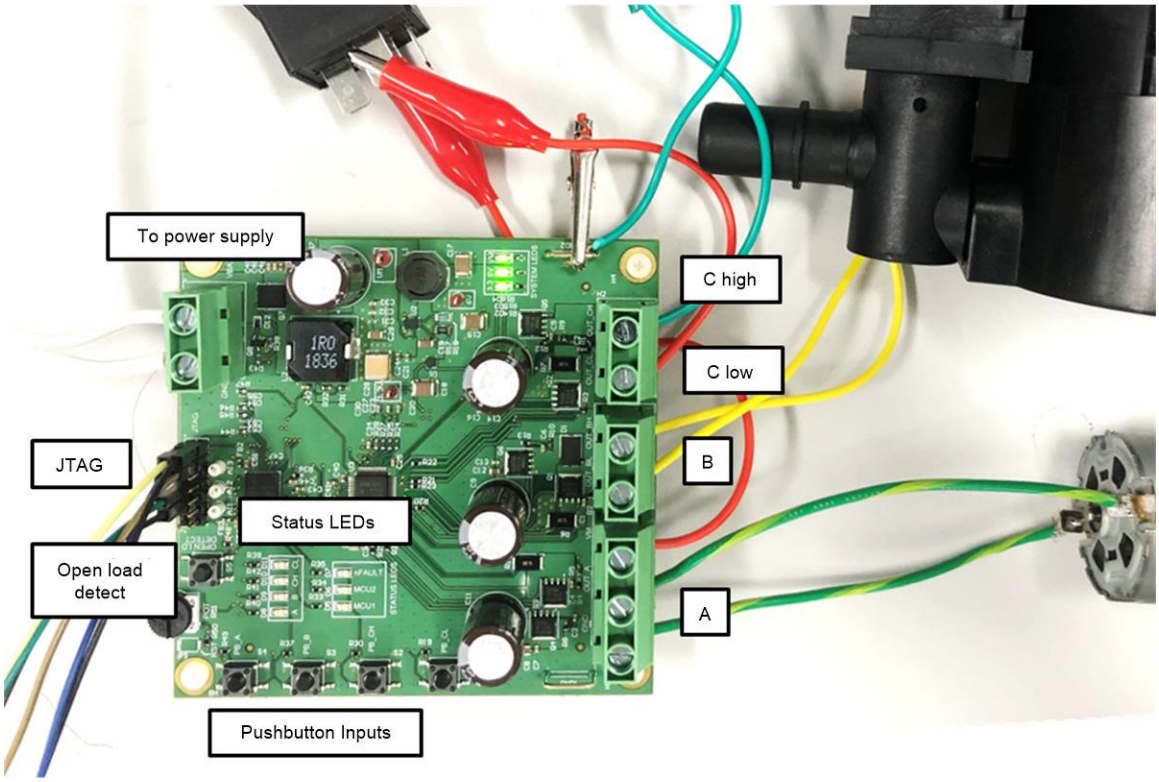
3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

To demonstrate the TIDA-060030 design, the following materials are used:

- TIDA-060030 reference design
- XDS110 JTAG Debug Probeon F280049 LaunchPad™
- Automotive 12-V or 24-V solenoid loads, such as:
  - Starter relay
  - Throttle control
  - EGR valve
  - Fuel pump relay
- 12-V or 24-V power supply or battery
- TIDA-060030 software on *Code Composer Studio*



3.1.1.1 Install JTAG Connections

Connect the XDS110 JTAG cable to header J1 (14-pin JTAG connector) at the top of the board.

3.1.1.2 Power Connections

Connect the 12-V or 24-V power supply or battery to the 2-pin screw terminal header H6 at the top of the board. The positive of the supply connects to VBAT and the negative of the supply connects to GND.

3.1.1.3 Load Connections

For phase A, connect a solenoid or brushed-DC motor to H5 (3-pin header) in the following manner:

- Connect the positive or high-side terminal of the motor to the OUT_A screw terminal
- Connect the negative or low-side terminal of the motor to the GND or VM screw terminal, depending on the push-pull configuration of the solenoid or direction of the brushed-DC motor

For Phase B, connect a solenoid to H1 (2-pin header) to the OUT_BH and OUT_BL screw terminals.

For phase C, connect a solenoid load using one of the following high- or low-side drivers:

- C high-side: Connect one end of the solenoid to the OUT_CH screw terminal, and the other end of the solenoid to GND
- C low-side: Connect one end of the solenoid to VM and connect the other end of the solenoid to the OUT_CL screw terminal.

3.1.2 Software

3.1.2.1 Download and Install Code Composer Studio™

Code Composer Studio is an integrated development environment (IDE) for Texas Instruments (TI) embedded processor families. *Code Composer Studio* comprises a suite of tools used to develop and debug embedded applications. It includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before and add functionality to their application thanks to sophisticated productivity tools. See the Code Composer Studio web page at for information on downloading the integrated development environment for the C2000 code.

Software examples for SPI communication, ePWM peripheral setup, I/O setup, ADC module setup, and more are found in C2000Ware to minimize development time. It includes device-specific drivers, libraries, and peripheral examples for the TMS320F28035.

3.2 Testing and Results

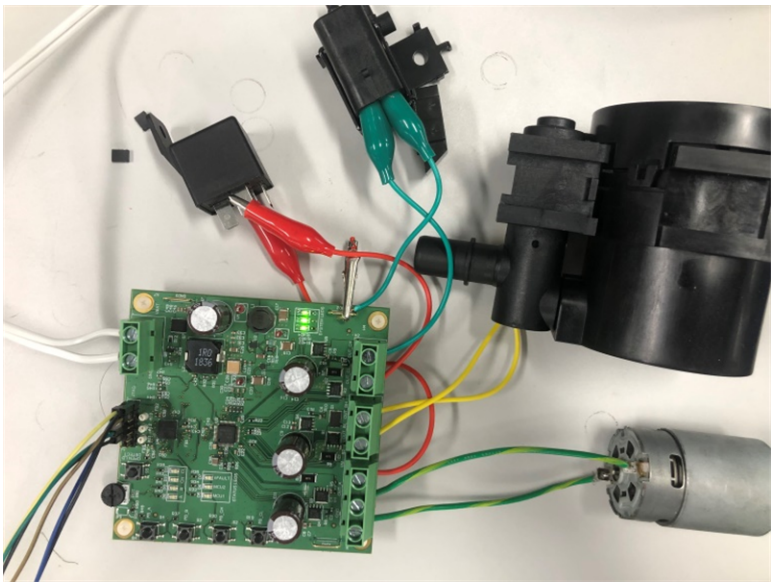
3.2.1 Test Setup

In the following test setup, the four output loads connected to phases A, B, C high-side, and C low-side are a brushed-DC motor, canister purge valve, wastegate solenoid, and fuel pump relay. All of these solenoids are rated for 12-V and are typically found as driver outputs in a 12-V gasoline or diesel engine system.

Specifically, the Brushed-DC motor is connected to OUT_A and VM, the canister purge valve connected to OUT_BH and OUT_BL, wastegate solenoid connected to OUT_CH and GND, and fuel pump relay connected to OUT_CL and VM. When their respective push button is pressed down, each output load will actuate independently and its corresponding LED will light up in the "Status LEDs" section of the PCB.

図 15 is an illustration of the TIDA-060030 test setup with a brushed-DC motor connected to OUT_A and VM, canister purge valve connected to OUT_BH and OUT_BL, wastegate solenoid connected to OUT_CH and GND, and fuel pump relay connected to OUT_CL and VM.

図 15. TIDA-060030 Test Setup



3.2.2 Test Results

3.2.2.1 Solenoid Operation

When the TIDA-060030 is powered through VBAT and launched with software, the solenoid loads connected to OUT_A, OUT_B, OUT_CH, and OUT_CL can be controlled with pushbuttons OUT_A, OUT_B, OUT_CH, and OUT_CL. LEDs D8–D11 (labeled A, B, CH, and CL) will also light up when buttons are pressed.

The oscilloscope screenshot in 図 16 shows the output of PB_A and OUT_A once pushbutton A is pressed.

図 16. Plot of PB_A and OUT_A (Brushed-DC Motor)

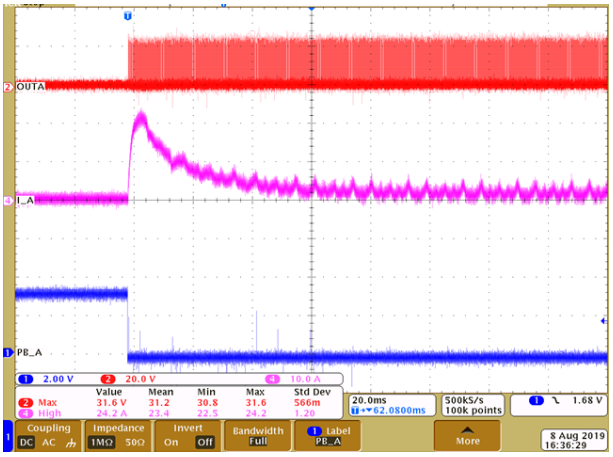
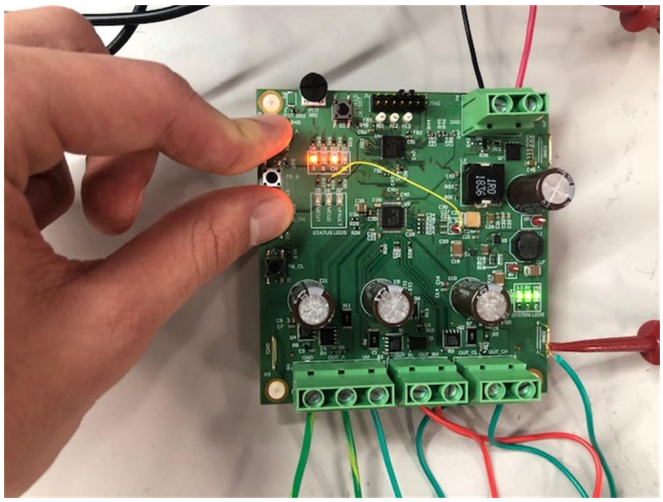


図 17. LED for Phase A is on When PB_A is Pressed (Brushed-DC Motor)



3.2.2.2 Power Supplies

Each solenoid load can be controlled independently and simultaneously, resulting in a summation of output currents for each phase. 表 2 shows the progression of output current summation by driving output loads A, B, C, and CH on top of each other and driving with fixed duty cycles for each phase.

表 2. TIDA-060030 Output Load Current Summation Testing

OUTPUT PHASES	LOAD	TOTAL OUTPUT CURRENT (A)
A	Brushed-DC motor	0.214
CL	12-V fuel pump relay	0.121
B	12-V canister purge valve	0.363
CH	12-V waste gate solenoid	0.169
A + B	Brushed-DC motor, 12-V fuel pump relay	0.341
A + B + CH	Brushed-DC motor, 12-V fuel pump relay, 12-V canister purge valve	0.710
A + B + CH + CL	Brushed-DC motor, 12-V fuel pump relay, 12-V canister purge valve, 12-V waste gate solenoid	0.878

3.2.2.3 Diagnostics and Protection

If a fault is generated during device operation, the nFAULT red LED will turn on as well as set the bit of the generated fault. 表 3 lists the register map corresponding to the FAULT Status Register. Each fault bit can be read directly from the "Expressions" window during run-time on Code Composer Studio by address of the fault bit according to the register map.

表 3. SPI Register Map for Faults and Diagnostics of DRV8343S-Q1

REGISTER NAME	7	6	5	4	3	2	1	0	Address
FAULT Status	FAULT	GDF	CPUV	UVLO	OCP	OTW	OTSD	OL_SHT	0x00
DIAG Status A	SA_OC	SHT_GND_A	SHT_BAT_A	OL_PH_A	VGS_LA	VGS_HA	VDS_LA	VDS_HA	0x01

表 3. SPI Register Map for Faults and Diagnostics of DRV8343S-Q1 (continued)

REGISTER NAME	7	6	5	4	3	2	1	0	Address
DIAG Status B	SB_OC	SHT_GND_B	SHT_BAT_B	OL_PH_B	VGS_LB	VGS_HB	VDS_LB	VDS_HB	0x02
DIAG Status C	SC_OC	SHT_GND_C	SHT_BAT_C	OL_PH_C	VGS_LC	VGS_HC	VDS_LC	VDS_HC	0x03

An Open Load Passive (OLP) detection test is initiated by pressing the "Open Load Detect" pushbutton. Software is programmed to run an OLP test by writing a "1" to the EN_OLP bit in address 0x05. If an open load is detected on a phase, the nFAULT LED will light up and the correct fault can be read by reading the DIAG Status A, DIAG Status B, or DIAG Status C registers. Likewise, a short-to-battery or short-to-ground test is initiated by writing a "1" to the EN_SHT_TST bit in address 0x05. If an short-to-battery or short-to-ground is detected on a phase, the nFAULT LED will light up and the correct fault can be read by reading the DIAG Status A, DIAG Status B, or DIAG Status C registers.

Many other faults such as gate driver faults (GDF), overcurrent protection (OCP), undervoltage (UVLO), and overtemperature (OTW / OTSD) can be monitored through SPI configuration. For more information of the SPI register map and fault information, see the *DRV8343-Q1 12-V / 24-V Automotive Gate Driver Unit (GDU) with Independent Half Bridge Control and Three Integrated Current Sense Amplifiers Data Sheet*.

表 4 shows the protection features and diagnostics tested on the TIDA-060030 design.

表 4. TIDA-060030 Protection Features and Diagnostics Responses

DIAGNOSTIC	TEST CONDITIONS	VM (V)	RESPONSE
Undervoltage	-	< 6	UVLO = 1, nFAULT on
Open load on phase A	Phase A disconnected	12	OL_PH_A = 1, OL_SHT = 1, nFAULT on
		24	
Open load on phase B	Phase B disconnected	12	OL_PH_B = 1, OL_SHT = 1, nFAULT on
		24	
Open load on phase C	Phase C disconnected	12	OL_PH_C = 1, OL_SHT = 1, nFAULT on
		24	
Short to ground on phase A	OUT_A connected to GND	12	SHT_GND_A = 1, OL_SHT = 1, nFAULT on
		24	
Short to ground on phase B	OUT_B connected to GND	12	SHT_GND_B = 1, OL_SHT = 1, nFAULT on
		24	
Short to ground on phase C	OUT_C connected to GND	12	SHT_GND_C = 1, OL_SHT = 1, nFAULT on
		24	
Short to battery on phase A	OUT_A connected to VM	12	SHT_BAT_A = 1, OL_SHT = 1, nFAULT on
		24	
Short to battery on phase B	OUT_B connected to VM	12	SHT_BAT_B = 1, OL_SHT = 1, nFAULT on
		24	
Short to battery on phase C	OUT_C connected to VM	12	SHT_BAT_C = 1, OL_SHT = 1, nFAULT on
		24	

4 Design Files

4.1 Altium Files

To download the Altium Designer® project files, see the design files at TIDA-060030.

4.1.1 Schematics

To download the schematics, see the design files at TIDA-060030.

4.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-060030.

4.1.3 PCB Layout Recommendations

The PCB design of motor drive systems is non-trivial and requires special considerations and techniques to achieve the best performance. Power efficiency, high-speed switching frequency, low-noise jitter, and compact board design are a few primary factors that designers must consider when laying out a motor drive system. Texas Instruments' DRV devices are ideal for such type of systems because they are highly integrated and well-equipped with protection circuitry. A major goal of this layout is to highlight the primary factors of a motor drive layout when using a DRV device and provide a best practice guideline for a high-performance solution that reduces thermal stress, optimizes efficiency, and minimizes noise in a motor drive application. The TIDA-060030 is a 4-layer board with TOP, POWER, GND, BOTTOM layers.

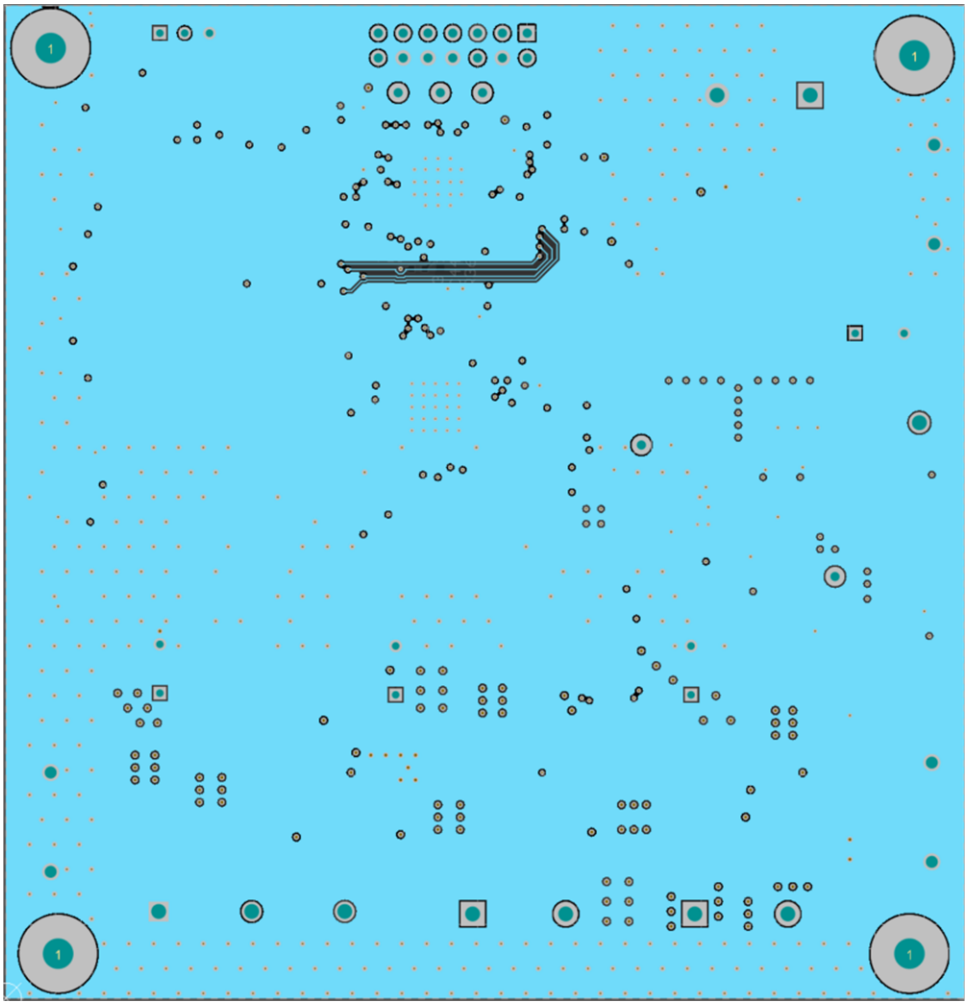
4.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-060030.

4.1.3.2 Grounding Optimization

A ground plane is used to provide a strong ground return path. Having a continuous ground plane allows signals to have the shortest return path and decrease coupling and interference. It is imperative to minimize ground discontinuity by carefully routing traces and placing vias in such a manner that it does not cause breaks on the GND plane.

図 18. GND Plane of TIDA-060030



4.1.3.3 Thermal Overview

A thermal pad allows for efficient heat dissipation over a larger area away from important signals and components. The thermal pad should be directly underneath any devices that build up large amounts of heat, current, or both. In the TIDA-060030 design, vias are placed on the thermal pads of the following devices:

- DRV8343S-Q1
- Vishay external FETs
- TMS320F28035

図 19. Vias Placed on Thermal Pads on Power MOSFETs

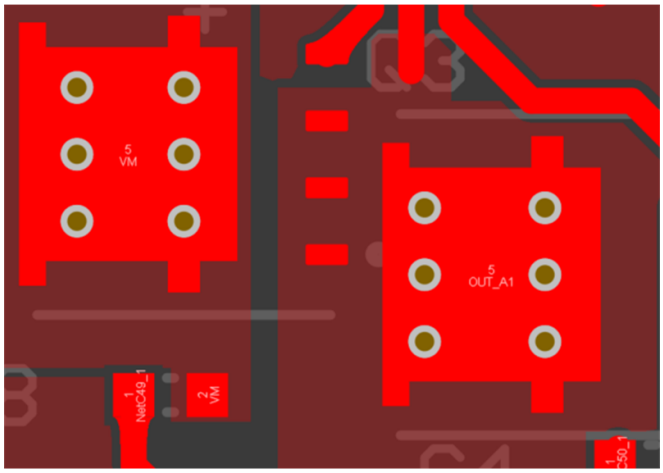
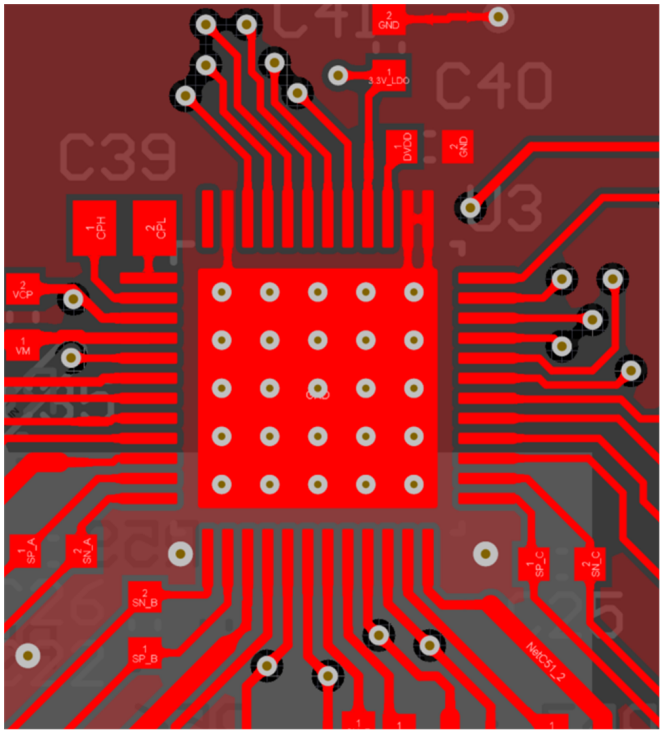
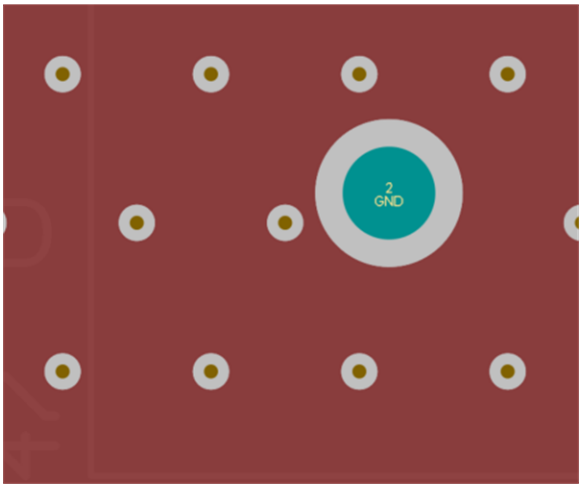


図 20. Vias Placed on Thermal Pads on DRV8343S-Q1



Another good technique to implement in order to dissipate heat to all layers of the board is thermal vias to ground. Thermal relief connections should not be used for the thermal vias because the path for heat to flow from the top plane through the via to the bottom plane is constricted. This constricted path for heat flow results in an increased temperature on the remaining part of the top plane around the via. Directly connecting vias allows for the lowest possible thermal resistance between the via and copper layers. The thermal vias should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole. Do not cover the vias with solder mask which causes excessive voiding.

図 21. Thermal Vias Stitched on the GND Plane



4.1.3.4 Vias

Vias are holes in a PCB that are electrically connected together. Many vias are used in TIDA-060030 to connect power and ground layers to signal layers (power tracks), or to transfer the signal to the top or bottom layer to allow continuity (signal tracks). There are also multi-vias, or “via stitching”, that is added to the GND pour of the top layer to electrically connect to the GND layer of the board. This allows for low impedance connections that maintain short current paths to ground and dissipate heat.

表 5 lists the current capacity for different via diameters per IPC-2152 standards.

表 5. Via Current Capacity

VIA DIAMETER	CURRENT CAPACITY
6 mil	0.2 A
8 mil	0.55 A
10 mil	0.81 A
12 mil	0.84 A
16 mil	1.1 A

図 22. Vias Used to Dissipate Current From Bulk VM Capacitor to VM Plane of Power Layer

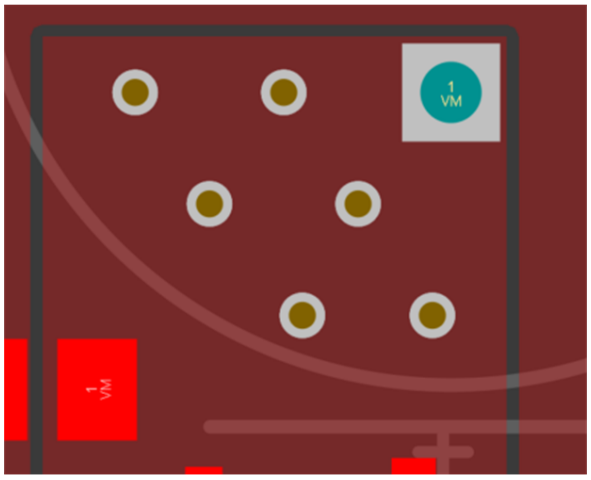
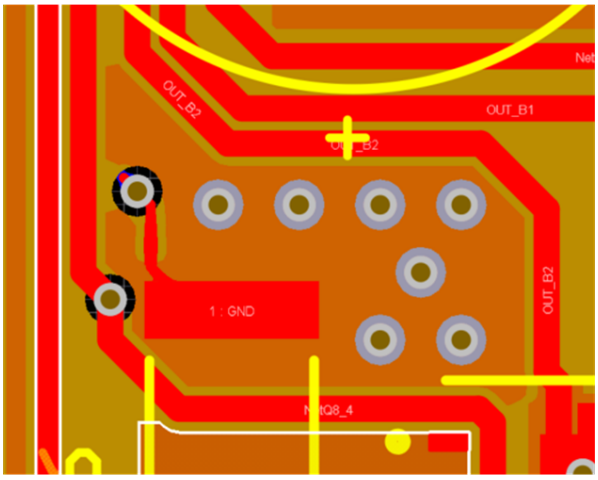


図 23. Vias Used to Dissipate Current Through Shunt Resistor to GND Layer

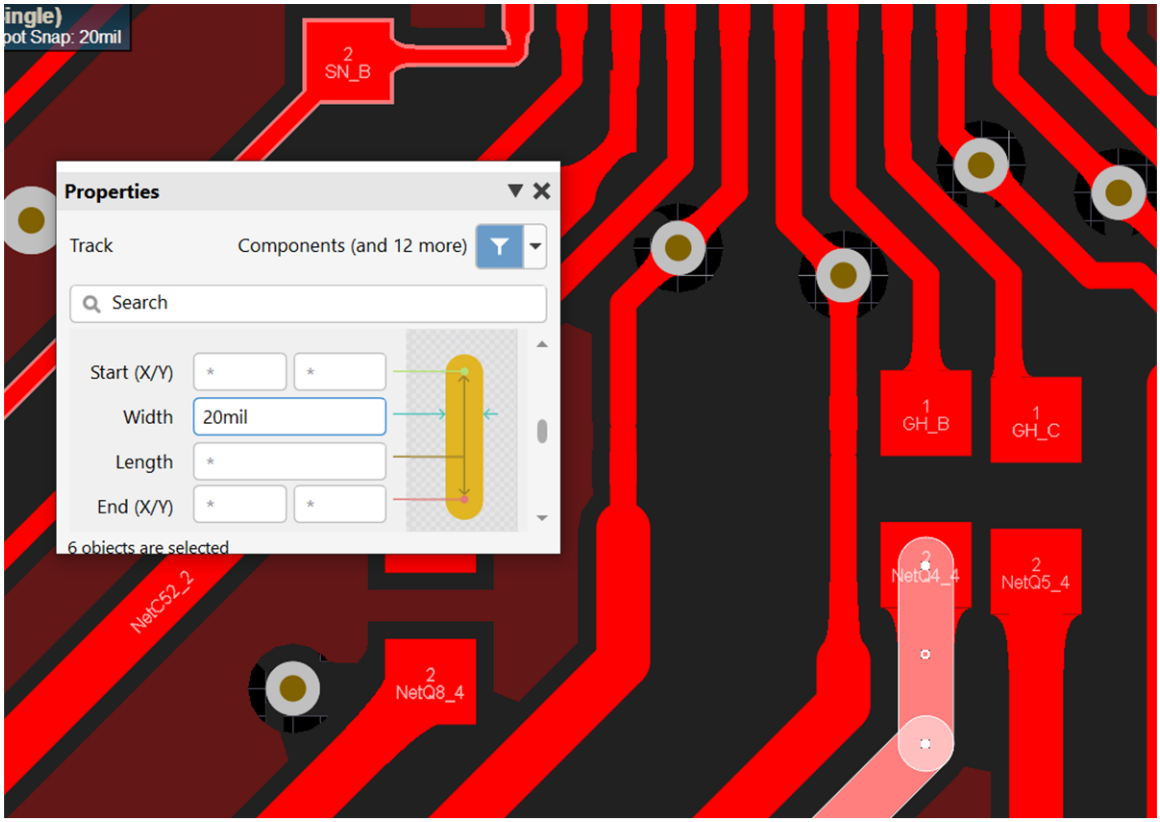


4.1.3.5 General Routing Techniques

Typically, PCBs utilize extensive routing techniques for logic level, low-current designs and applications. In the TIDA-060030, currents of up to 20 A can be driven to drive various automotive loads for engine management, therefore, wider traces need to be implemented to effective circulate current.

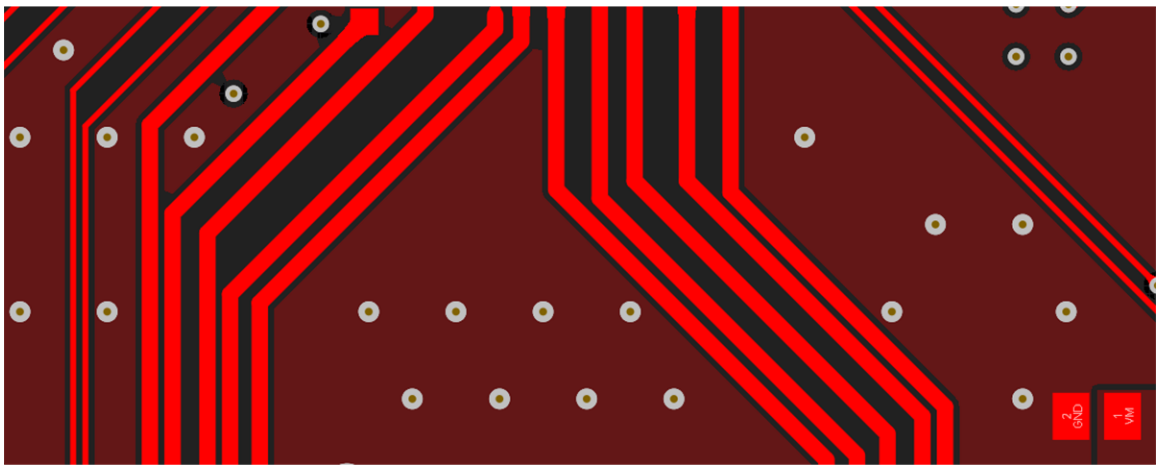
- Make gate drive, source high, and drain low traces wide and as short in length as possible. Start with a trace width of 20 mils for at least 1 oz of copper, more if required by high currents.

図 24. NetQ4_4, Which is Tied to GH_B by a 0-Ω Resistor, has a Width of 20 Mils After the Resistor



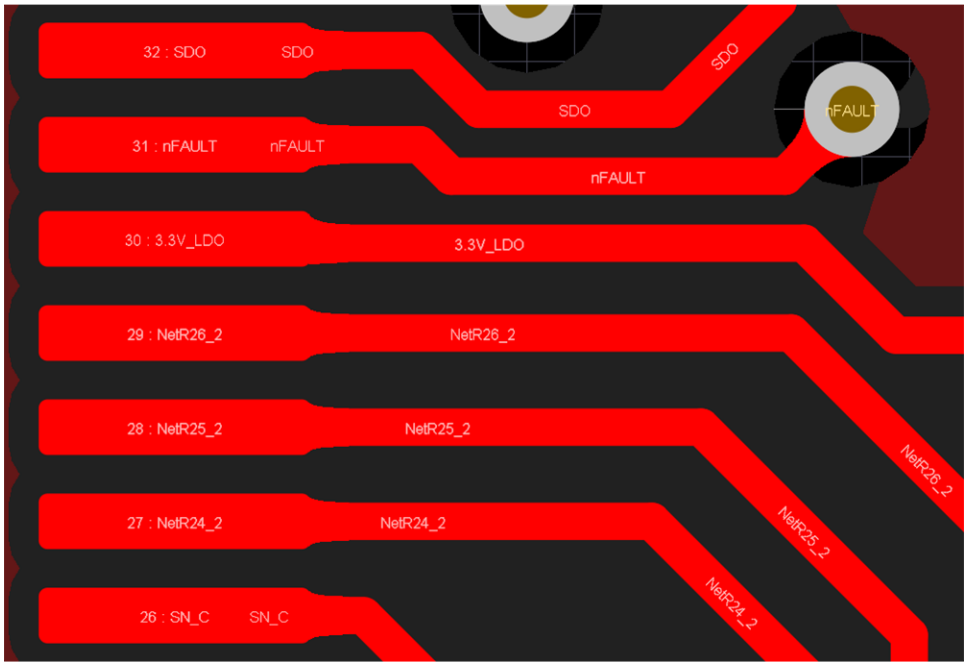
- Do not use right-angle traces because it can cause the current to reflect and act as an impedance. Sharp bends can cause electromagnetic interference (EMI) issues when motor phases are switching. The best practice is to use obtuse angles as 図 25 shows.

図 25. Parallel Gate Traces, Routed Using Obtuse Angles



- Transition vias to pads, especially from thin to thick traces on output pins. This technique is called teardrops – these allow for thermal stress to decrease on signal transitions and avoid cracking of traces.

図 26. Teardrops Used on Transitions From Vias to Pads



For high-current nets, polygon pours are implemented to create wide current paths for phase currents, power nodes on signal layers, and power rails on the POWER layer.

In the TIDA-060030 design, polygon pours are implemented using the following system diagram by layer:

- POWER
  1. VBAT – battery net
  2. VM – large net that connects to VM of the power management circuitry, bypass caps of the DRV8343S-Q1, and VM nodes of the power stage bulk capacitances
  3. 6V_BUCK – net that runs to or from the 6-V buck converter
  4. 3.3V_LDO – net that powers all logic-level circuitry, including C2000, LEDs, and input controls
- GND - Large GND pour over entire layer
- BOTTOM
  1. VM – pour that connects to the recirculation diode on the BOTTOM layer and VM on the POWER layer
  2. OUT_C1 – connects to OUT_C1 on top layer
  3. OUT_C2 – connects to OUT_C2 on top layer
  4. GND pour everywhere else
- TOP
  1. Similar nets (typically in power management and power stage circuitry) are connected together where possible such as VM, 6V_BUCK, output nets, and VBAT
  2. GND pour everywhere else

4.1.3.6 Bulk and Bypass Capacitor Placement

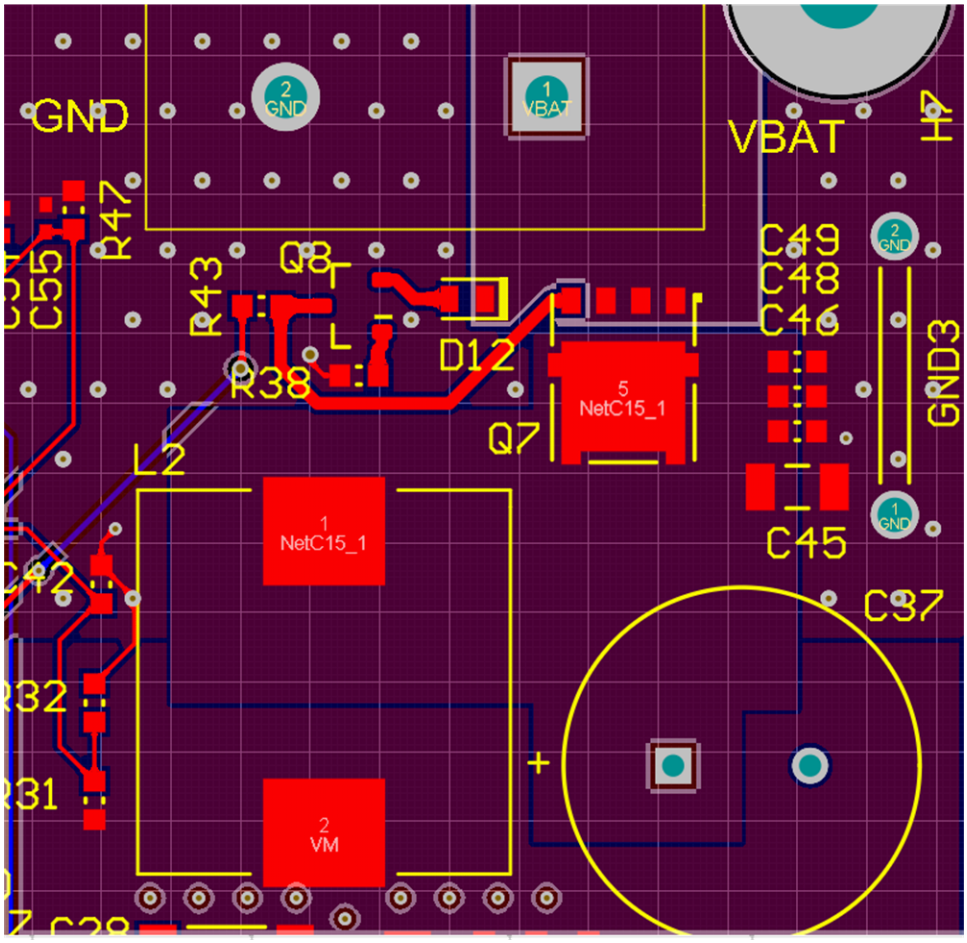
4.1.3.6.1 Bulk Capacitor Placement

In a motor drive system design, a bulk capacitor minimizes the effects of low-frequency current transient and stores charge to supply large currents required by the motor driver when it switches. When selecting a bulk capacitor, consider the highest current required by the motor system, supply voltage ripple, and type of motor.

Use bulk electrolytic capacitance to help source the low-frequency, high-value currents from the current that is driven through the motor winding. These capacitors usually are greater than 10 μF, depending on the application requirements.

Place all bulk capacitors near the power supply module or power entry point of the board. TI recommends that each bulk capacitor have multiple vias connecting the pad to the respective power plane. TI also recommends that all bulk capacitors have low equivalent series resistance (ESR).

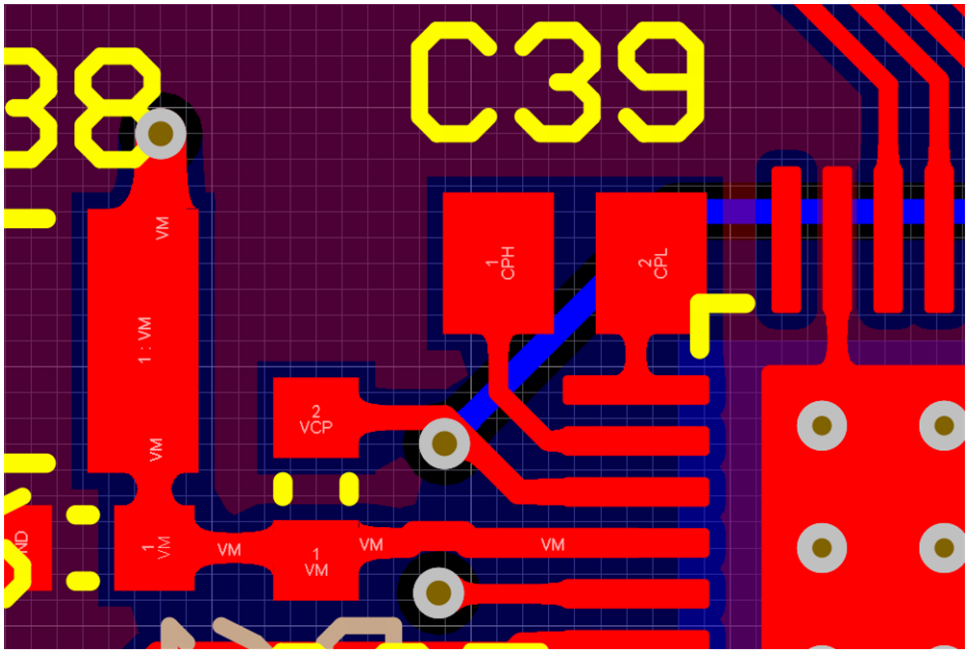
図 27. Bulk Capacitor Placed Near Power Supply of TIDA-060030



4.1.3.6.2 Charge Pump Capacitor

Many of TI's motor drivers use charge pump or bootstrap capacitors to fully switch the gate of the high-side N-channel MOSFET. Place these capacitors as close to the motor drive device as possible.

図 28. Charge Pump Capacitor Placement

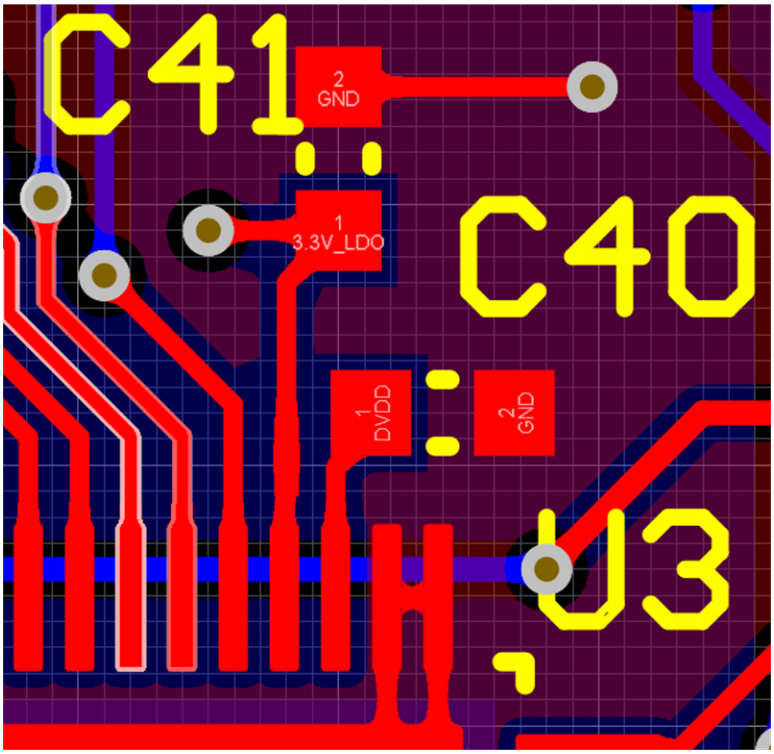


4.1.3.6.3 Bypass and Decoupling Capacitors

4.1.3.6.3.1 Near Power Supply

A bypass capacitor is used to minimize high-frequency noise into the supply pin of the DRV device. TI recommends placing capacitors as close as possible to the power input pins of the device and ground pins. If the trace lengths between the bypass capacitor and the device are not minimized, they can be inductive at the high frequencies that the bypass capacitor is meant to filter. The added impedance from trace inductance can cause ringing in the voltage or current at the supply pin which contributes to EMI and affects the performance of digital or analog circuits. A best practice is to place the capacitor with the lesser value as close as possible to the device to minimize the influence of the inductance of the trace.

図 29. Decoupling Capacitors Placed Near 3.3-V LDO Power Supply



- Do not use vias between the bypass capacitors and the active device. Visualize the high-frequency current flow and reduce loops of high-frequency current as much as possible.
- Make sure bypass capacitors are on the same layer as active components for best results. Do not place a via between the bypass capacitor pin and the IC supply or ground pin.

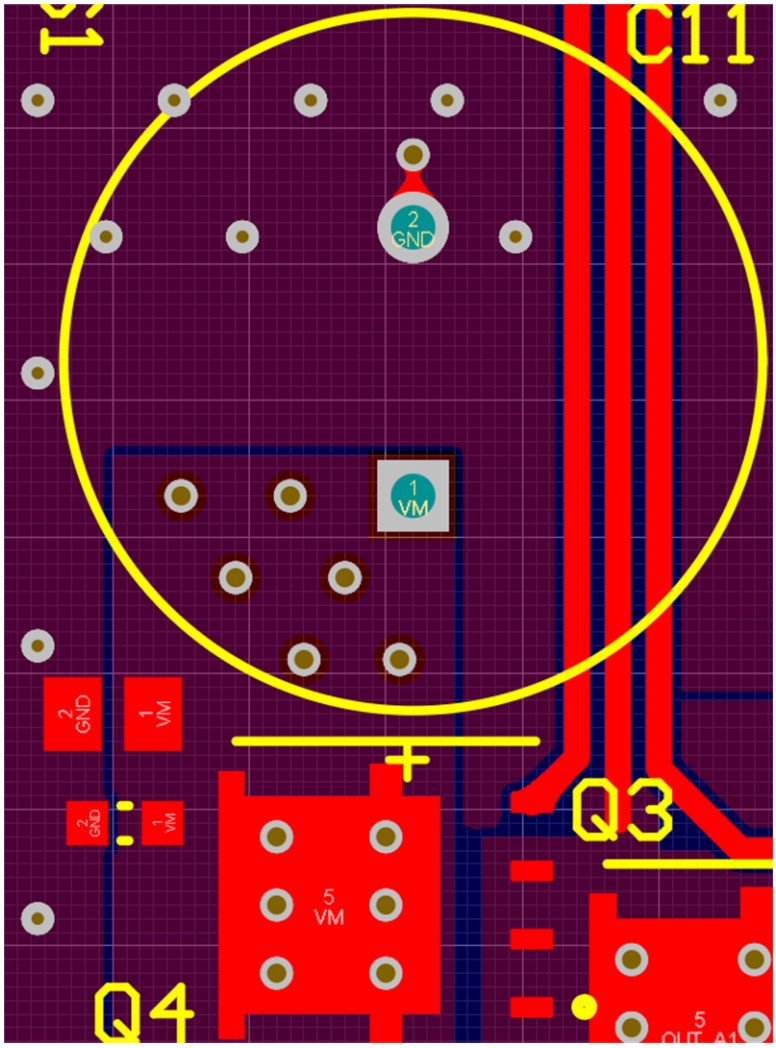
4.1.3.6.3.2 Near Power Stage

For bypass capacitance on the power stage, use small ceramic capacitors to attenuate high-frequency currents caused by switching from the MOSFETs and other parasitic capacitances. These capacitors typically have values of capacitance less than 10 μF, depending on the application requirements.

4.1.3.6.3.3 Near Switch Current Source

Correct layout and placement of these capacitors is critical to make sure they are effective. Any additional parasitic inductance between the capacitance and the source of the switching current decreases their effect. Ideally, place the capacitors as close as possible to the source of the switching currents, in this case, the motor and MOSFETs.

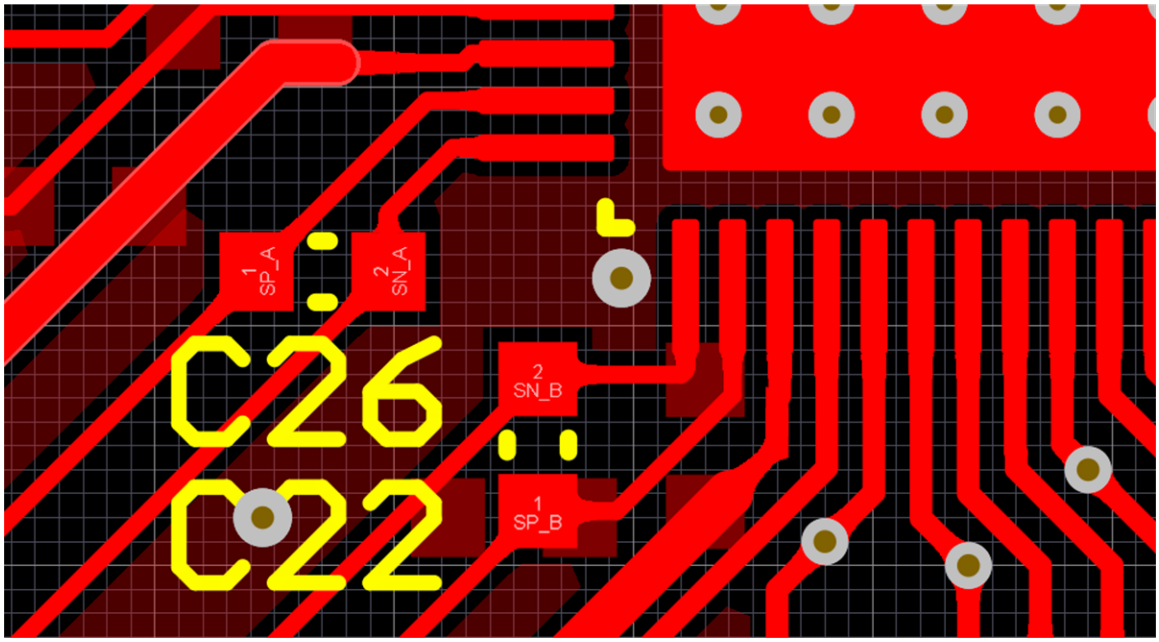
図 30. Bulk Capacitor Placed Near Switching Current Source in the Same VM Pour



4.1.3.6.3.4 Near Current Sense Amplifiers

For devices with integrated current sense amplifiers (CSA), TI recommends placing additional decoupling capacitors as close to the sensing pins as possible and using values of approximately 1 nF.

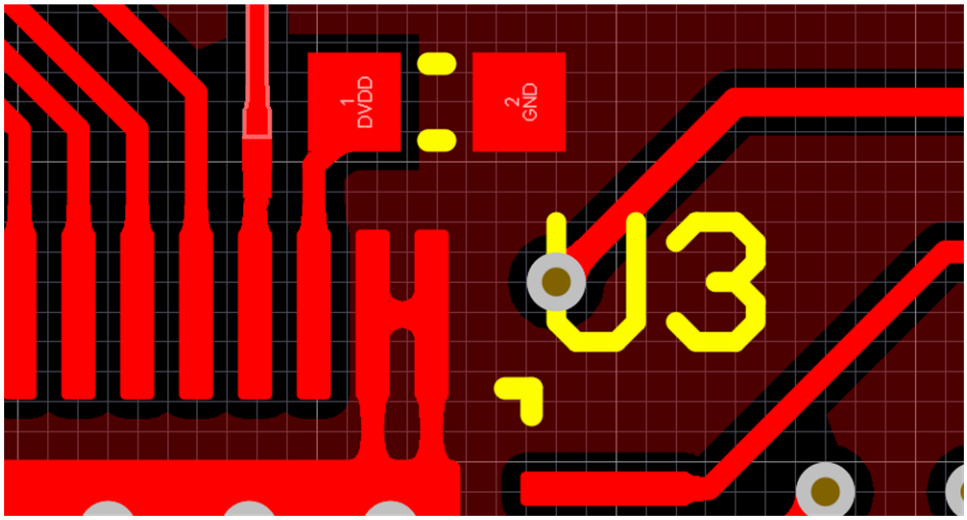
図 31. Decoupling Capacitors Placed Near SNx and SPx Pins



4.1.3.6.3.5 Near Voltage Regulators

For devices with voltage regulators, place the capacitor as close as possible to the pin. Minimize the ground return loop to the ground pin.

図 32. Decoupling Capacitor Placed Near DVDD Pin



4.1.3.7 MOSFET Placement and Powerstage Routing

Placement of the gate driver and power MOSFETs is critical for correct functionality and optimal performance in pre-driver motor drive solutions. In the TIDA-060030 design, the bottom half of the board is specifically dedicated to the power stage routing for optimal current dissipation, eliminating switch-node ringing, and efficient switching of current to the output loads.

Each output phase of TIDA-060030 has a unique layout optimized for its configuration. Phases have two external FETs for the GHx and GLx signals, but only phases B, C high, and C low have recirculation diodes to dissipate current and protect the load in the case both FETs are turned off independently. Each phase also is optimized in consideration of high-current loop paths to minimize overall loop inductance, voltage ripple, noise, and the need for extra bypass capacitance.

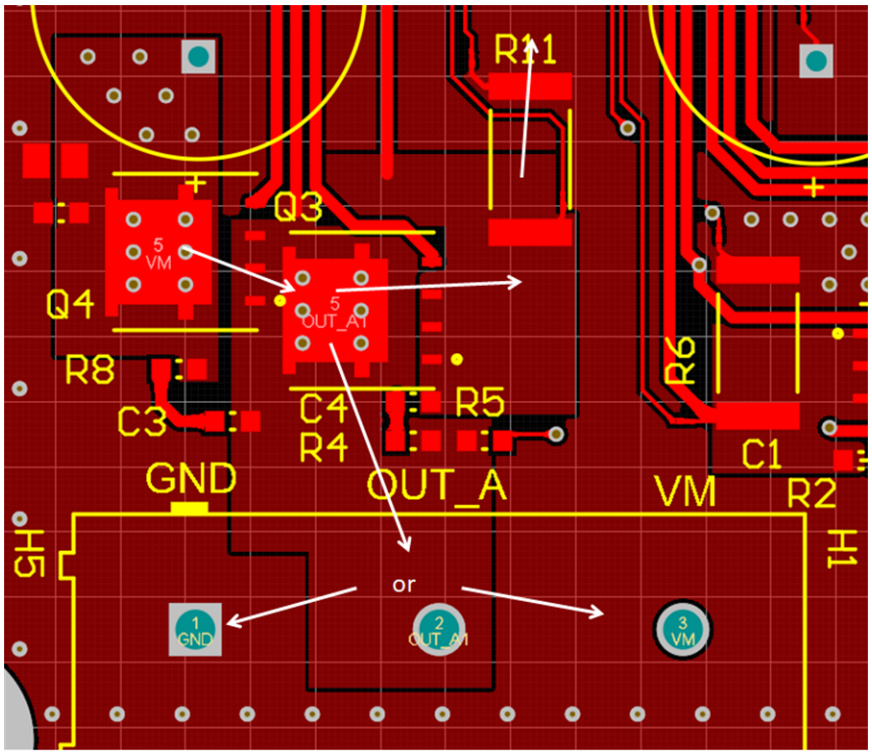
4.1.3.7.1 Phase A: Unidirectional BDC Motor

Phase A supports a unidirectional brushed-DC motor or solenoid load. One end of the load is connected to OUT_A1, and the other end is connected to either GND or VM. If the load is a brushed-DC motor, then the motor will spin in only one direction depending on the motor configuration. Likewise, a solenoid load will push or pull depending on the load configuration.

The system is rated for up to 15 A of current, so it recommended to have traces at least 150 mil wide to efficiently sink high current. Outputs of the powerstage use polygon pours to support high current flow and protect the board and components from any cracks in traces.

All phase A gate drive signals use 20-mil traces, and VSEN_A uses a 10-mil trace because they are low-current signals.

図 33. Power Stage Layout for Phase A

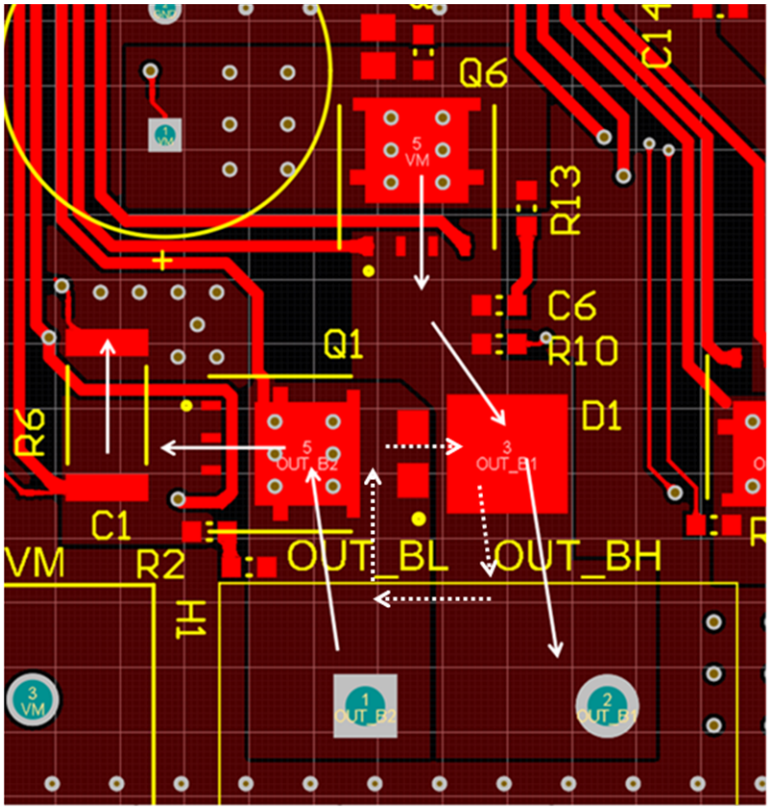


4.1.3.7.2 Phase B: Solenoid With Half-bridge

Phase B supports a solenoid output using a half-bridge configuration that provides short-to-battery and short-to-ground protection. The solenoid load is connected to OUT_BH and OUT_BL. A recirculation diode is placed in parallel with the load to dissipate current in the case the drivers are switched off. Likewise with phase A, power stage signals that can *detect* the full solenoid load current are to be 10 mil wide for every 1 A.

All phase B gate drive signals use 20-mil traces, and VSEN_B uses a 10-mil trace because they are low-current signals.

図 34. Power Stage Layout for Phase B



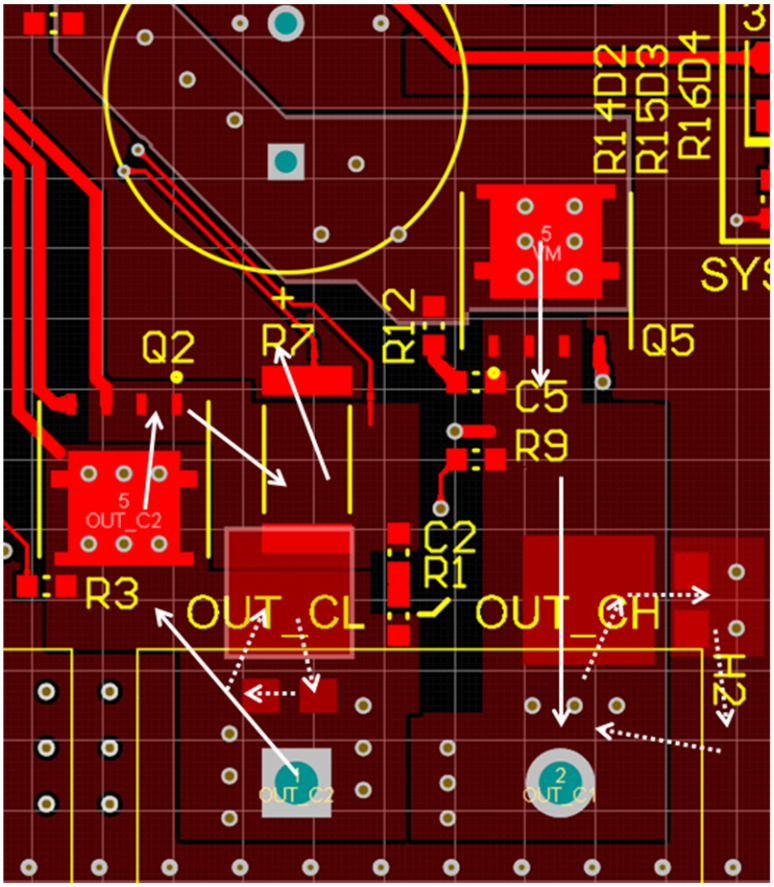
4.1.3.7.3 Phase C: Independent Loads Using Split Half-Bridge

Phase C supports two solenoid outputs using a split half-bridge configuration, a capability provided by the DRV8343S-Q1 device using independent FET mode. In this mode, the high-side and low-side drivers can independently drive two separate loads such as solenoids and unidirectional brushed-DC motors. In the layout, there exists two separate current paths to drive the output loads independently. Each topology requires a recirculation diode in parallel with the output load to dissipate current when the driver is off.

The solenoid load for the high side of phase C (CH) is connected to OUT_CH, and the low side is connected to GND. Likewise, the solenoid load for the low side of phase C (CL) is connected to OUT_CL, and the high side is connected to VM.

All phase C gate drive signals use 20-mil traces, and VSEN_CH and VSEN_CL use a 10-mil trace because they are low-current signals.

図 35. Power Stage Layout for Phase C High-Side and C Low-Side



4.1.3.8 Current Sense Amplifier Routing

Many of TI's motor drivers include built-in current sensing, most of which use an external shunt resistor as the measurement source. Including the current sense amplifier with the driver provides an all-in-one solution for the motor interface and allows higher-quality current sensing at a lower cost.

Two-phase and three-phase CSAs are a benefit to board layout because they have low common-mode voltage requirements. They also let each channel be measured individually, and therefore can be used in more complex control schemes such as field-oriented control (FOC).

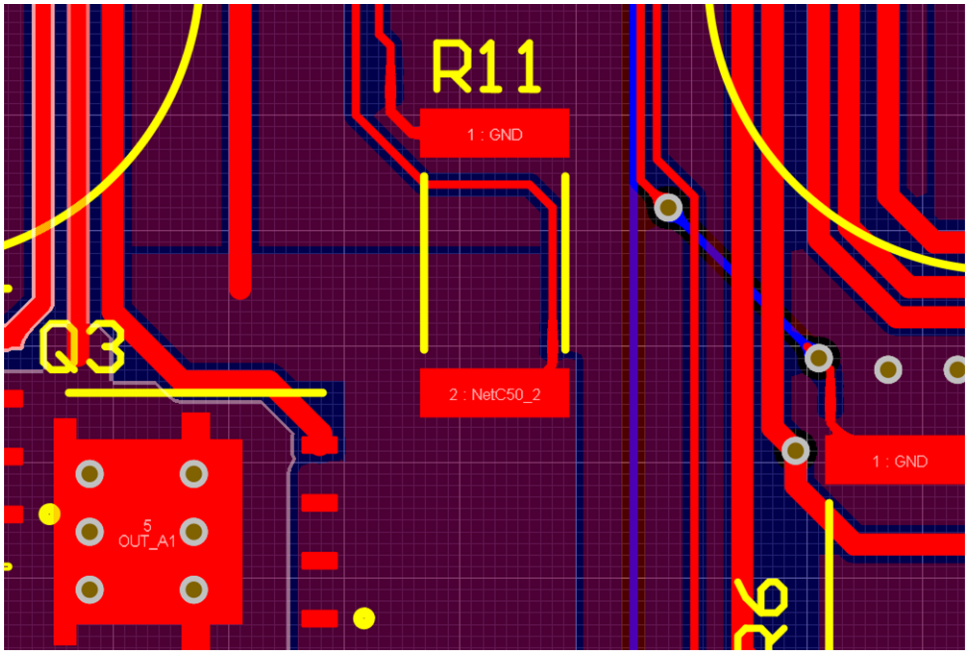
The tradeoffs of using two-phase and three-phase CSAs in board layout include:

- Higher susceptibility to ground noise
- Cannot detect ground shorts
- Could require more software to realize the total system current

For placement, the shunt resistor should be in line with the components of the power stage to minimize trace impedance. The shunt resistor should also be placed close to the connection to the CSA to decrease the possibility of coupling on other traces on the board. The shunt resistor should be placed between the source of the respective low-side MOSFET and the ground connection.

Use the copper pours from the source of the low side to tie to the high side of the CSA. The sense signals of the shunt resistors should be a differential pair and traces must run in parallel to the input of the IC.

図 36. Shunt Resistor Placement Between Low-Side MOSFET and Ground



4.1.3.9 Net Ties

When routing a PCB during the initial stages, the guides that help show which component routes can be deceptive in the case of the sense resistor routing. In the case of the low-side shunt resistor, the negative input could direct straight to ground, and the positive input could direct to the low-side source pin. To avoid these situations, place a Net Tie between the device and the shunt resistor so that the designer can place the route restriction during placement instead of during routing.

図 37. Net Ties in Layout

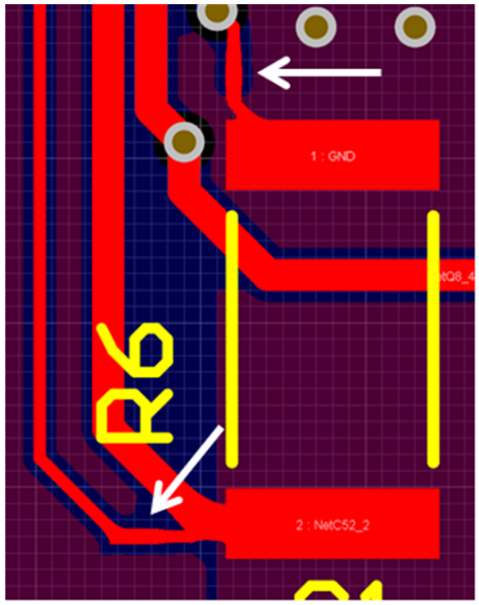
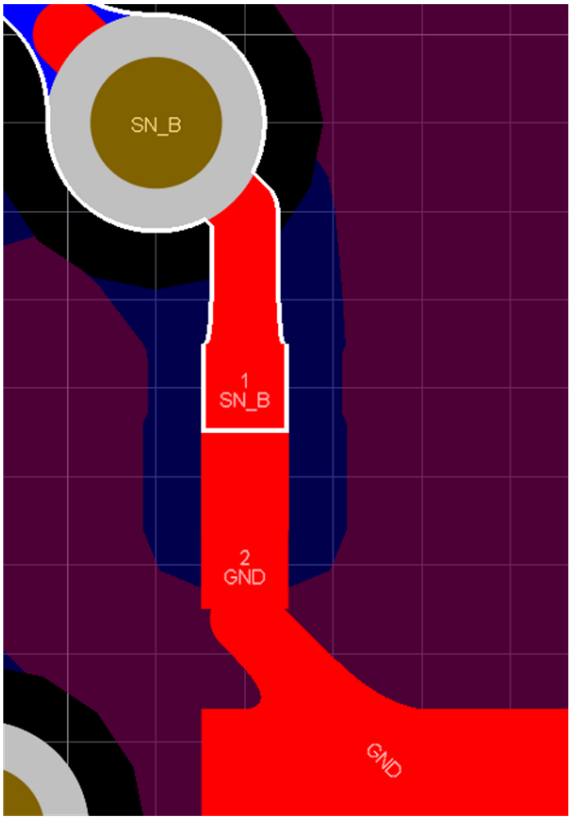


図 38. Net Ties in Layout, Zoomed in



4.2 Gerber Files

To download the Gerber files, see the design files at TIDA-060030.

4.3 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-060030.

5 Related Documentation

1. Texas Instruments, *DRV8343-Q1 12-V / 24-V Automotive Gate Driver Unit (GDU) with Independent Half Bridge Control and Three Integrated Current Sense Amplifiers Data Sheet*
2. Texas Instruments, *LMR36006-Q1 4.2-V to 60-V, 0.6-A Ultra-Small Synchronous Step-Down Converter Data Sheet*
3. Texas Instruments, *TPS7B81-Q1 150-mA, Off-Battery, Ultra-low-I_Q (3-μA), Low-Dropout Regulator Data Sheet*
4. *SQJ850EP Automotive N-Channel 60 V (D-S) 175 °C MOSFET* Vishay Siliconix www.vishay.com
5. *FSV20100V Ultra-Low VF Schottky Rectifier, 20 A, 100 V Data Sheet* ON Semiconductor www.onsemi.com
6. Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers Data Sheet*
7. Texas Instruments, *TMS320F2803x Piccolo™ Technical Reference Manual*
8. Texas Instruments, *Best Practices for Board Layout of Motor Drivers Application Report*
9. Texas Instruments, *Using DRV to Drive Solenoids - DRV8876/DRV8702-Q1/DRV8343-Q1 Application Report*

5.1 商標

5.2 Third-Party Products Disclaimer

6 Terminology

ADC - analog-to-digital converter

BOM - bill of materials

Buck - step-down switching-mode voltage converter

C2000 - real-time control microcontroller unit, 16-, 32-bit

CCS - Code Composer Studio

CSA - current shunt amplifier

DL - drain low

FET - field effect transistor

GND - ground

GH - gate high

ICE - internal combustion engine

LDO - linear dropout voltage regulator

MCU - microcontroller unit

MOSFET - metal oxide semiconductor field effect transistor

OEM - original equipment manufacturer

PB - push button

PCB - printed circuit board

TIRD - TI Reference Design

VBAT - battery voltage

VM - motor driver voltage, same as VBAT after filter

7 About the Author

AARON BARRERA is an Applications Engineer at Texas Instruments. He graduated from the University of Florida in December 2019 with a Bachelor of Science in Electrical Engineering. Aaron works with the BLDC Motor Driver team, and previously was a Product Marketing Intern for BLDC Motor Drivers. In his free time, he enjoys arranging and producing music, playing basketball, and watching sports.

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