



TPS22918-Q1 5.5V、2A、52mΩオン抵抗負荷スイッチ

1 特長

- AEC-Q100認定済み
- シングル・チャネル負荷スイッチを内蔵
- 車載アプリケーション向けに認定済み
 - デバイス温度グレード 2: 動作時周囲温度範囲 -40°C ~ +105°C
- **機能安全対応**
 - 機能安全システムの設計に役立つ資料を利用可能
- 入力電圧範囲: 1V ~ 5.5V
- 低いオン抵抗(R_{ON})
 - $V_{IN} = 5V$ で $R_{ON} = 52m\Omega$ (標準値)
 - $V_{IN} = 3.3V$ で $R_{ON} = 53m\Omega$ (標準値)
- 最大連続スイッチ電流: 2A
- 低静止電流
 - $V_{IN} = 3.3V$ において $8.3\mu A$ (標準値)
- 低い制御入力スレッシュホールドにより、1V 以上の GPIO を使用可能
- クイック出力放電(QOD)を構成可能
- CT ピンで立ち上がり時間を設定可能
- 小型の SOT23-6 パッケージ (DBV)
 - 2.9mm × 2.8mm、0.95mm ピッチ、高さ 1.45mm (リードを含む)
- AEC Q100 に準拠した ESD 性能テスト済み
 - HBM ±2kV、CDM ±750V

2 アプリケーション

- 車載用電子機器
- インフォテインメント
- クラスタ
- ADAS (先進運転支援システム)

3 概要

TPS22918-Q1は、シングル・チャネル負荷スイッチで、立ち上がり時間とクイック出力放電の両方を構成可能です。このデバイスにはNチャネルMOSFETが搭載され、1V ~ 5.5Vの入力電圧範囲で動作でき、最大で2Aの連続電流をサポートできます。スイッチはオン/オフ入力により制御され、低電圧の制御信号と直接接続が可能です。

デバイスの立ち上がり時間を構成可能なため、大きな負荷容量により発生する突入電流が低減され、電源ドロップが低減、または排除されます。TPS22918-Q1には構成可能なクイック出力放電(QOD)ピンが搭載されており、デバイスの立ち下がり時間を制御できるため、電源オフおよびシーケンシングについて柔軟な設計が可能になります。

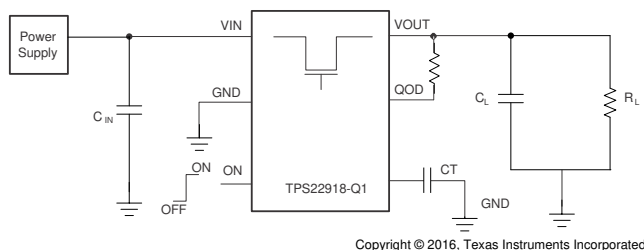
TPS22918-Q1は小型のリード付きSOT-23パッケージ(DBV)で供給されるため、ハンダ接合部の目視検査が可能です。このデバイスは、自由通気で-40°C ~ +105°Cの温度範囲で動作するよう規定されています。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS22918-Q1	SOT-23 (6)	2.90mm×1.60mm

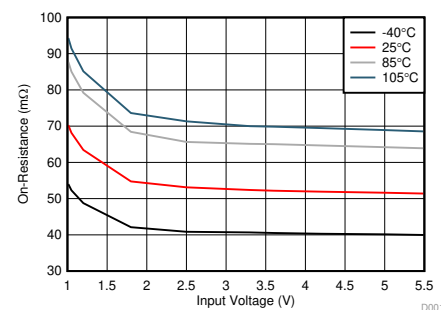
(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



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オン抵抗と入力電圧の 標準値との関係



$I_{OUT} = -200mA$

D001



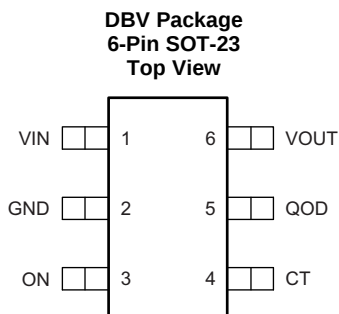
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4 改訂履歴

Revision A (July 2016) から Revision B に変更	Page
• 「 特長 」セクションに機能安全対応のリンクを追加	1
2016年7月発行のものから更新	Page
• デバイスのステータスを製品プレビューから量産データへ変更	1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Place ceramic bypass capacitor(s) between this pin and GND. See the Detailed Description section for more information
2	GND	—	Device ground
3	ON	I	Active high switch control input. Do not leave floating
4	CT	O	Switch slew rate control. Can be left floating. See the Feature Description section for more information
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways - Placing an external resistor between VOUT and QOD - Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) - Disabling QOD by leaving pin disconnected See the Quick Output Discharge (QOD) section for more information
6	VOUT	O	Switch output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage	−0.3	6	V
V _{OUT}	Output voltage	−0.3	6	V
V _{ON}	ON voltage	−0.3	6	V
I _{MAX}	Maximum continuous switch current, T _A = 70°C ⁽³⁾		2	A
I _{MAX}	Maximum continuous switch current, T _A = 85°C ⁽³⁾		1.5	A
I _{PLS}	Maximum pulsed switch current, pulse < 300 μs, 2% duty cycle		2.5	A
T _J	Maximum junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Assumes 12-K power-on hours at 100% duty cycle. This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI's semiconductor products.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged-device model (CDM), per AEC Q100-011	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{IN}	Input voltage		1	5.5	V
V _{ON}	ON voltage		0	5.5	V
V _{OUT}	Output voltage			V _{IN}	V
V _{IH, ON}	High-level input voltage, ON	V _{IN} = 1 V to 5.5 V	1	5.5	V
V _{IL, ON}	Low-level input voltage, ON	V _{IN} = 1 V to 5.5 V	0	0.5	V
T _A	Operating free-air temperature ⁽¹⁾		−40	105	°C
C _{IN}	Input Capacitor		1 ⁽²⁾		μF

- (1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(MAX)}] is dependent on the maximum operating junction temperature [T_{J(MAX)}], the maximum power dissipation of the device in the application [P_{D(MAX)}], and the junction-to-ambient thermal resistance of the part-package in the application (θ_{JA}), as given by the following equation: T_{A(MAX)} = T_{J(MAX)} − (θ_{JA} × P_{D(MAX)}).
- (2) See the [Application and Implementation](#) section.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TPS22918-Q1	UNIT
	DBV (SOT-23)	
	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	183.2
R _{θJC(top)}	Junction-to-case (top) thermal resistance	151.6
R _{θJB}	Junction-to-board thermal resistance	34.1
ψ _{JT}	Junction-to-top characterization parameter	37.2
ψ _{JB}	Junction-to-board characterization parameter	33.6

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the following operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ (full). Typical values are for $T_A = 25^{\circ}\text{C}$.

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{Q, VIN}$ Quiescent current	$V_{ON} = 5\text{ V}, I_{OUT} = 0\text{ A}$	$V_{IN} = 5.5\text{ V}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	9.2	16	μA
		$V_{IN} = 5\text{ V}$		8.7	16	
		$V_{IN} = 3.3\text{ V}$		8.3	15	
		$V_{IN} = 1.8\text{ V}$		10.2	17	
		$V_{IN} = 1.2\text{ V}$		9.3	16	
		$V_{IN} = 1\text{ V}$		8.9	15	
$I_{SD, VIN}$ Shutdown current	$V_{ON} = 0\text{ V}, V_{OUT} = 0\text{ V}$	$V_{IN} = 5.5\text{ V}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	0.5	5	μA
		$V_{IN} = 5\text{ V}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	0.5	4.5	
		$V_{IN} = 3.3\text{ V}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	0.5	3.5	
		$V_{IN} = 1.8\text{ V}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	0.5	2.5	
		$V_{IN} = 1.2\text{ V}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	0.4	2	
		$V_{IN} = 1\text{ V}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$	0.4	2	
I_{ON} ON pin input leakage current	$V_{IN} = 5.5\text{ V}, I_{OUT} = 0\text{ A}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			0.1	μA
R_{ON} On-Resistance	$V_{IN} = 5.5\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		51	59	$\text{m}\Omega$
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			78	
	$V_{IN} = 5\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		52	59	
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			79	
	$V_{IN} = 4.2\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		52	59	
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			79	
	$V_{IN} = 3.3\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		53	59	
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			80	
	$V_{IN} = 2.5\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		53	61	
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			80	
	$V_{IN} = 1.8\text{ V}, I_{OUT} = -200\text{ mA}$	25°C		55	65	
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			88	
V_{HYS} ON pin hysteresis	$V_{IN} = 1\text{ V to } 5.5\text{ V}$	$-40^{\circ}\text{C to } +105^{\circ}\text{C}$		107		mV
R_{PD} Output pull down resistance	$V_{IN} = 5\text{ V}, V_{ON} = 0\text{ V}$	25°C		24		Ω
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			30	
	$V_{IN} = 3.3\text{ V}, V_{ON} = 0\text{ V}$	25°C		25		
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			35	
	$V_{IN} = 1.8\text{ V}, V_{ON} = 0\text{ V}$	25°C		45		
		$-40^{\circ}\text{C to } +105^{\circ}\text{C}$			60	

6.6 Switching Characteristics

See timing test circuit in [Figure 21](#) (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where VIN is already in steady state condition before the ON pin is asserted high. Test Conditions: $V_{ON} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = 5 V					
t _{ON} Turnon time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		1950		μs
t _{OFF} Turnoff time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		2		μs
t _R V _{OUT} rise time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		2540		μs
t _F V _{OUT} fall time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		2		μs
t _D Delay time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		690		μs
V_{IN} = 3.3 V					
t _{ON} Turnon time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		1430		μs
t _{OFF} Turnoff time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		2		μs
t _R V _{OUT} rise time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		1680		μs
t _F V _{OUT} fall time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		2		μs
t _D Delay time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		590		μs
V_{IN} = 1.8 V					
t _{ON} Turnon time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		965		μs
t _{OFF} Turnoff time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		2		μs
t _R V _{OUT} rise time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		960		μs
t _F V _{OUT} fall time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		2		μs
t _D Delay time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		480		μs
V_{IN} = 1 V					
t _{ON} Turnon time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		725		μs
t _{OFF} Turnoff time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		3		μs
t _R V _{OUT} rise time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		560		μs
t _F V _{OUT} fall time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		2		μs
t _D Delay time	R _L = 10 Ω, C _{IN} = 1 μF, C _{OUT} = 0.1 μF, CT = 1000 pF		430		μs

6.7 Typical DC Characteristics

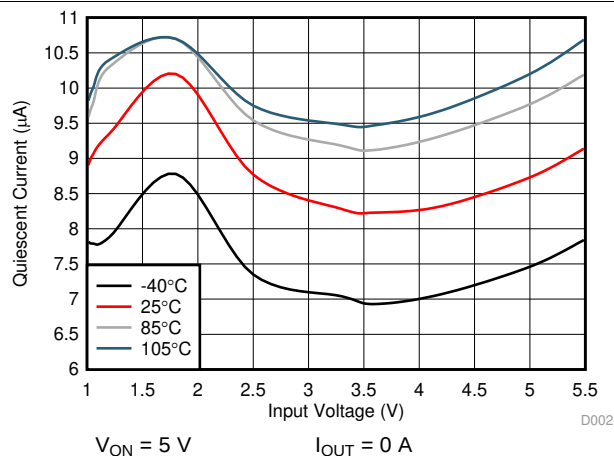


Figure 1. Quiescent Current vs Input Voltage

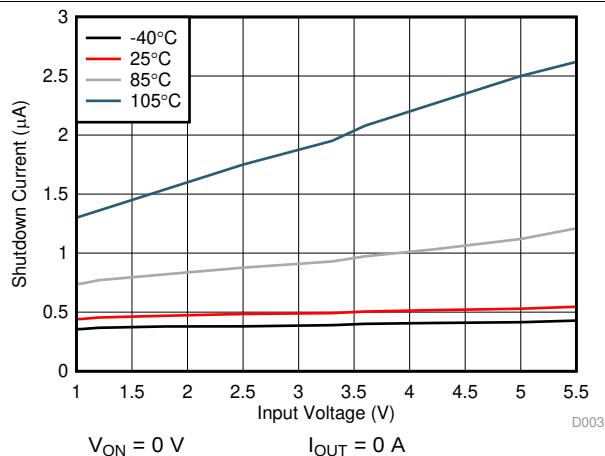


Figure 2. Shutdown Current vs Input Voltage

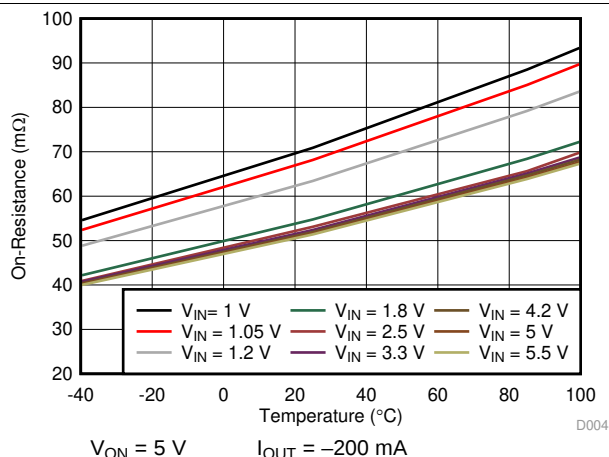


Figure 3. On-Resistance vs Temperature

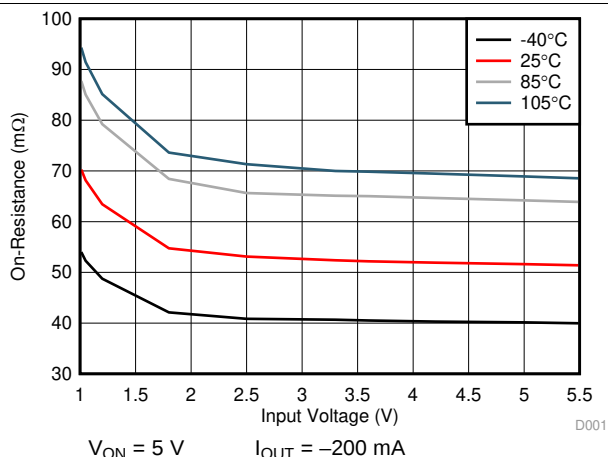


Figure 4. On-Resistance vs Input Voltage

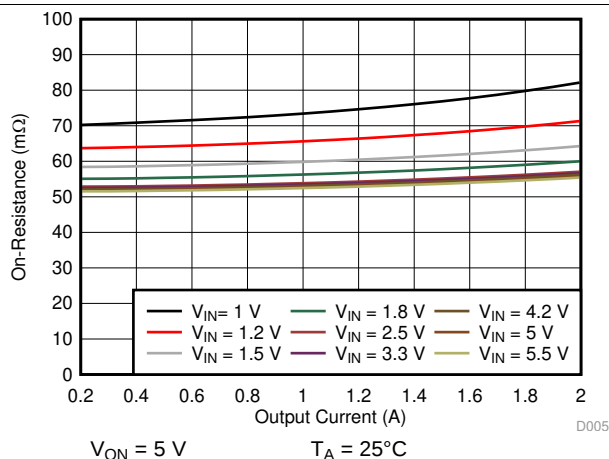


Figure 5. On-Resistance vs Output Current

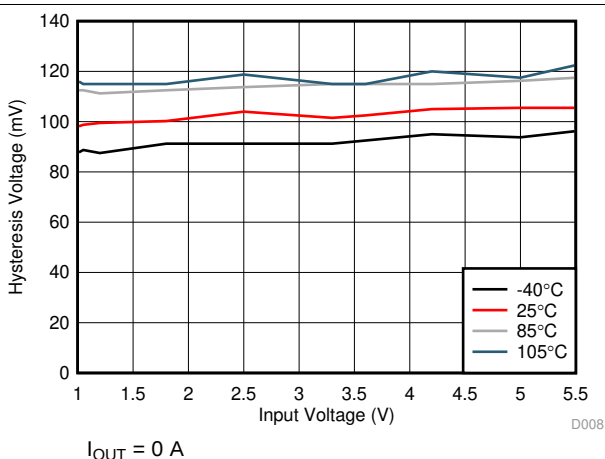


Figure 6. Hysteresis Voltage vs Input Voltage

Typical DC Characteristics (continued)

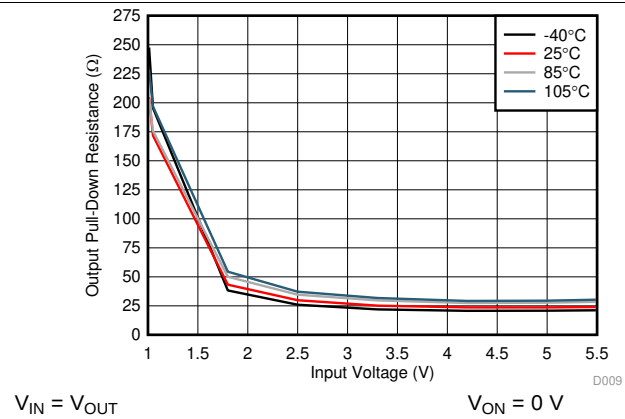
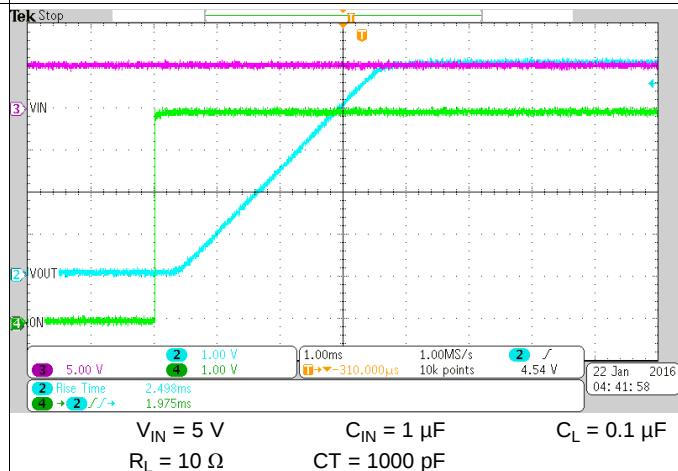
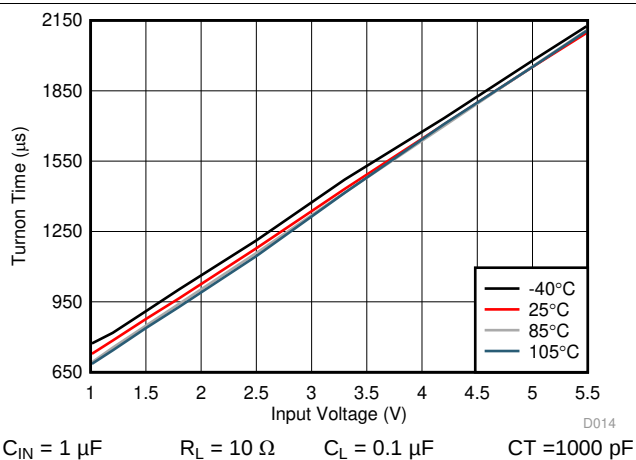
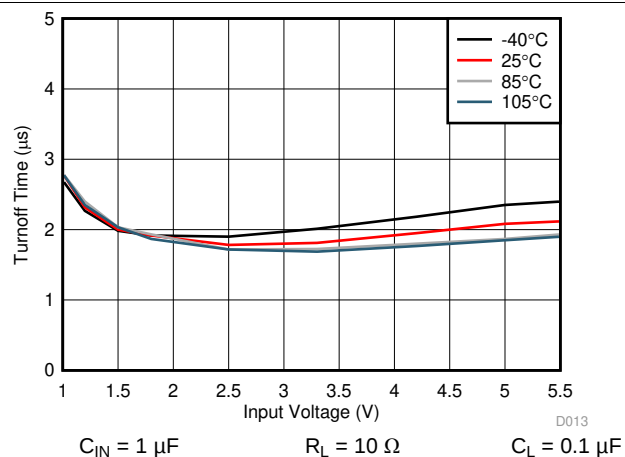
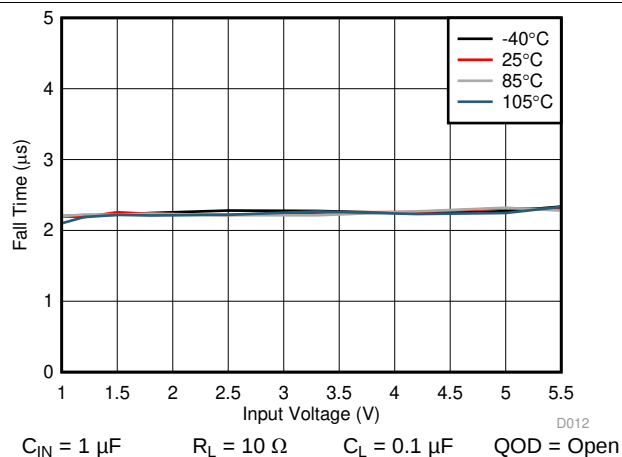
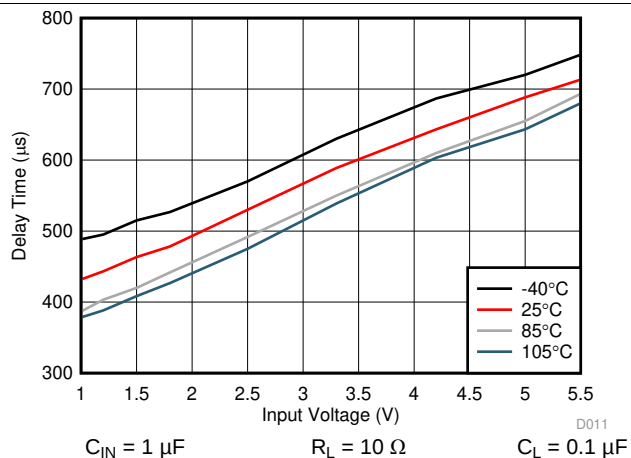
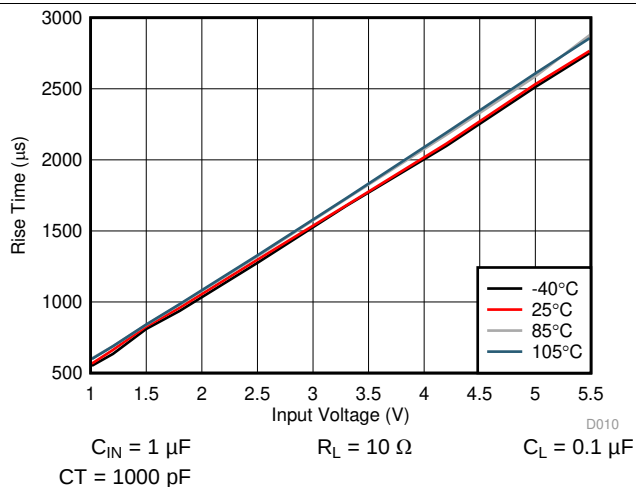
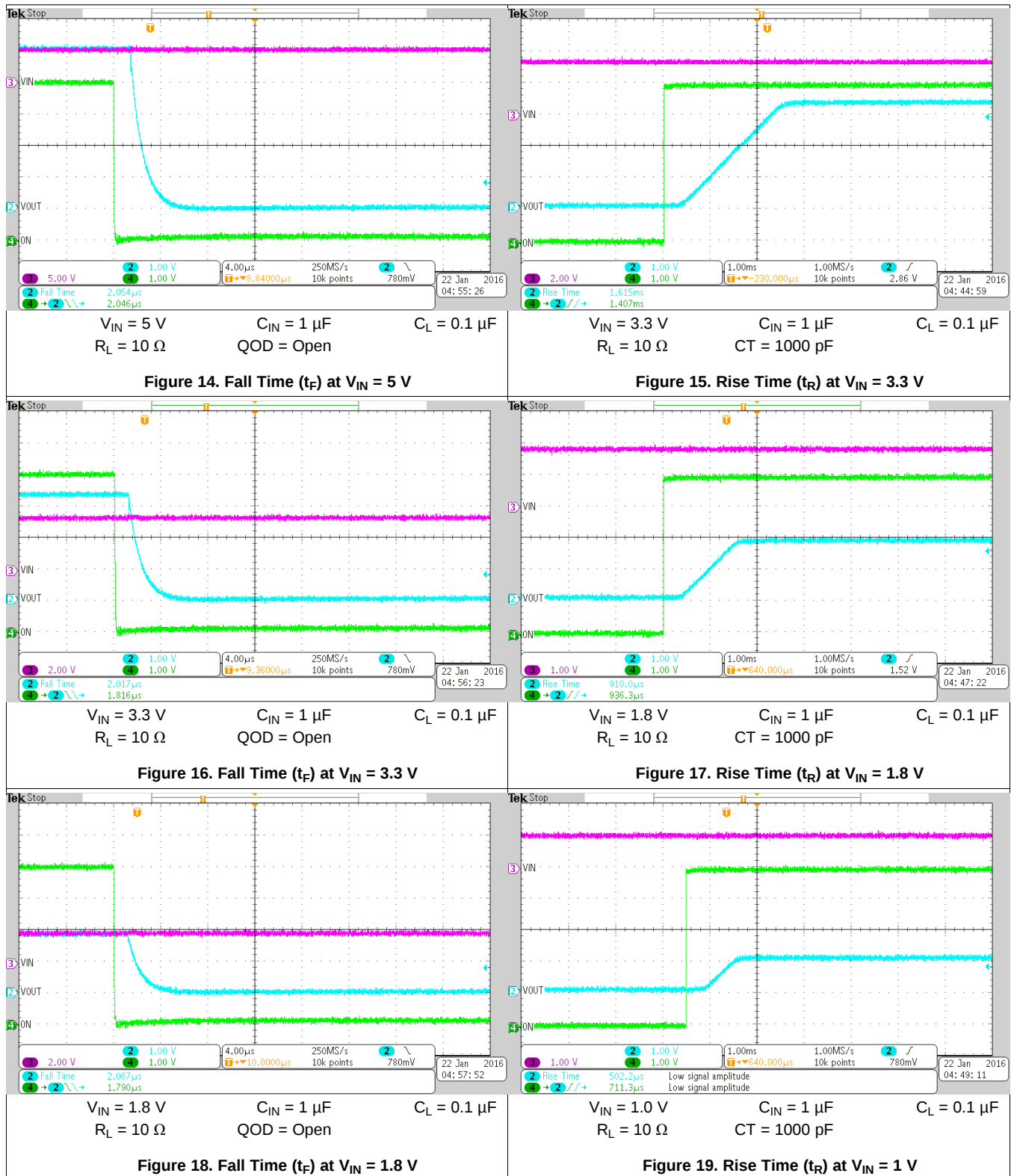


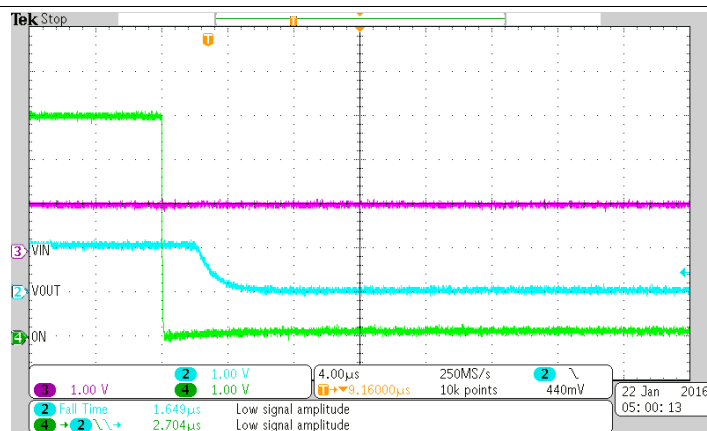
Figure 7. Output Pull-Down Resistance vs Input Voltage

6.8 Typical AC Characteristics



Typical AC Characteristics (continued)


Typical AC Characteristics (continued)



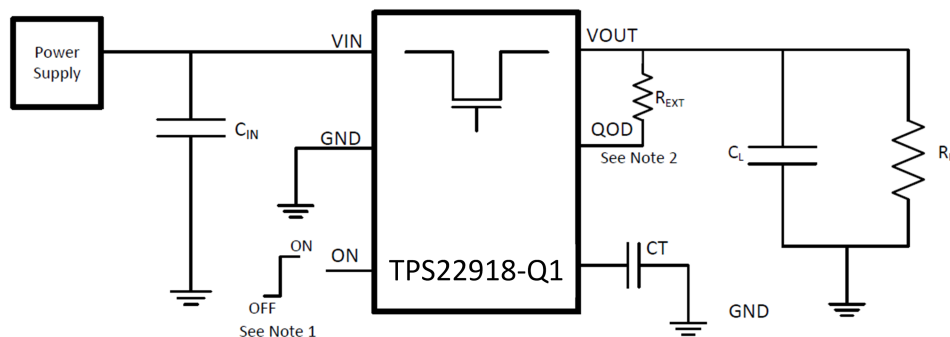
$V_{IN} = 1.0 \text{ V}$
 $R_L = 10 \text{ } \Omega$

$C_{IN} = 1 \text{ } \mu\text{F}$
 QOD = Open

$C_L = 0.1 \text{ } \mu\text{F}$

Figure 20. Fall Time (t_F) at $V_{IN} = 1 \text{ V}$

7 Parameter Measurement Information



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- (1) Rise and fall times of the control signal is 100 ns.
- (2) Turnoff times and fall times are dependent on the time constant at the load. For TPS22918-Q1, the internal pull-down resistance R_{PD} is enabled when the switch is disabled. The time constant is $(R_{QOD} \parallel R_L) \times C_L$ where R_{QOD} equals $R_{PD} + R_{EXT}$.

Figure 21. Test Circuit

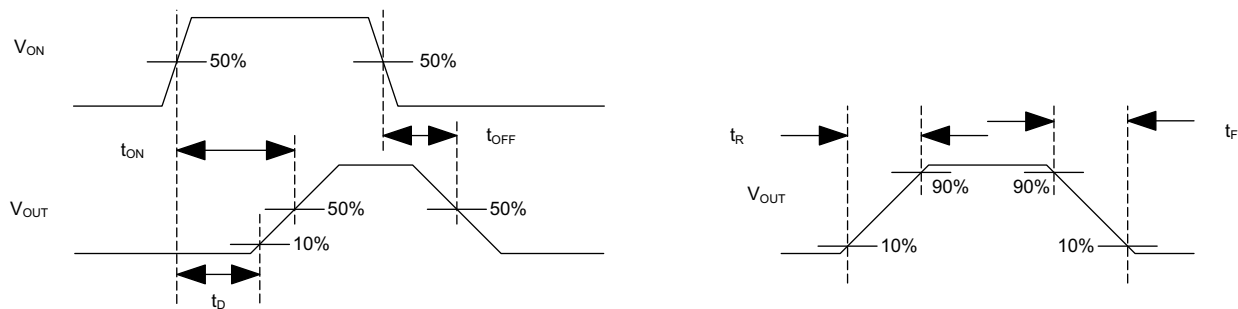


Figure 22. Timing Waveforms

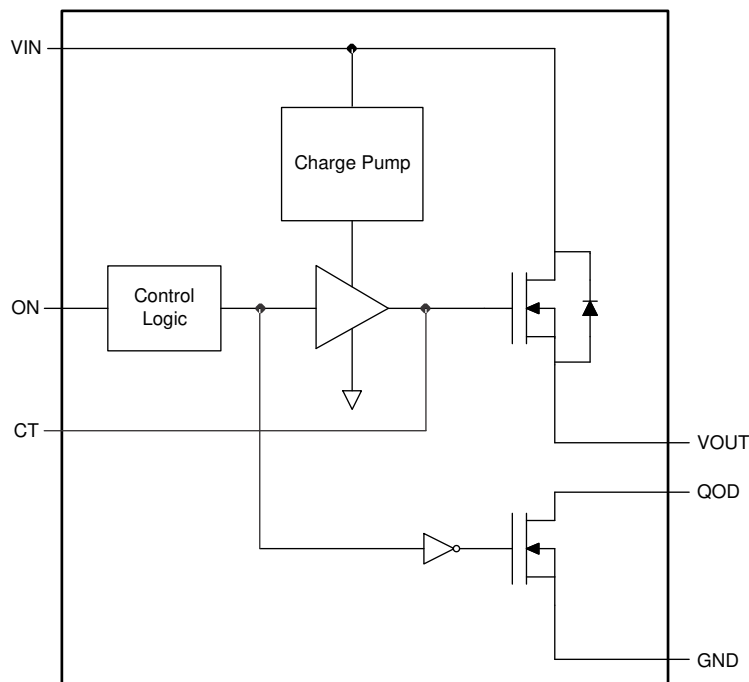
8 Detailed Description

8.1 Overview

The TPS22918-Q1 is a 5.5-V, 2-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage through the device.

The device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows to configure the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

8.3.2 Quick Output Discharge (QOD)

The TPS22918-Q1 includes a QOD feature. The QOD pin can be configured in one of three valid ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance R_{PD} . The value of this resistance is listed in the [Electrical Characteristics](#) table.
- QOD pin connected to VOUT pin using an external resistor R_{EXT} . After the switch becomes disabled, the discharge rate is controlled by the value of the total resistance of the QOD. To adjust the total QOD resistance, [Equation 1](#) can be used.

Feature Description (continued)

$$R_{QOD} = R_{PD} + R_{EXT}$$

Where:

- R_{QOD} is the total output discharge resistance
 - R_{PD} is the internal pulldown resistance
 - R_{EXT} is the external resistance placed between the VOUT and QOD pin. (1)
- QOD pin is unused and left floating. Using this method, there is no quick output discharge functionality, and the output remains floating after the switch is disabled.

The fall times of the device depend on many factors including the total resistance of the QOD, V_{IN} , and the output capacitance. When QOD is shorted to VOUT, the fall time changes over V_{IN} as the internal R_{PD} varies over V_{IN} . To calculate the approximate fall time of V_{OUT} for a given R_{QOD} , use [Equation 2](#) and [Table 1](#).

$$V_{CAP} = V_{IN} \times e^{-t/\tau}$$

Where:

- V_{CAP} is the voltage across the capacitor (V)
- t is the time since power supply removal (s)
- τ is the time constant equal to $R_{QOD} \times C_L$ (2)

The fall times' dependency on V_{IN} becomes minimal as the QOD value increases with additional external resistance. See [Table 1](#) for QOD fall times.

Table 1. QOD Fall Times

V_{IN} (V)	FALL TIME (μ s) 90% - 10%, $C_{IN} = 1 \mu$ F, $I_{OUT} = 0$ A, $V_{ON} = 0$ V ⁽¹⁾					
	$T_A = 25^\circ\text{C}$			$T_A = 85^\circ\text{C}$		
	$C_L = 1 \mu$ F	$C_L = 10 \mu$ F	$C_L = 100 \mu$ F	$C_L = 1 \mu$ F	$C_L = 10 \mu$ F	$C_L = 100 \mu$ F
5.5	42	190	1880	40	210	2150
5	43	200	1905	45	220	2200
3.3	47	230	2150	50	260	2515
2.5	58	300	2790	60	345	3290
1.8	75	430	4165	80	490	4950
1.2	135	955	9910	135	1035	10980
1	230	1830	19625	210	1800	19270

(1) Typical values with QOD shorted to VOUT

8.3.2.1 QOD when System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN} . Past a certain V_{IN} level, the strength of the R_{PD} is reduced. If there is still remaining charge on the output capacitor, this results in longer fall times. For further information regarding this condition, see the [Shutdown Sequencing During Unexpected System Power Loss](#) section.

8.3.2.2 Internal QOD Considerations

Special considerations must be taken when using the internal R_{PD} by shorting the QOD pin to the VOUT pin. The internal R_{PD} is a pulldown resistance designed to quickly discharge a load after the switch has been disabled. Care must be used to ensure that excessive current does not flow through R_{PD} during discharge so that the maximum T_J of 150°C is not exceeded. When using only the internal R_{PD} to discharge a load, the total capacitive load must not exceed 200μ F. Otherwise, an external resistor, R_{EXT} , must be used to ensure the amount of current flowing through R_{PD} is properly limited and the maximum T_J is not exceeded. To ensure the device is not damaged, the remaining charge from C_L must decay naturally through the internal QOD resistance and must not be driven.

8.3.3 Adjustable Rise Time (CT)

A capacitor to GND on the CT pin sets the slew rate for each channel. The capacitor to GND on the CT pin must be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate is shown in Equation 3.

$$SR = 0.55 \times CT + 30$$

where

- SR is the slew rate (in $\mu\text{s/V}$)
- CT is the capacitance value on the CT pin (in pF)
- The units for the constant 30 are $\mu\text{s/V}$. The units for the constant 0.55 are $\mu\text{s}/(\text{V} \times \text{pF})$

Equation 3 accounts for 10% to 90% measurement on V_{OUT} and does not apply for CT less than 100 pF. Use Table 2 to determine rise times for when CT is greater or equal to 100 pF.

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 2 contains rise time values measured on a typical device.

Table 2. Rise Time Table

CTx (pF)	RISE TIME (μs) 10% - 90%, $C_L = 0.1 \mu\text{F}$, $C_{\text{IN}} = 1 \mu\text{F}$, $R_L = 10 \Omega$ Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT						
	VIN = 5 V	VIN = 3.3 V	VIN = 2.5 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.0 V
0	135	95	75	60	50	45	40
220	650	455	350	260	220	185	160
470	1260	850	655	480	415	340	300
1000	2540	1680	1300	960	810	660	560
2200	5435	3580	2760	2020	1715	1390	1220
4700	12050	7980	6135	4485	3790	3120	2735
10000	26550	17505	13460	9790	8320	6815	5950

As the voltage across the capacitor approaches the capacitor rated voltage, the effective capacitance reduces. Depending on the dielectric material used, the voltage coefficient changes. See Table 3 for the recommended minimum voltage rating for the CT capacitor.

Table 3. Recommended CT Capacitor Voltage Rating

VIN (V)	RECOMMENDED CT CAPACITOR VOLTAGE RATING (V) ⁽¹⁾
1 V to 1.2 V	10
1.2 V to 4 V	16
4 V to 5.5 V	20

(1) If using $V_{\text{IN}} = 1.2 \text{ V}$ or 4 V, it is recommended to use the higher voltage rating.

8.4 Device Functional Modes

Table 4 describes the connection of the VOUT pin depending on the state of the ON pin.

Table 4. VOUT Connection

ON	QOD Configuration	TPS22918-Q1
L	QOD pin connected to VOUT with R_{EXT}	GND (via $R_{\text{EXT}} + R_{\text{PD}}$)
L	QOD pin tied to VOUT directly	GND (via R_{PD})
L	QOD pin left open	Open
H	Any valid QOD configuration	VIN

9 Application and Implementation

NOTE

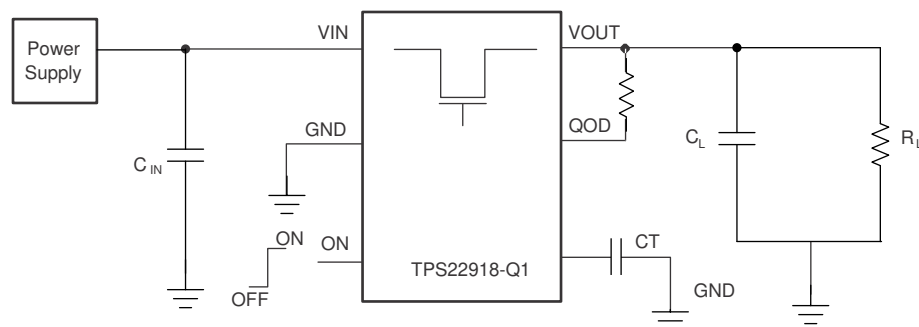
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available in the product page of this device on www.ti.com (See the [デバイス・サポート](#) section for more information).

9.2 Typical Application

This typical application demonstrates how the TPS22918-Q1 can be used to power downstream modules.



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Figure 23. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the input parameters listed in [Table 5](#).

Table 5. Design Parameter

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5 V
Load current	2 A
C_L	22 μ F
t_F	4 ms
Maximum acceptable inrush current	400 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between VIN and GND. A 1 μ F ceramic capacitor, C_{IN} , placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.2.2.2 Output Capacitor (C_L) (Optional)

Because of the integrated body diode in the MOSFET, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.2.2.3 Shutdown Sequencing During Unexpected System Power Loss

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22918-Q1, adding a load switch to each power rail can be used to manage the power down sequencing in the event of an unexpected system power loss (battery removal). To determine the QOD values for each load switch, first confirm the power down order of the device this is wished to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down. Next, refer to [Table 1](#) in the [Quick Output Discharge \(QOD\)](#) section to determine appropriate C_{OUT} and R_{QOD} values for each power rail's load switch so that the load switches' fall times correspond to the order in which they need to be powered down. In the above example, make sure this power rail's fall time to be 4 ms. Using [Equation 2](#), to determine the appropriate R_{QOD} to achieve our desired fall time. Because fall times are measured from 90% of V_{OUT} to 10% of V_{OUT} , [Equation 2](#) becomes [Equation 4](#).

$$.5 V = 4.5 V \times e^{-(4 \text{ ms}) / (R \times (22 \mu\text{F}))} \quad (4)$$

$$R_{QOD} = 83.333 \Omega \quad (5)$$

Refer to [Figure 7](#), R_{PD} at $V_{IN} = 5 V$ is approximately 25 Ω . Using [Equation 1](#), the required external QOD resistance can be calculated as shown in [Equation 6](#).

$$83.333 \Omega = 25 \Omega + R_{EXT} \quad (6)$$

$$R_{EXT} = 58.333 \Omega \quad (7)$$

[Figure 24](#) through [Figure 29](#) are scope shots demonstrating an example of the QOD functionality when power is removed from the device (both ON and VIN are disconnected simultaneously). The input voltage is decaying in all scope shots below.

- Initial $V_{IN} = 3.3 V$
- QOD = Open, 500 Ω , or shorted to VOUT
- $C_L = 1 \mu\text{F}$, 10 μF
- V_{OUT} is left floating

NOTE: V_{IN} may appear constant in some figures. This is because the time scale of the scope shot is too small to show the decay of C_{IN} .

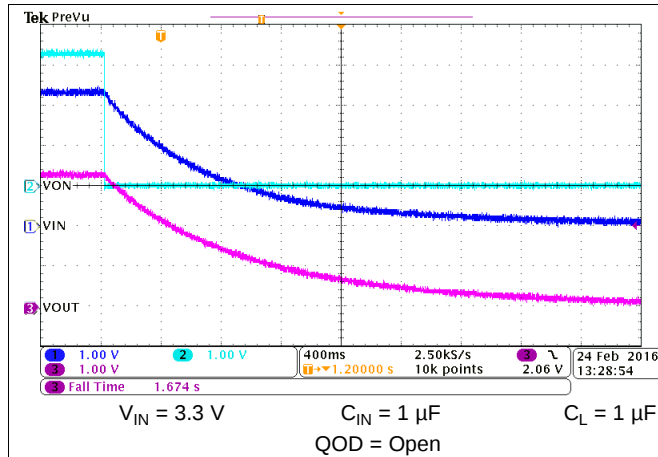


Figure 24. Fall Time (t_F) at $V_{IN} = 3.3\text{ V}$

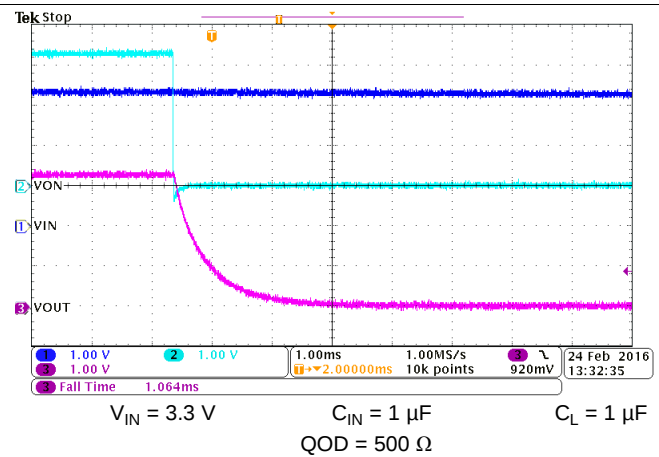


Figure 25. Fall Time (t_F) at $V_{IN} = 3.3\text{ V}$

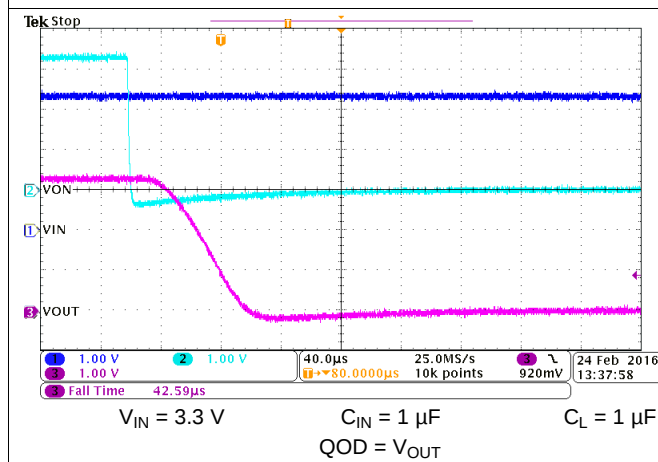


Figure 26. Fall Time (t_F) at $V_{IN} = 3.3\text{ V}$

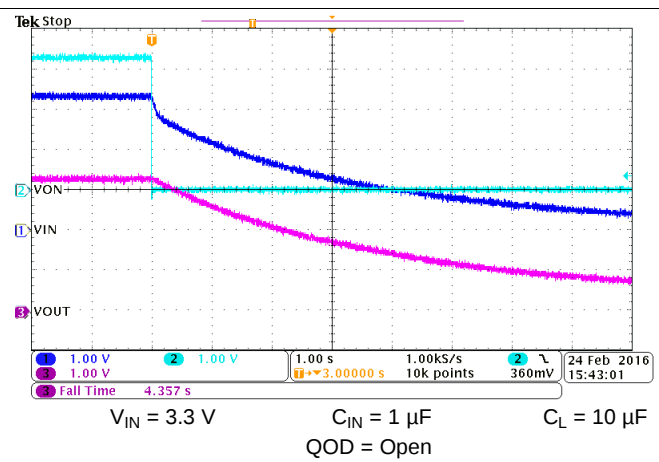


Figure 27. Fall Time (t_F) at $V_{IN} = 3.3\text{ V}$

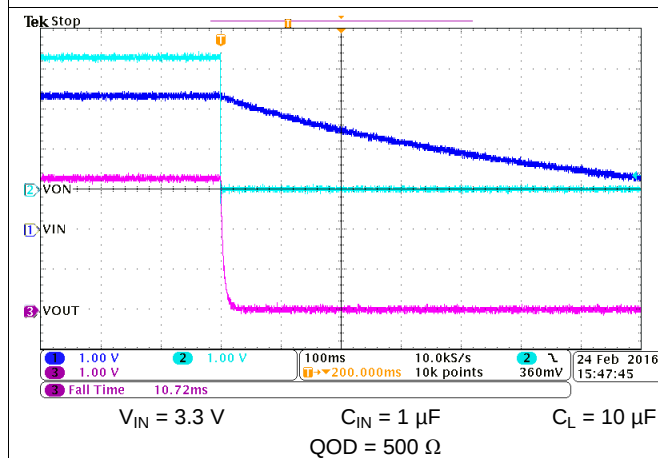


Figure 28. Fall Time (t_F) at $V_{IN} = 3.3\text{ V}$

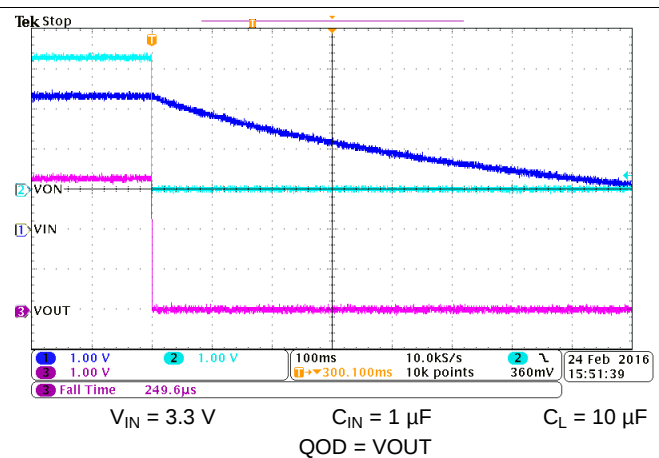


Figure 29. Fall Time (t_F) at $V_{IN} = 3.3\text{ V}$

9.2.2.4 V_{IN} to V_{OUT} Voltage Drop

The V_{IN} to V_{OUT} voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} conditions of the device. Refer to the R_{ON} specification of the device in the [Electrical Characteristics](#) table. When the R_{ON} of the device is determined based upon the V_{IN} conditions, use [Equation 8](#) to calculate the V_{IN} to V_{OUT} voltage drop.

ΔV is the $I_{LOAD} \times R_{ON}$

where

- ΔV is the voltage drop from V_{IN} to V_{OUT}
- I_{LOAD} is the load current
- R_{ON} is the On-resistance of the device for a specific V_{IN}

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated. (8)

9.2.2.5 Inrush Current

Use Equation 9 to determine how much inrush current is caused by the C_L capacitor.

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the capacitance on V_{OUT}
- dt is the output voltage rise time during the ramp up of V_{OUT} when the device is enabled
- dV_{OUT} is the change in V_{OUT} during the ramp up of V_{OUT} when the device is enabled

The appropriate rise time can be calculated using the design requirements and the inrush current equation. As the rise time (measured from 10% to 90% of V_{OUT}) is calculated, this is accounted in the dV_{OUT} parameter (80% of $V_{OUT} = 4$ V) as shown in Equation 10.

$$400 \text{ mA} = 22 \mu\text{F} \times 4 \text{ V} / dt \quad (10)$$

$$dt = 220 \mu\text{s} \quad (11)$$

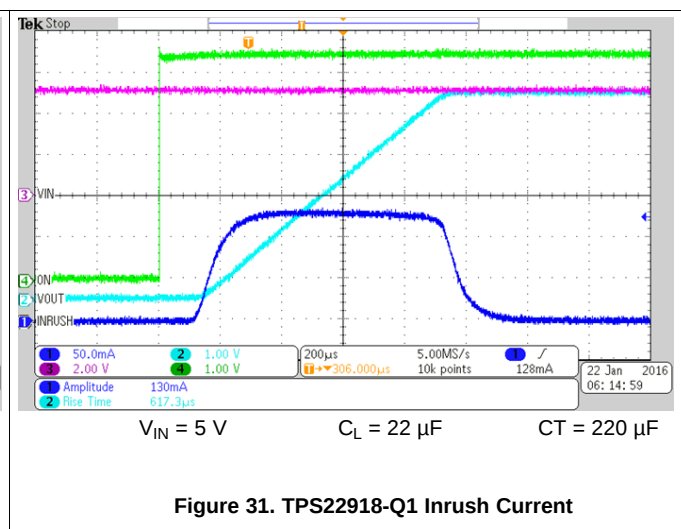
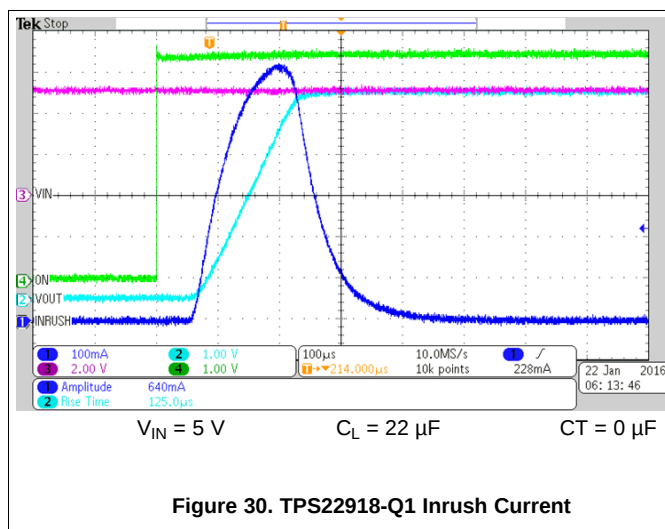
To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 220 μs . Referring to the Table 2 at $V_{IN} = 5$ V, $CT = 220 \mu\text{F}$ provides a typical rise time of 650 μs . Adding this rise time and voltage into Equation 9, yields Equation 12.

$$I_{Inrush} = 22 \mu\text{F} \times 4 \text{ V} / 650 \mu\text{s} \quad (12)$$

$$I_{Inrush} = 135 \text{ mA} \quad (13)$$

This inrush current can be seen in the Application Curves section. An appropriate C_L value must be placed on V_{OUT} such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

9.2.3 Application Curves



10 Power Supply Recommendations

The TPS22918-Q1 is designed to operate from a VIN range of 1 V to 5.5 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1- μ F bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 1 μ F may be sufficient.

11 Layout

11.1 Layout Guidelines

- VIN and VOUT traces must be as short and wide as possible to accommodate for high current.
- The VIN pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1 μ F ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- The VOUT pin must be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the VIN bypass capacitor of X5R or X7R dielectric rating. This capacitor must be placed as close to the device pins as possible.

11.2 Layout Example

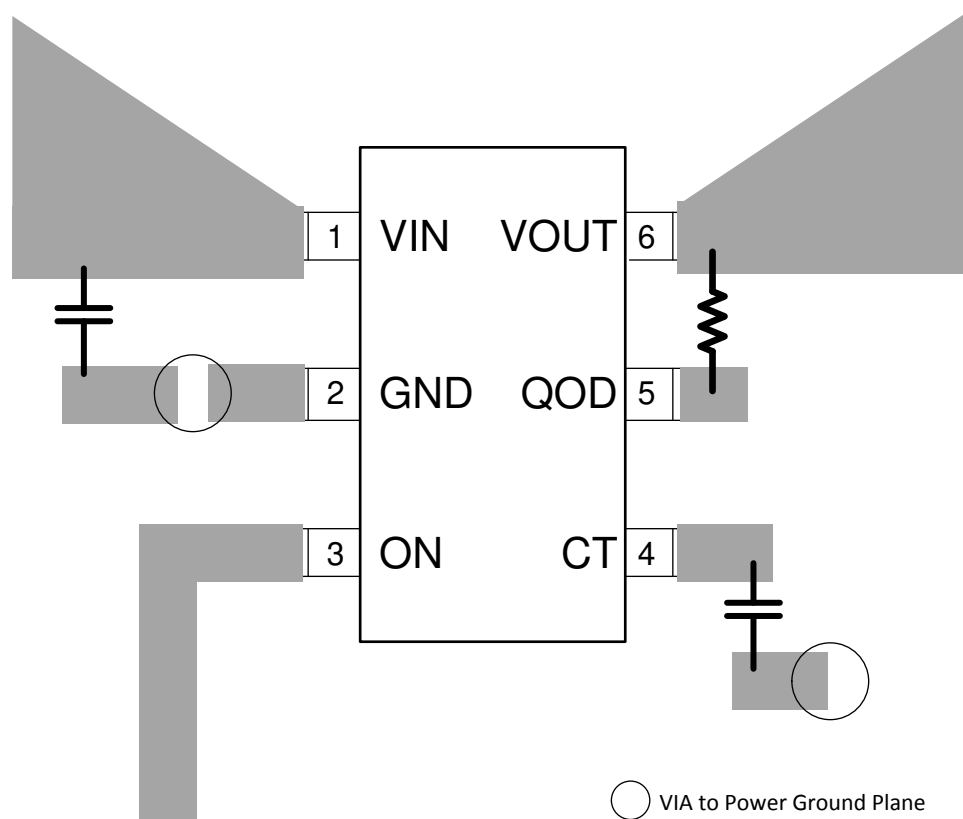


Figure 32. Recommended Board Layout

11.3 Thermal Considerations

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

Thermal Considerations (continued)

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(\max)}$ for a given output current and ambient temperature, use [Equation 14](#).

$$P_{D(\max)} = \frac{T_{J(\max)} - T_A}{\theta_{JA}} \quad (14)$$

Where:

$P_{D(\max)}$ is the maximum allowable power dissipation

$T_{J(\max)}$ is the maximum allowable junction temperature (150°C for the TPS22918-Q1)

T_A is the ambient temperature of the device

θ_{JA} is the junction to air thermal impedance. See the [Thermal Information](#) table. This parameter is highly dependent upon board layout.

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

TPS22918 PSpiceトランジェント・モデルについては、[SLVMBI6](#)を参照してください。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- 『TPS22918 5.5V、2A、50mΩ オン抵抗負荷スイッチ 評価基板』、[SLVUAP0](#)
- 『負荷スイッチの消費電力における静止電流とシャットダウン時電流』、[SLVA757](#)
- 『負荷スイッチのオン抵抗の基礎』、[SLVA771](#)

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

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12.7 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22918TDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	13NW	Samples
TPS22918TDBVTQ1	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	13NW	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22918TDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS22918TDBVTQ1	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

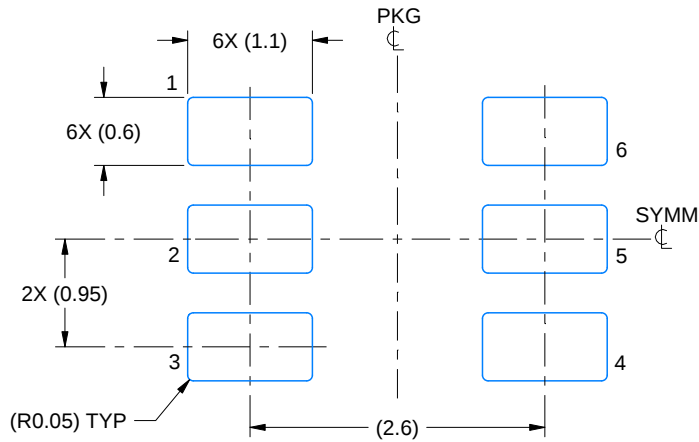
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22918TDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TPS22918TDBVTQ1	SOT-23	DBV	6	250	190.0	190.0	30.0

EXAMPLE BOARD LAYOUT

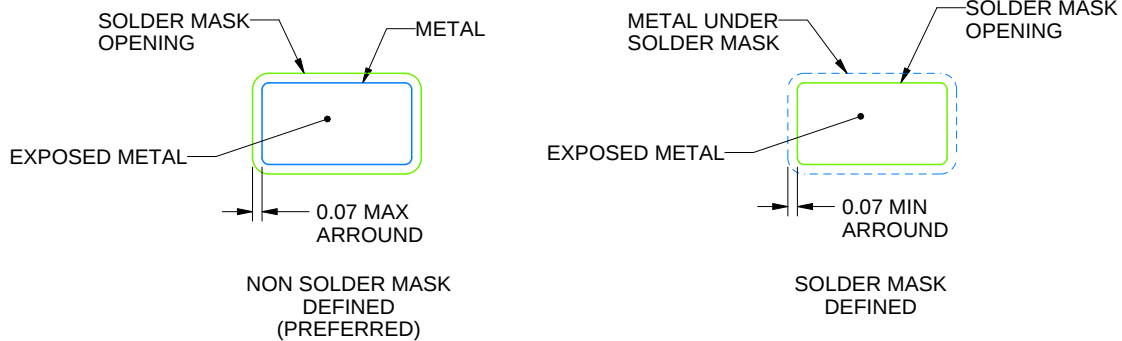
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

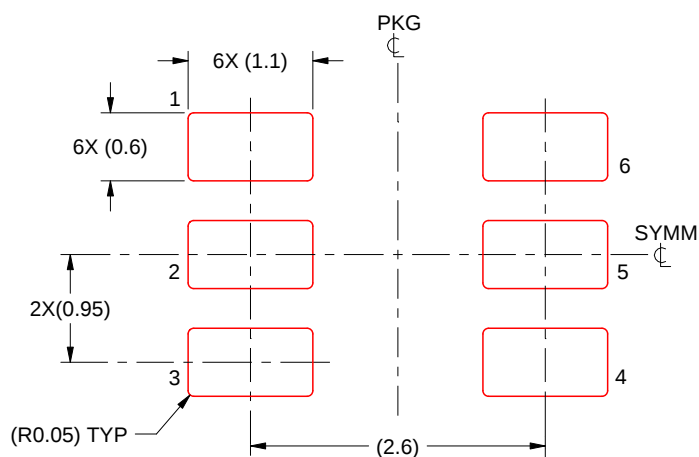
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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