TLV1805-Q1 40V、レール・ツー・レール入力、プッシュプル出力、シャットダウン機能付きの高電圧車載用コンパレータ

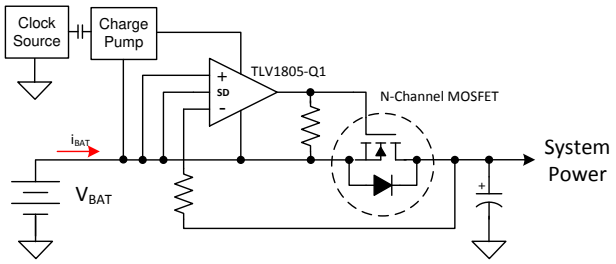
1 特長

- 次の結果で AEC-Q100 認定済み
  - デバイス温度グレード 1:動作時周囲温度 -40°C～+125°C
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC6
- 電源電圧範囲：3.3V～40V
- 低い静止電流: 135µA
- ピーク電流の大きいプッシュプル出力
- 位相反転保護機能付きのレール・ツー・レール入力
- 内蔵ヒステリシス：14mV
- 伝搬遅延時間：250ns
- 低い入力オフセット電圧：500µV
- ハイ・インピーダンス出力のシャットダウン
- パワーオン・リセット (POR)
- SOT-23-6 パッケージ

2 アプリケーション

- 逆電流保護のスマート・ダイオード・コントローラ
- 過電圧、低電圧、過電流の検出
- OR 接続 MOSFET コントローラ
- MOSFET ゲート・ドライバ
- 高電圧発振器
- システム監視
  - 車載用インフォテインメントおよびクラスタ
  - HEV/EV とパワートレイン

N チャネル MOSFET による逆電流保護



3 概要

TLV1805-Q1 高電圧コンパレータは、広い電源電圧範囲、プッシュプル出力、レール・ツー・レール入力、小さい静止電流、シャットダウン機能、高速な出力応答を持ち合わせた独自の製品です。これらすべての特長から、このコンパレータはスマート・ダイオード・コントローラの逆電流保護、過電流検出、およびプッシュプル出力段を使用して P チャネルまたは N チャネル MOSFET スイッチのゲートを駆動する過電圧保護回路など、正または負の電圧レールでの検出を必要とするアプリケーションに適しています。

高電圧コンパレータとしては珍しく、ピーク電流の大きいプッシュプル出力段には、どちらの電源レールへの負荷も高いエッジ速度でアクティブに駆動できるという利点があります。これは、予期しない高電圧電源へのホストの接続/切断を制御するために、MOSFET ゲートを迅速に HIGH または LOW に駆動する必要があるアプリケーションでは特に重要です。その他にも、低い入力オフセット電圧、低い入力バイアス電流、High-Z のシャットダウンなどの特長を備えているため、TLV1805-Q1 は広範なアプリケーションを柔軟に処理できます。パワー・オン・リセットにより、電源オン時の誤出力が防止されます。

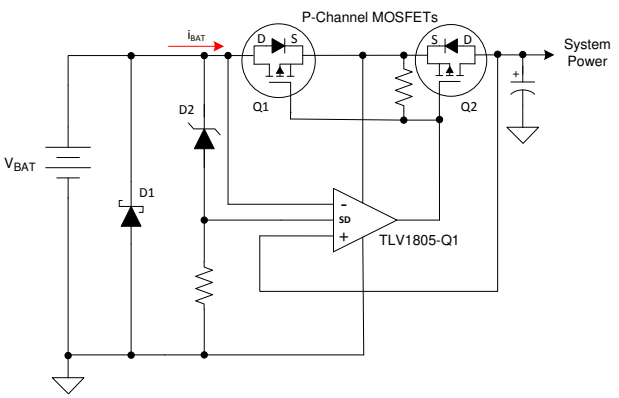
TLV1805-Q1 は 6 ピン SOT-23 パッケージで AEC-Q100 認定済みであり、車載用グレード 1 温度範囲の -40°C～+125°C で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLV1805-Q1	SOT-23 (6)	1.60mm×2.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

P チャネル MOSFET による逆電流および過電圧保護



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (May 2019) から Revision B に変更 **Page**

- 「アプリケーション」一覧にリンクを 追加 ... 1
- 変更 Output High and Low vs Supply Graphs ... 10

2018年8月発行のものから更新 **Page**

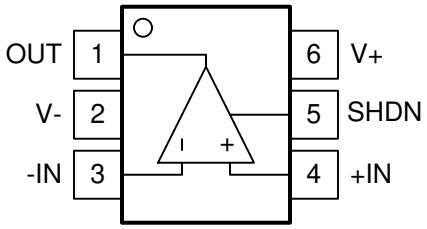
- 事前情報から量産データに 変更 ... 1

Revision A (May 2019) から Revision B に変更 **Page**

- 「アプリケーション」一覧にリンクを 追加 ... 1
- 変更 Output High and Low vs Supply Graphs ... 10

5 Pin Configuration and Functions

TLV1805-Q1 DBV Package
6-Pin SOT-23
Top View



Note the reversed positions of the input pins. This differs from a similar popular pinout.

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN+	4	I	Noninverting input
IN–	3	I	Inverting input
OUT	1	O	Output
SHDN	5	I	Shutdown (active high)
V+	6	P	Positive (highest) power supply
V–	2	P	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	-0.3	42	V
Input pins (IN+, IN–)(2)	(V–) – 0.3	(V+) + 0.3	V
Shutdown pin (SHDN)(3)	(V–) – 0.3	(V–) + 5.5	V
Current into Input pins (IN+, IN–, SHDN)(2)		±10	mA
Output (OUT)	(V–) – 0.3	(V+) + 0.3	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 10 mA or less.
(3) Shutdown pin is diode-clamped to (V–). Input to SHDN that can swing more than 0.3 V below (V–) must be current-limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	3.3	40	V
Ambient temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV1805-Q1 DBV (SOT23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	166.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_S = 3.3 V to 40 V, V_{CM} = V_S / 2; T_A = 25°C (unless otherwise noted). Typical values are at V_S = 12 V and T_A = 25°C,V_{CM} = V_S / 2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIO	Input offset voltage	V_S = 3.3V, 12V and 40V	-4.5	±0.5	4.5	mV
		V_S = 3.3V, 12V and 40V, T_A = –40°C to +125°C	-6.5		6.5	
dV_{IO}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±2.5		µV/°C
V_{HYS}	Input hysteresis voltage			14		mV
V_{CM}	Common-mode voltage range	T_A = -40℃ to +125℃	(V–) – 0.2		(V+) + 0.2	V
I_B	Input bias current			0.05		pA
I_{OS}	Input offset current			0.05		pA
PSRR	Power-supply rejection ratio	V_{CM} = V-		95		dB
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+)		80		dB
V_{OL}	Voltage output swing from (V–)	I_{SINK} ≤ 5mA, input overdrive = –100 mV, V_S = 5V, T_A = –40°C to +125°C			300	mV
V_{OH}	Voltage output swing from (V+)	I_{SOURCE} ≤ 5mA, input overdrive = +100 mV, V_S = 5V, T_A = –40°C to +125°C			300	mV
Isc_source	Peak charging current (sourcing) with output shorted to V- (1)	Vs = 5 V to 40 V		100		mA
Isc_sink	Peak dis-charging current (sinking) with output shorted to V+ (1)	Vs = 5 V to 40 V		100		mA
I_Q	Quiescent current	V_S = 12 V, no load, V_{ID} = –0.1 V (output low), T_A = 25°C		135	200	µA
		V_S =12V to 40V no load, V_{ID} = –0.1 V (output low), T_A = –40°C to +125°C			400	µA
t_{OFF}	Time to enter shutdown	C_L = 15 pF		1.0		µs
t_{ON}	Time to exit shutdown	C_L = 15 pF		2.3		µs
V_{SD}	Shutdown input: voltage range (2)	V_s= 3.3 to 40V, T_A = -40 to 125 °C	0		5.5	V
V_{SD_VIH}	SHDN pin input high level	V_S = 3.3 V and 40V, T_A = -40 to 125 °C	2	1.35		V
V_{SD_VIL}	SHDN pin input low level	V_S = 3.3 V and 40V, T_A = -40 to 125 °C		0.65	0.4	V
I_{B-SDH}	SHDN bias current	V_S = V_{SD} = 5.5 V		0.015		nA
		V_S = 5 V, V_{SD} = 0 V		0.001		nA
I_{Q-SD}	Quiescent current (Shutdown)	V_S = 12V; T_S = 25°C; V_{SD} > $V_{SD\_VIH\ Min}$		9.5	13	µA

(1) Continuous short circuit can result in excessive heating and exceeding the maximum allowed junction temperature of 150°C. Please refer to the Maximum Output Current Derating curve in the Typical Operation Plots.
(2) The recommended voltage range if V_{SD} is independent of V_S.

6.6 Switching Characteristics

Typical values are at T_A = 25°C, V_S = 12 V, V_{CM} = V_S / 2; Input overdrive = 100 mV (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low (1)	C_L = 15 pF		250		ns
		C_L = 4 nF		450		ns
t_{PLH}	Propagation delay time, low-to-high (1)	C_L = 15 pF		250		ns
		C_L = 4 nF		500		ns
t_R	Rise time	20% to 80%, C_L = 15 pF		18		ns
		20% to 80%, C_L = 4 nF		0.3		µs
t_F	Fall time	20% to 80%, C_L = 15 pF		10		ns
		20% to 80%, C_L = 4 nF		0.26		µs
t_{START}	Power-up time (2)			45		µs

(1) High-to-low and low-to-high refers to the transition at the input.
(2) During power on, V_S must exceed 3.3 V for t_{ON} before the output is in a correct state.

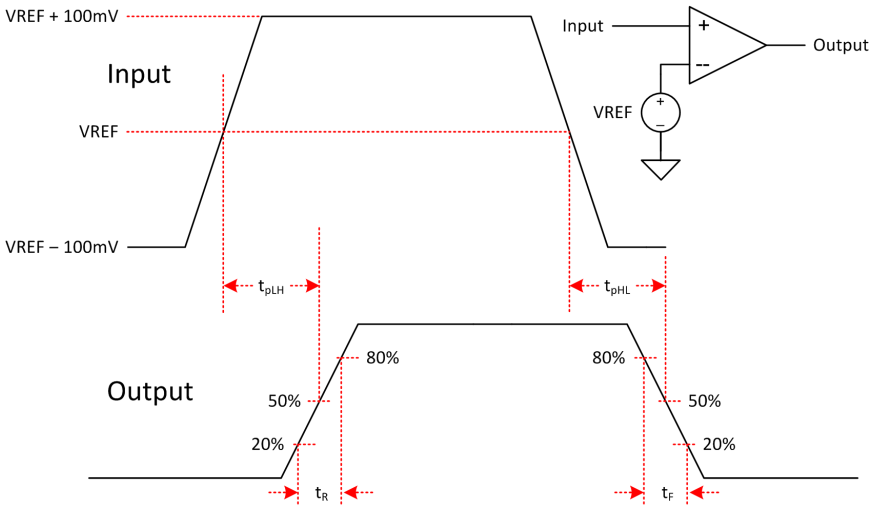


図 1. Propagation Delay

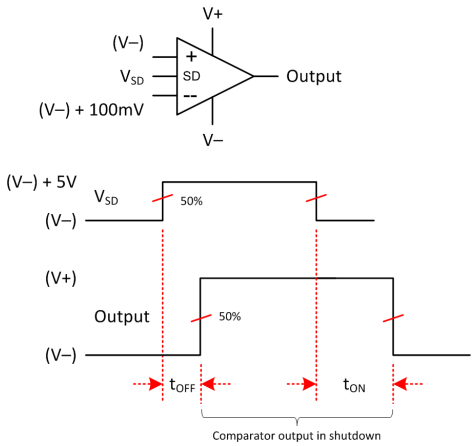


図 2. Shutdown Timing

6.7 Typical Characteristics

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)

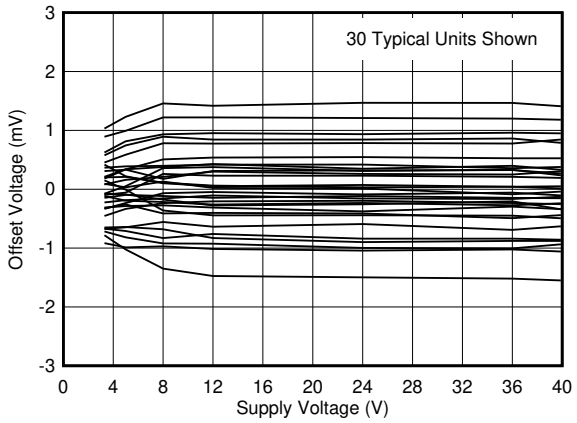


図 3. Input Offset Voltage vs. Supply Voltage

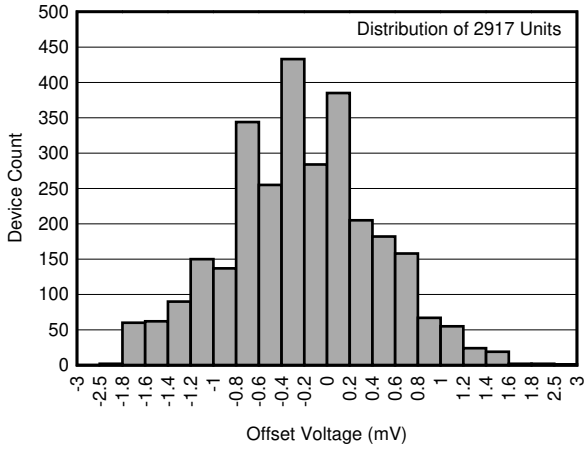


図 4. Offset Voltage Histogram

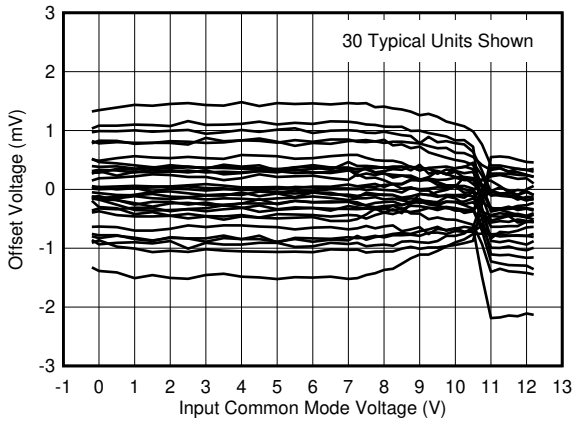


図 5. Offset Voltage vs. Common Mode

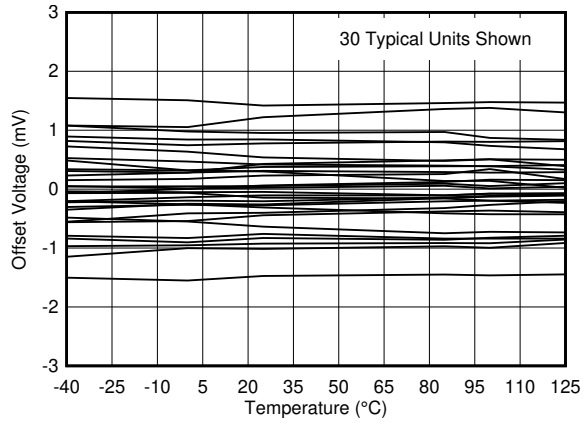
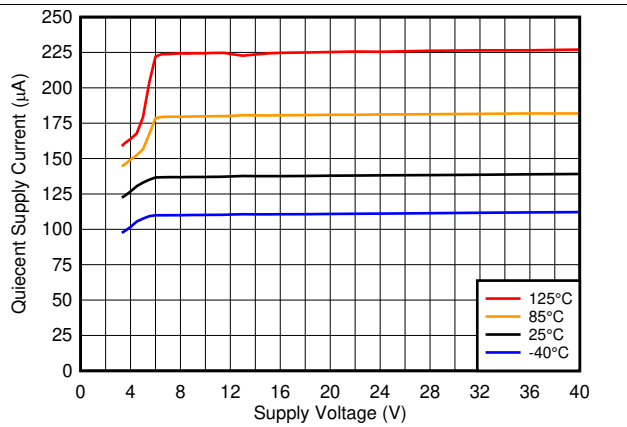
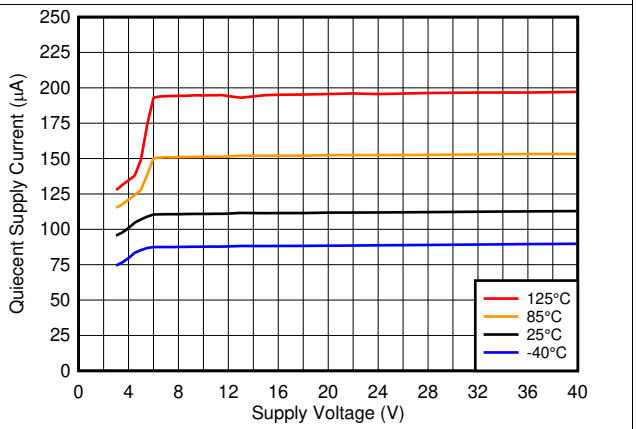


図 6. Offset Voltage vs Temperature



V_{CM} = V- Output Low (V_{ID} = -0.1 V)

図 7. Supply Current vs. Supply Voltage, Output Low



V_{CM} = V- Output High (V_{ID} = 0.1 V)

図 8. Supply Current vs. Temperature, Output High

Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)

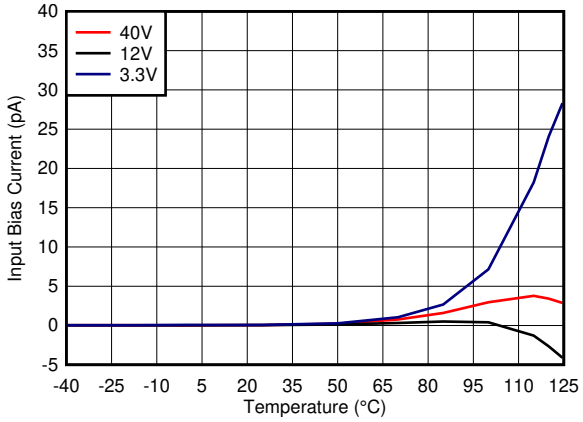


図 9. Input Bias Current vs. Temperature

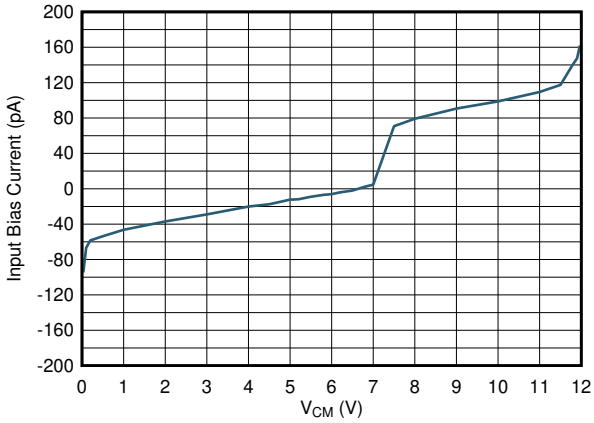


図 10. Input Bias Current vs. Common Mode, 125°C

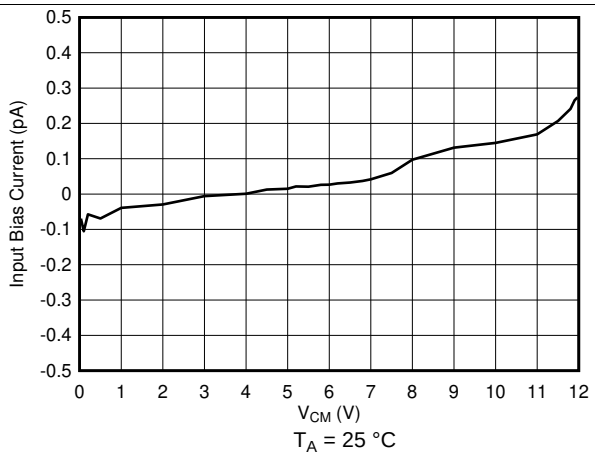


図 11. Input Bias Current vs. Common Mode, 25°C

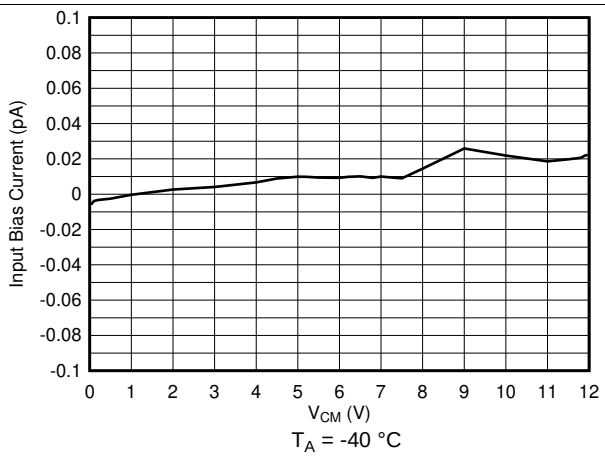


図 12. Input Bias Current vs. Common Mode, -40°C

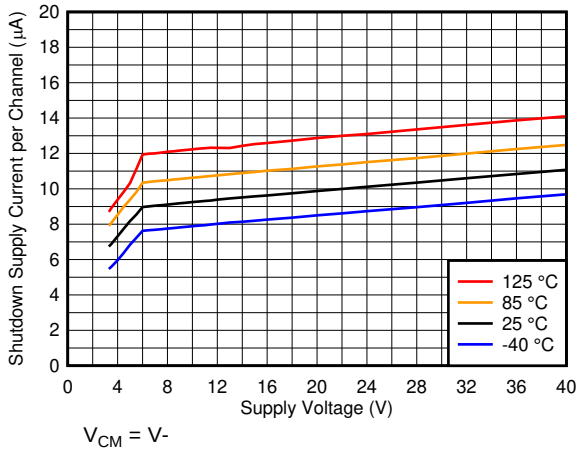


図 13. Shutdown Supply Current vs. Supply Votlage

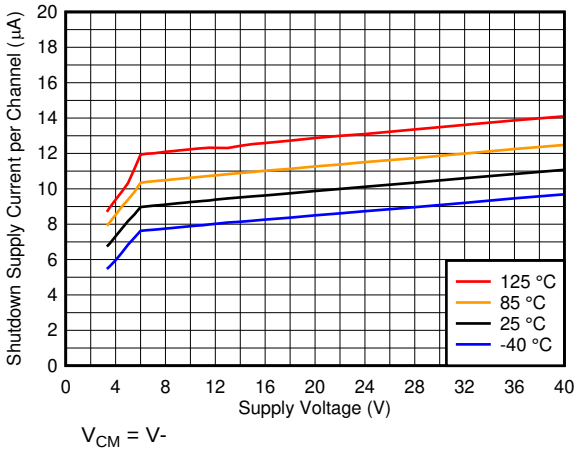


図 14. Shutdown Supply Current vs. Supply Votlage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)

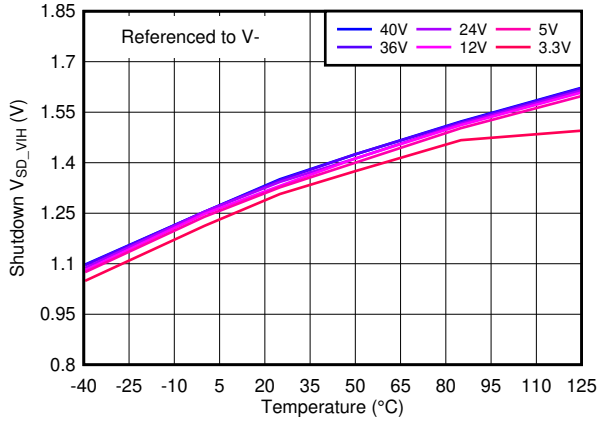


図 15. Shutdown Voltage High Threshold vs. Temperature

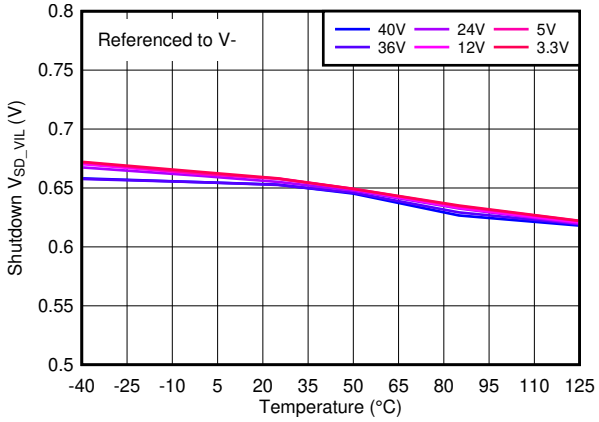


図 16. Shutdown Voltage Low Threshold vs. Temperature

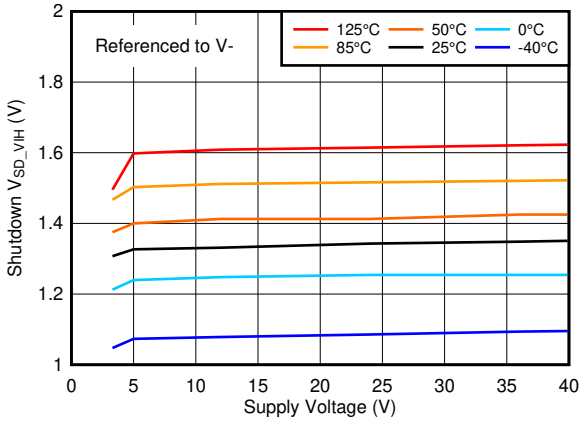


図 17. Shutdown Voltage High Threshold vs. Supply Voltage

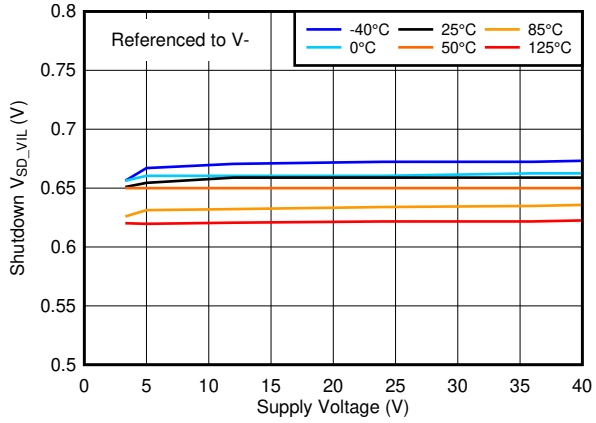


図 18. Shutdown Voltage Low Threshold vs. Supply Voltage

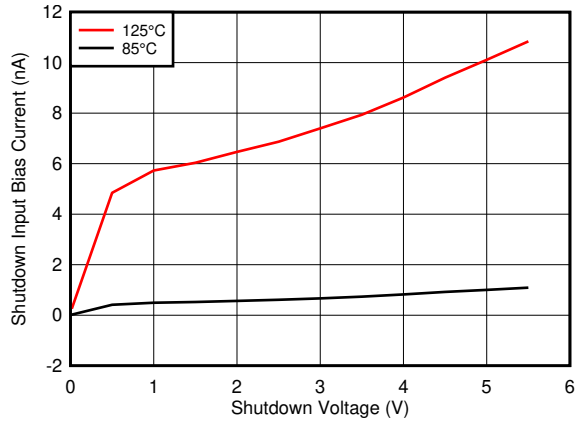


図 19. Shutdown Input Bias Current vs. Shutdown Input Voltage, High Temperatures

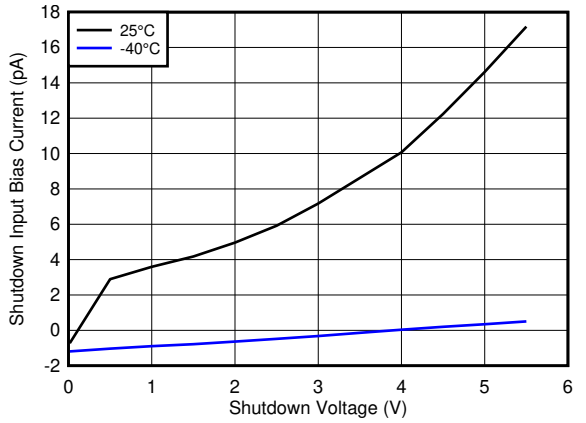


図 20. Shutdown Input Bias Current vs. Shutdown Input Voltage, Low Temperatures

Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)

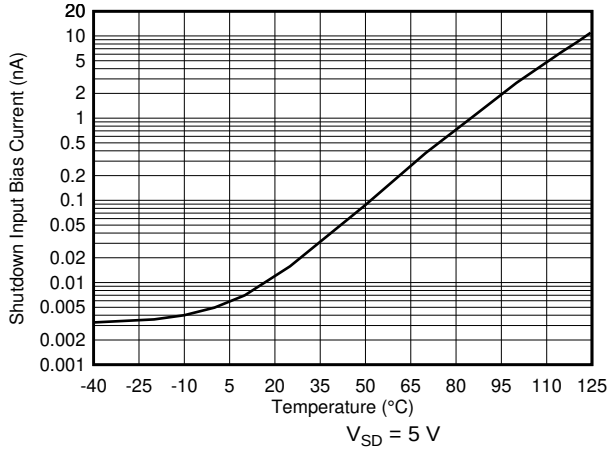


図 21. Shutdown Input Bias Current vs. Temperature

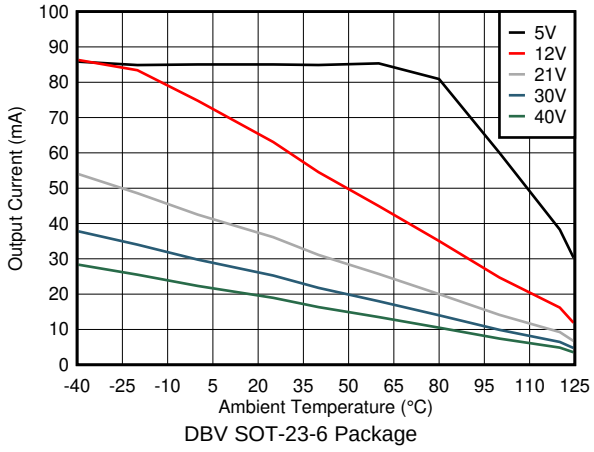


図 22. Maximum Continuous Output Current vs. Ambient Temperature

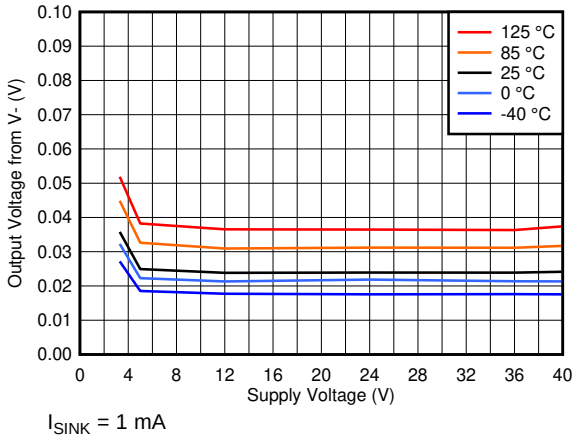


図 23. Output Low Voltage vs. Supply Voltage

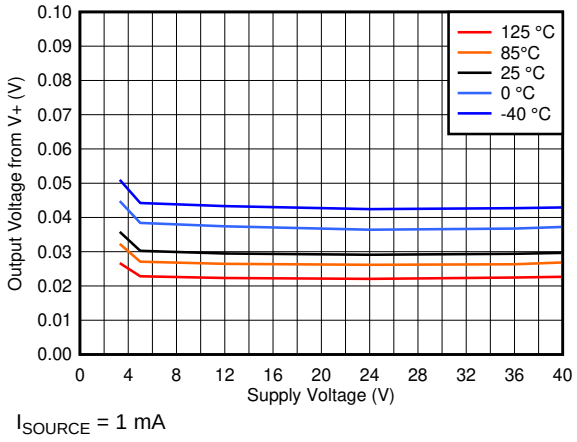


図 24. Output High Voltage vs. Supply Voltage

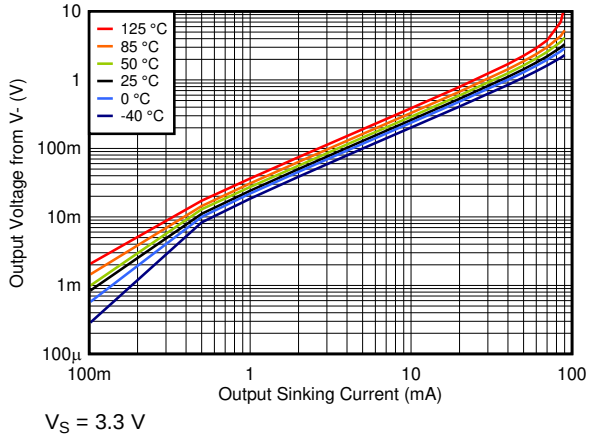


図 25. Output Voltage vs. Output Sinking Current at 3.3V

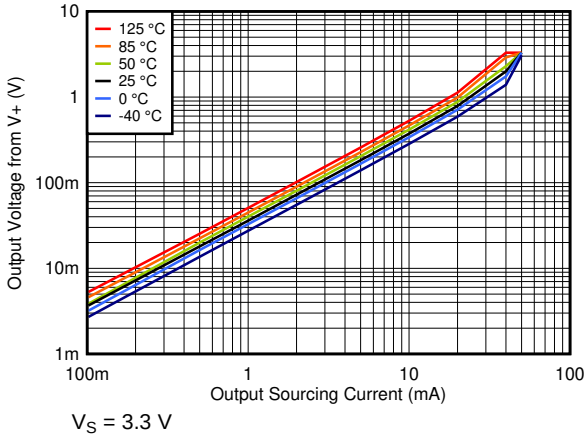
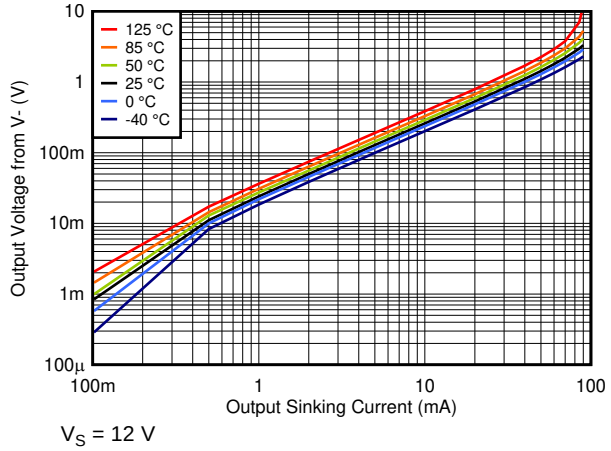


図 26. Output Voltage vs. Output Sourcing Current at 3.3V

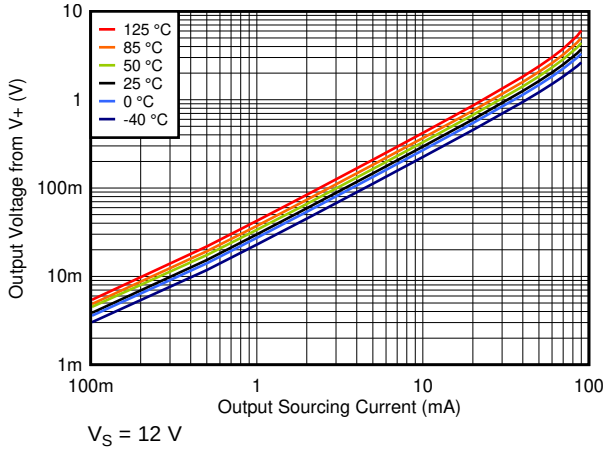
Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)



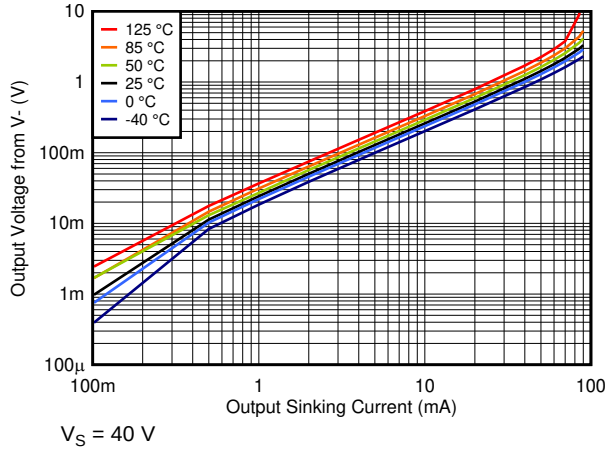
V_S = 12 V

図 27. Output Voltage vs. Output Sinking Current at 12V



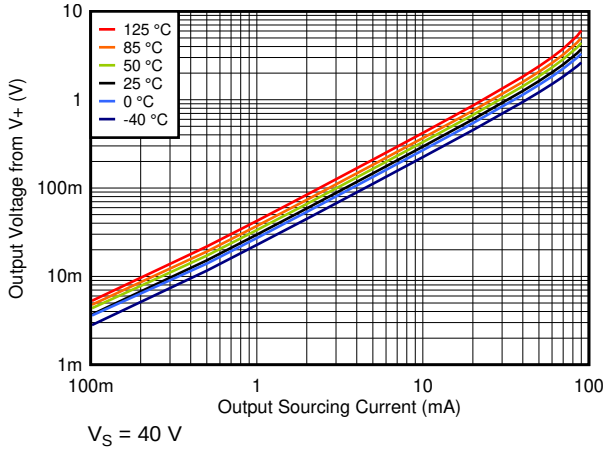
V_S = 12 V

図 28. Output Voltage vs. Output Sourcing Current at 12V



V_S = 40 V

図 29. Output Voltage vs. Output Sinking Current at 40V



V_S = 40 V

図 30. Output Voltage vs. Output Sourcing Current at 40V

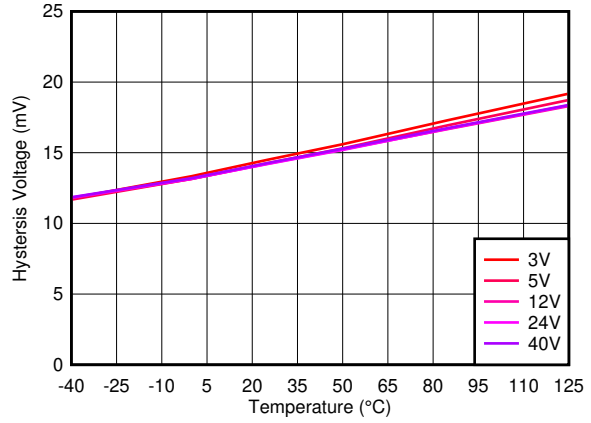


図 31. Hysteresis vs. Temperature

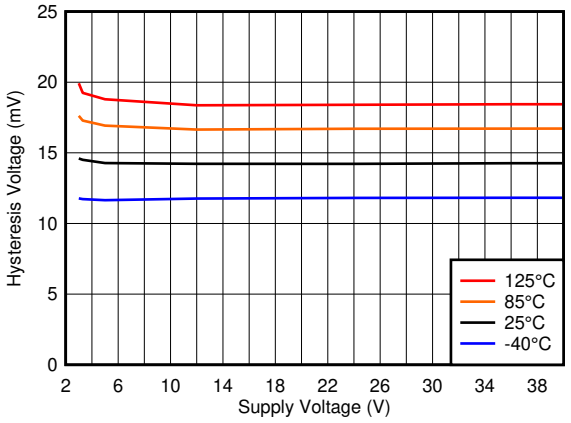


図 32. Hysteresis vs. Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)

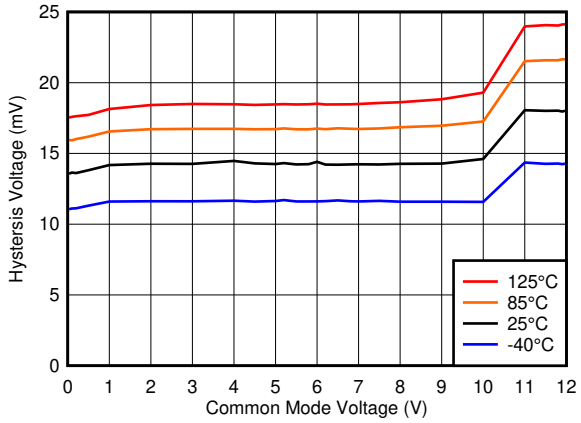


図 33. Hysteresis vs Common-Mode Voltage

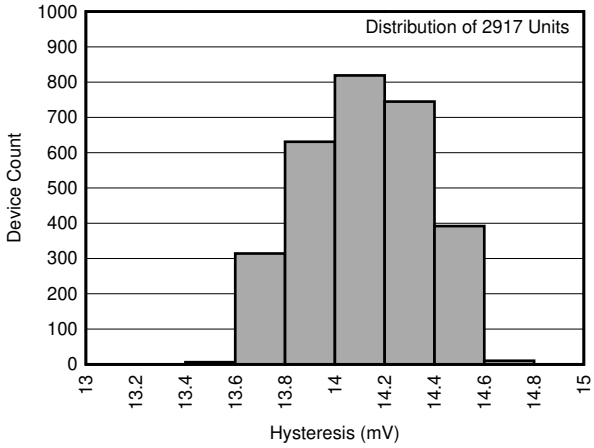
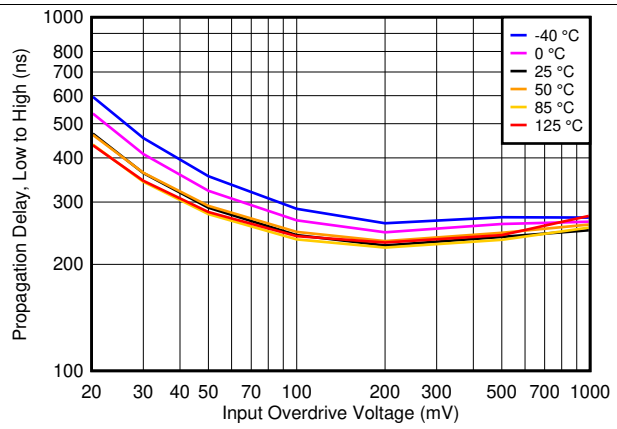
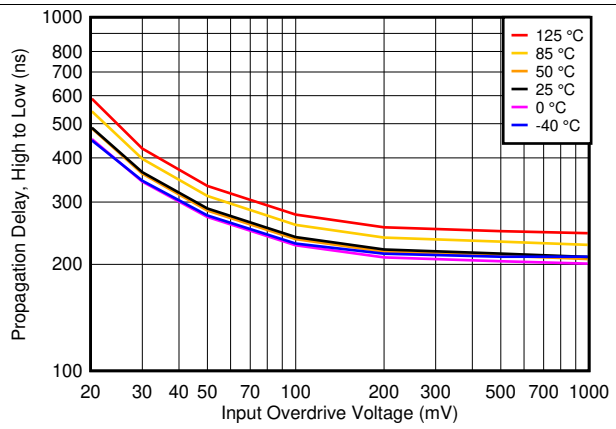


図 34. Hysteresis Histogram



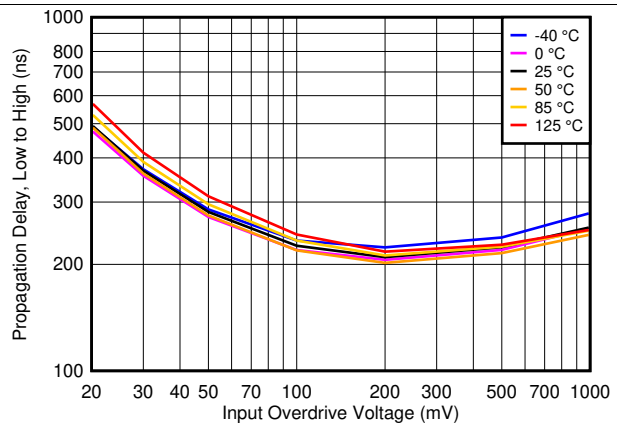
V_S = 3.3 V C_L = 15pF

図 35. T_{PLH} Response Time vs. Overdrive at 3.3V



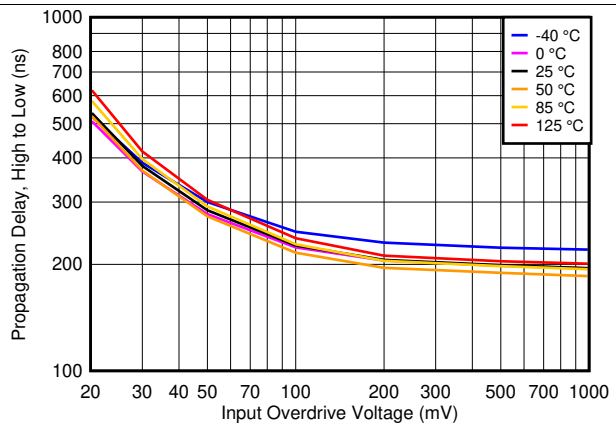
V_S = 3.3 V C_L = 15pF

図 36. T_{PHL} Response Time vs. Overdrive at 3.3V



V_S = 5 V C_L = 15pF

図 37. T_{PLH} Response Time vs. Overdrive at 5V



V_S = 5 V C_L = 15pF

図 38. T_{PHL} Response Time vs. Overdrive at 5V

Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)

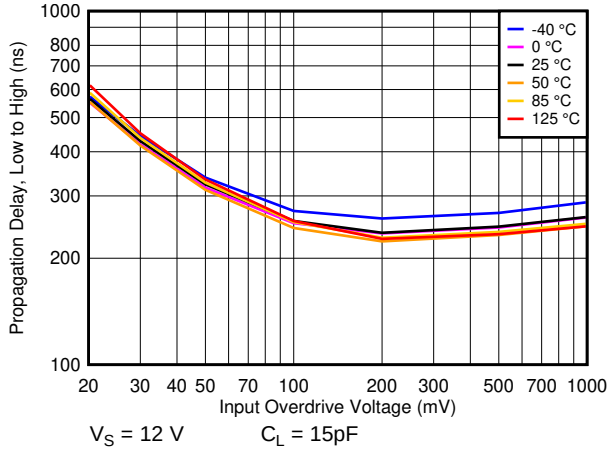


図 39. T_{PLH} Response Time vs. Overdrive at 12V

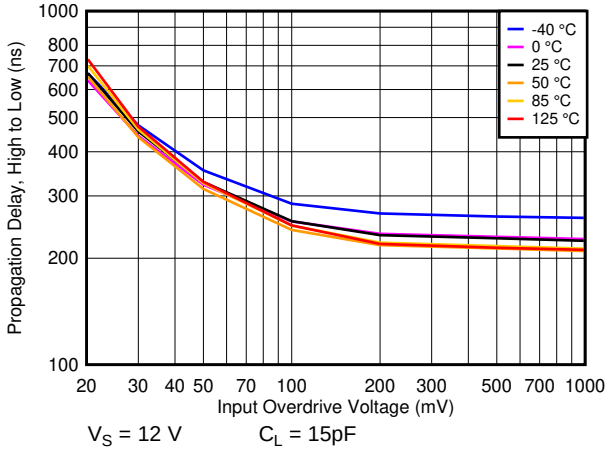


図 40. T_{PHL} Response Time vs. Overdrive at 12V

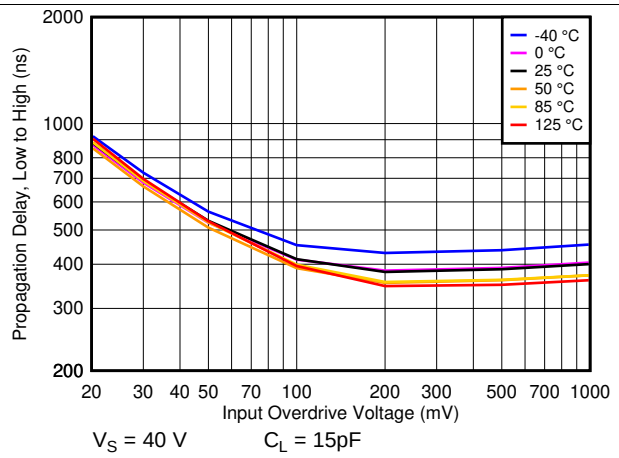


図 41. T_{PLH} Response Time vs. Overdrive at 40V

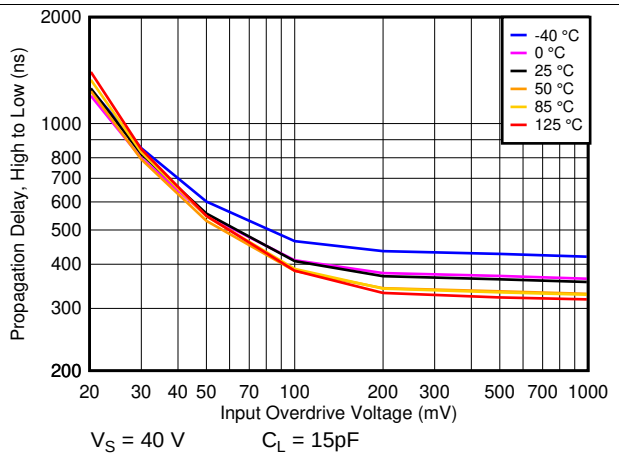


図 42. T_{PHL} Response Time vs. Overdrive at 40V

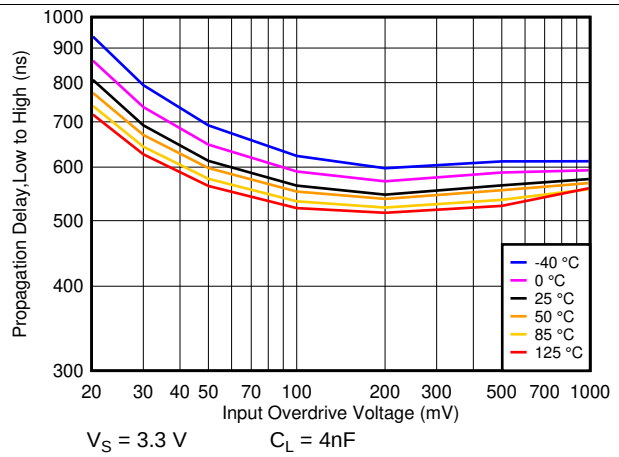


図 43. T_{PLH} Response Time vs. Overdrive at 3.3V

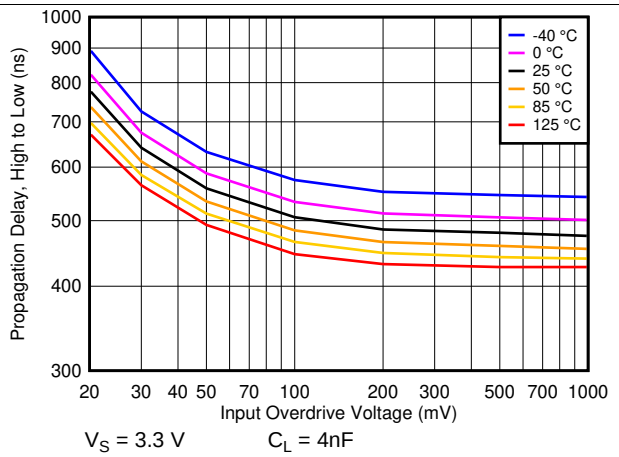


図 44. T_{PHL} Response Time vs. Overdrive at 3.3V

Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)

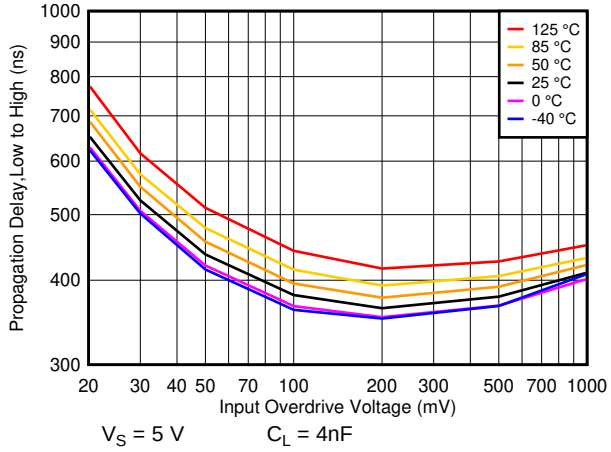


図 45. T_{PLH} Response Time vs. Overdrive at 5V

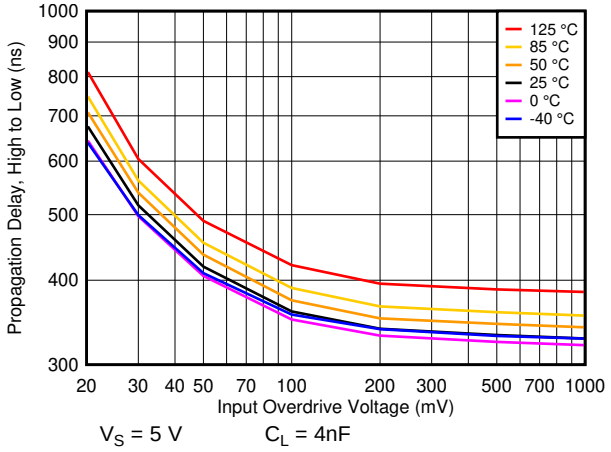


図 46. T_{PHL} Response Time vs. Overdrive at 5V

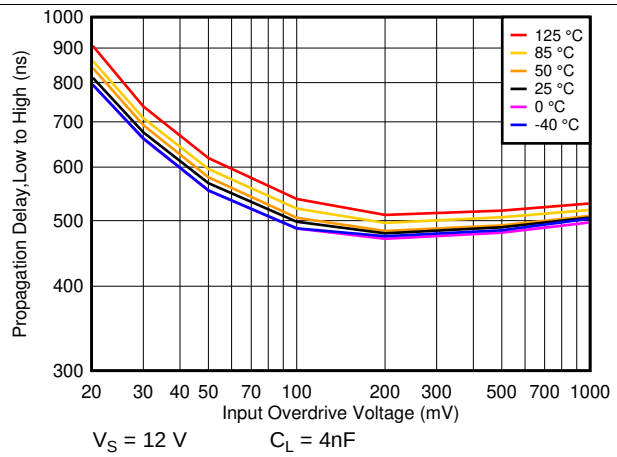


図 47. T_{PLH} Response Time vs. Overdrive at 12V

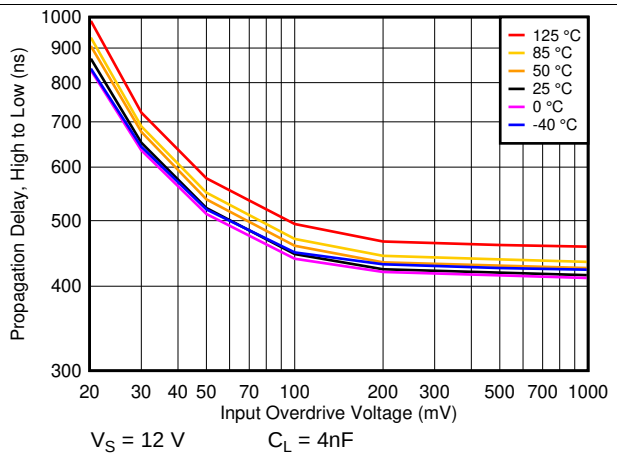


図 48. T_{PHL} Response Time vs. Overdrive at 12V

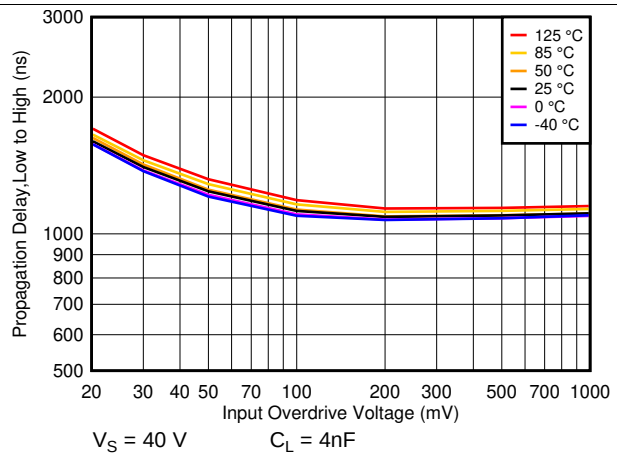


図 49. T_{PLH} Response Time vs. Overdrive at 40V

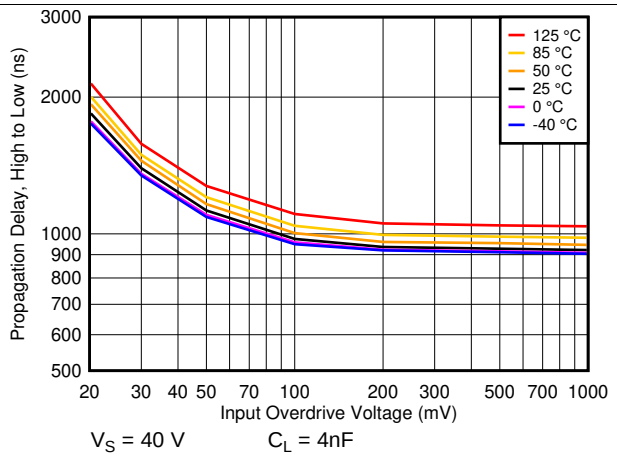
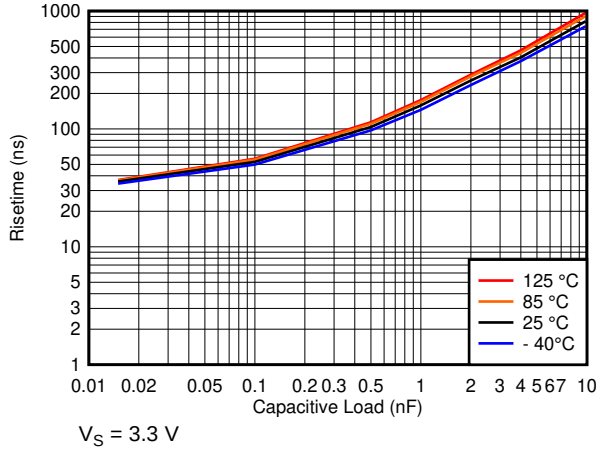


図 50. T_{PHL} Response Time vs. Overdrive at 40V

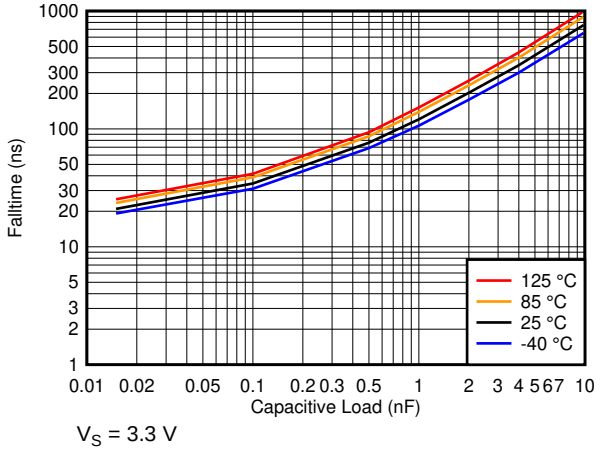
Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)



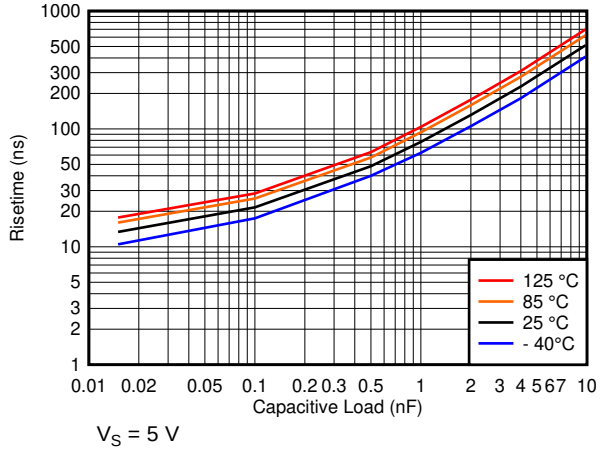
V_S = 3.3 V

図 51. t_{RISE} vs. Capacitive Load at 3.3V



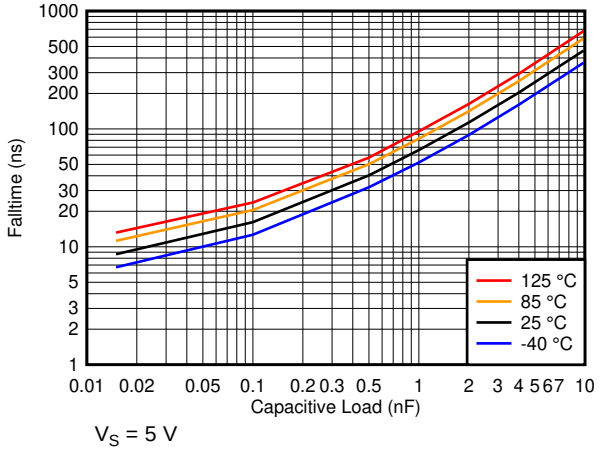
V_S = 3.3 V

図 52. t_{FALL} vs. Capacitive Load at 3.3V



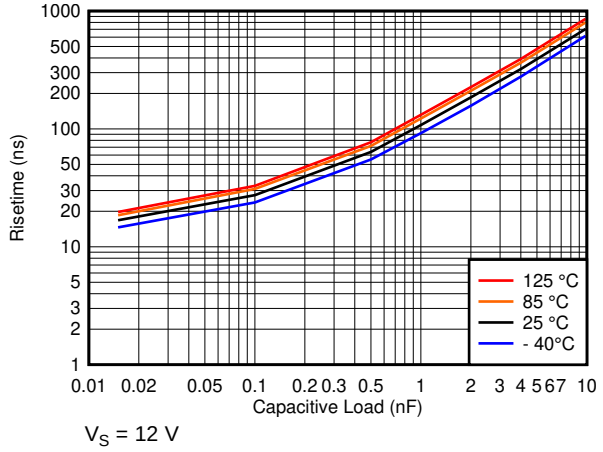
V_S = 5 V

図 53. t_{RISE} vs. Capacitive Load at 5V



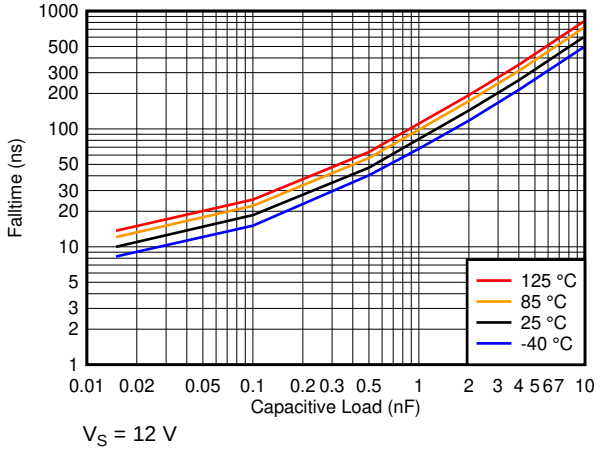
V_S = 5 V

図 54. t_{FALL} vs. Capacitive Load at 5V



V_S = 12 V

図 55. t_{RISE} vs. Capacitive Load at 12V

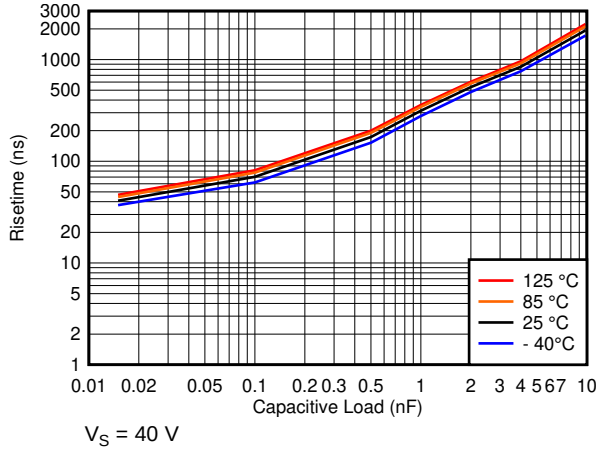


V_S = 12 V

図 56. t_{FALL} vs. Capacitive Load at 12V

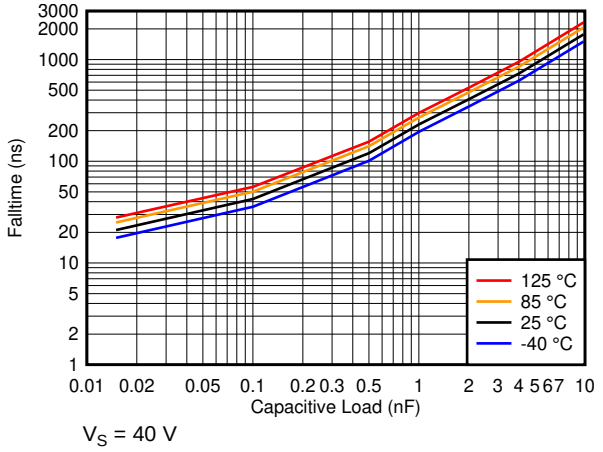
Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = V_S/2, and input overdrive = 100 mV (unless otherwise noted)



V_S = 40 V

図 57. t_{RISE} vs. Capacitive Load at 40V



V_S = 40 V

図 58. t_{FALL} vs. Capacitive Load at 40V

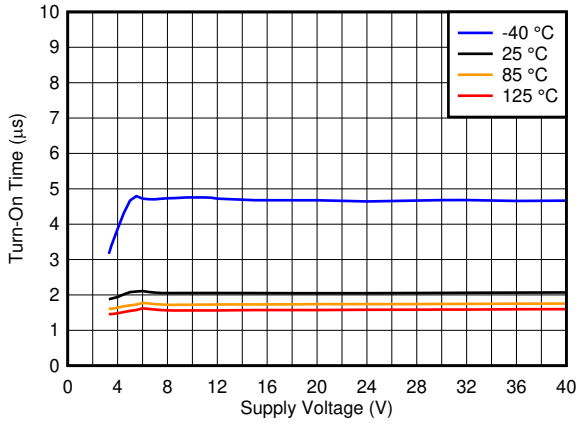


図 59. Turn-On Time vs Supply Voltage

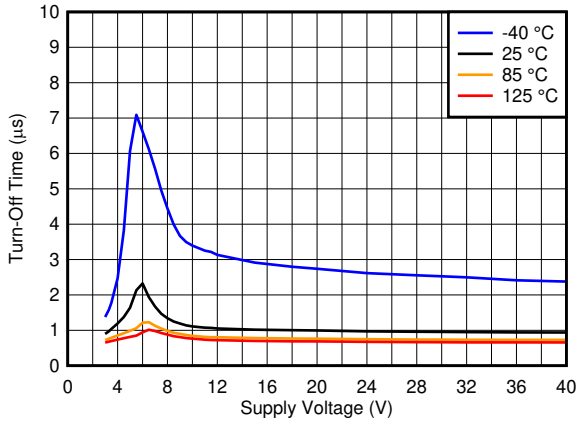


図 60. Turn-Off Time vs Supply Voltage

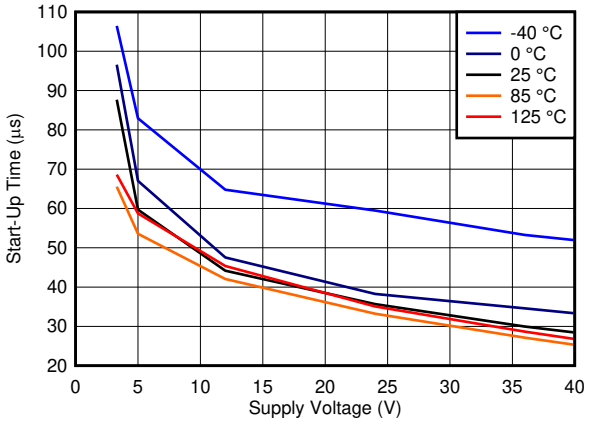


図 61. Start-Up Time vs Supply Voltage

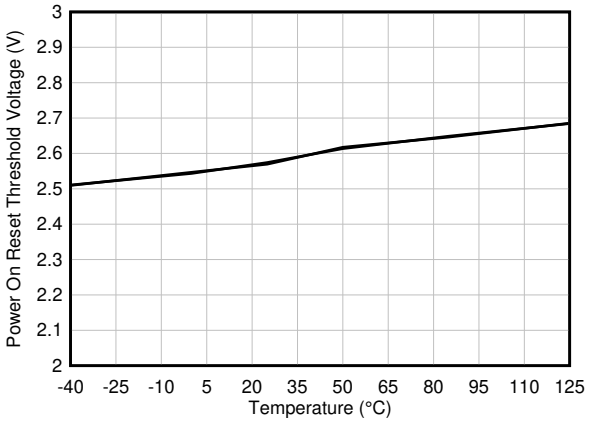


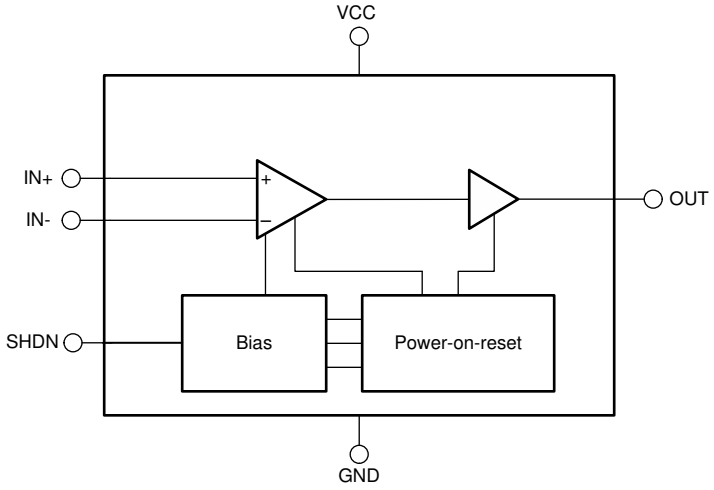
図 62. Power On Reset Voltage vs. Temperature

7 Detailed Description

7.1 Overview

The TLV1805-Q1 comparator features a rail-to-rail inputs with a push-pull output stage that operates at supply voltages as high as 40 V or ±20 V. The rail-to-rail input stage enables detection of signals close to the supply and ground while the push-pull output stage creates fast transition edges to either supply rail. A low supply current of 135 μA per channel with small, space-saving packages, makes these comparators versatile for use in a wide range of applications, from portable to industrial.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Rail to Rail Inputs

The TLV1805-Q1 comparator features a CMOS input with a common-mode range that includes both supply rails. The TLV1805-Q1 is designed to prevent phase inversion when the input pins exceed the supply voltage.

7.3.2 Power On Reset

The TLV1805-Q1 incorporates a power-on reset that holds the output in a High-Z state until the minimum operating supply voltage has been reached for at least 20μs. After this time the output will start responding to the inputs. This feature prevents false outputs during power-up and power-down.

7.3.3 High Power Push-Pull Output

The push-pull output stage, which is unique for high-voltage comparators, offers the advantage of allowing the output to actively drive the load to either supply rail with a fast edge rate. A high output sink and source peak current of over 100mA allows quickly charging and dis-cahrging capacitive loads such as cables and power MOSFET gates. Caution must be taken to ensure that the package power dissipation is not exceeded when switching at these high supply voltages. See 図 22 for the output current derating curve.

7.3.4 Shutdown Function

The TLV1805-Q1 has a logic level SHDN input. When the shutdown SHDN input is 1.4V above V-, the TLV1805-Q1 is disabled. When disabled, the output becomes high impedance (Hi-Z), and the supply current drops to below 10μA. The input bias current remains unchanged. Voltages may still be applied to the comparator inputs as long as V+ power is still applied and the applied input voltages are still within the specified input voltage range.

Feature Description (continued)

注意

The maximum voltage on the shutdown pin is +5.5V referred to V-, regardless of supply voltage. Connect the SHDN pin to V- if shutdown is not used. Do not float the SHDN pin.

A high value pull-up or pull-down resistor on the output may be required if a specific logic level is required during shutdown (when the output is High-Z). This prevents logic inputs from floating to illegal states when the comparator output is in High-Z mode.

Since the Shutdown threshold voltage is a tested parameter, the shutdown pin can also be used as a second comparison input to provide a secondary measurment, such as overvoltage monitoring, as shown in the *P-Channel Reverse Current Protection With Overvotlage Protection* circuit.

7.3.5 Internal Hysteresis

The TLV1805-Q1 contains 14mV of internal hysteresis.

The hysteresis transfer curve is shown in 図 63. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (14 mV for the TLV1805-Q1).

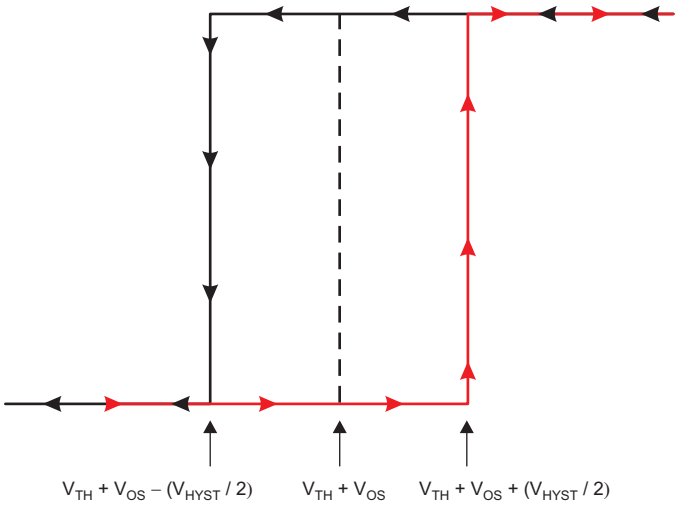


図 63. Hysteresis Transfer Curve

7.4 Device Functional Modes

7.4.1 External Hysteresis

External Hysteresis may be added to further improve response to noisy or slow-moving input signals.

Device Functional Modes (continued)

7.4.1.1 Inverting Comparator With Hysteresis

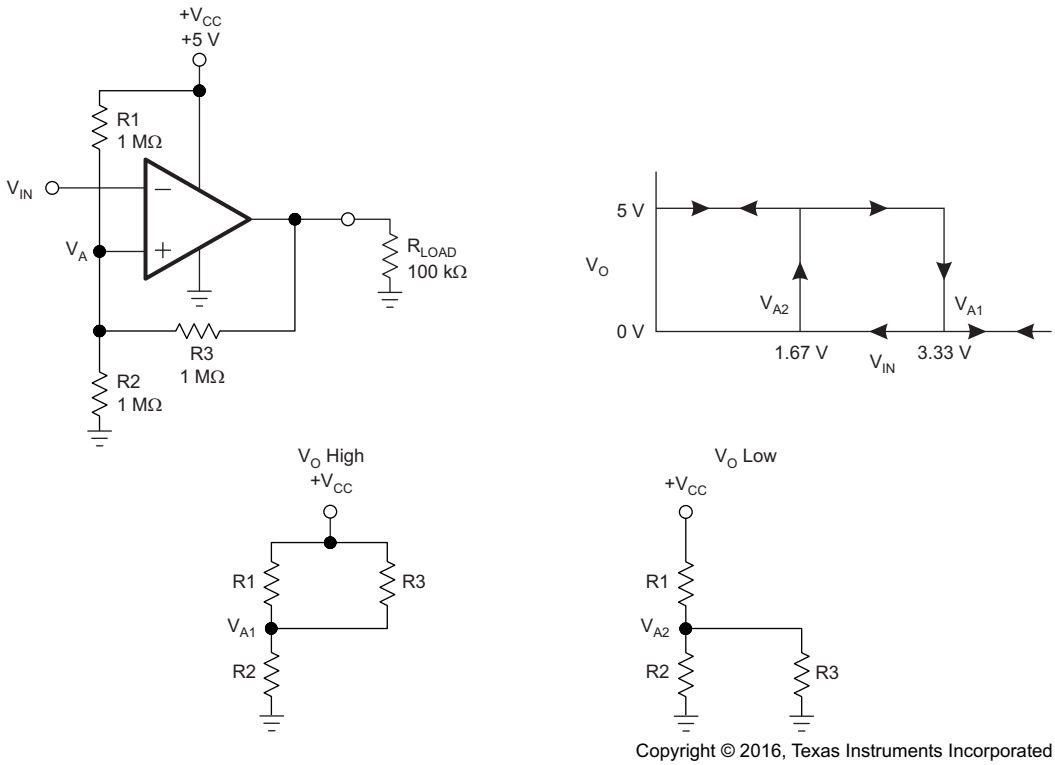


図 64. TLV1805-Q1 in an Inverting Configuration With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in 図 64. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. 式 1 defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. Use 式 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

式 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

Device Functional Modes (continued)

7.4.1.2 Noninverting Comparator With Hysteresis

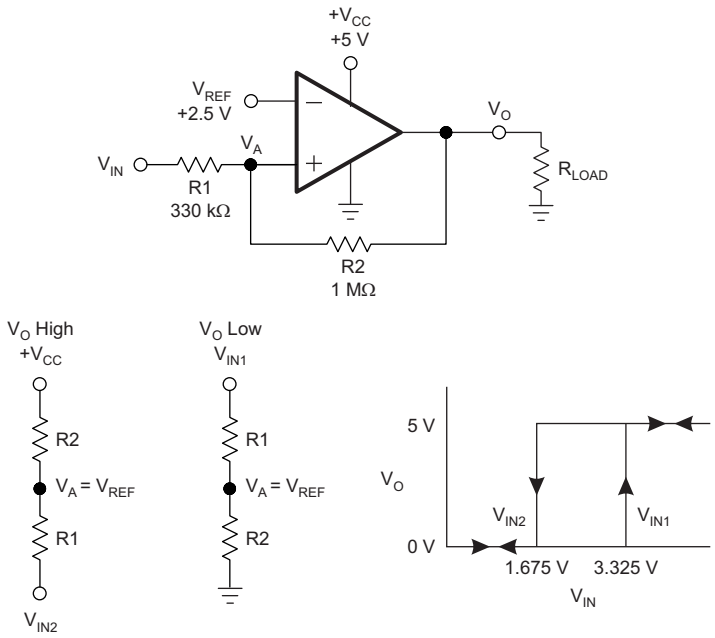


図 65. TLV1805-Q1 in a Noninverting Configuration With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in 図 65, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise to V_{IN1}. Use 式 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is high, the output is also high. For the comparator to switch back to a low state, V_{IN} must drop to V_{IN2} such that V_A is equal to V_{REF}. Use 式 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in 式 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV1805-Q1 family of devices can be used in a wide variety of applications, such as MOSFET gate drivers, zero crossing detectors, window comparators, over and undervoltage detectors, and high-side voltage sense circuits.

8.2 Typical Applications

Comparators are used to differentiate between two different signal levels. For example, a comparator differentiates between an over-temperature and normal-temperature condition. However, noise or signal variation at the comparison threshold causes multiple transitions. This application example sets upper and lower hysteresis thresholds to eliminate the multiple transitions caused by noise.

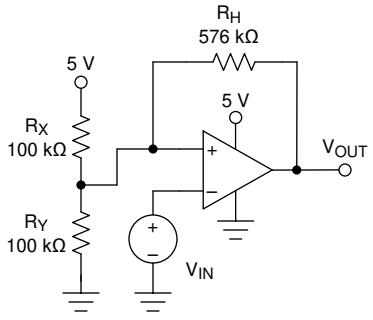


図 66. Comparator with Hysteresis

8.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 5 V
- Input: 0 V to 5 V
- Lower threshold (VL) = 2.3 V ±0.1 V
- Upper threshold (VH) = 2.7 V ±0.1 V
- VH – VL = 2.4 V ±0.1 V
- Low-power consumption

8.2.2 Detailed Design Procedure

A small change to the comparator circuit can be made to add hysteresis. Hysteresis uses two different threshold voltages to avoid the multiple transitions introduced in the previous circuit. The input signal must exceed the upper threshold (V_H) to transition low, or below the lower threshold (V_L) to transition high.

図 66 illustrates hysteresis on a comparator. Resistor R_H sets the hysteresis level.

When the output is at a logic high (5 V), R_H is in parallel with R_X. This configuration drives more current into Ry, and raises the threshold voltage (VH) to 2.7 V. The input signal must drive above VH = 2.7 V to cause the output to transition to logic low (0 V).

Typical Applications (continued)

When the output is at logic low (0 V), Rh is in parallel with Ry. This configuration reduces the current into Ry, and reduces the threshold voltage to 2.3 V. The input signal must drive below VL = 2.3 V to cause the output to transition to logic high (5 V).

For more details on this design, refer to Precision Design TIPD144, *Comparator with Hysteresis Reference Design*.

8.2.3 Application Curve

図 67 shows the upper and lower thresholds for hysteresis. The upper threshold is 2.76 V and the lower threshold is 2.34 V, both of which are close to the design target.

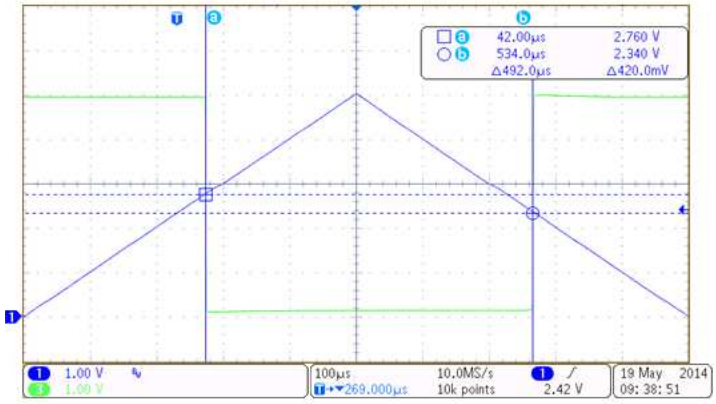


図 67. TLV1805-Q1 Upper and Lower Threshold with Hysteresis

Typical Applications (continued)

8.2.4 Reverse Current Protection Using MOSFET and TLV1805-Q1

An N-Channel or P-Channel MOSFET may be used to protect against reverse current. Reverse current is defined as current flowing from the load (V_{LOAD}) to the source (V_{BATT}). Both the P-Channel and N-Channel circuits work on the same basic principle, where a comparator monitors the voltage across the MOSFET's Source and Drain terminals (monitoring V_{DS}). The described circuits also protect against reverse voltage.

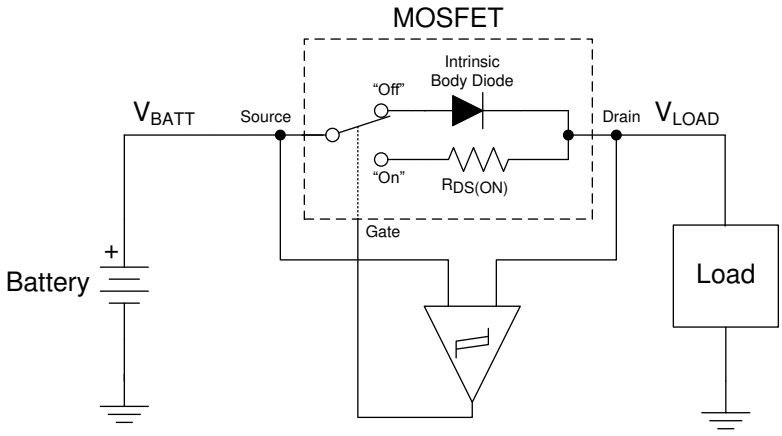


図 68. Simplified Operational Theory

When the current is flowing from the battery (V_{BATT}) to the load (V_{LOAD}), the battery voltage will be higher than the load voltage due to voltage drop across the MOSFET caused by the $R_{DS(ON)}$ or the intrinsic body diode forward voltage drop. The comparator will detect this and turn "on" the MOSFET so that the load current is now flowing through the low loss $R_{DS(ON)}$ path.

In a reverse current condition, V_{LOAD} will be higher than V_{BATT}. The comparator will detect this and drive the gate to set V_{GS} = 0 to turn "off" the MOSFET (non-conducting). The body diode is reverse biased and will block current flow.

For a P-Channel MOSFET, the gate must be driven at least 4V or more *below* the battery voltage to turn "on" the MOSFET.

For a N-Channel MOSFET, the gate must be driven 4V or more *above* the battery voltage to turn "on" the MOSFET. If a higher voltage is not available in the system, a charge pump is usually required to generate a voltage higher than the battery voltage to provide the necessary positive gate drive voltage.

8.2.4.1 Minimum Reverse Current

There is a minimum amount of reverse current that is needed to trip the comparator. To detect this reverse current, a voltage must be dropped across the MOSFET (V_{MEAS}).

When the MOSFET is off, V_{GS} will be in the -600mV to -1V range due to the forward voltage drop (V_F) of the MOSFET body diode. Response to this large voltage will be immediate.

However, with the MOSFET "on" (conducting), the current required to create the trip voltage will be much greater. The trip voltage drop required across the MOSFET $R_{DS(ON)}$ will be the comparator offset voltage plus half of the hysteresis.

The maximum offset voltage of the TLV1805-Q1 is 5mV with a typical hysteresis of 14mV. The trip voltage can be calculated from:

$$V_{TRIP} = V_{OS(max)} + (V_{HYST} / 2) = 5 \text{ mV} + 7 \text{ mV} = 12 \text{ mV} \quad (7)$$

The actual current trip point will depend on the MOSFET $R_{DS(ON)}$ and V_{GS} drive level. Assuming the MOSFET has a 22 mΩ on resistance, the trip current is found from:

$$I_{TRIP} = V_{TRIP} / R_{DS(ON)} = 12 \text{ mV} / 22 \text{ m}\Omega = 546\text{mA} \quad (8)$$

Typical Applications (continued)

8.2.4.2 N-Channel Reverse Current Protection Circuit

In order to turn "on" the N-Channel MOSFET, the MOSFET gate must be brought "High" above V_{BATT}. If a higher voltage is not available, a charge pump circuit is required to provide the comparator with a supply voltage above V_{BATT}.

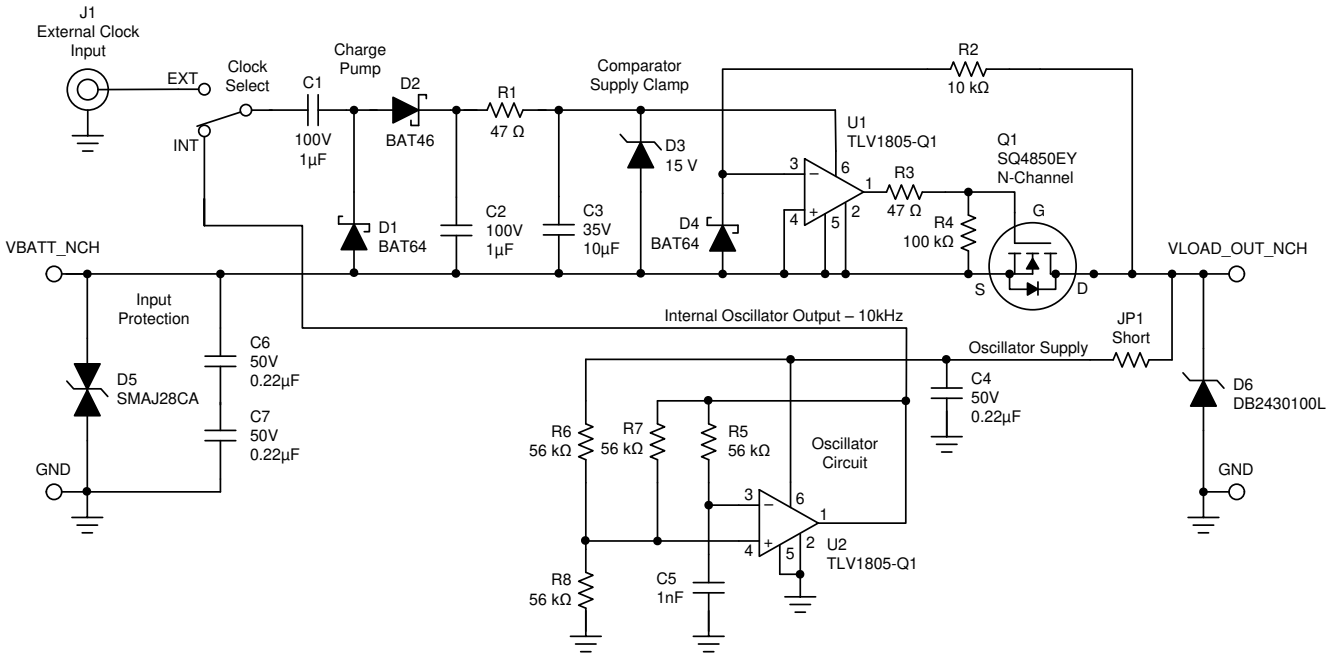


図 69. N-Channel Reverse Current Schematic with Oscillator

C1, D1, D2 & C2 form the charge pump. The AC drive signal is applied through C1 into the charge pump. The result is a voltage across C2 that is approximately equal to the peak-to-peak amplitude of the AC waveform, minus 700mV. If a 12Vpp waveform is applied to the C1 input, 11.3V will be generated across C2. This voltage is on top of the V_{BATT} voltage, so the voltage seen from the D2-C2 junction ground is 23.3V. This provides the needed higher voltage to drive the MOSFET and power the comparator.

An external oscillator source may be used, such as the gate drive output of a switcher, system clock or any avaialbe clock source in the 1kHz to 10MHz range. The charge pump should be fed by a 50 percent duty cycle square wave source of 5Vpp or more. Since the input capacitor of the charge-pump effectively AC-couples the input, the oscillator may be ground referenced.

R1 and D3 form the comparator supply clamp to limit the gate drive to prevent exceeding the $V_{GS(MAX)}$ of the MOSFET during an overvotlage event. R1 must be sized to dissapate any expected overvoltage.

D4 and R2 clamp the input should V_{BATT} drop below V_{LOAD} (as in a supply reversal).

The output diode D6 is used to anchor the output during light or floating loads. At light or no loads, there is a possibility the MOSFET could turn on due to the comparator offset voltage. The diode provides enough of a negative leakage to turn the MOSFET off.

8.2.4.2.1 N-Channel Oscillator Circuit

The oscillation frequency is determined by R5 and C5. The default configuration oscillates around 10kHz (depending on RC component tolerances). For further information on selecting these RC values, please see the Engineers Cookbook Circuit entitled *Oscillator Circuit* (SNOA990). Do note that R5 does present an AC load to the oscillator output, and should be sized appropriately to minimize the peak charging currents of C5 (use large resistors and small capacitors).

Typical Applications (continued)

The output amplitude is roughly equivalent to the V_{LOAD} voltage minus the TLV1805-Q1 output saturation (approximately 300mV). With a maximum supply voltage of 40V for the TLV1805-Q1, the oscillator circuit is capable of generating up to 39Vpp!

The TLV1805-Q1 oscillator typically starts oscillating when V_{LOAD} reaches 2.8V, though full specified operation does not occur until 3.3V.

For more information, please see the TLV1805-Q1 Evaluation Module Users Guide *TLV1805-Q1 Evaluation Module Users Guide* (SNOU158).

8.2.5 P-Channel Reverse Current Protection Circuit

図 70 shows the P-Channel circuit. In order to turn "on" the P-Channel MOSFET, the gate must be brought "Low" below V_{BATT} . To accomplish this, the comparators Inverting input is tied to the battery side of the MOSFET to set the output low during forward current.

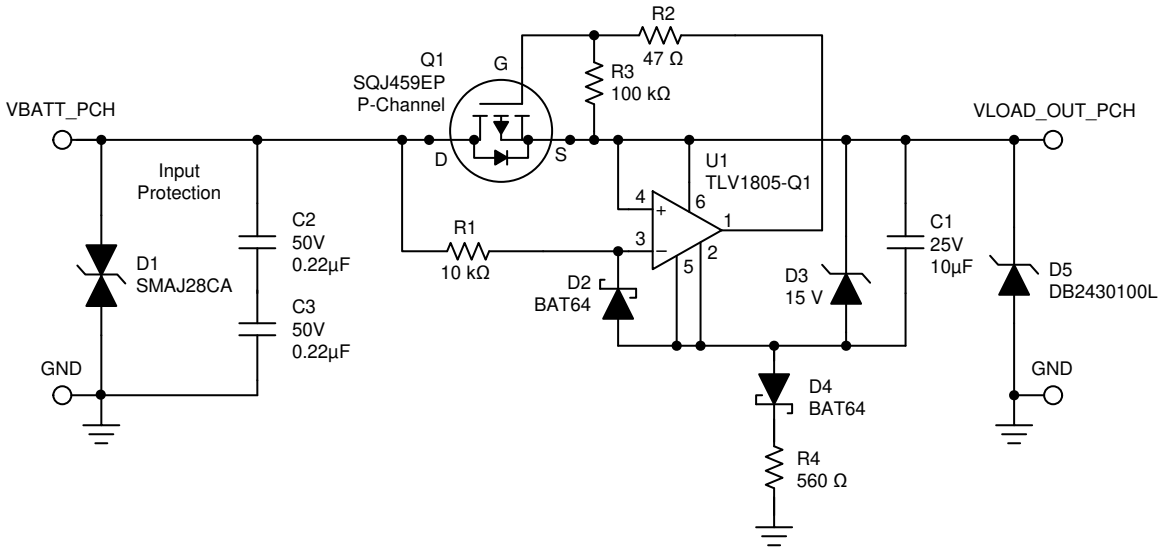


図 70. P-Channel Reverse Current Schematic

This design implements a "floating ground" topology, using D3, D4 and R12, to allow for clamping the comparator supply voltage as to not exceed the $V_{GS(MAX)}$ of the MOSFET. During a reverse voltage or supply drop, D4 also prevents C1 from discharging to allow some standby time to keep the comparator powered during the event.

During "normal" forward current operation, the quiescent current of the comparator circuit flows through D4 and R4. D3 provides the clamping during an overvoltage event.

R4 is sized to allow for minimum voltage drop during "normal" operation, but also to allow for dissipation during overvoltage events. R4 will see the battery voltage minus the D3 Zener voltage during an overvoltage event. Since the comparator supply voltage is clamped by D3, the maximum battery voltage is determined by the power dissipated by R4 and the $V_{DS(MAX)}$ of the MOSFET.

R2 limits the gate current should there be any transients and should be a low value to allow the peak currents needed to drive the MOSFET gate capacitance. R3 provides the pull-down needed when the comparator output goes high-Z during power-off to ensure the gate is pulled to zero volts to turn off the MOSFET.

R1 and D2 clamp the input voltage should the V_{BATT} input go below the floating ground Voltage (such as in a battery reversal). A bonus feature is that during a reverse battery voltage condition, D2 and R1 pull the floating ground down towards the negative potential, providing power to the comparator during reverse voltage.

The output clamp diode D5 is used to anchor the output during light or floating loads. At light or no loads, there is a possibility the MOSFET could turn on due to the comparator offset voltage. The diode provides enough of a negative leakage to turn the MOSFET off.

Typical Applications (continued)

If shutdown of the comparator circuit is desired, a transistor or MOSFET switch can be placed between the ground end of R4 and ground. The MOSFET will be in body diode mode when the comparator is disabled.

8.2.6 P-Channel Reverse Current Protection With Overvotlage Protection

The SHDN pin can be utilized to add Overvotlage Protection (OVP) by adding a second MOSFET, zener diode and resistor, as shown in 図 71.

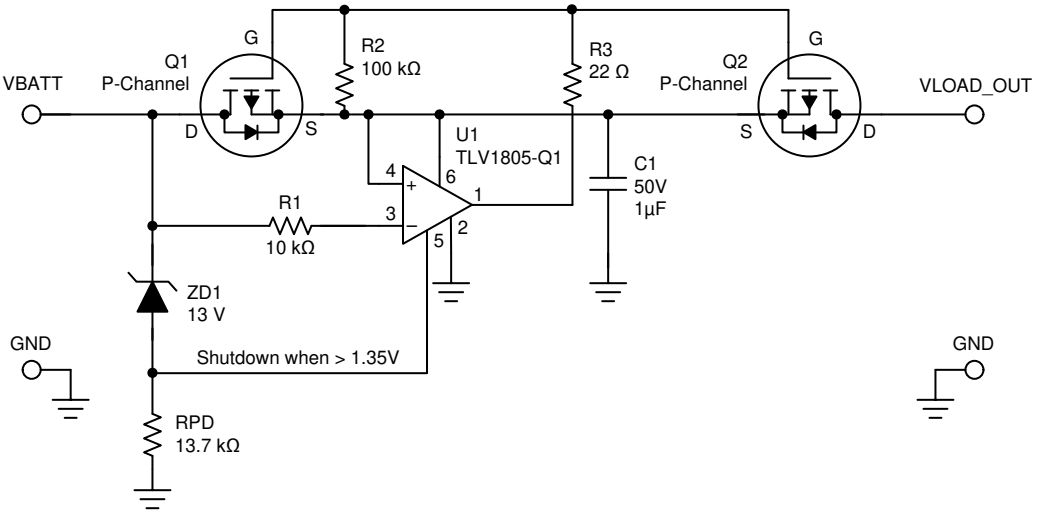


図 71. Adding Overvoltage Protection Using SHDN Pin

When the SHDN pin is pulled 1.35 V above V-, the comparator is placed in shutdown. During shutdown, the comparator output goes Hi-Z and R2 pulls the gate and source together to turn off the MOSFET (V_{GS} = 0 V).

RPD pulls the SHDN pin low while the Zener diode is not conducting (< V_Z). When ZD1 reaches its breakdown voltage and starts conducting, it will pull RPD up to a voltage calculated to place >1.35 V on the shutdown pin.

The Zener diode ZD1 should be chosen so that the breakdown voltage (V_B) is 1.35 V below the desired overvoltage point. The Zener should have low sub-threshold leakage and a sharp knee, such as the low power 1N47xx or BZD series.

The pull-down resistor RPD should be chosen to create 1.35 V at the desired Zener diode current (usually 100uA to 1mA) at the Zener breakdown voltage. Actual resistor value should be verified on the bench due to differences in actual Zener diode threshold voltages.

If a 14.3 V overvotlage trip point (OVP) is desired, the Zener Diode voltage should be 12.95 V. We will choose a 100uA Zener current. The required Zener diode breakdown voltage is determined from:

$$V_B = V_{OV} - 1.35\ V = 14\ .3V - 1.35\ V = 12.95\ V \quad (9)$$

$$RPD = 1.35\ V / 100\ \mu A = 13.5\ k\Omega\ (13.7k\Omega\ \text{nearest value}) \quad (10)$$

Resistor RPD may be split into two resistors to create a voltage divider if more precise trip points are needed, or a more convenient zener voltage is desired. Series voltage references can also be used if more accuracy is desired. A second resistor in series with the Zener or reference can extend the breakdown voltage.

The maximum voltage allowed on the Shutdown pin is 5.5V, so make sure the highest V_{BATT} voltage does not exceed 5.5 V.

Note that the above circuit, as shown for simplicity, does not protect against reverse voltage. Reverse clamping diodes would be needed on the -IN, SHDN and Load Output. Also make sure V_{BATT} does not exceed the $V_{GS(MAX)}$ of the MOSFET.

Typical Applications (continued)

8.2.7 ORing MOSFET Controller

The previous reverse current circuits may be combined to create an OR'ing supply controller, utilizing either the P-Channel or N-Channel topologies.

For the previous P-Channel circuit, if no negative input voltages are possible, and the input voltage is below the MOSFET's $V_{GS(MAX)}$, then D3, D4 and R4 may be eliminated (the D2 anode, U1 pins 2 and 5, and C1 can be directly grounded).

For the N-Channel circuit, the oscillator drive can be shared between the channels, or eliminated if a higher system voltage is available to provide the higher votlage.

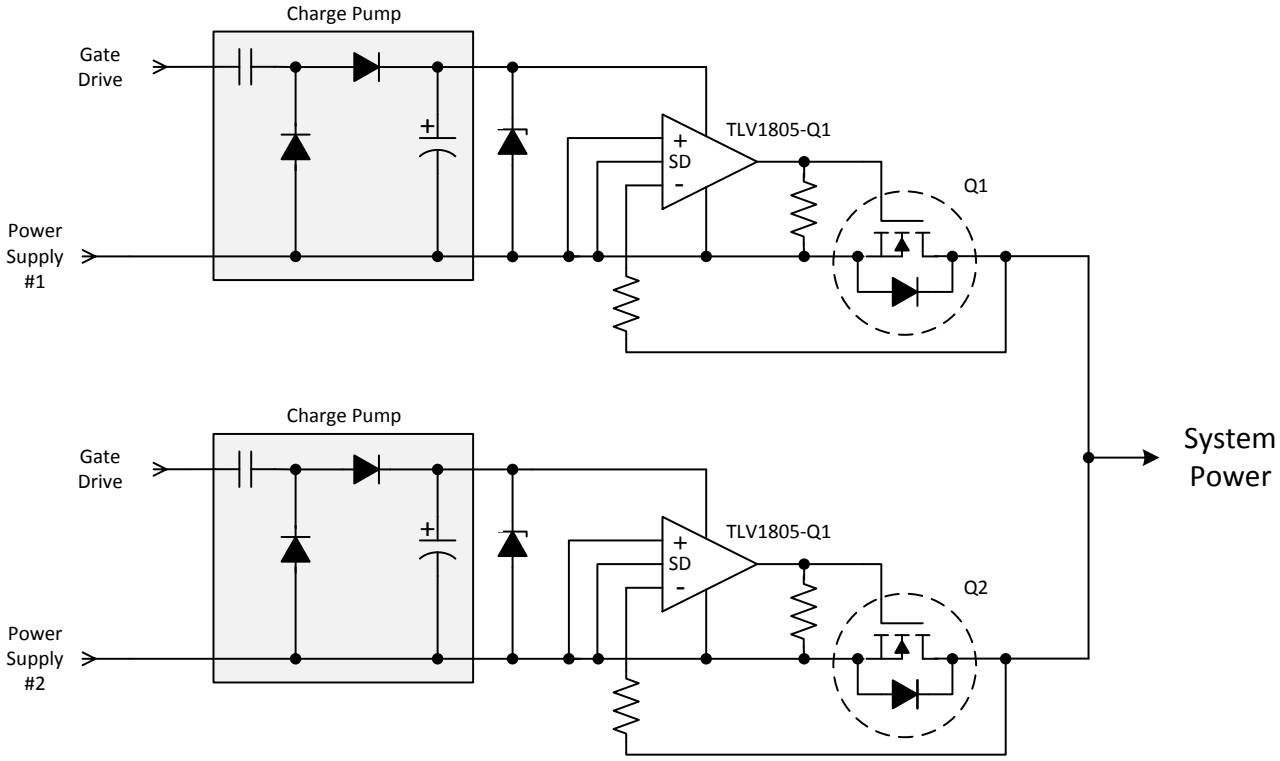


図 72. N-Channel OR'ing MOSFET Controller

9 Power Supply Recommendations

The TLV1805-Q1 family of devices is specified for operation from 3.3 V to 40 V (±1.65 to ±20 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

> **注意**
>
> Supply voltages larger than 40 V can permanently damage the device; see the *Recommended Operating Conditions* section.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the *Layout Guidelines* section.

The TLV1805-Q1 does not contain reverse battery protection, so applying negative voltage to the supply pins must be avoided. The TLV1805-Q1 cannot withstand ISO 16750 type waveforms alone and requires external protection circuitry.

10 Layout

10.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, maintain the following layout guidelines:

- Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane. Proper grounding (use of ground plane) helps maintain specified performance of the TLV1805-Q1 family of devices.
- To minimize supply noise, place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to V_S as shown in 図 73.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- Run the ground pin ground trace under the device up to the bypass capacitor, shielding the inputs from the outputs.

10.2 Layout Example

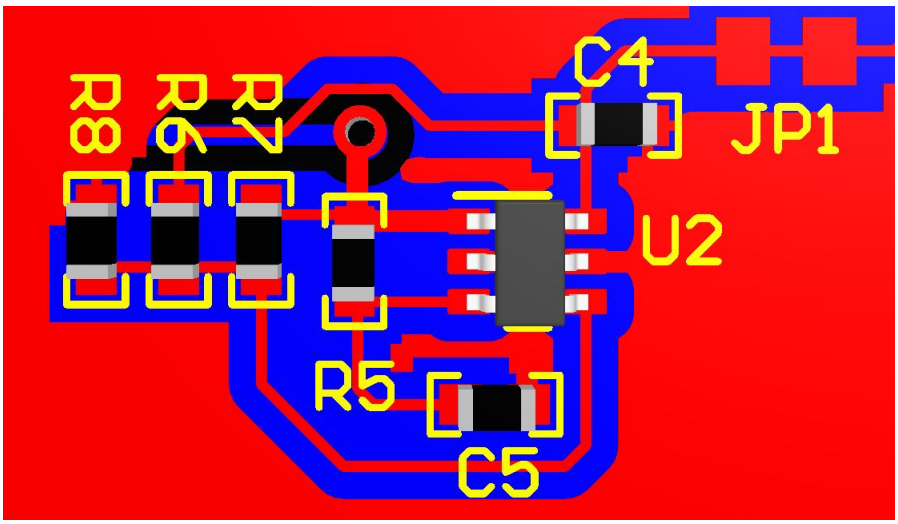


図 73. Oscillator Circuit Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

Precision Design、*『ヒステリシス付きコンパレータのリファレンス・デザイン』*、TIDU020

リファレンス・デザイン、*『ウィンドウ・コンパレータのリファレンス・デザイン』*、TIPD178

アプリケーション・レポート、*『Using Comparators in Reverse Current Applications』(英語)*、SNOAA23

アプリケーション・レポート、*『TLV1805-Q1 EVM ISO testing results』(英語)*、SNOAA13

EVM ユーザー・ガイド、*『TLV1805-Q1 逆電流評価基板・ユーザー・ガイド』*、SNOU158

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 商標

E2E is a trademark of Texas Instruments.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV1805QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1ULF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

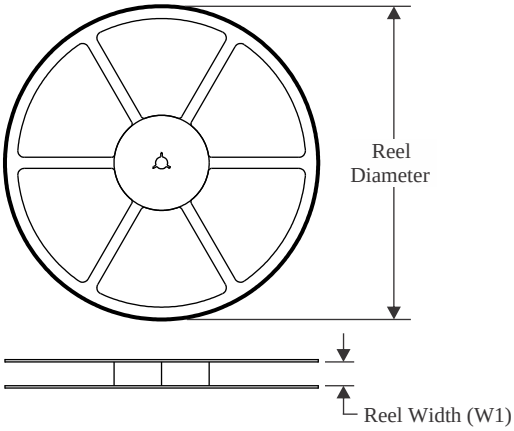
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

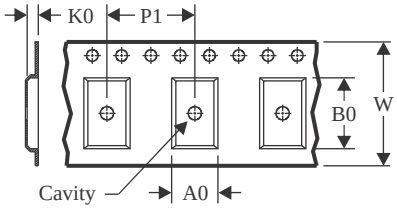
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

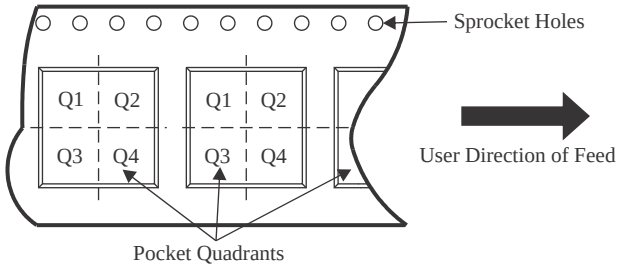


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

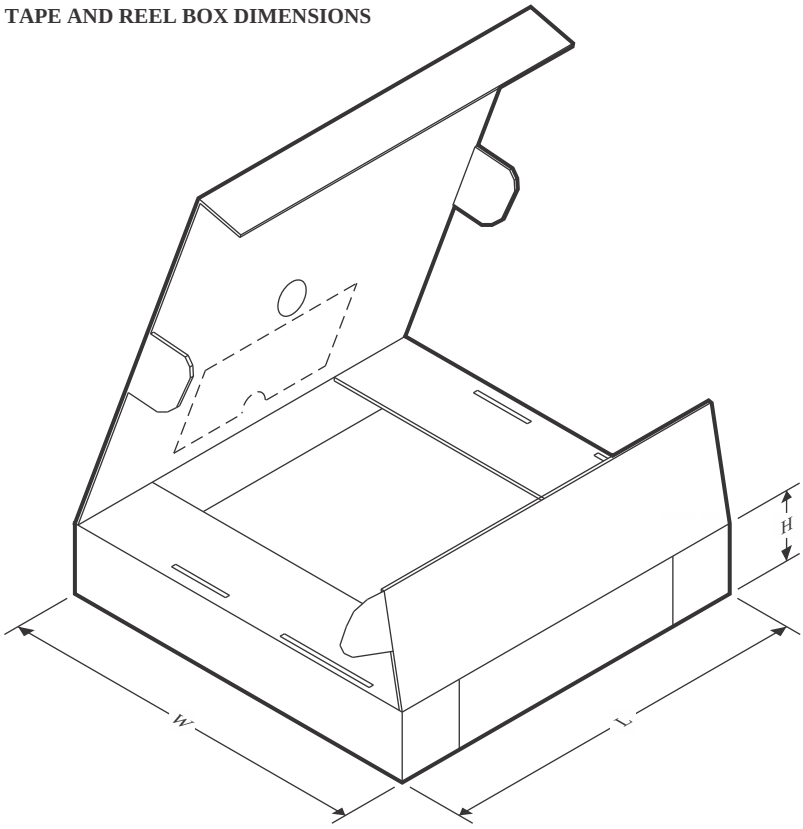
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1805QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

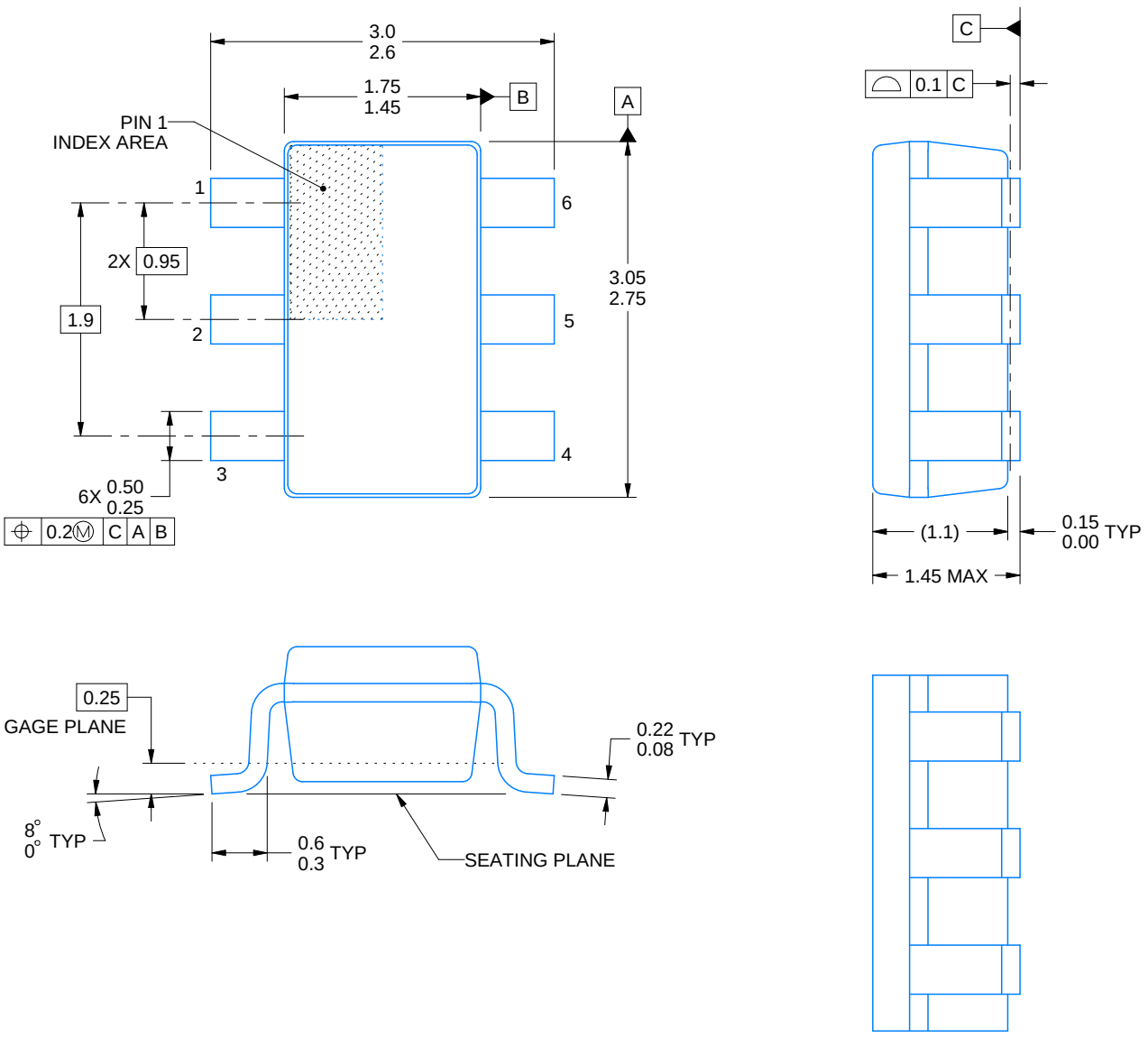
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1805QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

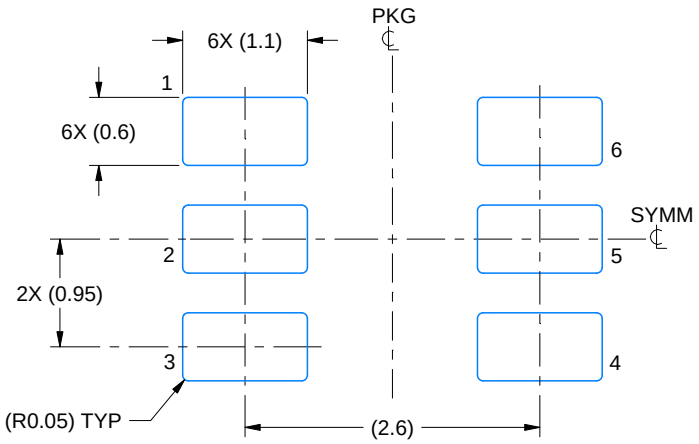


ALTERNATIVE PACKAGE SINGULATION VIEW

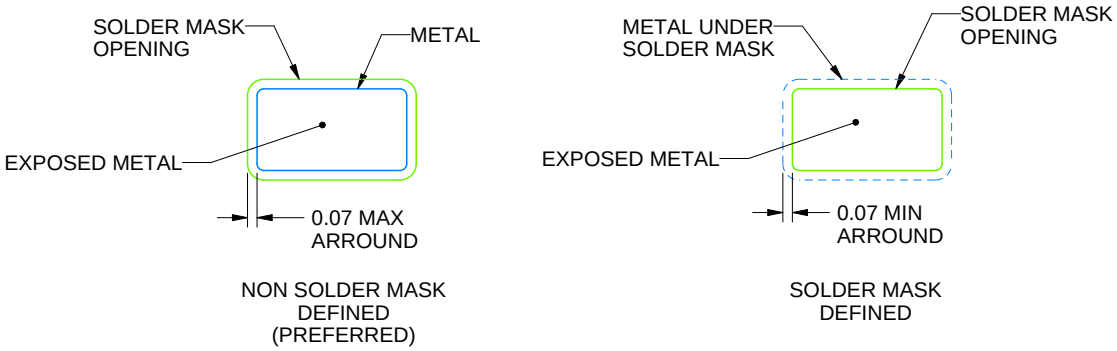
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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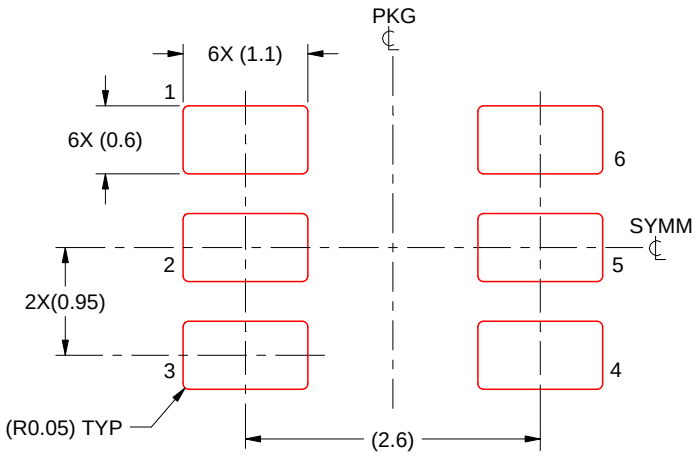
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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