

TI Designs: TIDA-01051

チャンネル数が非常に多い自動テスターでFPGAの活用率とデータ・スループットを最適化するリファレンス・デザイン



概要

TIDA-01051デザインでは、データ収集(DAQ)システムのうち、自動テスト機器(ATE)に使用されるものなど非常にチャンネル数の多いものについて、チャンネル密度、統合、消費電力、クロック分配、信号チェーン性能を最適化する方法を紹介いたします。TIのDS90C383Bなどのシリアライザを使用して、多くの同時サンプリングADCの出力を複数のLVDSラインとして組み合わせることで、ホストFPGAが処理する必要のあるピン数を劇的に減らすことができます。その結果、単一のFPGAで処理できるDAQチャンネル数が大幅に増大し、基板の配線の複雑性も大幅に減少します。

リソース

- | | |
|--|---------------|
| TIDA-01051 | デザイン・フォルダ |
| MUX36D04, DS90C383B | プロダクト・フォルダ |
| OPA827, OPA625, THS4551 | プロダクト・フォルダ |
| ADS8910B, REF6041, OPA376 | プロダクト・フォルダ |
| LM53635, TPS7A47, LM7705 | プロダクト・フォルダ |
| LM46001, TPS7A3001, TPS82084 | プロダクト・フォルダ |
| SN74AHC1G04, SN74AUP1G80 | プロダクト・フォルダ |
| CD4081B | プロダクト・フォルダ |
| LMK61E2, LMK00804B | プロダクト・フォルダ |
| TIDA-01050, TIDA-01052 | デザイン・フォルダ |
| TINA-TI™ | SPICEシミュレータ |
| WEBENCH® | デザイン・ツール・フォルダ |



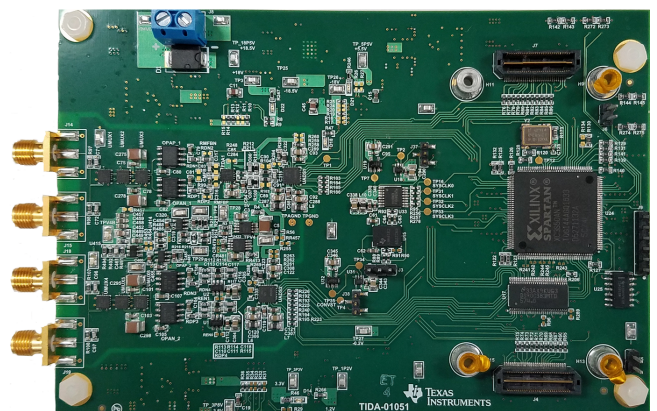
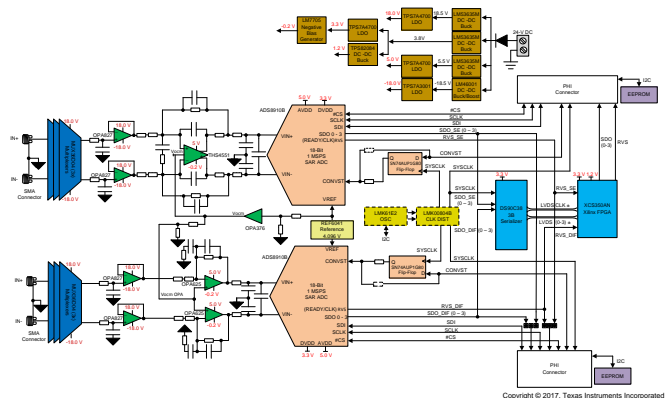
[E2Eエキスパートに質問](#)

アプリケーション

- 自動テスト機器
- 半導体試験用機器
- データ収集
- LCD試験用機器
- メモリ・テスト機器
- バッテリ・テスト機器

特長

- ADC出力のシリアル化により、DAQチャンネル数の増大を可能にし、FPGAピンを最適化
- スケーラブルでチャンネル数の多い、モジュール式のフロントエンドのリファレンス・デザイン
- 2つの18ビットDAQチャンネル(28まで拡張可能)
- 3レベルのMUXツリーを使用して、最大64のチャンネルと、それらが信号チェーンのSNRに及ぼす影響をエミュレート
- 最大±12Vの入力信号(24V_{pp}差動)
- 完全差動アンプ・ドライバとデュアル高精度アンプ・ドライバとの比較





使用許可、知的財産、その他免責事項は、最終ページにあるIMPORTANT NOTICE(重要な注意事項)をご参照くださいますようお願いいたします。英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

1 System Description

Multi-input systems requiring the simultaneous or parallel sampling of many data channels present many design challenges to engineers developing data acquisition (DAQ) modules and automatic test equipment (ATE) for applications such as semiconductor tests, memory tests, LCD tests, and battery tests. In these systems, hundreds or even thousands of data channels are required. As a result, key design criteria include maximizing signal-to-noise ratio (SNR) performance while minimizing power, component count, and cost. The analog front-end (AFE) signal chain often consists of a series of multiplexers (muxes), a scaling and/or programmable gain amplifier (PGA) followed by an antialiasing, noise limiting, low-pass filter (LPF), which is paired with the appropriate analog-to-digital converter (ADC) driver prior to digitization. The ADC converts the time varying analog input to either a serial or parallel binary bit stream, which is then passed to the embedded host controller (MCU or FPGA). Depending on the application, the ADC may contain the necessary reference and/or the associated buffer integrated as part of the ADC. Furthermore, portions or the entire AFE may also be integrated as a single device for specific applications, but this can also limit flexibility.

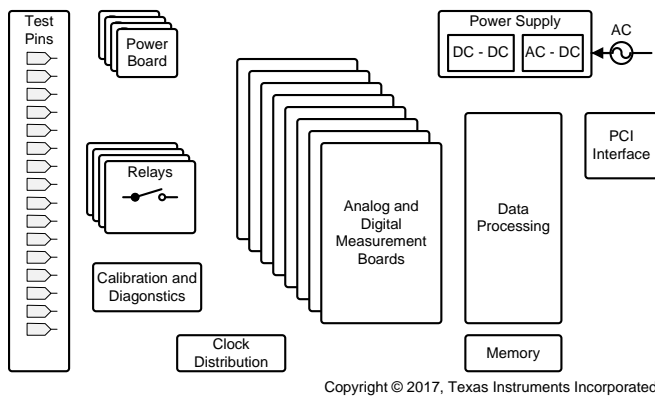


図 1. Multichannel Test System

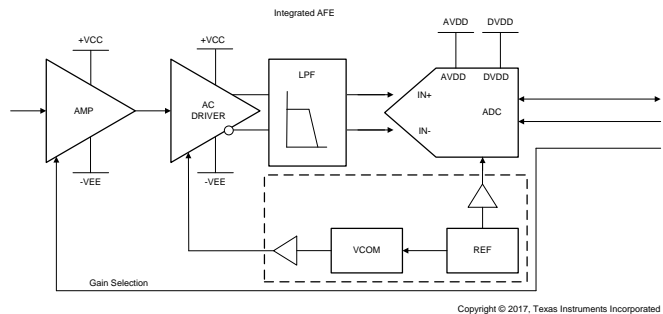


図 2. Generic AFE

1.1 Key System Level Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	MEASURED
Number of channels	Dual	Dual
Input type	Differential	Differential
Input range	$\pm 24 \cdot V_{PP}$ fully differential	$\pm 24 \cdot V_{PP}$ fully differential
Input frequency	2 kHz	2 kHz
Resolution	18 bits	18 bits
SNR	> 96 dB	98.53 dB
THD	< -120 dB	-123.26 dB
ENOB	> 15.0	16.07
System Power	< 2.5 W	2.3 W
Form factor (L x W)	120 x 100 mm	116.59 x 99.82 mm

2 System Overview

2.1 Block Diagram

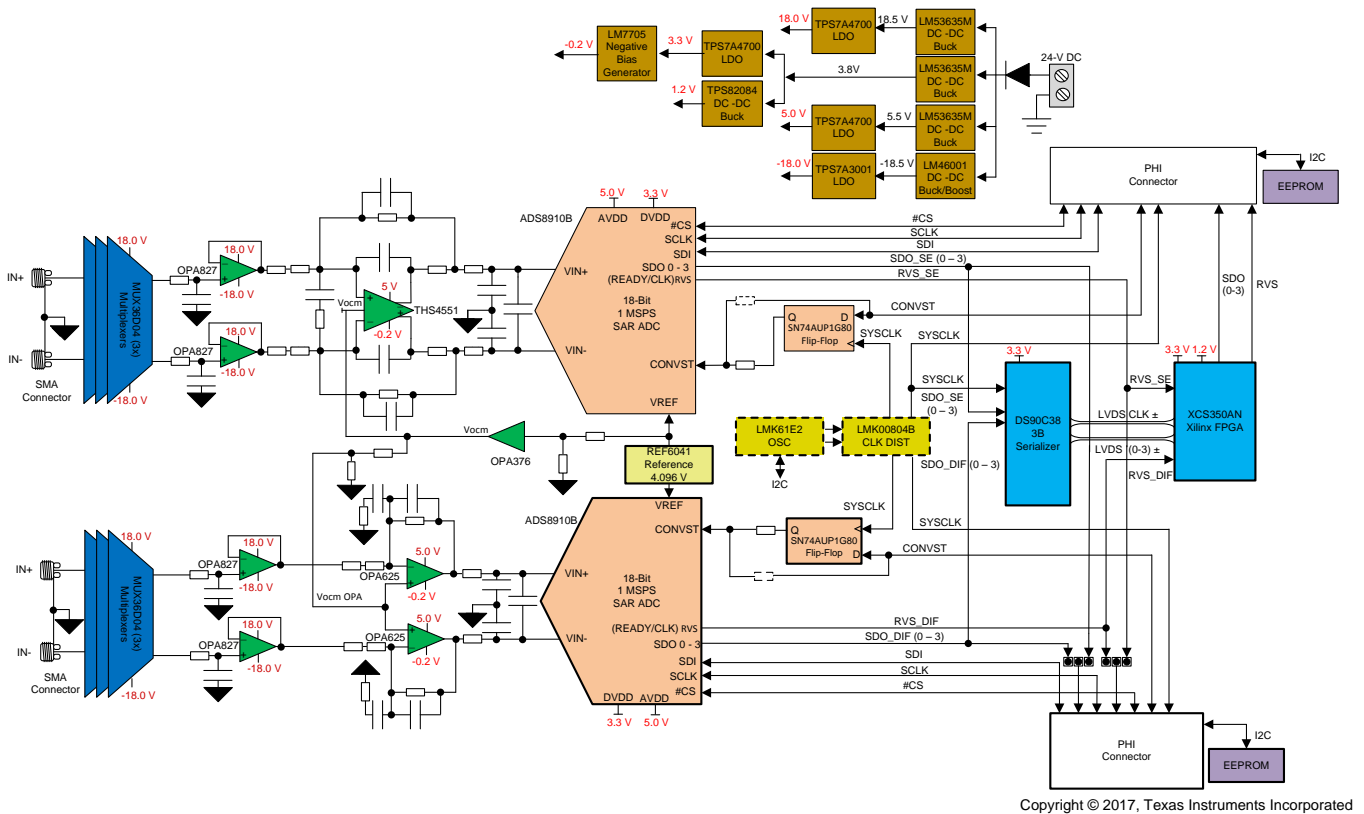


図 3. TIDA-01051 Block Diagram

2.2 System Design Theory

ATE complexity continues to grow as its applications demand ever increasing input channels with some applications requiring more than 5000 inputs. In this reference design, a modular solution is proposed to promote a design that will scale to the required number of inputs by the application. End equipment such as mixed signal SOC testers, memory testers, battery testers, LCD testers, high-density DAQ cards, high-density power cards, X-ray inspection, and so on require multiple, simultaneous-sampling channels with excellent DC and AC performance while managing power in order to maximize PCB density.

The AFE typically contains the high-speed signal chain, and the associated point-of-load (POL) power supplies as required. In order to optimize the different performance metrics of a modular multisampling ATE system, this TI Design uses two different front ends to compare the performance and application when used to drive identical high-performance 20-bit successive-approximation register (SAR) ADCs. One front end uses a fully differential amplifier (FDA), and the second uses two precision operational amplifiers (OPA). The resulting digital data from the ADC output is connected to the Texas Instruments precision host interface (PHI, available for purchase with the [ADS8910B evaluation board](#)) where the data is analyzed for SNR, total harmonic distortion (THD), and other performance parameters.

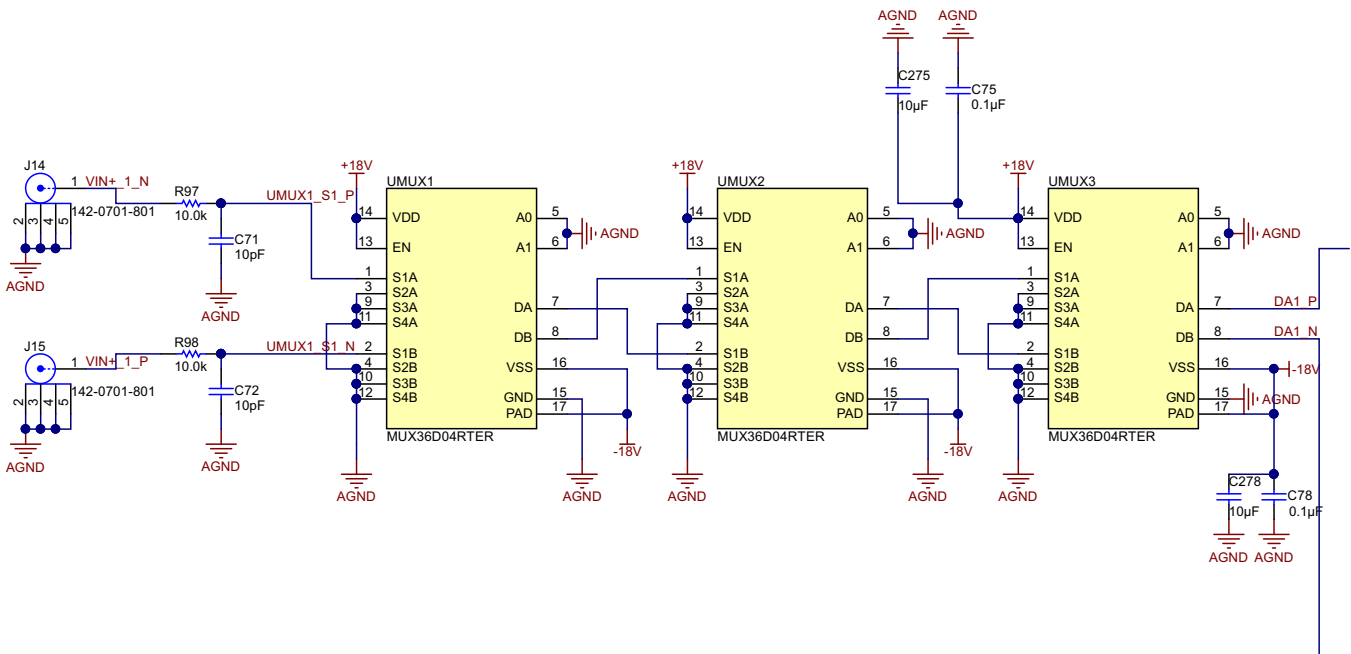
The following sections detail the design challenges presented by high channel count systems, including theory, calculations, component selection, simulations, PCB layout design, and measurement results. Unless otherwise noted, TI's SPICE and design developments tools [TINA-TI](#) and [WEBENCH](#) were used to aid in development.

2.2.1 MUX36D04 Input Chain

SMA connectors attach an input signal to the system, which supports an input voltage range of ± 5 V up to ± 12 V. Three MUX36D04 with supplies of ± 18 V were placed directly after the analog circuit input. The purpose of the muxes is to showcase a flexible multichannel solution that would allow up to 64 different analog inputs and measure the signal chain impact they create. The mux tree is scalable to allow for more input channels, which could be used at lower speeds where the ENOB with a one-, two-, or three-mux solution compared.

As seen in [Figure 4](#), R97, R98, C71, and C72 form an antialiasing filter on both the positive and negative inputs. The 3-dB cutoff frequency of this filter is 1.59 MHz. The purpose of this filter is to prevent possible aliasing on the input of the muxes.

Decoupling capacitors of 10 μ F and 0.1 μ F are present on both the VDD and VSS pins of the muxes to help remove any power supply noise. The 0.1- μ F decoupling capacitors were selected as a smaller capacitance is better at filling the very fast transients. The larger 10 μ F is better at dealing with a more sustained voltage droop. The two capacitors work together to improve the effectiveness of decoupling. These decoupling capacitor values can be found in many places throughout the system for decoupling.



Copyright © 2017, Texas Instruments Incorporated

図 4. MUX Input Chain Schematic

Pins A0 and A1 are the address line pins of the multiplexer. These pins configure the output pins (DA and DB) to be connected to a certain input pin. In this system, pins A0 and A1 are grounded. According to 表 2, the state of the muxes is permanently configured to channels 1A and 1B. 図 4 shows that the input signal is connected to pins S1A and S1B. DA and DB of the first mux is then connected to S1A and S2B of the second mux. This means that the output of the mux chain will always be connected to the input signal of the system in this configuration.

表 2. MUX36D04 Truth Table

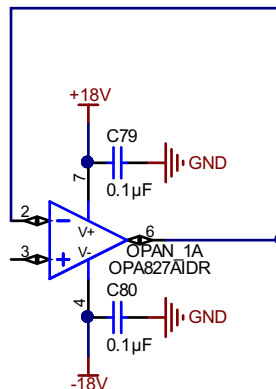
EN	A1	A0	STATE
0	X ⁽¹⁾	X ⁽¹⁾	All channels are off
1	0	0	Channels 1A and 1B
1	0	1	Channels 2A and 2B
1	1	0	Channels 3A and 3B
1	1	1	Channels 4A and 4B

⁽¹⁾ X denotes *don't care*

The EN pin, or the enable pin, to each MUX is connected to VDD. When this pin is high, the A[1:0] logic inputs determine which pair of switches is turned on. See the MUX36D04 for more information regarding this device.

2.2.2 OPA827

The first stage of the input chain is a buffer stage consisting of two OPA827s. Illustrated in 図 5, the purpose of this stage is to buffer the input signal at the ±18-V level and achieve very high-input impedance. This amplifier was chosen due to its JFET input stage and 36-V capabilities. Additionally, the OPA827 has very good noise performance, which is crucial for a front-end butter in order to preserve signal chain ENOB. The OPA827 datasheet recommends using 0.1-μF decoupling capacitors on both the positive and negative supplies to help remove any power supply noise. For detailed AFE design considerations, see the TIDA-01050 design.



Copyright © 2017, Texas Instruments Incorporated

図 5. OPA827 Buffer Schematic

2.2.3 THS4551 ADC Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a flywheel RC filter. Amplifiers are used for input signal conditioning and its low-output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched capacitor input stage and functions as an antialiasing filter to band-limit the wideband noise. Careful front-end circuit design is required to meet the resolution, linearity, and noise performance of capabilities of the 18-bit ADS8910B. The input op amp must support following key specifications:

1. Rail-to-rail input and output (RRIO)
2. Low noise
3. High small-signal bandwidth with low distortion at high frequencies
4. Low power

For DC signals with fast transients that are common in a multiplexed application, the input signal must settle within an 18-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier datasheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 18-bit accuracy. Therefore, it is required to verify the settling behavior of the input driver within the simulators such as TINA-TI to help select the appropriate amplifier.

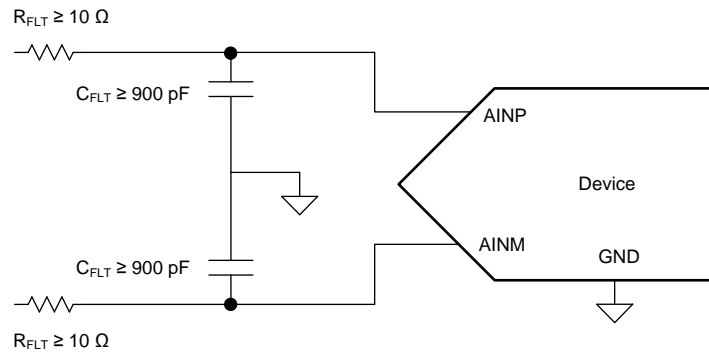
Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum of interest known as aliasing. Therefore, an analog antialiasing filter must be used to remove the noise and harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass, RC filter, where the 3-dB bandwidth is optimized based on specific application requirements.

For DC signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurate settling of the signal at the inputs of the ADC during the small acquisition time window.

For AC signals, keeping the filter bandwidth low is desirable to band-limit the noise fed into the input of the ADC, thereby increasing the system SNR. Besides filtering the noise from the front-end drive circuitry, the filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT} , is connected from each input pin of the ADC to the ground (as shown in 式 1 and 図 6).

This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 15 times the specified value of the ADC sampling capacitance. For the ADS8910B, it is recommended to keep C_{FLT} greater than 900 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.


$$f_{-3dB} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \quad (1)$$



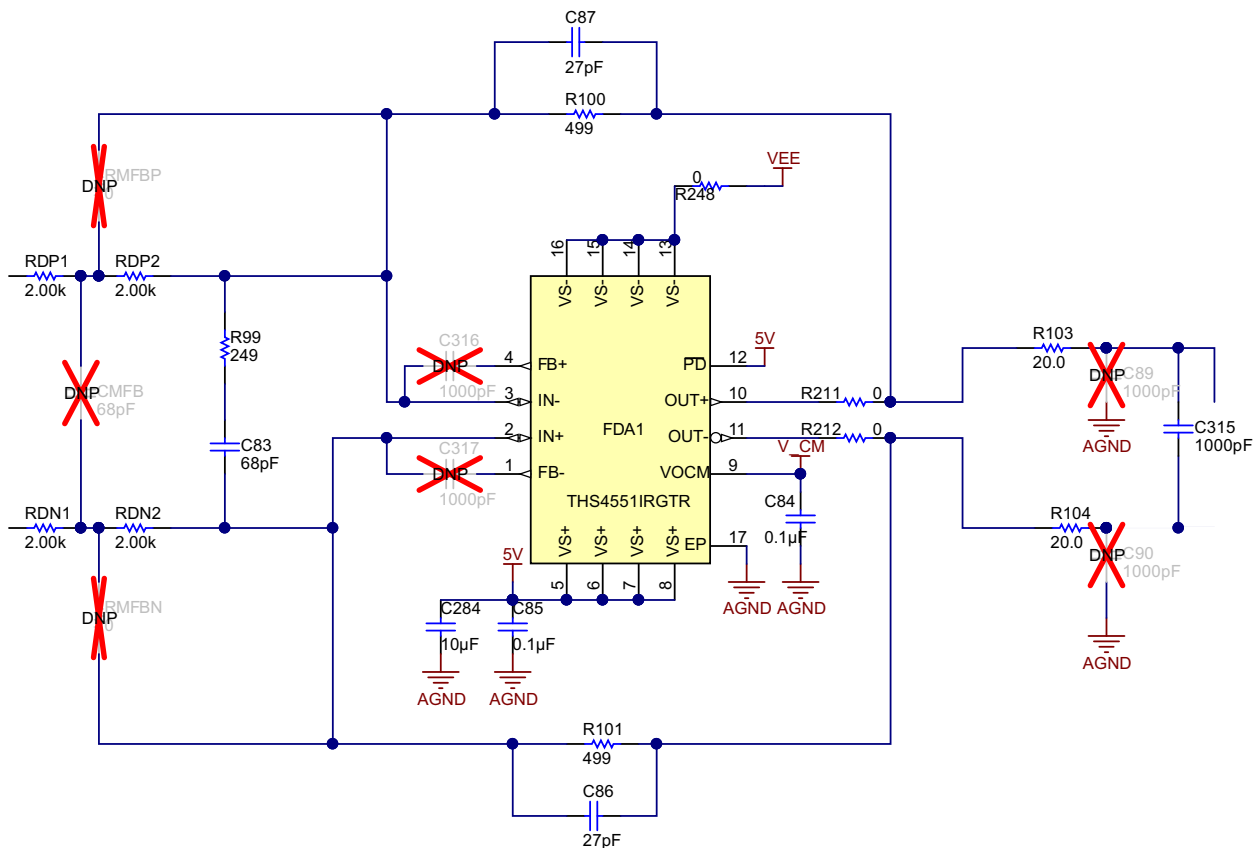
Copyright © 2017, Texas Instruments Incorporated

図 6. Antialiasing Filter Configuration Diagram

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT} or R_{ISO}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design. For the ADS8910B, limiting the value of R_{FLT} to a maximum of 10Ω is recommended to avoid any significant degradation in linearity performance. The tolerance of the selected resistors must be kept less than 1% to keep the inputs balanced. The driver amplifier must be selected such that its closed-loop output impedance is at least five times lesser than the R_{FLT} .


Following the OPA827, one of the ADC drivers is the THS4551. The THS4551 is a fully differential amplifier specifically designed to be used with high-performance SAR ADCs. In this TI Design, the THS4551 needed to be implemented as an attenuator in order to ensure the ADC input is between 0 and 4.096 V. The gain of this stage is configured to be 1/8. RDP1 and RDP2 in  are connected in series to give 4 kΩ while R101 is 499 Ω. These values give a gain of 1/8. RDN1, RDN2, and R101 deliver the same gain for the negative input to the fully differential amplifier.

Additionally, R99, C83, C87, C86, R211, R212, R103, R104, and C315 were added to ensure stability. The selection of these components is discussed in the [TIDA-01050](#) design. R211 and R212 are 0-Ω placeholder resistors for later study (for example, in case larger isolation is required). Capacitors C89, C90, and C315 are flywheel or "charge bucket" capacitors designed to quickly charge the sample-and-hold circuit inside the ADC. It is important in some cases to place the single-ended capacitors C89 and C90 from each ADC input to GND in addition to the differential capacitor C315 to ensure the common-mode voltage is stable during the switching of the sample-and-hold circuit.



Copyright © 2017, Texas Instruments Incorporated

図 7. THS4551 Stage Altium Schematic

In , the power down pin (pin 12) of the THS4551 is connected to 5 V. The power down pin is logic low, meaning that when it is grounded, the chip is in power off mode. When this pin is high, it is in normal operation mode. For this application, the amplifier will always be in normal operation mode. Pin 17 is the thermal pad and is connected to ground to ensure that the chip has a proper heat sink. The voltage driven at the common-mode voltage pin is 2.048 V.

2.2.4 Dual OPA625 ADC Driver

The OPA625 is designed to drive precision (up to 18-bit) SAR ADCs at sample rates up to 2 MSPS. The combination of low-output impedance (1 Ω at 1 MHz), low THD, low noise (2.5 nV/√Hz), and fast settling time (4-V step, 16-bit levels within 280 ns) make the OPA625 the ideal choice for driving both the SAR ADC inputs as well as the reference input to the ADC (see [Figure 8](#)).

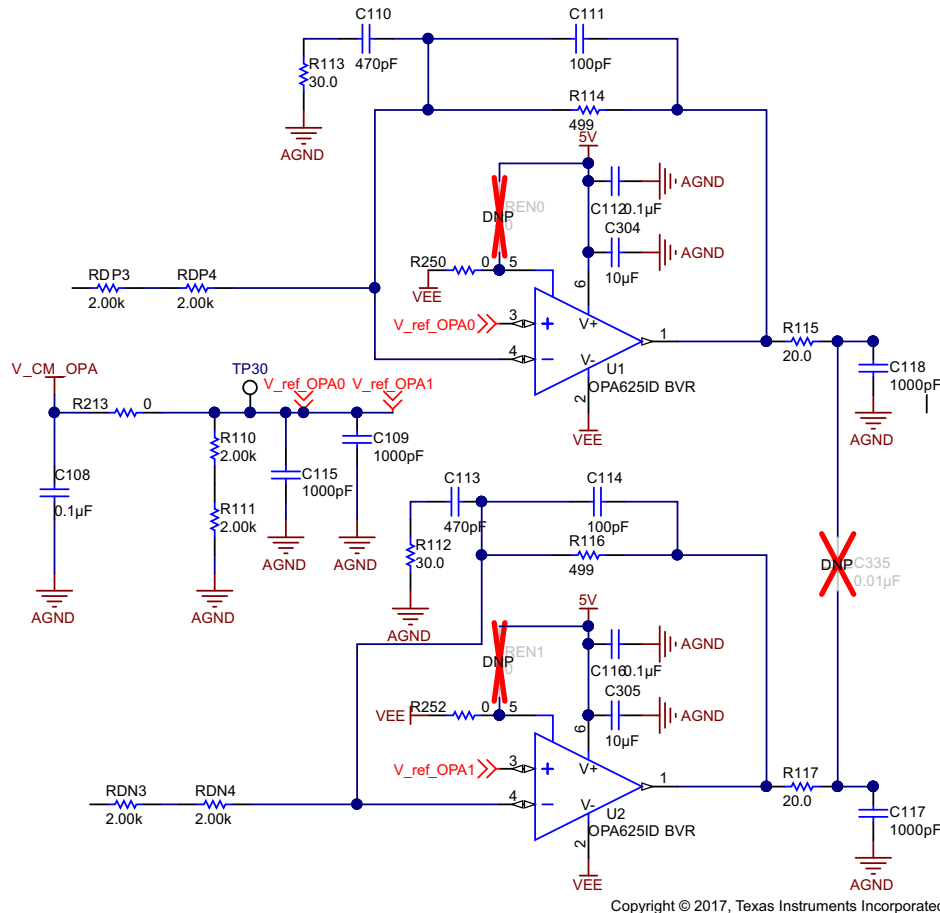


Figure 8. Dual OPA625 Stage Altium Schematic

The second channel uses a different front-end attenuator driver stage to compare the performance of the two. Similar to the THS4551 driver, the gain of this stage is 1/8. This is executed with RDP3, RDP4, and R114 for the positive signal and RDN3, RDN4, and R116 for the negative signal. A similar approach was taken with the OPA625 devices to ensure circuit stability. See the [TIDA-01050](#) design to learn more about the design of this stage.

The output of the OPA625 is centered at 2.048 V, which is the midpoint of the reference voltage of the ADC. In [Figure 8](#), the non-inverting inputs of the OPA625 devices are connected together; this is done to make the two OPA625 op amps work in the same fashion as a fully differential amplifier.

The common-mode voltage for the OPA625 op amps has to be slightly lower than that of the THS4551 to compensate for the OPA625 gain. Thus, another resistor divider is used to drop the common-mode voltage to 1.82 V.

2.2.5 Driver Amplifier Comparison

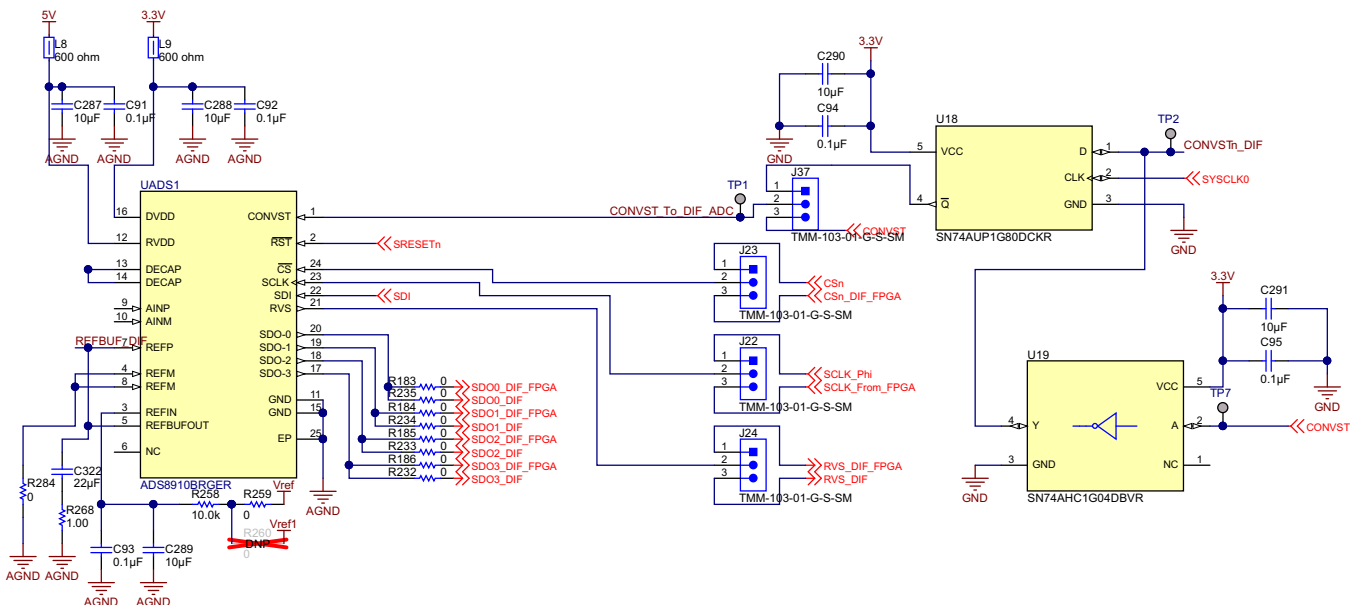
It is crucial that the noise of the buffer stage of an ADC driver is kept to an absolute minimum. The analog signal going into the ADC must be as pure as possible. Any noise added to the analog signal will transfer through into the digital signal, leading to inaccuracies and poor data integrity. When comparing the performance of the dual OPA625 driver and the single THS4551 FDA driver, there are advantages and disadvantages to both. The final decision on which front end to use will be based on the system bandwidth, THD, and power consumption requirements.

The FDA architecture will grant a benefit in THD through the reduction of the second harmonic distortion (HD2). When comparing the two configurations, an improvement of up to 4 dB in THD could be achieved when using an FDA. See [TIDA-01050](#) and [TIDA-01053](#) designs to learn more about design benefits with each amplifier.

2.2.6 ADS8910B ADC and Conversion Start Sync

Two ADS8910B high-speed SAR ADCs are used to convert data from an analog signal to a digital signal. The ADC directly follows either the THS4551 fully differential amplifier driver stage or the two OPA625s configured as a differential amplifier driver stage. The outputs of the driver stages are directly fed into the AINP and AINM pins on the ADS8910B. The ADS8910B is configured based as the specification recommends. For more information, see the [TIDA-01050](#) design. Pin 3 is an analog input for the reference voltage, the reference voltage is generated externally to the ADC and is discussed in [2.3.13](#).

As seen in [Figure 9](#), two different reference voltage nodes are attached to this pin using 0-Ω resistors as placeholders to select between the two options. This is done as one of the traces on the PCB would be made much longer to observe the potential losses and the effect that has on the accuracy of the ADC. R258, C289, and C93 were used as a low-pass filter to remove any potential high-frequency noise on the reference voltage. Pins 11 and 15 are the ground pins of the ADC and are connected to the systems ground. Pin 25 is the enable pin of the ADC; it is connected to ground to make sure the chip is always enabled.



Copyright © 2017, Texas Instruments Incorporated

図 9. ADS8910B and CONVST Sync Stage Altium Schematic

The SDO pins of the ADC (pins 17 to 20) were connected using 0- Ω resistors to two different locations. One of the traces goes directly towards a PHI connector where the performance of this ADC is analyzed. The other trace goes to an field-programmable gate array (FPGA), where the digital data can be compared with the serialized and de-serialized data to ensure no data is lost in translation. The RVS pin of the ADC also has two potential locations, selectable by a jumper (J24). One of those traces goes to the FPGA and the other goes to the PHI connector.

The serial data input (SDI) pin on the ADC, pin 22, is connected to the SDI of the PHI connector board. This connection makes it so that the ADC is controlled by the FPGA on the PHI board. The SDI pin feeds data or commands into the device. The FPGA on the PHI board is generating the SDI signal. Both of the ADCs are connected to the same SDI signal; because only one ADC would be tested at a time, no interference would be generated by doing this. The SCLK pin, pin 23, is the clock input pin for the serial interface.

All system-synchronous data transfer protocols are timed with respect to the SCLK signal. As seen in [Figure 9](#), there are two options for the source of SCLK. One of the options is to use the SCLK from the PHI connector, and the other option is to generate an SCLK signal from the FPGA on the board and feed that into the ADC. These two options are selectable with a two-pin jumper (J22). The chip select pin, pin 24, also has the option to be connected to the external PHI connector or to the onboard FPGA. The chip-select pin is active low and requires a low input for the device to take control of the data bus. The reset pin, pin 2, is also connected to the PHI connector in the same manner as the SDI signal is. Just like with the SDI signal, both ADCs are connected to the same reset signal. A low pulse on the reset pin resets the device. All register bits will then return to the default state.

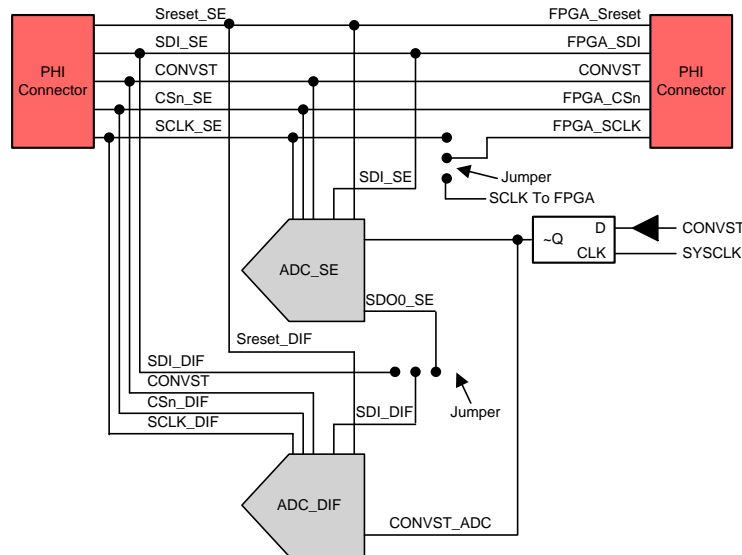
表 3. SN74AUP1G80 Function Table

INPUTS		OUTPUT
CLK	D	\bar{Q}
\uparrow	H	L
\uparrow	L	H
L or H	X	\bar{Q}_0

As seen in [Figure 9](#), a unique approach is taken with the conversion start signal. Pin 1 on the ADC, CONVST, is used to start the ADC conversion. However, the CONVST signal needs to be synchronized with the SYSCLK signal to ensure proper data integrity. To achieve this, an inverter and a D flip-flop are used to synchronize the conversion start signal coming from the PHI connector to the SYSCLK signal generated by the clock circuit. The CLK input to the flip-flop is the SYSCLK signal that is consistent throughout the system. Decoupling capacitors of 1 μ F and 10 μ F were used on both the flip-flop and inverter. J33 in [Figure 9](#) was placed so that the unsynchronized conversion start signal could be used if wanted.

To ensure the best results, onboard clocking was implemented. When maximizing system performance, clock jitter must be kept to an absolute minimum. TI's PHI is an external device. Clock jitter can be added to the system through the connection between the PHI and the TIDA-01051 board. This is prevented by using onboard clocking and the onboard CONVST/SYSCLK synchronization.

図 10 highlights the input signals going into each ADC. Two PHI connectors are present on the board: one takes data from the ADCs directly, while the other receives the de-serialized data coming out of the onboard FPGA. However, both ADCs are sharing input signals coming from each PHI connector. The reset signal is connected to each PHI connector and ADC. This is also the case for the SDI signal, the conversion start signal, the chip select signal, and the SCLK signal. The ADC with the differential amplifier in the front end has a jumper on the SDI signal. One end of the jumper connects to the same SDI signal as the other ADC while the other end of the jumper connects to SDO-0 of the other ADC. This is done so that both ADCs could be run in daisy-chain mode.



Copyright © 2017, Texas Instruments Incorporated

図 10. ADC Input Signal Tree

図 11 highlights the necessary connections required to operate in a daisy-chain configuration. The CONVST, CS, and SCLK inputs of all devices are connected together and controlled by a single CONVST, CS, and SCLK pin of the host controller, respectively. The SDI input pin of the first device in the chain (Device 1) is connected to the SDO pin of the host controller, the SDO-0 output pin of Device 1 is connected to the SDI input pin of Device 2, and so on. The SDO-0 output pin of the last device in the chain (Device N) is connected to the SDI pin of the host controller.

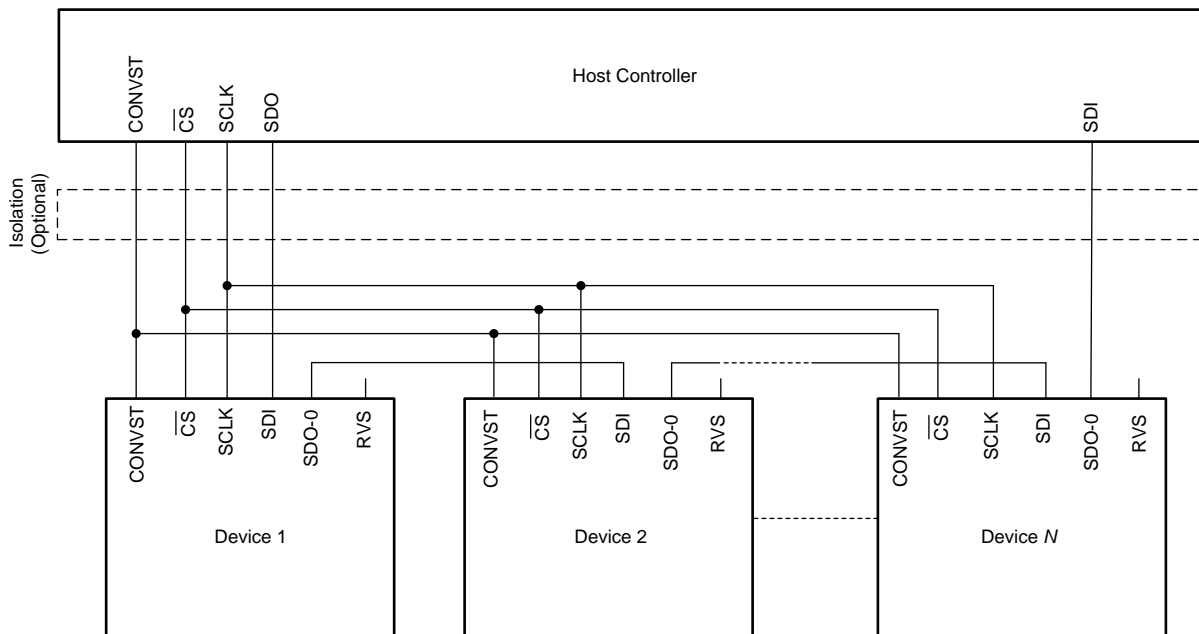


図 11. ADC Daisy-Chain Connections

To operate multiple devices in a daisy-chain topology, the host controller sets the configuration registers in each device with identical values and operates with any of the legacy, SPI-compatible protocols for data-read and data-write operations ($SDO_CNT[7:0] = 00h$ or $01h$). With these configurations settings, the 22-bit ODR and 22-bit IDR registers in each device collapse to form a single, 22-bit unified shift register (USR) per device, as shown in 図 12.

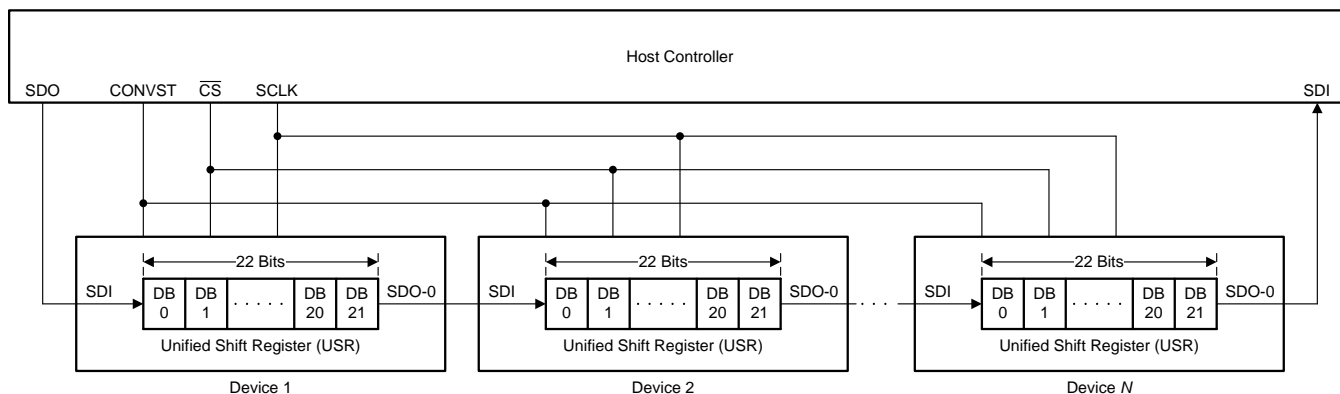


図 12. Unified Shift Register

All devices in the daisy-chain topology sample the respective device analog input signals on the CONVST rising edge. The data transfer frame starts with a CS falling edge. On each SCLK launch edge, every device in the chain shifts out the MSB of the respective USR on to the respective SDO-0 pin. On every SCLK capture edge, each device in the chain shifts in data received on the respective SDI pin as the LSB bit of the respective USR. Therefore, in a daisy-chain configuration, the host controller receives the data of Device N, followed by the data of Device N – 1, and so on (MSB-first). On the CS rising edge, each device decodes the contents in the respective USR, and takes appropriate action.

A typical timing diagram for three devices connected in daisy-chain topology using the SPI-00-S protocol is shown in [Figure 13](#).

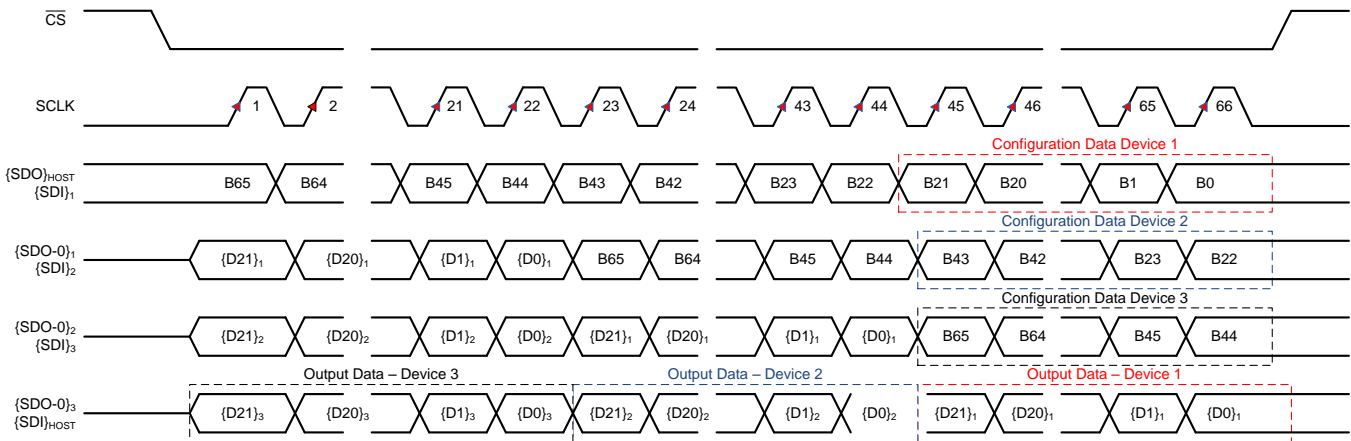


Figure 13. Three-Device, Daisy-Chain Timing

In daisy-chain topology, the overall throughput of the system is proportionally reduced as more devices are connected in the daisy-chain.

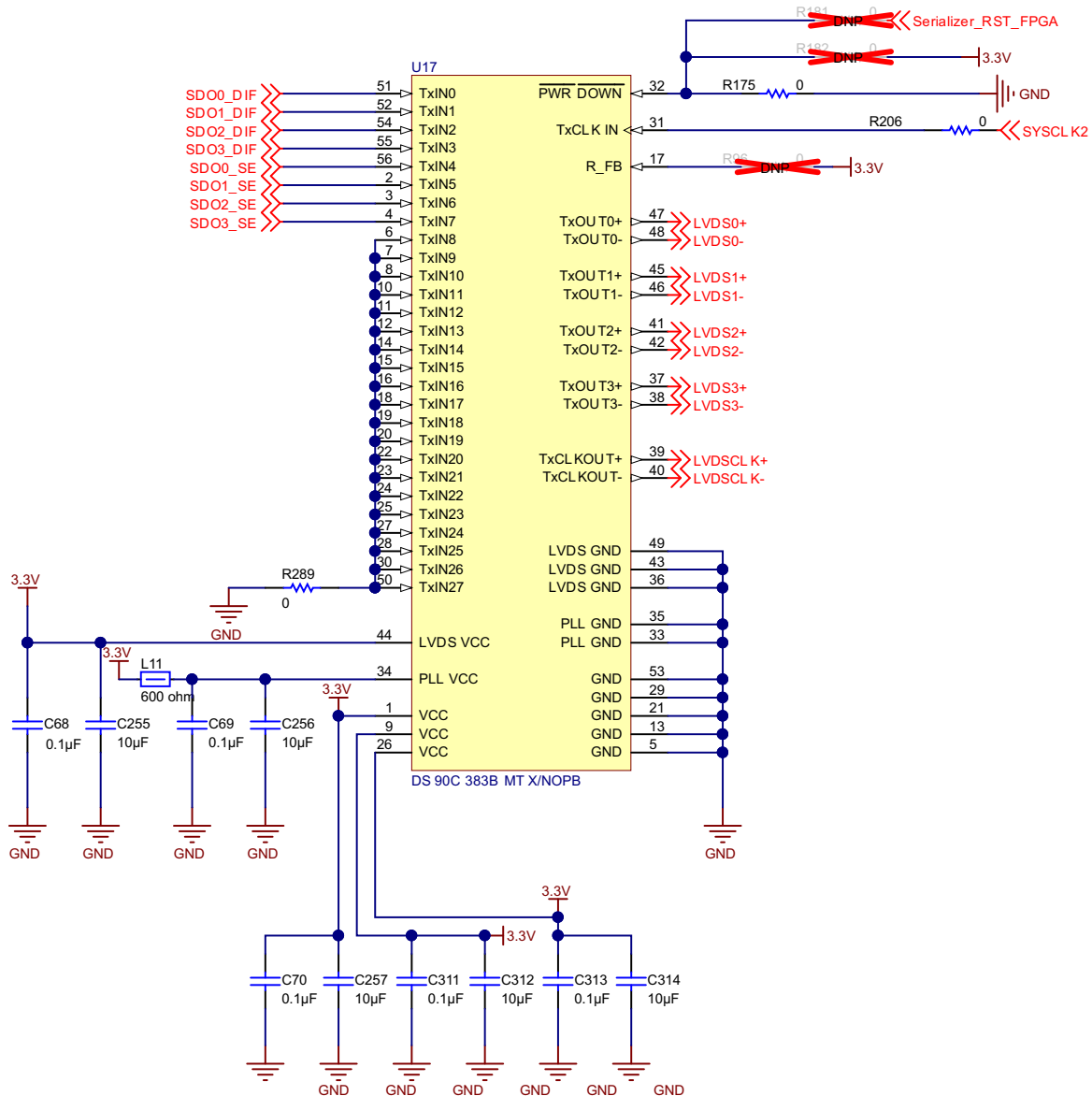
The ability to operate in daisy-chain mode was added as a proof of concept and is not tested in this design guide. There are disadvantages to using daisy-chain mode as well. If many devices are added in daisy-chain mode, an additional delay will be added to transfer the data out. This affects the maximum possible sampling rate of the system.

As seen in [Figure 10](#), there is also a jumper on the SCLK line. This option is included to make sure all the SCLK signals are connected together when data is being read individually from each ADC. In addition to that, there is also the option to feed the SCLK signal into the FPGA. When reading de-serialized data out of the FPGA, the data will be synchronized to this SCLK signal and made readable to the PHI connector.

2.2.7 DS90C383B Serializer

After the input data is converted from an analog signal to a digital signal, the data has the option to go to two different locations. The data will either be read by the PHI connector and checked for accuracy, or it will be sent to the serializer where it is converted to an low-voltage differential signaling (LVDS) signal at 7x the speed.

The first eight TxIN pins connect to the SDO pins on the ADCs as seen in [Figure 14](#). These are all TTL inputs. The same SYSCLK signal is input to the serializer as to the FPGA, ADC, and PHI connector. SYSCLK is always running. This ensures that the phase locked loop for the CLK frequency multiplier inside the serializer is locked when the data is shipped to it. TxCLK IN is the pin where SYSCLK is input to the serializer. This pin is for the TTL level clock input. The falling edge acts as the data strobe.



Copyright © 2017, Texas Instruments Incorporated

図 14. DS90C383B Serializer Altium Schematic

Three different power supplies are present inside the serializer. One of these is for the TTL inputs, another is for the phase locked loop, and the third is for the LVDS outputs. As seen in 図 14, each power pin is connected to 3.3 V with their own 10- and 0.1- μ F decoupling capacitors. This is done to ensure each power pin has the ability to filter out noise present on the power rail. Because the phase locked loop is much more sensitive to noise, a ferrite bead is added on its power supply to ensure proper stable operation.

The DS90C383B serializer takes the output data from the ADCs and converts it into an LVDS signal at 7 \times the speed. As seen in 図 15, the data shipped on each output line corresponds to the value of the input pin. The bits are aligned as shown in 図 15. For each clock cycle, 7 bits are shipped on each of the four output lines. This makes for a total of 28 bits, corresponding to the 28 available input pins on the serializer. Because this application only requires eight inputs, only bits 0 to 7 will be considered. Bits 8 to 27 will always be logic low.

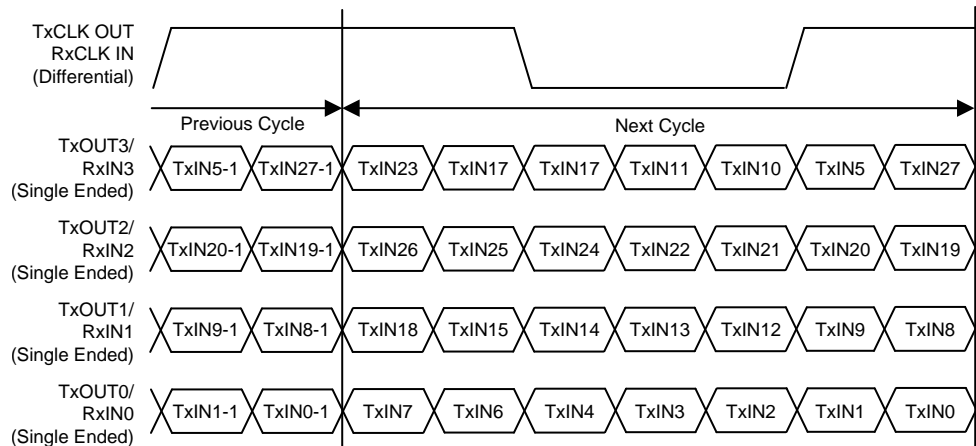


図 15. DS90C383B 28 Parallel TTL Data Inputs Mapped to LVDS Outputs

Traditional LVCMOS signals have one common ground wire that is the same for multiple signal lines. An LVDS signal is a low-voltage differential signal that requires two wires. LVDS signals are able to carry much higher frequencies than traditional LVCMOS signals. A 100- Ω resistor termination is placed in between the two parallel LVDS lines at the point of termination.

By serializing the digital data coming out of each ADC, the amount of pins used on an FPGA can be reduced by approximately a factor of 4. As seen in the data mapping of [図 14](#), 28 data input bits can be sent during one clock cycle over four LVDS signals. This is a much more efficient implementation of sending this data to an FPGA from the multiple data converters compared to sending each signal individually.

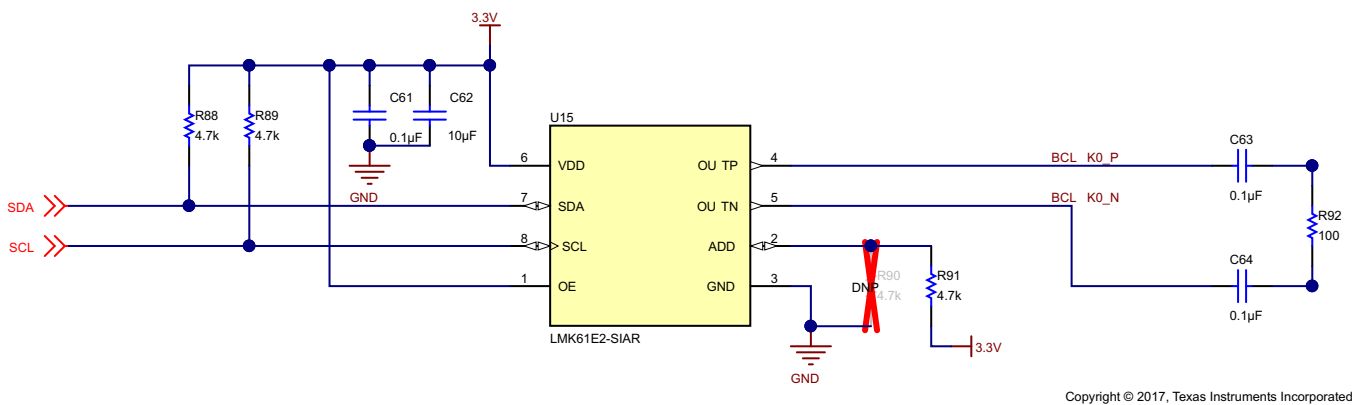
As seen in [図 14](#), there is also an LVDSCLK output coming out of pins 39 and 40. This clock takes the SYSCLK input and converts it to an LVDSCLK. This LVDSCLK is synchronized with the LVDS data lines, as shown in [図 15](#).

The R_FB pin, pin 17, is used to control the programmable strobe select. When connecting this pin to VCC, the serializer works on the rising edge strobe. If this pin is connected to ground or left open (NC), the serializer works on the falling strobe edge. In this application, a 0- Ω resistor is connected to VCC and can be removed to alter the programmable strobe select.

2.2.8 Clocking

The PHI is used to analyze ADC performance; however, the connection between the external PHI board and the system adds jitter. The LMK61E2 was used as the internal master clock in order to minimize the jitter effects. The LMK61E2 is an ultra-low jitter PLLatinum™ programmable oscillator with a fractional-N frequency synthesizer with integrated VCO that generates commonly used reference clocks. The outputs can be configured as LVPECL, LVDS, or HCSL. The device features self-startup from on-chip EEPROM that is factory programmed to generate a 156.25-MHz LVPECL output.

The device registers and EEPROM settings are fully programmable in system through an I²C serial interface. Internal power conditioning provide excellent power supply ripple rejection (PSRR), reducing the cost and complexity of the power delivery network. The device operates from a single 3.3-V ± 5% supply. The device provides fine and coarse frequency margining options through I²C serial interface to support system design verification tests (DVT) such as standard compliance and system timing margin testing.



Copyright © 2017, Texas Instruments Incorporated

図 16. LMK61E2 Altium Schematic

As seen in 図 16, pins 7 and 8 are connected to an external USB2ANY header (J3). SDA and SCL are used for the I²C serial interface. The USB2ANY header is used to connect an external I²C programmer. Both pins require an external pullup resistor to VCC.

VDD is connected to 3.3 V, and two decoupling capacitors are used. For the best electrical performance of the LMK61E2 device, use a combination of 10 μF, 1 μF, and 0.1 μF on its power supply bypass network. It is also recommended to use component side mounting of the power supply bypass capacitors, which is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections as short as possible between the bypass capacitors and the power supply on the device. Ground the other side of the capacitor using a low-impedance connection to the ground plane. The output enable pin of the LMK61E2 is also connected to VDD, which allows the output to always be enabled.

Pin 2 on the LMK61E2 is another digital control interface pin. When left open, LSB of the I²C slave address is set to "01". When tied to VDD, LSB of the I²C slave address is set to "10". When tied to GND, LSB of the I²C slave address is set to "00". As seen in 図 17, ADD can be connected to either VCC or GND through the configuration of the two 4.7-kΩ resistors. The default configuration is to connect ADD to VCC.

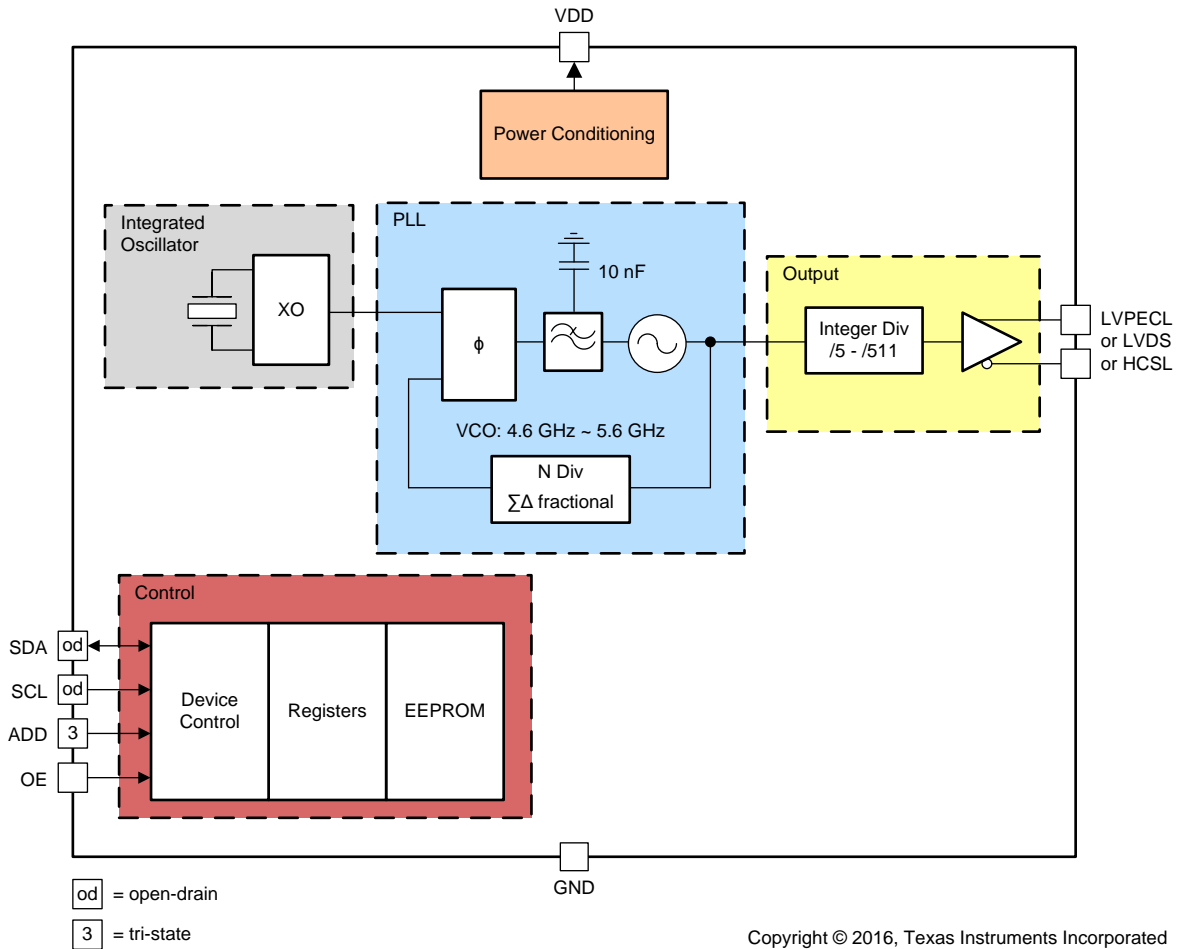


図 17. LMK61E2 Functional Block Diagram

The clock generator is configured to output a 65-MHz frequency clock signal across pins 5 and 4 of the device. These two pins comprise an LVDS signal that is then passed through a 0.1- μF capacitor and terminated with a 100- Ω resistor (see [Figure 18](#)).

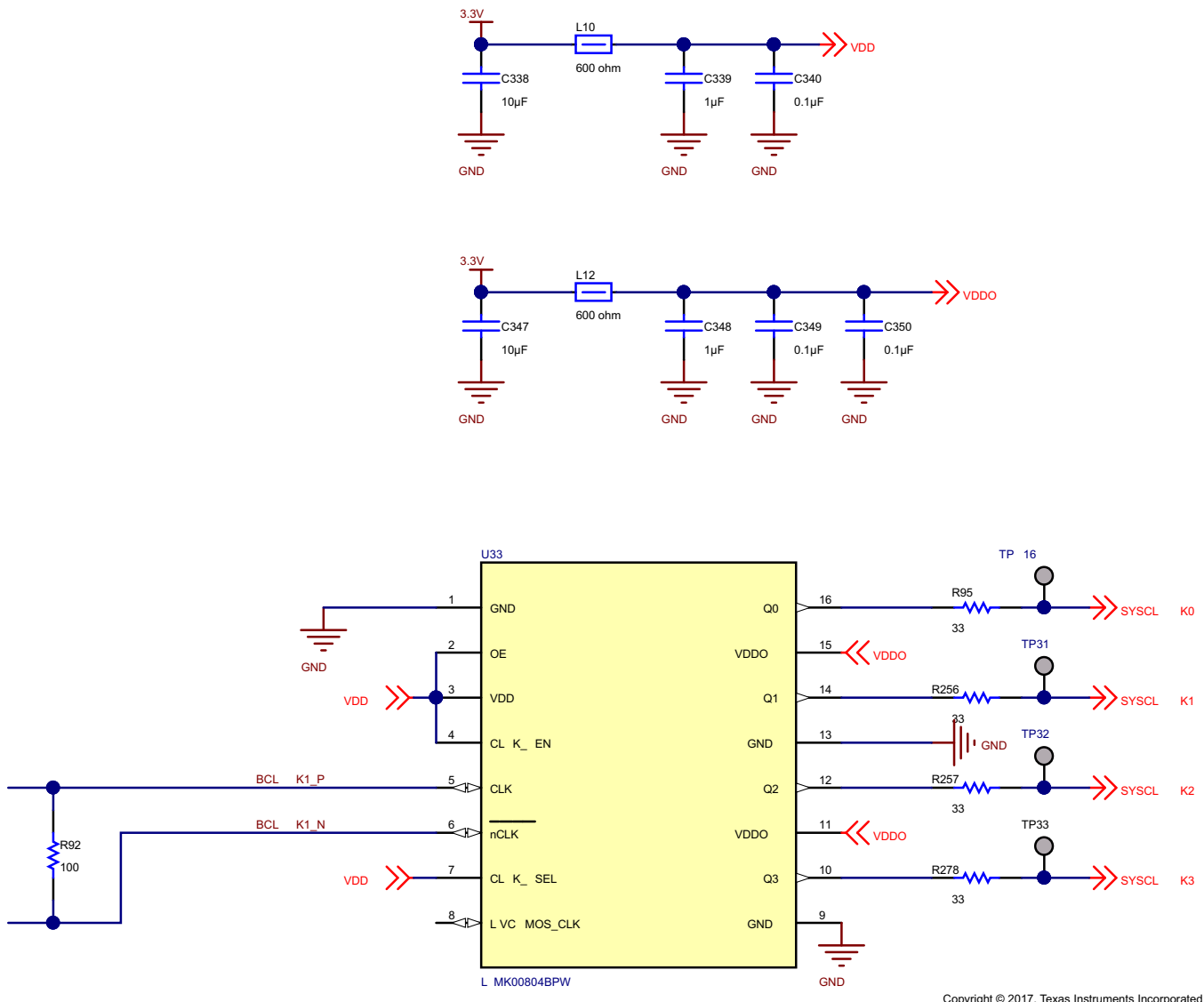


Figure 18. LMK00804BPW Clock Distributor Altium Schematic

The LMK61E2 outputs one LVDS clock signal; however, the system requires SYSCLK to go to four different locations. Each of these locations accepts an LVCMOS clock signal only. To handle this requirement, an LMK00804BPW is used. The LMK00804 is a clock fanout buffer that distributes four LVCMOS clocks. The LMK00804 is configured to accept a differential input clock and distribute it to four LVCMOS clocks that are all synchronized.

Pin 7, the CLKSEL pin, is used to configure what type of input clock is used. In this device, an LVDS clock was generated from the LMK61E2 so the LMK00804 needed to be configured to accept and LVDS clock. This is done by connecting pin 7 to VDD. If pin 7 is grounded, an LVCMOS clock can be input.

The four outputs from the LMK00804 go to four different places within the system. One of the clock outputs goes to the ADC conversion start synchronization logic, another goes to the DS90C383B serializer, another to the PHI connectors, and the last one to the onboard FPGA. The LMK61E2 generates a 65-MHz LVDS clock signal and the LMK00804B distributes this clock into four synchronized 65-MHz LVCMOS clock signals.

2.2.9 Power

This system requires a wide variety of voltage rails to meet the specification of the TI Design. The input voltage required for the system is 24-V DC. [Figure 19](#) highlights the distribution of the power tree into the different required rails. See the [TIDA-01050](#) design to learn more about the power stage design of this TI Design.

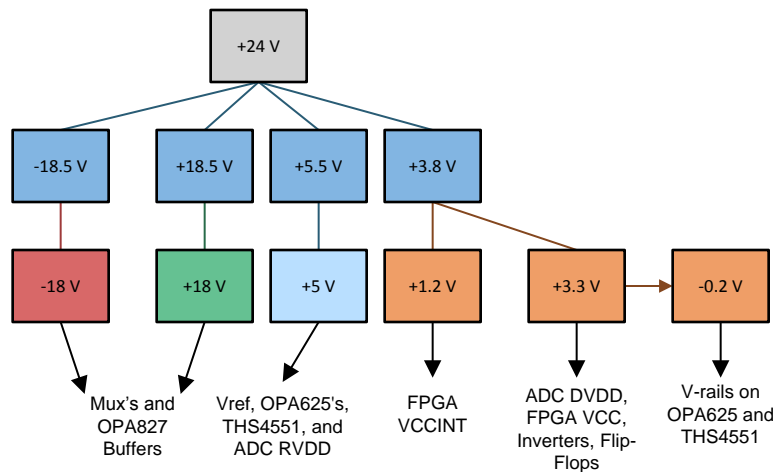


Figure 19. System Power Tree

2.2.9.1 3.3-V Rail Design Theory

To minimize the board size and switching power supply noise coupling into the signal path the 3.3-V rail circuitry was placed on the opposite side of the PCB as far away from the AFE components as possible. But even with this placement the AFE could be vulnerable to electromagnetic interference (EMI) generated by this supply. To avoid this, the LM53635M is used as the switching regulator. The LM53635M is a low EMI DC-DC converter. The evaluation module for the LM53635M was used to evaluate the EMI performance of the part before implementing it in this system. The output voltage was set to 3.8 V by adjusting the value of R_{FBB} according to [Equation 2](#):

$$R_{FBB} = \frac{R_{FBT} \times V_{REF}}{V_{OUT} - V_{REF}} \tag{2}$$

R_{FBT} is set to 100 kΩ and V_{REF} is equal to 1 V. This results in a value of 36 kΩ for the feedback resistance. See the [TIDA-01054](#) design to learn more about the 3.8-V power rail design.

The 3.8-V output of the LM53635M was then connected to a TPS7A47 adjustable output LDO to attenuate the ripple and to bring the DC voltage down to 3.3 V (see [Figure 20](#)).

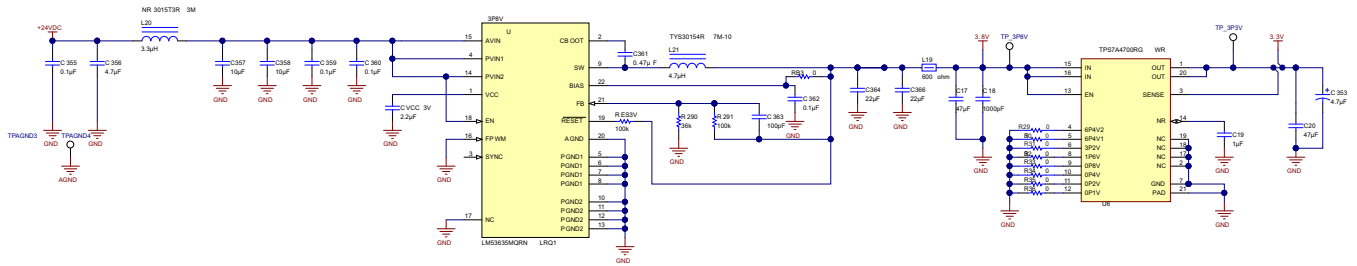


図 20. 3.3-V Rail Altium Schematic

Copyright © 2017, Texas Instruments Incorporated

A similar approach was taken for the design of the 5- and 18-V rails (see [Figure 21](#)). Again, the TPS7A47 adjustable LDOs are used to attenuate the ripple voltage. The value of R_{FBB} was calculated using [Equation 2](#). See the [TIDA-01054](#) design to learn more about the 5- and 18-V power rail design.

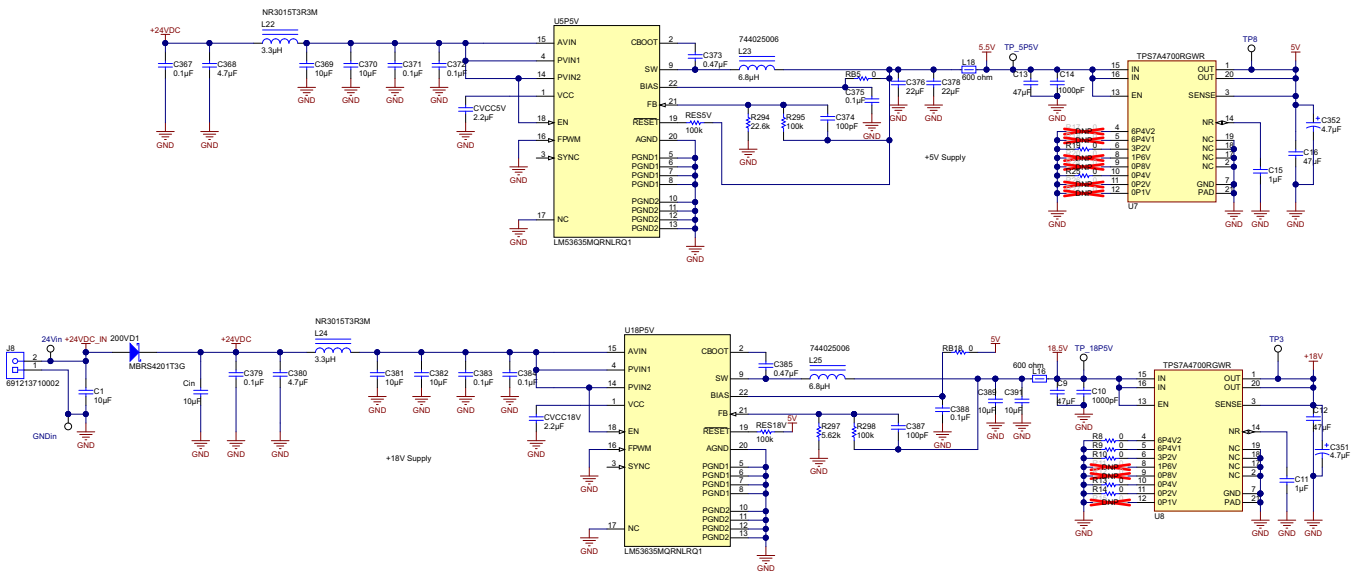
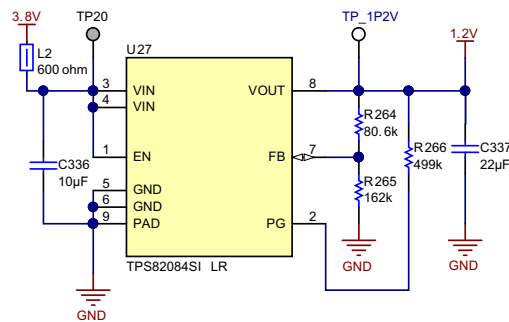


Figure 21. 18.5- and 5.5-V Rails Altium Schematic

2.2.9.2 1.2-V Rail Design Theory

A 1.2-V rail is required for one of the FPGA power supplies. Because this is a digital supply only, the switching frequencies are not much of a concern. Due to this, a second switching regulator was used to maximize the efficiency of this rail. The TPS82084 has an integrated inductor to simplify design, reduce external components, and enable a very small solution size. As seen in [Figure 22](#), implementing this device is simple.



Copyright © 2017, Texas Instruments Incorporated

Figure 22. 1.2-V Rail Altium Schematic

The output voltage is set by an external resistor divider according to :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8 \text{ V} \times \left(1 + \frac{R1}{R2}\right)$$

Where R1 is R264 from [Figure 22](#) and R2 is R265. R2 should not be higher than 180 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. [Figure 22](#) shows a recommended external resistor divider value for a 1.2-V output. Choose appropriate resistor values for other output voltages. Datasheet guidelines were followed in selecting the values and the appropriate types of the input and output capacitors.

2.2.10 Xilinx™ Spartan® 3 FPGA and Verilog Code

An FPGA is used to convert the serialized LVDS data back to an LVCMOS format. The FPGA also compares the data coming directly out of the ADC with the de-serialized data to check for discrepancies. The Xilinx Spartan 3 was chosen for this TI Design. See the [TIDA-00732](#) design for more information on the Spartan 3.

To generate code for the FPGA, the ISE® Project Navigator from Xilinx was used. Verilog modules were developed for each component in the signal chain to simulate changes in clocking and data throughout the system.

The first module was to generate the SYSCLK. Initially, a clock 7× the speed of SYSCLK was generated on the test bench. The system clock was then generated by dividing this 7× clock signal. To divide the clock by 7, the positive and negative edges of the 7× clock are counted from 0 to 13 in the software. Whenever the edge count is less than 6, the output of SYSCLK will be high. Whenever the edge count is between 6 and 13, the output of SYSCLK will be low.

Figure 23 highlights the test bench results from simulating the SYSCLK module. The SYSCLKx7 signal has a frequency 7× larger than the SYSCLK frequency.

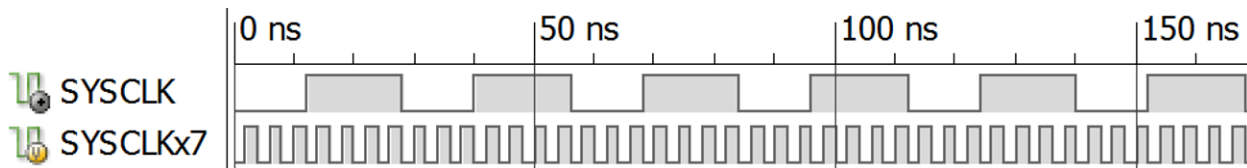


Figure 23. SYSCLK Test Bench Results

Next, a Verilog module was developed to generate an SCLK signal. In the final system, the SCLK signal would be created from the PHI module and would not come from the onboard FPGA. This SCLK signal was generated for simulation purposes only to thoroughly test the FPGA code. The CONVST signal was also generated on the test bench and was used in the SCLK module to synchronize the SCLK signal. In the SCLK module, when the conversion start signal goes high, 22 clock pulses of SYSCLK are output as SCLK. To operate the ADC in source-synchronous mode, SCLK must go through 22 clocks to allow for proper conversion. After the 22 clock pulses are sent, the SCLK line will go low until the next rising edge of CONVST.

The test bench results in Figure 24 confirm that the SCLK module behaves as expected. For every rising edge of conversion start, 22 clock cycles are transmitted on the SCLK line at the same frequency as SYSCLK. However, the SCLK is synchronized with the CONVST signal as it is done in this TI Design with the additional flip-flop and inverter.

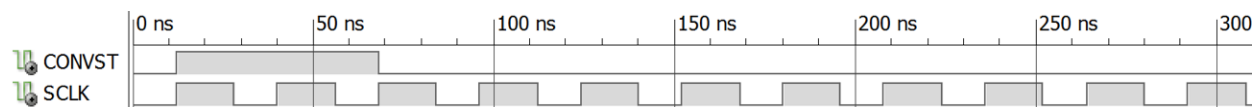


Figure 24. SCLK Test Bench Results

A Verilog module simulating a signal generator was created to change the input to the ADC with each conversion. The input to this module was the conversion start signal and 28 data lines were output. Although this specific system will be able to have at most 2 data inputs, 28 were simulated as a proof of concept for the modularity of this system and software.

An 18-bit register named "init_signal" was used to initialize the input signal. Then with each conversion start rising edge, an adjustable amount was added to the value of init_signal, and each signal was shifted to the next data input. For example, data from the 27th input line went to the 26th input line, and data from the 26th input line went to the 25th input line at each conversion start (see [Figure 25](#)).

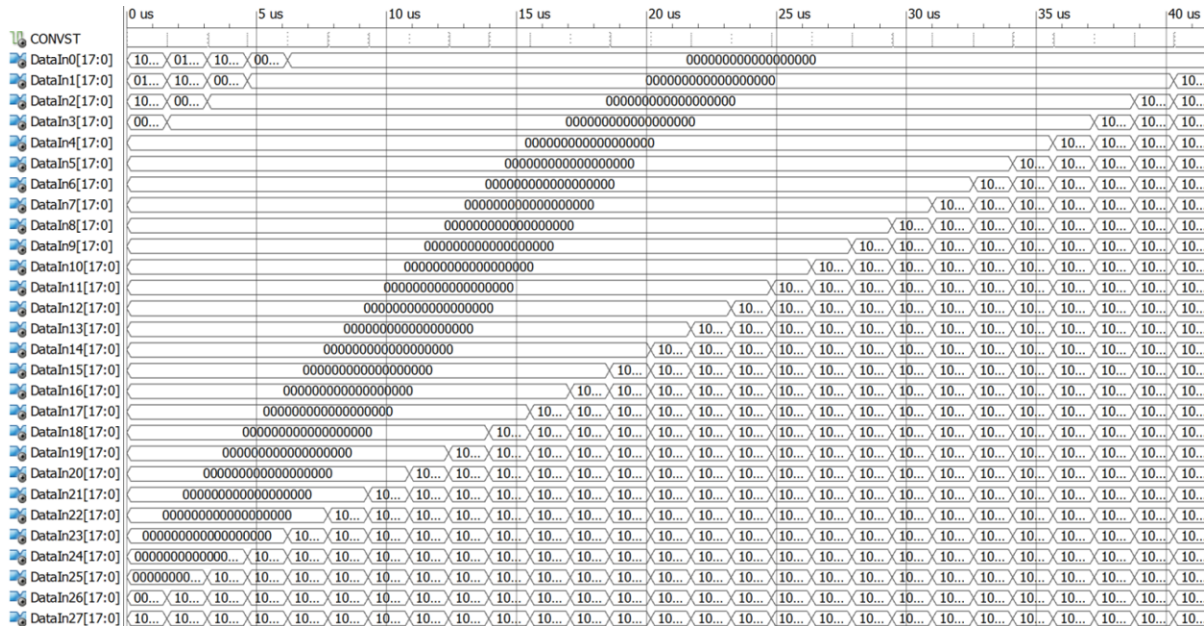


Figure 25. SigGen Test Bench Results

Because this is a digital environment, analog signals could not be generated in this simulation. Instead, 18-bit signals were. The ADC Verilog module would then take each 18-bit signal and distribute it over the respective SDO lines in the same manner that the ADC would output data in synchronization with the SCLK signal. An RVS signal was also generated in the ADC module configured to be in the source-synchronous mode from the [ADS8910B datasheet](#).

At each rising edge of conversion start, the input data is shifted into the data registers of the ADC module. Once data is present on the data register, it will be output one bit at a time at each rising edge of the SCLK signal. After the 18th bit has been sent out on the corresponding SDO line, the SDO line will be low until the next data is available on the data register.

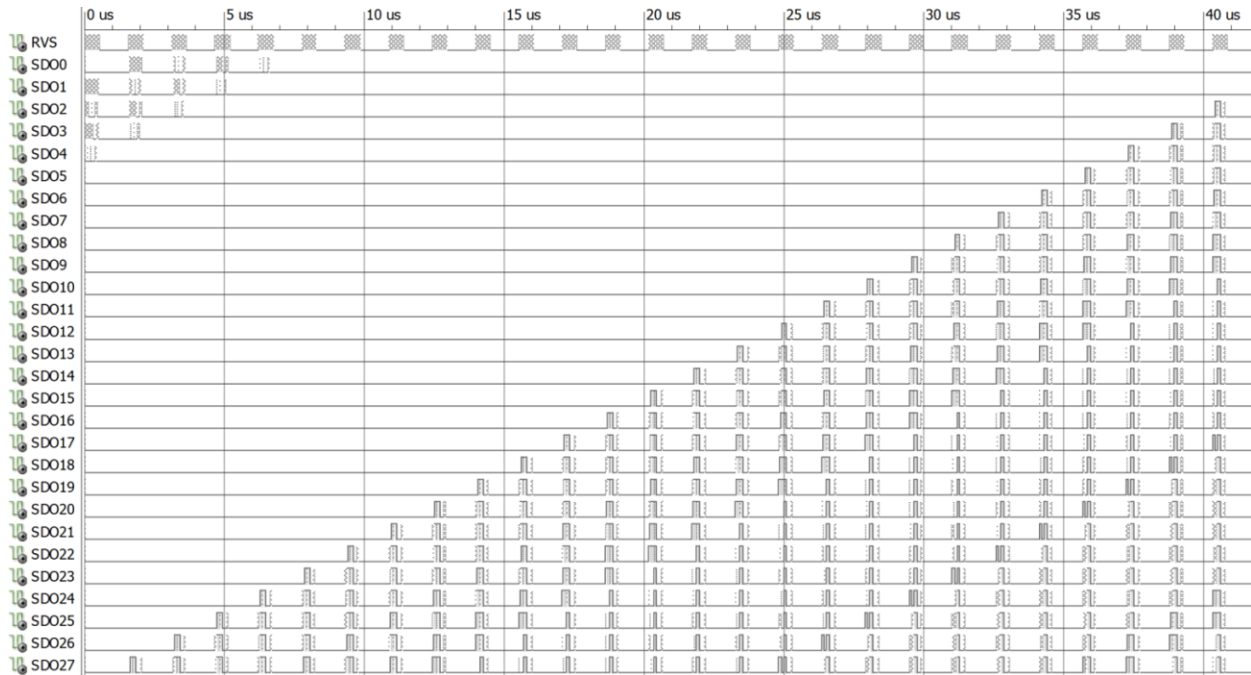


図 26. ADC Module Test Bench Results

The ADS8910B SAR ADC adds a delay between the SCLK signal and RVS output signal. 図 27 highlights this delay and refers to it as t_{d_CKSTR} . This delay is equal on both the rising and falling edge of the SCLK signal. The data lines are then delayed by an additional amount to the RVS signal. 図 27 refers to this delay as t_{off_STRDO} . This delay is also equal on the rising and falling edge. The ADC Verilog module implements these delays as well to properly simulate the response of the entire system.

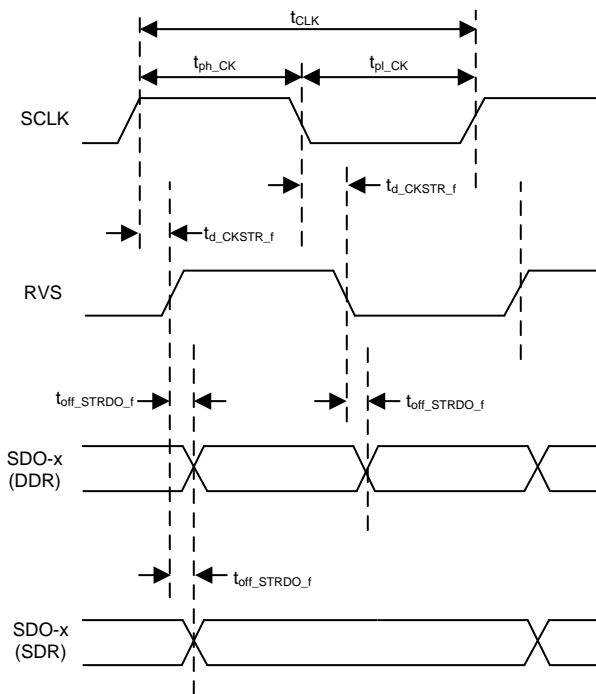


図 27. Source-Synchronous Serial Interface Timing

After the data is output by the ADC, it will be sent to the serializer. Here the data will be transformed into a differential signal and be sent out at 7x the speed on four LVDS lines. A Verilog module for the serializer was created to simulate the behavior of this subsystem. The DS90C383B serializer also takes in the SYSCLK frequency and outputs it in an LVDS format. This was implemented in the module by outputting two clocks at the SYSCLK frequency, one in phase with the original SYSCLK and the other an inverted version of SYSCLK. This allowed the LVDS signals to be simulated.

Figure 28 highlights how the 28 data bits would be output by the four LVDS lines of the serializer. The Verilog Serializer module takes the 7x clock input and delays it by 6 ns. The datasheet states the typical delay for the clock is 5 ns. However, for this simulation, it was easier to implement 6 ns as this corresponded to three periods of the SYSCLKx7 signal. Once the 7x clock was properly delayed according to spec, the data bits could be output on the delayed clock signal. A falling strobe edge was used on the serializer. The Verilog module counts the falling edges of the delayed 7x SYSCLK signal and then uses shift registers to output the correct bits at the correct time. As shown in Figure 28, the first two bits are output on the high side of the incoming clock signal. The next three are output during the low time of the incoming clock signal. Finally, the last 2 bits are output at the next high side of the incoming clock signal.

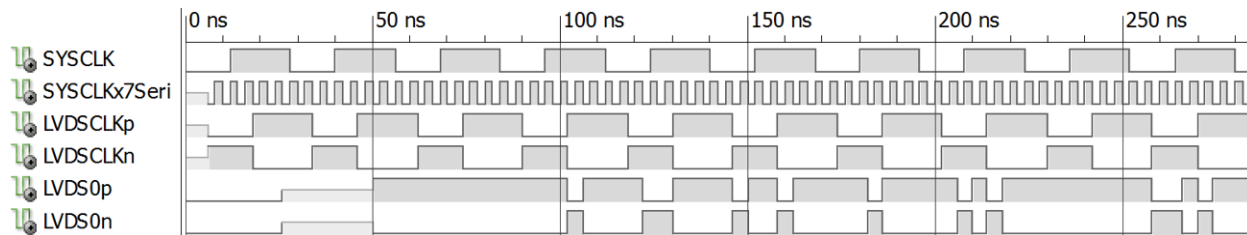


Figure 28. Serializer Module Test Bench Results

Figure 28 highlights the results of simulating the serializer Verilog module. Random data was input to the system at this time. It is evident that the LVDSCLK signal is delayed from the SYSCLK signal as described in the [DS90C383B datasheet](#). The LVDS0 data is aligned with the LVDSCLK signal as described in Figure 27. The other LVDS data lines are also matching with the specifications of the DS90C383B. To simplify the PCB routing, the data lines were inverted on the input of the FPGA so that the traces could go straight from the serializer to the FPGA without having to cross. However, this option is not available for the clocking signal. To properly simulate this inversion, the data coming out of the serializer module was also inverted.

To then deserialize the data and send it out to the other PHI module. A deserialization program from Xilinx was used. See [Xilinx's XAPP485](#) to learn more about deserialization.

Follow these steps to set up XAPP485 to work in this TI Design:

1. Download and create an ISE project for the files included in "4bit_verilog" from [XAPP485](#).
2. Generate a UCF file for the output and input pins used.
3. In the "serdes_4b_1to7.v" module, move the 24th bit to the 0-bit position in line 176.
4. Delay the RVS input signal by 16 to 17 periods of the rxclk35 signal.
5. Output dataouta[0] and the delayed RVS signal to the PHI module.

After the LVDS output data was deserialized, it was compared to the initial input signal. To avoid redundancy here, only the first data input was compared. To implement this program, the output data was placed into an 18-bit shift register. Whenever all 18 bits were filled, the data was output and is compared to the input signal data. The input signal data was delayed by the same amount of time that the conversion would take. These two registers were then compared and whenever the value of this difference was not 0, an LED on the board would turn on.

As seen in [Figure 29](#), the difference between the first 18-bit output data register and the first data input signal is 0 throughout the simulation. This confirms the functionality of the deserializer and ensures that the data coming out of the system is equal to what is coming into the system.

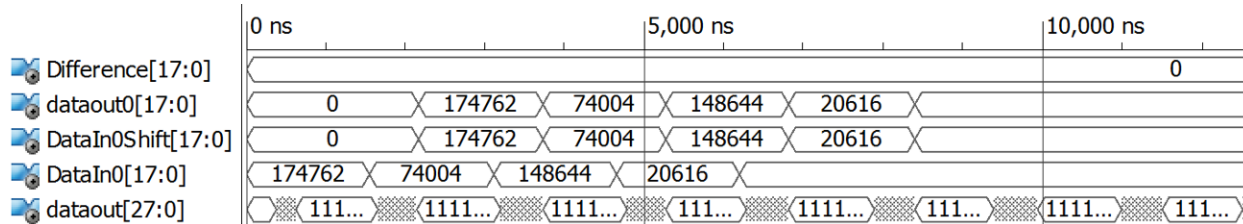


Figure 29. Output Data Comparison Test Bench Results

2.2.11 System Timing

Four SYSCLK signals are generated through the LMK61E2 and LMK00804B clocking circuitry (see [Figure 30](#)). The frequency of the system clock is 65 MHz as that is the highest frequency the DS90C383B serializer will accept. When the SYSCLK signal travels from the clocking circuit to the attached PHI board, there will be a slight delay added due to propagation on the PCB trace. The conversion start signal is sent to the flip flop by the ADC to be synchronized with the SYSCLK signal. There is also a slight delay in this signal.

When data is ready to be converted, the RVS signal goes high for the corresponding ADC. These two signals are "Anded" by the FPGA and the output of that and gate is sent to the FPGA on the PHI board. When the FPGA on the PHI board sees a high on the RVS input, it will generate SCLK starting at the next rising edge of SYSCLK. The SCLK signal then receives a slight propagation delay as it travels from the PHI connector to the ADC. Once the ADC receives the SCLK signal, digital data will begin to be transmitted on the SDO lines. Again, a slight propagation delay is added on this data as well when it travels to the FPGA on the PHI board. The ADC then generates a CLK on the RVS pin that is synchronized with the serial output data.

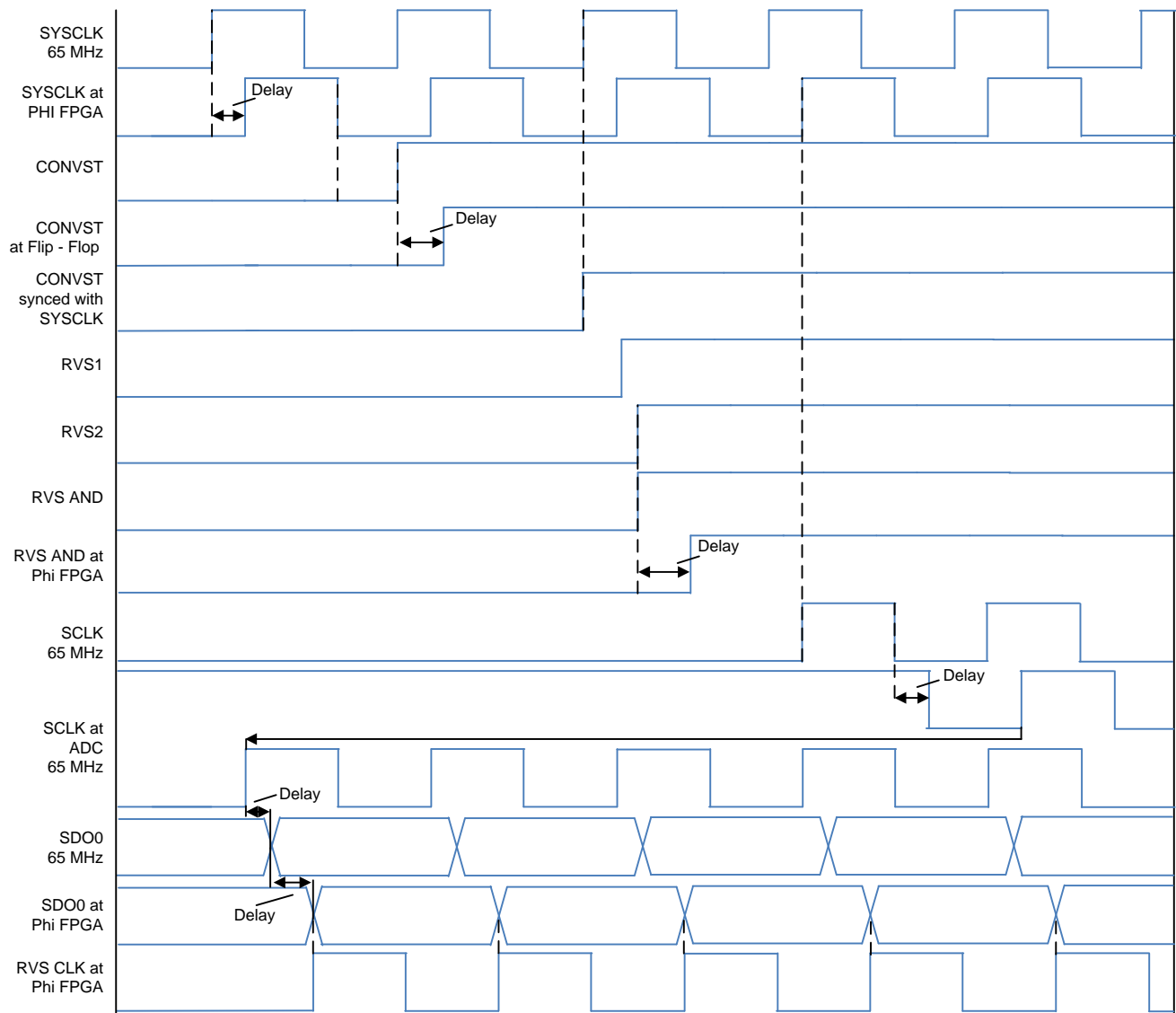


図 30. Timing Diagram for PHI Connector

The timing for the data traveling through the serializer is slightly different from that of the PHI board (see [Figure 31](#)). The same four SYSCLK signals are generated from the clocking circuitry. The conversion start signal is generated from the PHI board and is synchronized with the system clock through the inverter and flip flop by the ADC. The RVS signals coming from each ADC are then "Anded" and go into the onboard FPGA. The SCLK signal is then sent to the onboard FPGA from the PHI board with a slight propagation delay.

The FPGA then recreates this signal and sends it to the ADC. Once it arrives at the ADC, the ADC will ship out serial data towards the serializer. The serializer has an internal 7× clock multiplier. The serializer is always running on the system clock signal so that the internal phase lock loop is always locked. Once data enters the serializer, it is exported in an LVDS form based on the timing diagram in [Figure 15](#). The serializer also outputs an LVDS version of SYSCLK. These LVDS signals then go into the onboard FPGA where they are analyzed and deserialized. The code on the FPGA is using a 3.5× clock multiplier and is sampling on the rising and falling edge to have the same effect as a 7× clock.

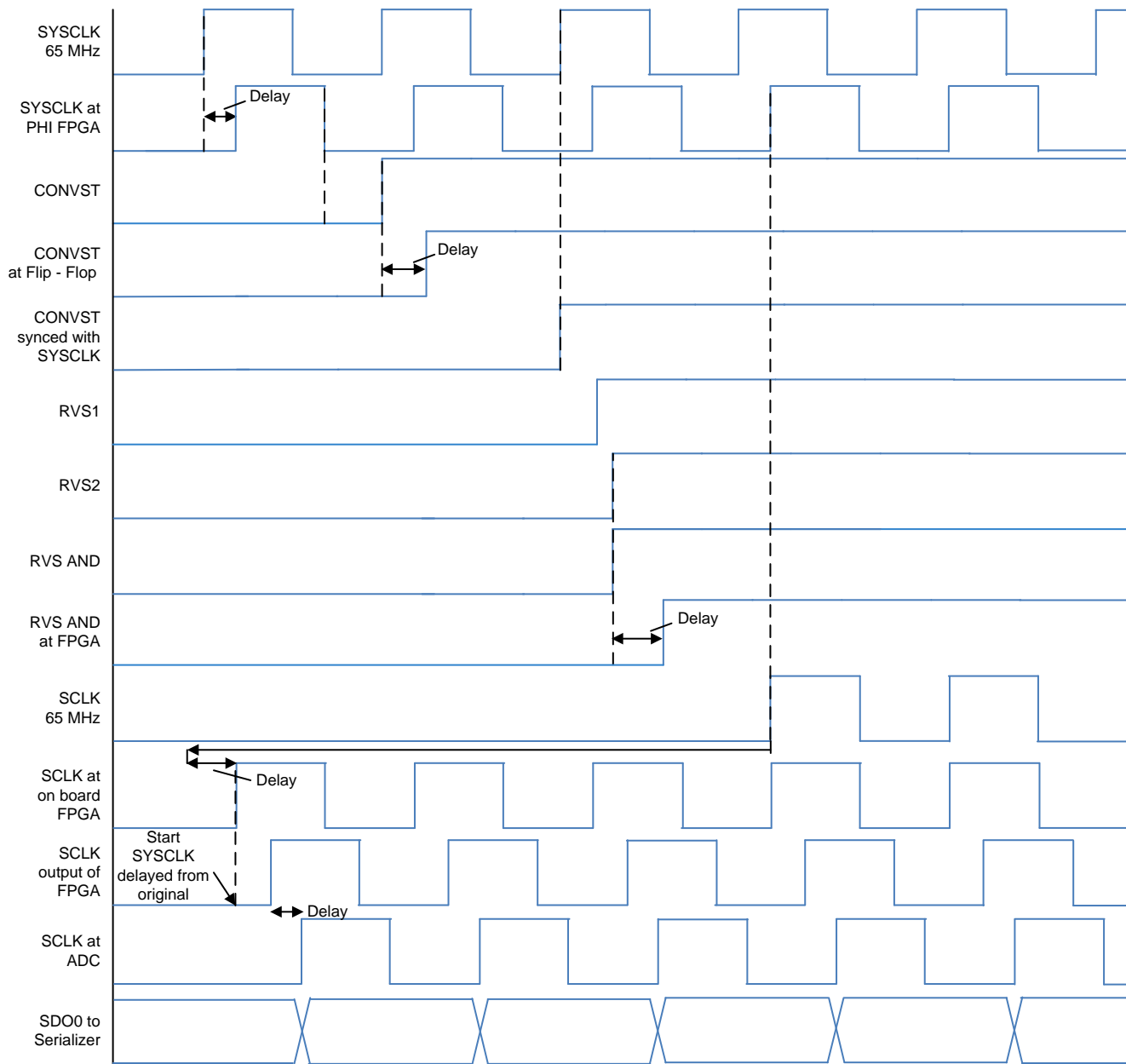


図 31. Timing Diagram for Serializer Data

2.2.12 Host Interface

This TI Design supports the following host interface to evaluate system performance:

- PHI is TI's SAR ADC evaluation platform, which supports the entire TI SAR ADC family. By using PHI, the system easily communicates with the host PC using a USB interface. PHI supports the ADS8910 multiSPI™ and onboard configuration I²C EEPROM interface. PHI GUI software can be used to evaluate both AC and DC parameter of the ADS8910B. For more information on PHI, see the [ADS8910B EVM-PDK](#).

The PHI module software was modified to include the ability to accept an external clock input. This same software was used in the [TIDA-01035](#) design.

2.3 Highlighted Products

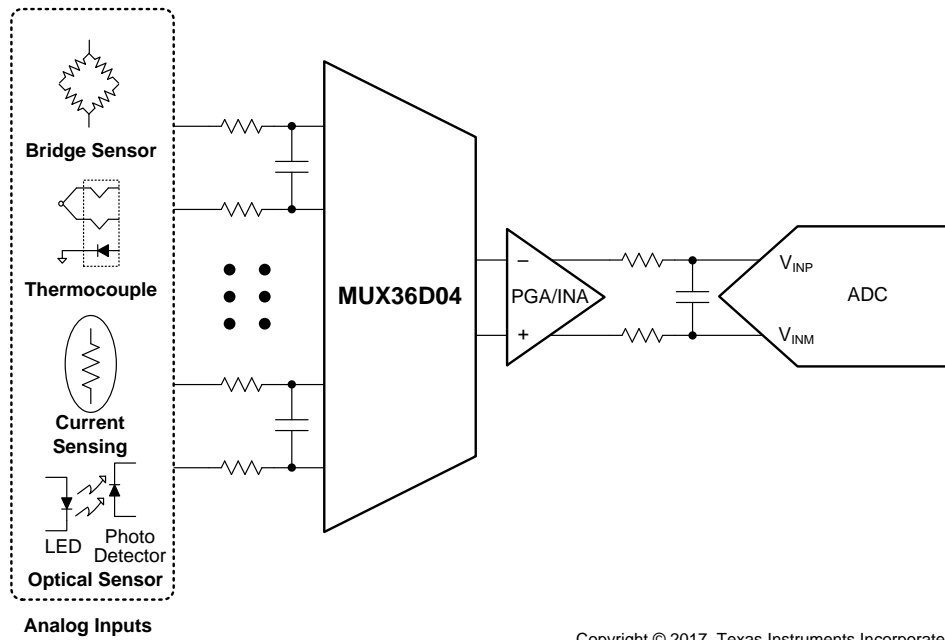
Key features for selecting the devices for this reference design are highlighted in the following subsections. Find the complete details of the highlighted devices in their respective product datasheets.

2.3.1 MUX36D04

The MUX36S08 and MUX36D04 (MUX36xxx) are modern complementary metal-oxide semiconductor (CMOS) analog multiplexers (muxes). The MUX36S08 offers 8:1 single-ended channels, whereas the MUX36D04 offers differential 4:1 (8:2) channels (see [Figure 32](#)).

The MUX36S08 and MUX36D04 work equally well with either dual supplies (± 5 to ± 18 V) or a single supply (10 to 36 V). They also perform well with symmetric supplies (such as $V_{DD} = 12$ V, $V_{SS} = -12$ V), and asymmetric supplies (such as $V_{DD} = 12$ V, $V_{SS} = -5$ V). All digital inputs have TTL logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. The MUX36S08 and MUX36D04 have very low on and off leakage currents, allowing these multiplexers to switch signals from high input impedance sources with minimal error. A low supply current of 45 μ A enables use in portable applications.

The specification of this system required a large input voltage swing of 12 to -12 V. To achieve this specification, ± 18 -V rails needed to be used. The MUX36D04 is specifically chosen for this design due to its low on-capacitance, low input leakage, low charge injection, and rail-to-rail operation. The MUX36D04 is also the only 36-V mux currently at TI. The device supports the design specifications for the 200-kHz input signal and three levels of the mux tree.



Copyright © 2017, Texas Instruments Incorporated

図 32. MUX36D04 Simplified Schematic

2.3.2 OPA827

The OPA827 series of JFET operational amplifiers combine outstanding DC precision with excellent AC performance. These amplifiers offer low offset voltage (150 μV , maximum), very low drift over temperature (0.5 $\mu\text{V}/^\circ\text{C}$, typical), low-bias current (3 pA, typical), and very low 0.1-Hz to 10-Hz noise (250 nV_{PP}, typical). The device operates over a wide supply voltage range (± 4 to ± 18 V) on a low supply current (4.8 mA/Ch, typical).

Excellent AC characteristics, such as a 22-MHz gain bandwidth product (GBW), a slew rate of 28 V/ μs , and precision DC characteristics make the OPA827 series well-suited for a wide range of applications including 16- to 18-bit mixed signal systems, transimpedance (I/V-conversion) amplifiers, filters, precision ± 10 -V front ends, and professional audio applications. The OPA827s are used as signal buffers in this system. The OPA827 is currently the highest bandwidth 36-V op amp offered by TI.

2.3.3 OPA625

The OPAX625 family of op amps are excellent 16- and 18-bit SAR ADC drivers that are high precision with low THD and noise allow for a unique power-scalable solution. This family of devices is fully characterized and specified with a 16-bit settling time of 280 ns that enables a true 16-bit effective number of bits (ENOB). Along with a high DC precision of only a 100- μV offset voltage, a wide gain-bandwidth product of 120 MHz, a low wideband noise of 2.5 nV/ $\sqrt{\text{Hz}}$, this family is optimized for driving high-throughput, high-resolution SAR ADCs, such as the ADS88xx family of SAR ADCs.

The OPA625 is used in many SAR ADC reference designs. The device is also used in the [ADS8910B evaluation model](#). The OPA625 is often regarded as the best 5-V ADC driver amplifier available today from Texas Instruments.

Figure 33 shows a block diagram of the OPA625:

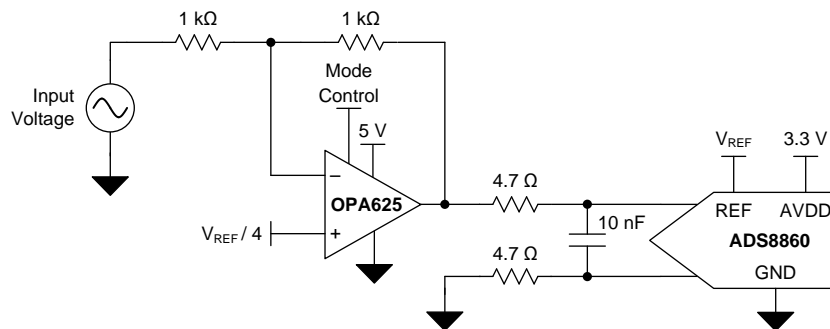


Figure 33. OPA625 SAR ADC Driver Configuration

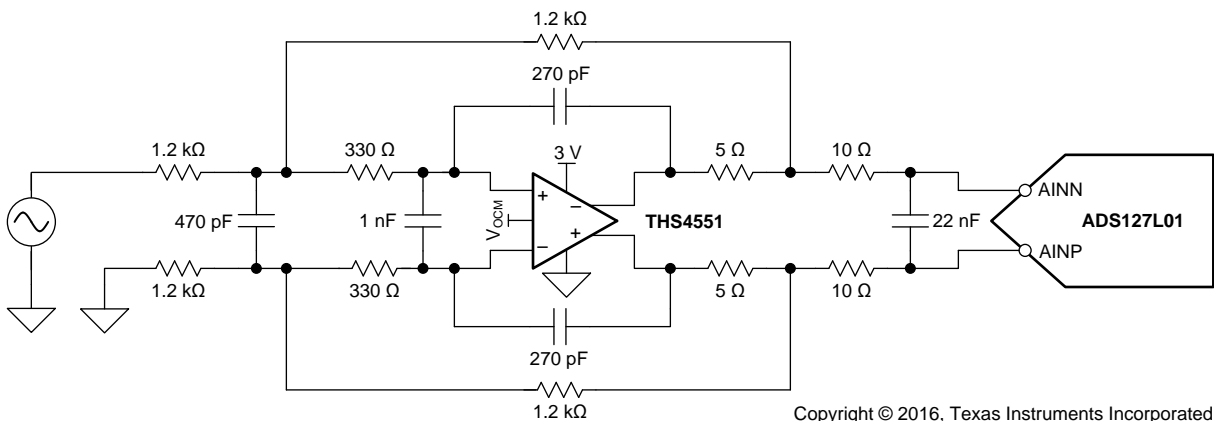
2.3.4 THS4551

The THS4551 fully differential amplifier offers an easy interface from single-ended sources to the differential output required by high-precision ADCs. Designed for exceptional DC accuracy, low noise, and robust capacitive load driving, this device is well suited for DAQ systems where high precision is required along with the best SNR and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.

The THS4551 features the negative rail input required when interfacing a DC-coupled, ground-centered, source signal to a single-supply differential input ADC. Very low DC error and drift terms support the emerging 16- to 20-bit SAR input requirements. A wide-range output common-mode control supports the ADC running from 1.8- to 5-V supplies with ADC common-mode input requirements from 0.7 V to greater than 3.0 V.

The THS4551 is commonly used in SAR ADC driver circuits. However, it is unclear where using a fully differential amplifier is beneficial over using two precision op amps and vice versa. This TI Design aims to clear up that uncertainty and distinguish benefits to using both configurations. To see a direct comparison of AFE performance between the OPA625 and the THS4551, see the [TIDA-01050](#) and [TIDA-01053](#) designs.

Figure 34 shows a block diagram of the THS4551:



Copyright © 2016, Texas Instruments Incorporated

Figure 34. THS4551 SAR ADC Driver Configuration

2.3.5 ADS8910B

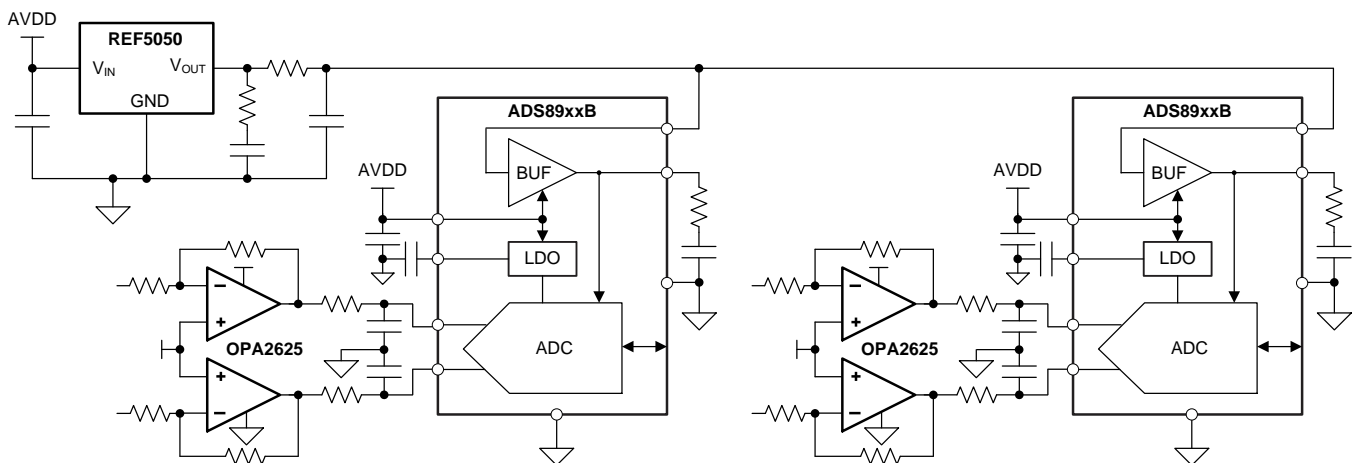
The ADS8910B, ADS8912B, and ADS8914B (ADS891xB) belong to a family of pin-to-pin compatible, high-speed, high-precision SAR ADCs with an integrated reference buffer and integrated low-dropout regulator (LDO). These devices support unipolar, fully differential, analog input signals with ± 0.5 -LSB INL and 102.5-dB SNR specifications under typical operating conditions.

The integrated LDO enables single-supply operation with low-power consumption. The integrated reference buffer supports burst-mode data acquisition with a 18-bit precision for the first sample. External reference voltages in the range of 2.5 to 5 V are supported, offering a wide selection of input ranges without additional input scaling.

The integrated multiSPI digital interface is backward compatible to the traditional SPI protocol. Additionally, configurable features simplify board layout, timing, and firmware, and support high throughput at lower clock speeds. The multiSPI digital interface allows for easy interface with a variety of microcontrollers, digital signal processors (DSPs), and FPGAs.

The ADS8910B has a high sample rate of 1 MSPS, meeting the specification of the system. It also features single-supply low-power operation. The key differentiation of the ADS8910B that makes it ideal for the multichannel simultaneous sampling Test and Measurement systems is its integrated reference buffer. In addition to the higher level of integration, which enables smaller board footprint, the devices also helps to eliminate the channel-to-channel variation caused by the external reference buffer variations. Another advantage of this SAR ADC is its zero latency, which makes it a perfect choice for higher sampling rate muxed applications.

☒ 35 shows a block diagram of the ADS8910B:



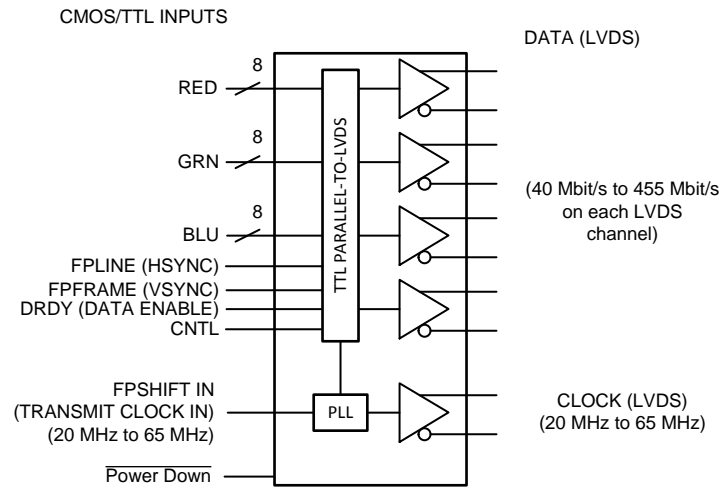
☒ 35. Multiple ADC Design

2.3.6 DS90C383B

The DS90C383B transmitter converts 28 bits of CMOS/TTL data into four LVDS data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. For every cycle of the transmit clock, 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65-MHz clock, the data throughput is 227 Mbps. The DS90C383B transmitter can be programmed for the rising or falling edge strobe through a dedicated pin.

This serializer is used to be able to take multiple data output lines from multiple ADCs and ship this data out faster, on fewer pins, to an FPGA. The DS90C383B does not require any special start-up sequence between clock, data, and power down pins.

☒ 36 shows a block diagram of the DS90C383B:



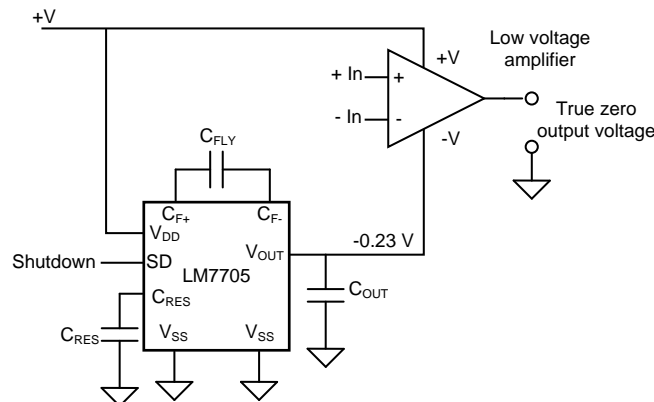
☒ 36. DS90C383B Block Diagram

2.3.7 LM7705

The LM7705 device is a switched capacitor voltage inverter with a low-noise, -0.23-V fixed negative voltage regulator. This device is designed to be used with low-voltage amplifiers to enable the amplifiers output to swing to 0 V . The -0.23 V is used to supply the negative supply pin of an amplifier while maintaining less than 5.5 V across the amplifier. Rail-to-rail output amplifiers cannot output 0 V when operating from a single-supply voltage and can result in error accumulation due to amplifier output saturation voltage being amplified by following gain stages. A small negative supply voltage prevents the amplifiers output from saturating at 0 V and helps maintain an accurate zero through a signal processing chain. Additionally, when an amplifier is used to drive an input of the ADC, the amplifier can output a 0-V signal and the full input range of an ADC can be used. The LM7705 device has a shutdown pin to minimize standby power consumption.

The LM7705 was selected based on its high efficiency, ease of implementation, and low quiescent current. The LM7705 is used in multiple reference designs where true rail-to-rail performance is required.

☒ 37 shows a block diagram of the LM7705:



Copyright © 2017, Texas Instruments Incorporated

☒ 37. LM7705 Typical Application

2.3.8 TPS7A47

The TPS7A47 is a family of positive voltage (36 V), ultra-low-noise ($4 \mu\text{V}_{\text{RMS}}$), LDOs capable of sourcing a 1-A load.

The TPS7A4700 output voltages are user-programmable (up to 20.5 V) using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count. The TPS7A4701 output voltage can be configured with a user-programmable PCB layout (up to 20.5 V) or adjustable (up to 34 V) with external feedback resistors.

The TPS7A47 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering op amps, ADCs, digital-to-analog converters (DACs), and other high-performance analog circuitry in critical applications such as medical, radio frequency (RF), and test and measurement.

In addition, the TPS7A47 is ideal for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversions, maximum system performance is ensured in sensitive instrumentation, test and measurement, audio, and RF applications.

The TPS7A47 is used to drop the output voltage of the switching regulators by half a volt while simultaneously filtering the voltage ripple for the analog supplies. This device was selected due to its adjustability and very low noise, which allowed for it to be used in multiple places in this TI Design.

2.3.9 LM3635M

The LM3635M is used in this TI Design to bring the 24-V input voltage down to 3.8 V, 5.5 V, and 18.5 V in a highly efficient manner. This part was selected based on its excellent EMI performance and compact PCB layout. The automotive-qualified Hotrod QFN package with wettable flanks reduces parasitic inductance and resistance while increasing efficiency, minimizing switch node ringing, and dramatically lowering EMI. Seamless transition between PWM and PFM modes and low-quiescent current (only 15 μA for the 3.3 V option) ensure high efficiency and superior transient responses at all loads.

2.3.10 LM46001

The LM46001 device is used to generate a -18.5-V rail in a highly efficient manner. This part was selected based on its excellent EMI performance and compact PCB layout. The LM46001 provides exceptional efficiency, output accuracy, and drop-out voltage in a very small solution size (see [Figure 38](#)).

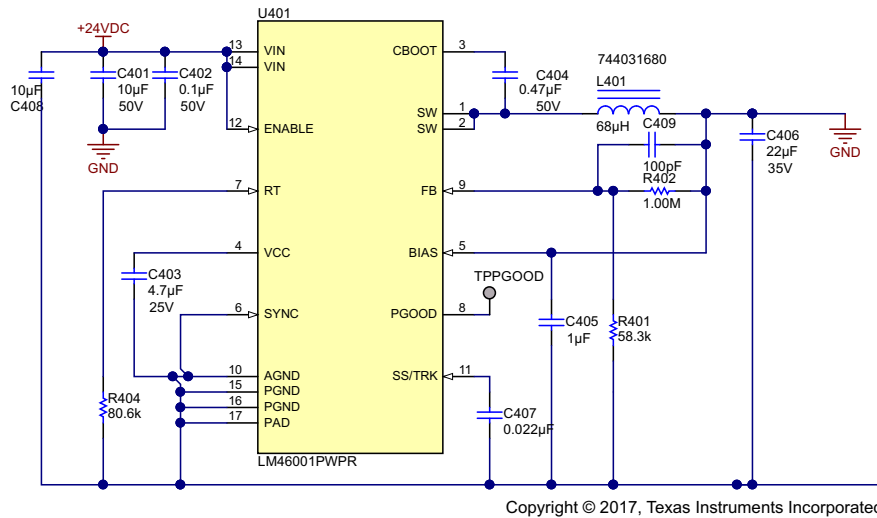


図 38. LM46001 Simplified Application Schematic

2.3.11 TPS7A3001

The TPS7A30 series of devices are negative, high-voltage (-35 V), ultra-low-noise ($15.1\ \mu\text{V}_{\text{RMS}}$, 72-dB PSRR) linear regulators that can source a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin and capacitor-programmable soft-start function that allows for customized power-management schemes. Other features include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A30 family is designed using bipolar technology, and is ideal for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This TI Design makes the device an excellent choice to power op amps, ADCs, DACs, and other high-performance analog circuitry.

In addition, the TPS7A30 family of linear regulators is suitable for post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, maximum system performance is provided in sensitive instrumentation, test and measurement, audio, and RF applications.

The TPS7A3001 is used to drop the -18.5-V rail down to the -18-V rail.

2.3.12 TPS82084

The TPS82084 device is a 2-A step-down converter MicroSIP module optimized for small solution size and high efficiency. The power module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area. The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

This device is used to drop the 3.8-V rail down to 1.2 V in a highly efficient manner. The 1.2-V rail is used for a digital supply on the FPGA.

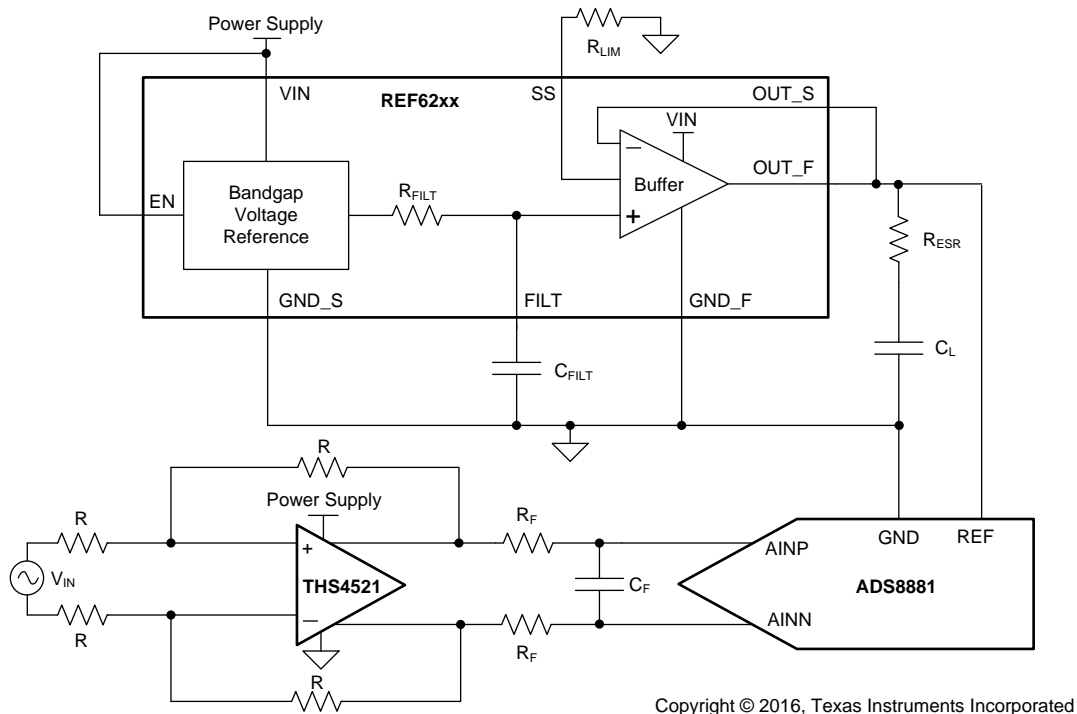
2.3.13 REF6041

The REF6000 family of voltage references have an integrated low-output impedance buffer that enable the user to directly drive the REF pin of precision data converters, while preserving linearity, distortion, and noise performance. Most precision SAR and delta-sigma ADCs switch binary-weighted capacitors onto the REF pin during the conversion process. In order to support this dynamic load, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF6000 family devices are well suited, but not limited, to drive the REF pin of the ADS88xx family of SAR ADCs, and ADS127xx family of delta-sigma ADCs, as well as other DACs.

The REF6000 family of voltage references is able to maintain an output voltage within 1 LSB (18-bit) with minimal droop, even during the first conversion while driving the REF pin of the ADS8910B. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems. The REF60xx variants of REF6000 family specify a maximum temperature drift of just 5 ppm/°C and initial accuracy of 0.05% for both the voltage reference and the low output impedance buffer combined.

A 4.096-V reference voltage is required to meet the LSB specifications of this design. The REF6041 also contains an internal buffer enabling multiple ADCs to be driven in parallel.

Figure 39 shows a block diagram of the REF6041:



Copyright © 2016, Texas Instruments Incorporated

Figure 39. REF6041 Typical Application Circuit

2.3.14 OPA376

The OPA376 family represents a new generation of low-noise operational amplifiers with eTrim™, offering outstanding DC precision and AC performance. RRIO, low offset (25 μV, maximum), low noise (7.5 nV/√Hz), a quiescent current of 950 μA (maximum), and a 5.5-MHz bandwidth make this part very attractive for a variety of precision and portable applications. In addition, this device has a reasonably wide supply range with excellent PSRR, making it attractive for applications that run directly from batteries without regulation. In addition to that this part is unity gain stable and capable of driving high capacitive loads, which makes it an excellent choice for buffering the output common-mode voltages for THS4551 and OPA625.

2.3.15 SN74AHC1G04

The TPS709xx series of linear regulators are ultra-low, quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 μA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety.

These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA, typical.

The TPS70918 is used to generate a 1.8-V digital supply. Although not used in this TI Design, it allows for additional modularity with the FPGA inputs.

See [図 40](#) for a simplified schematic of the SN74AHC1G04:



図 40. SN74AHC1G04 Simplified Schematic

2.3.16 SN74AUP1G80

The SN74AUP1G80 is a single positive-edge-triggered D-type flip-flop. When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire VCC range of 0.8 to 3.6 V, resulting in increased battery life. This product also maintains excellent signal integrity.

The SN74AUP1G80 is used in coalition with the SN74AHC1G04 inverter to synchronize the conversion start signal with the SCLK signal at the ADC.

2.3.17 CD4081B

The CD4073B, CD4081B and CD4082B AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of CMOS gates.

This AND gate is used to and the two RVS signals coming from the two ADCs so that data would be read when both ADCs are ready to be read from. [図 41](#) shows a functional diagram of the CD4081B:

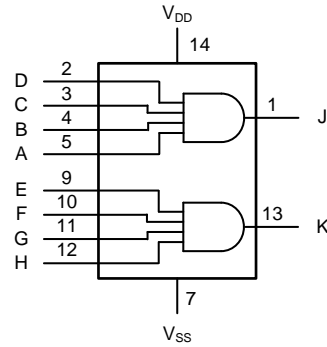


図 41. CD4081B Functional Diagram

2.3.18 LMK61E2

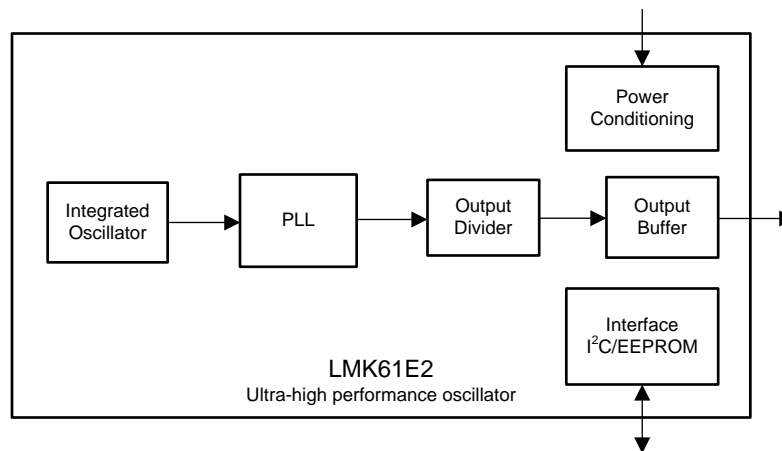
The LMK61E2 is an ultra-low jitter PLLatinum programmable oscillator with a fractional-N frequency synthesizer with integrated VCO that generates commonly used reference clocks. The outputs can be configured as LVPECL, LVDS, or HCSL.

The device features self-startup from on-chip EEPROM that is factory programmed to generate a 156.25-MHz LVPECL output. The device registers and EEPROM settings are fully programmable in-system through a I²C serial interface. Internal power conditioning provide excellent PSRR, reducing the cost and complexity of the power delivery network. The device operates from a single 3.3-V \pm 5% supply.

The device provides fine and coarse frequency margining options through the I²C serial interface to support system DVT, such as standard compliance and system timing margin testing.

This clock generator is used as the main system clock generator. It was selected based on its adjustability, very low jitter, low power, and robust supply noise immunity.

☒ 42 shows a simplified block diagram of the LMK61E2:



Copyright © 2016, Texas Instruments Incorporated

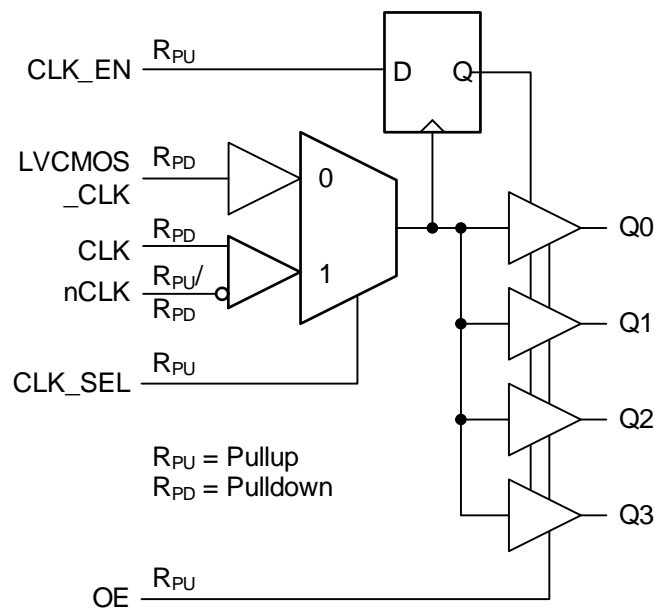
☒ 42. LMK61E2 Simplified Block Diagram

2.3.19 LMK00804B

The LMK00804B is a low-skew, high-performance clock fanout buffer that can distribute up to four LVCMOS or LVTTTL outputs (3.3-V, 2.5-V, 1.8-V, or 1.5-V levels) from one of two selectable inputs, which can accept differential or single-ended inputs. The clock enable input is synchronized internally to eliminate runt or glitch pulses on the outputs when the clock enable terminal is asserted or de-asserted. The outputs are held in logic low state when the clock is disabled. A separate output enable terminal controls whether the outputs are active state or high-impedance state. The low additive jitter and phase noise floor, and guaranteed output and part-to-part skew characteristics make the LMK00804B ideal for applications demanding high performance and repeatability.

The output of the LMK61E2 is a differential LVDS signal. However, all of the components requiring clocking accept a single ended LVCMOS clock input. The LMK00804B takes the LVDS signal from the LMK61E2 and splits it into four synchronized LVCMOS outputs. This allowed for the same buffered clock signal to be present at each clocked device. The LMK00408B was selected as it contains the correct number of outputs in the correct format, has very low additive jitter, and is easy to implement.

See [Figure 43](#) for a simplified schematic of the LMK00804B:



Copyright © 2017, Texas Instruments Incorporated

Figure 43. LMK00804B Simplified Schematic

3 Getting Started Hardware and Software

The following subsections outline how to get the board up and running as fast as possible. Take care when moving jumper pins to avoid possible damage to the components.

3.1 Jumper Configuration

This system has a large amount of configurable options. These options are selectable through the use of three pin jumpers. 表 4 highlights the purpose of each jumper as well as the default configurations.

表 4. Jumper Configuration

JUMPER NAME	SHORT PINS 1 AND 2	SHORT PINS 2 AND 3	DEFAULT CONFIGURATION
J29	Serial data from single-ended ADC to PHI connector	Serial data from differential ADC to PHI connector	Short Pins 2 and 3
J30	Serial data from single-ended ADC to PHI connector	Serial data from differential ADC to PHI connector	Short Pins 2 and 3
J31	Serial data from single-ended ADC to PHI connector	Serial data from differential ADC to PHI connector	Short Pins 2 and 3
J32	Serial data from single-ended ADC to PHI connector	Serial data from differential ADC to PHI connector	Short Pins 2 and 3
J33	RVS from single-ended ADC to PHI connector	RVS from differential ADC to PHI connector	Short Pins 2 and 3
J34	SCLK from PHI connector to FPGA	SCLK from PHI connector to ADC	Short Pins 2 and 3
J22	SCLK from PHI connector into differential ADC	SCLK from FPGA into differential ADC	Short Pins 1 and 2
J23	Chip select signal from PHI connector to differential ADC	Chip select signal from FPGA into differential ADC	Short Pins 1 and 2
J24	RVS from differential ADC going to FPGA	RVS from differential ADC going to PHI connector	Short Pins 2 and 3
J25	Chip select signal from PHI connector to single-ended ADC	Chip select signal from FPGA into single-ended ADC	Short Pins 1 and 2
J26	SDI from PHI connector into single-ended ADC	SDO0 from differential ADC into single-ended ADC SDI	Short Pins 1 and 2
J27	SCLK from PHI connector into single-ended ADC	SCLK from FPGA into single-ended ADC	Short Pins 1 and 2
J28	RVS from single-ended ADC going to FPGA	RVS from single-ended ADC going to PHI connector	Short Pins 2 and 3
J10	Mode Switch 0 Low	Mode Switch 0 High	Short Pins 2 and 3
J11	Mode Switch 1 Low	Mode Switch 1 High	Short Pins 2 and 3
J35	Mode Switch 2 Low	Mode Switch 2 High	Short Pins 2 and 3
J36	Mode Switch 3 Low	Mode Switch 3 High	Short Pins 2 and 3

3.2 PHI Hardware

Before using the PHI connector, short jumpers J5 and J6 and attach the PHI board to the onboard connector. The PHI EEPROM must be initialized first before the board can be used. To do this, launch the PHI Software Launcher software and select EEPROM Loader. Next, select the ADS8910B from the list of devices and click Load. Once the proper device is selected, click Write and Verify. The EEPROM will now be loaded and initialized for use.

3.3 Measuring SNR, THD, SFDR, SINAD, and ENOB

The TIDA-01051 hardware testing requires a high-quality signal generator with a differential output because the generator's performance can limit measurement results. The Audio Precision AP-2700 series was used to generate the inputs necessary for system characterization and its characteristics are given in [表 5](#).

表 5. External Source Requirements

SPECIFICATION DESCRIPTION	SPECIFICATION VALUE
External source type	Balanced differential
External source impedance (RS)	10 to 30 Ω
Maximum noise	10 μV_{RMS}
Maximum SNR	110 dB
Maximum THD	-130 dB

Using SMA cables, attach the signal from the signal generator to either the single-ended or fully differential front-end. Next, attach the PHI module to the respective connector. Set the signal generator to a 2-kHz differential output at the amplitude of choice. Remove the corresponding shorting links from the input of the system.

Install and run the ADS8910B EVM software, click on *Spectral Analysis* and set the SCLK frequency and sampling rate to the desired amounts. Once the software is configured, click *Capture*. The software will take the corresponding number of samples and calculate the SNR, THD, SFDR, SINAD, and THD.

3.4 Using Onboard Clocking and Jitter Cleaner

To program the LMK61E2, use the USB2ANY controller from Texas Instruments. Connect the SCL signal to pin 3 of J3 and connect the SDA signal to pin 2 of J3. Pin 1 of J3 will be connected to ground. Once the device is connected to the USB2ANY controller, install and run [Codeloader](#). Once installed, click on *Select Device* and select the LMK61E2 under *Clock Conditioners*. Next, click on *Find I2C Address* to locate the I²C address of the onboard LMK61E2. Once the address has been located, select the desired clocking frequency and select LVDS as the output format. Click *Generate Configuration* and then *Program EEPROM* to set the device.

Now that the LMK61E2 is generating the clock, change the setting on jumpers J32 and J33 to activate the jitter cleaner and conversion start synchronization circuitry. Next, go back to the ADS8910B EVM software, select multiSPI under *SDO Mode* and select INTCLK under *Clock Source*. Make sure to set the SCLK frequency to the same frequency as the LMK61E2 frequency to receive proper measurements.

Once the hardware and software have been configured to accept the onboard clock, capture data using the ADS8910B EVM software and observe the results.

4 Testing and Results

To test the performance of this AFE and ADC, an Audio Precision 2700 series signal generator was used for the signal source. The AP2700 has adequate noise and THD specifications and the system would not be limited by its performance. It is crucial to use a quality source as the systems performance will be limited if the signal source specifications are too low. A generic DC power supply was used to generate the 24-V DC input voltage.

Once the board was powered up and the signal was connected through an SMA cable, the shorting links on the input jumpers could be removed. Next, the PHI module is attached and the software is enabled on the host PC. Within the software, the ADC can be configured to the desired settings and tests can be run. Measuring SNR, THD, and ENOB can be performed when running a spectral analysis from the ADS8910B EVM GUI.

To use the serializer and FPGA make sure the jumpers are configured correctly as described in 表 4. Next, connect the Xilinx JTAG connector to load the code onto the FPGA. Using Xilinx IMPACT programmer, select the bit file containing the FPGA code. Once the FPGA is connected, program the FPGA and flash to load the code. The FPGA is now ready to use.

The AP2700 was set to output a 2-kHz, 24-Vpk-pk sinusoid; this was chosen as 2 kHz is the standard frequency used when measuring noise and THD. A 24-Vpk-pk signal was used as it would grant full range on the THS4551 or OPA625 amplifier and would thus grant full range at the ADC from 0 to V_{REF} .



図 44. THS4551 Data Before Serialization



図 45. THS4551 Data After Serialization



図 46. OPA625 Data Before Serialization

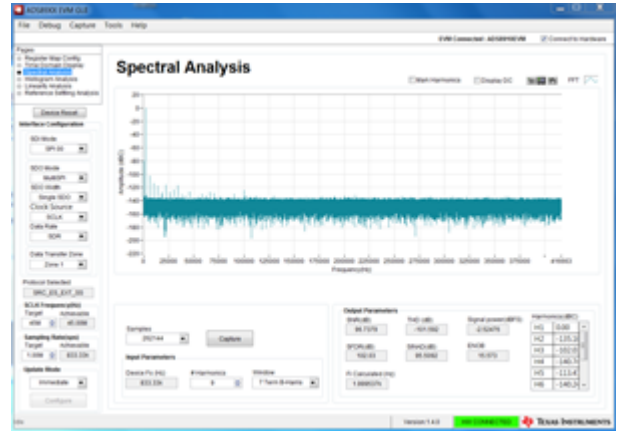


図 47. OPA625 Data After Serialization

表 6 shows that there is no performance degradation when serializing and de-serializing data. The performance metrics for both acquisition methods highlight roughly the same results.

表 6. Results

SPECIFICATION	SERIALIZED DATA (OPA625)	NON-SERIALIZED DATA (OPA625)	SERIALIZED DATA (THS4551)	NON-SERIALIZED DATA (THS4551)
THD (dB)	-101.55	-101.59	-124.42	-124.10
SNR (dB)	96.69	96.74	98.27	98.12
ENOB	15.56	15.58	16.03	16.01
SFDR (dB)	102.03	102.03	129.70	130.14
SINAD (dB)	95.46	95.51	98.26	98.11

図 48 highlights the delay seen when serializing the data. The delay is about 100 ns.

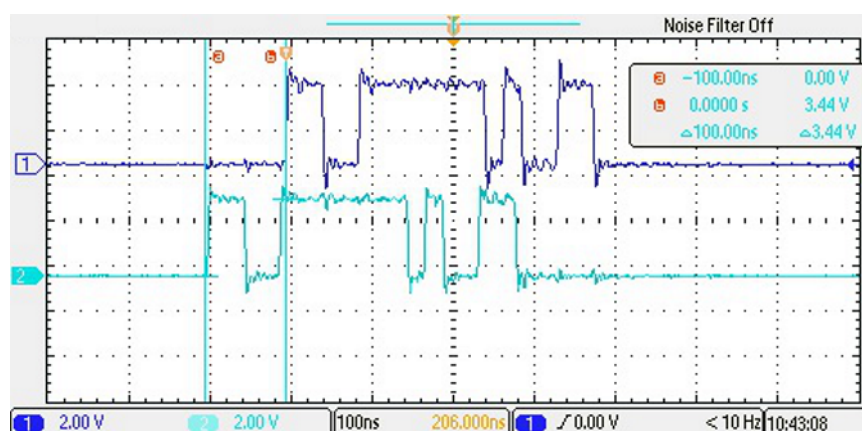


図 48. Data Delay With Serialization

5 Design Files

5.1 Schematics

To download the schematics, see the design files at [TIDA-01051](#).

5.2 Bill of Materials

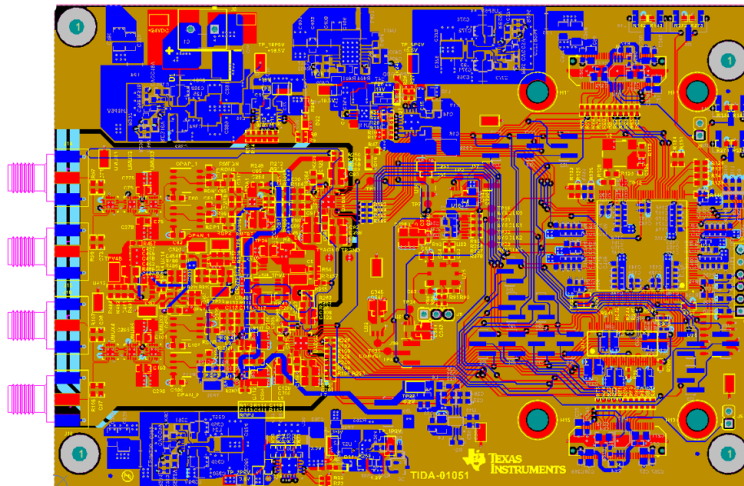
To download the bill of materials (BOM), see the design files at [TIDA-01051](#).

5.3 PCB Layout Recommendations

Due to the complexity of this TI Design, many design considerations need to be taken when developing the PCB layout.

This design features a split ground plane. The ground plane is split between an analog ground and a digital ground. The two grounds meet underneath the ADCs to connect the two planes. The digital ground includes all of the power switching regulators, all the digital signals from the ADC, the FPGA, and the PHI connectors. The analog ground covers all of the analog circuitry prior to the ADC. It is important to keep the differential input signal traces the same length in order to negate any potential propagation loss on these lines.

☒ 49 highlights the layout for the TIDA-01051 design. The brownish colored layer is the ground plane. The ground plane is split between the analog and digital sections. The split is highlighted by the black line starting at the edges of the SMA connectors and going around the ADCs. It is also evident that the signal path of the differential inputs is the same length.



☒ 49. Layout Preview

5.3.1 Power Layout Design

When designing the layout for the power section of this TI Design, device datasheets were carefully analyzed for layout guidelines. [Fig 50](#) highlights the PCB layout for the power components. The switching regulators are placed on the outside edge of the board as far away as possible from the sensitive analog signals. The LDOs are then placed below the switching regulators to keep the power traces as short as possible to the isolated analog section. The input and output capacitors for each device are placed as close as possible to the input and output pins. Each capacitor's ground is also placed on the same ground as the respective device. This same design process was taken for all of the different power rails. [Fig 50](#) shows the 18-V, 5-V, and -18-V rails on the top half of the image. The bottom half contains the 3.3-V, 1.2-V, and -0.2-V rails.

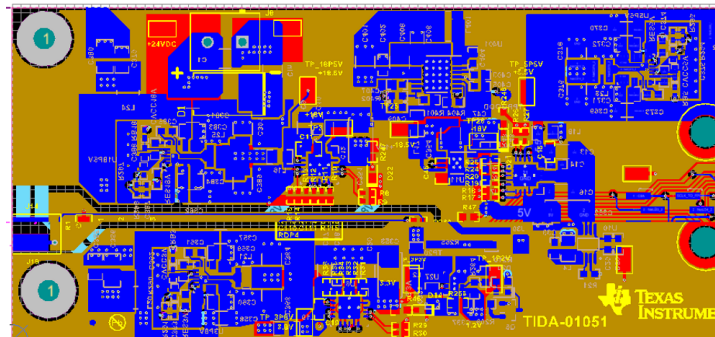


図 50. Power PCB Layout

For more PCB layout guidelines on power, see the respective device datasheets.

5.3.2 AFE Layout Design

When designing the PCB layout for the AFE, the main goal is to keep the signal path as short and symmetric as possible (see [Fig 51](#)). The MUX36D04, OPA827, OPA625, THS4551, and all surrounding passive components were placed and routed with the signal path length being the main design concern. Input and output capacitors were placed as close as possible to the devices' power and output pins as possible. See the respective device datasheets for more layout guidelines.

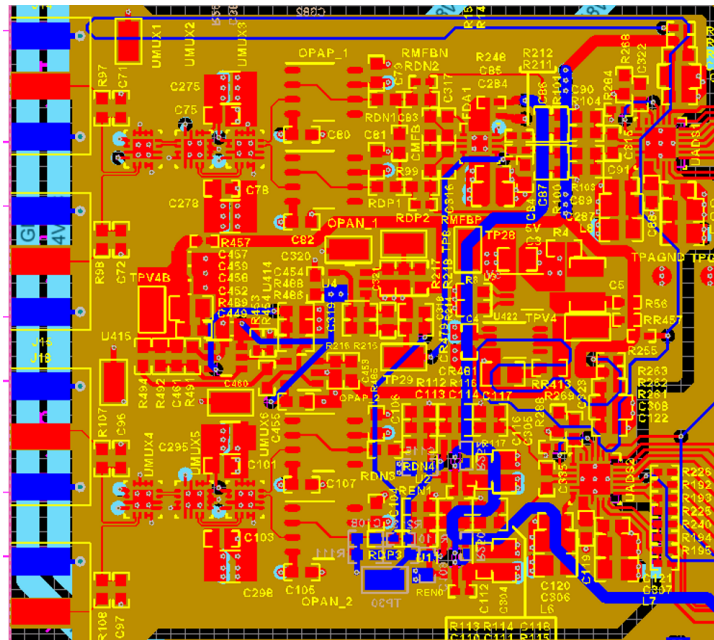


図 51. AFE Layout

5.3.3 PHI Connector, FPGA, and Clocking Layout Design

Past the ADC, all of the signals are digital and trace length is no longer much of a concern. Again, input and output capacitors are placed as close as possible to the respective devices (see [Figure 52](#)). Clocking is centrally placed in between the two PHI connectors on the digital ground. The FPGA is placed in the middle of the board on the top layer. To simplify routing, the decoupling capacitors are placed on the bottom layer. This allowed for easy routing to each individual IO pin. For more layout guidelines, see the respective device datasheets.

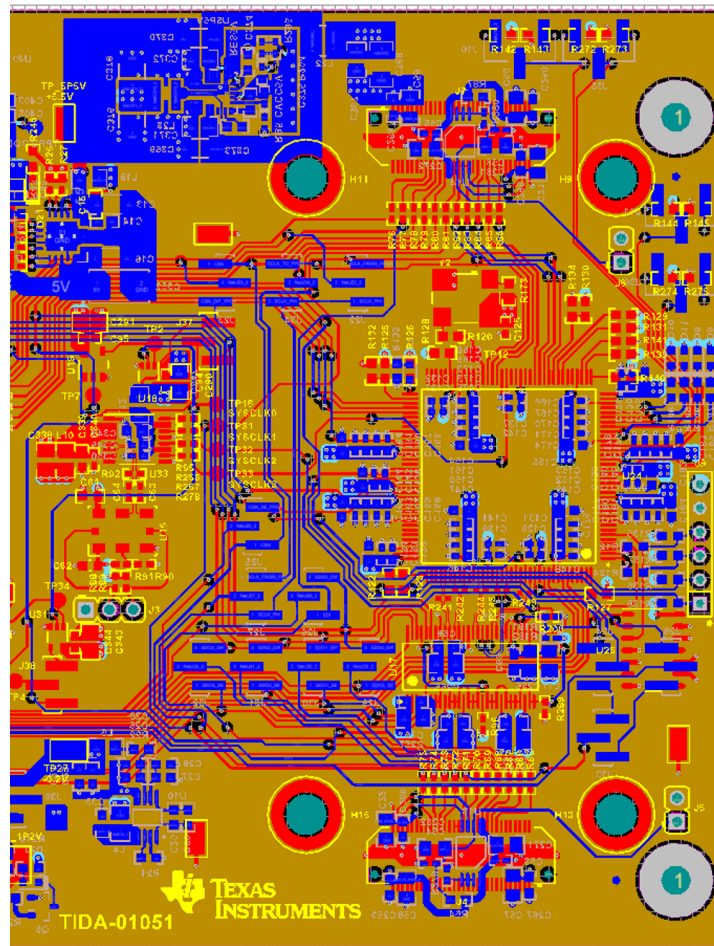


図 52. PHI Connector, FPGA, and Clocking Layout

5.3.4 Layout Prints

To download the layer plots, see the design files at [TIDA-01051](#).

5.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01051](#).

5.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01051](#).

5.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01051](#).

6 Software Files

To download the software files, see the design files at [TIDA-01051](#).

7 Related Documentation

1. Texas Instruments, [Optimized Analog Front-End DAQ System Reference Design for 18-Bit SAR Data Converters](#), TIDA-01050 Design Guide (TIDUCF5)

7.1 商標

TINA-TI, PLLatinum, multiSPI, eTrim are trademarks of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

Xilinx is a trademark of Xilinx.

Spartan, ISE are registered trademarks of Xilinx.

すべての商標および登録商標はそれぞれの所有者に帰属します。

8 About the Authors

ERIC BELJAARS is a systems architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Eric earned his bachelor of science in electrical engineering (BSEE) from the University of Oklahoma in Norman, OK.

TARAS DUDAR is a systems design engineer and architect at Texas Instruments, where he is responsible for developing reference design solutions for the test and measurement industry. Previously, Taras designed high-speed analog SOC integrated circuits for Gbps data communications. Taras has earned his master of science in electrical engineering (MSEE) degree from the Oregon State University in Corvallis, OR.

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的で、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジーまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的にかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示的保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁済または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際の、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(<http://www.ti.com/sc/docs/stdterms.htm>)、評価モジュール、およびサンプル(<http://www.ti.com/sc/docs/sampterm.htm>)についてのTIの標準条項が含まれますが、これらに限られません。