参考資料

TI Designs

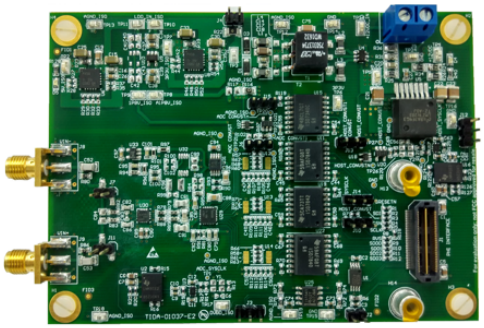
アイソレータの最適化によってSNRとサンプル・レートを最大化する、20ビット、1MSPSのデータ収集リファレンス・デザイン

概要

TIDA-01037は20ビット、1MSPSの絶縁アナログ入力データ収集(DQA)リファレンス・デザインで、2つの異なるアイソレータ・デバイスを使用して、信号チェーンのSNRとサンプル・レート性能を最大化しています。ADCサンプリング・クロックなど低ジッタを必要とする信号向けには、TIのISO73xxファミリの低ジッタ・デバイスが使用されます。一方、データのサンプル・レートを最大化するにはTIの高速ISO78xxファミリのデバイスが使用されます。これら2つのアイソレータ・ソリューションを組み合わせると、絶縁境界をまたぐサンプル・クロック・ジッタが最小化されるため、高周波数での性能が大幅に向上し、アイソレータの信号レートの最大化によりデータ・スループットが増大します。TIの高度なADC multiSPI™およびソース同期機能を使用することで、さらに性能を向上できます。最後に、すべての主要な設計理論が説明され、4.2に示すような測定結果が得られています。

リソース

TIDA-01037	デザイン・フォルダ
ADS8900B、REF5050、THS4551	プロダクト・フォルダ
ISO7840、ISO7842、ISO1541、ISO7340	プロダクト・フォルダ
SN6501、LMZ14203、TPS7A4700	プロダクト・フォルダ
TPS70918、OPA376、LMK61E2	プロダクト・フォルダ
SN65LVDS4RSET、SN74AUP1G80	プロダクト・フォルダ
SN74AHC1G04	プロダクト・フォルダ
ADS8900B EVM-PDK	関連デザイン



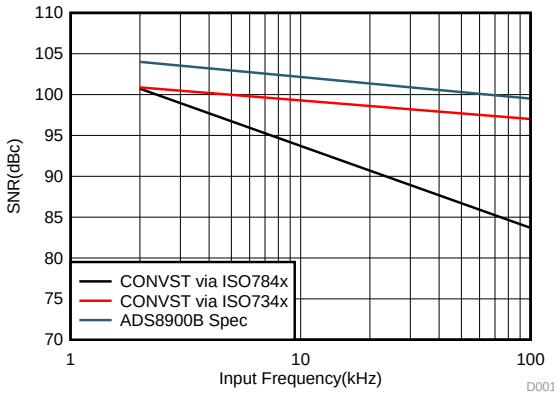
特長

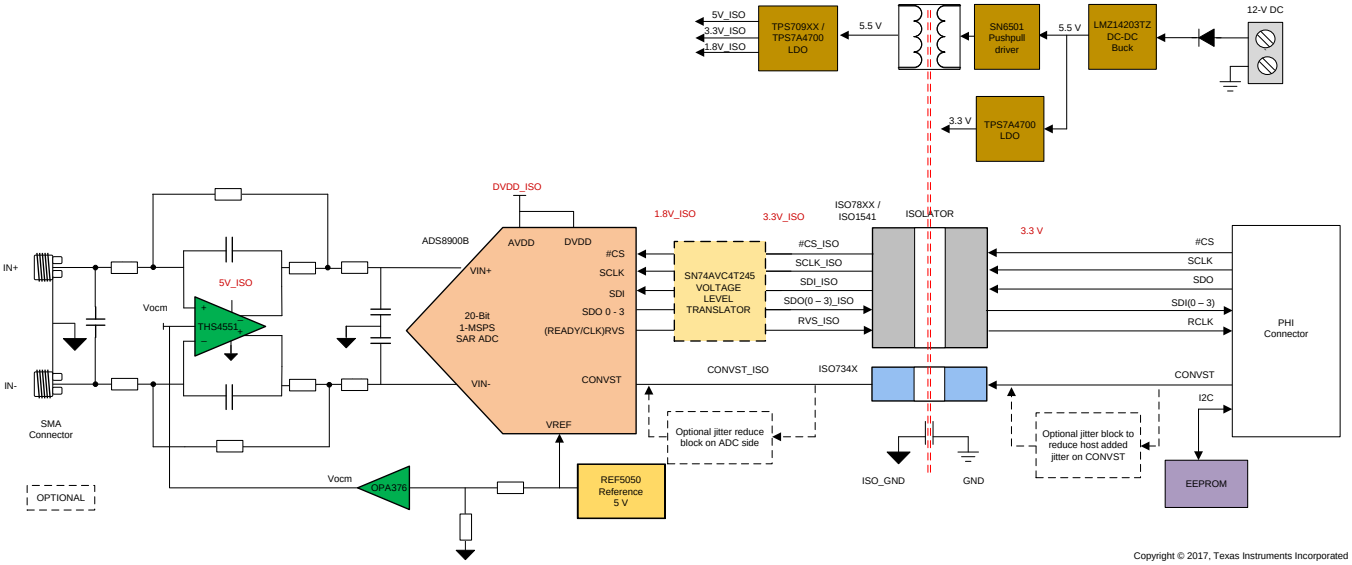
- 差動入力、絶縁、20ビット、1MSPSのDAQのリファレンス・デザイン
- 最高100kHzの入力信号に最適化されたアイソレータ・ソリューション
- 追加のジッタ低減回路が不要
- TIの革新的なmultiSPI™およびソース同期モードADCデジタル・インターフェイスによる低SPIクロック・レートのデモンストレーション
- サンプル・クロック・ジッタにより、システムのSNR性能を評価可能
- 理論、計算、コンポーネントの選択、PCBの設計、測定結果を記載

アプリケーション

- データ収集(DAQ)
- 実験室用計測機器および現場用計測機器
- デザインの検証と確認
- リモート・プロセスの監視および制御

TI E2E™ Community　E2Eエキスパートに質問





1 System Overview

Data acquisition (DAQ) systems are found in numerous applications from simple temperature monitoring to high-end process and control. DAQs are primarily used to measure real-world analog electrical or physical properties (voltage, current, temperature, pressure, vibration, and so on), apply the appropriate signal conditioning (amplification and filtering), and digitize the signal so it can be further processed by the host processor or computer. The electronics that support and interface with the physical transducer, amplifier, and analog-to-digital converter (ADC) are often referred to as the analog input DAQ module and are the focus of this reference design. 図 1 illustrates an analog input module and how the DAQ is integrated within the system. Find more details in Section 2 of the TIDA-00732 design guide.

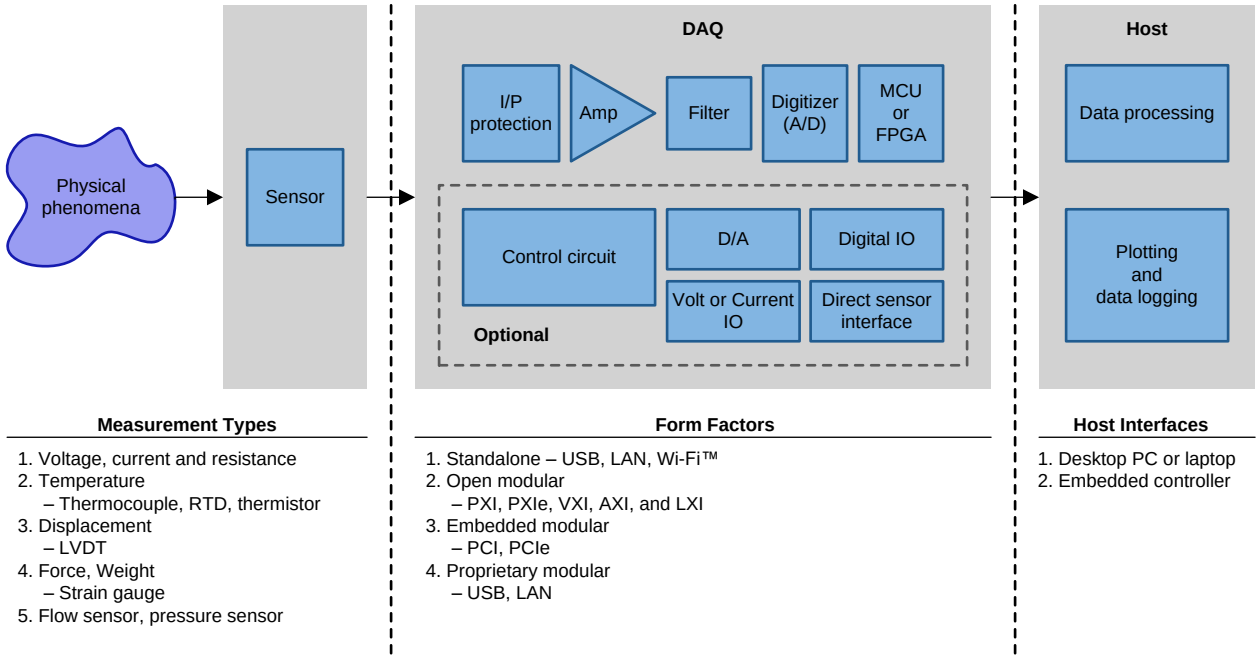


図 1. Generic DAQ System Block Diagram

The environmental and performance requirements of many DAQ end equipment applications require galvanic isolation in order to break ground loops and improve measurement accuracy. Harsh environments often require the transducer to be electrically isolated from the system controller to enable measurements at higher voltages while preventing the threat of electrical shock. Furthermore, the electrical isolation can also improve noise immunity, especially between input channels, enhancing the signal-to-noise ratio (SNR) of the data channel.

Depending on the system requirements, isolation can be achieved through the analog domain (before ADC) or digital domain (after ADC). Signal chain metrics, such as dynamic range, system bandwidth (BW), SNR, and power all play a role in determining which is the best solution; however, due to ADC dynamic range constraints, cost, and complexity, digital isolation is often the preferred solution. Because each digital line requires isolation, minimizing the number of digital lines with serial peripheral interface (SPI) communication while maximizing the data rate is a system design challenge presented by digitalized isolated input DAQs. Furthermore, the isolation boundary presents non-ideal signal transfer, limiting data rate due to propagation delay and adding nondeterministic signal jitter making system timing challenging.

In this comprehensive reference design, the designer is shown how to mitigate the challenges presented by the isolated propagation delay and jitter while optimizing signal chain SNR performance.

1.1 System Description

This design guide focuses on maximizing the signal integrity characteristics of an isolated analog input module as illustrated in 図 2, which outlines the input protection, analog front end (AFE), digital isolation, isolated power, non-isolated power, and host processor functions of the DAQ. The input signal from the measuring sensor is received by the DAQ input connector. Many systems will require input protection, which must be selected to provide the necessary protection without impacting signal integrity. Due to the normally small signal being detected and the associated noisy environment, the AFE consists of a scaling or programmable gain amplifier (PGA) followed by an anti-aliasing, noise limiting, low pass filter (LPF),

which is paired with the appropriate ADC driver prior to digitization. The ADC converts the time varying analog input to either a serial or parallel binary bit stream, which is then passed across the digital isolation barrier to the embedded host controller (MCU or FPGA). Depending on the application, the ADC may contain the necessary reference and/or the associated buffer integrated as part of the ADC. Furthermore, portions or the entire AFE may also be integrated as a single device for specific applications, but this can also limit flexibility.

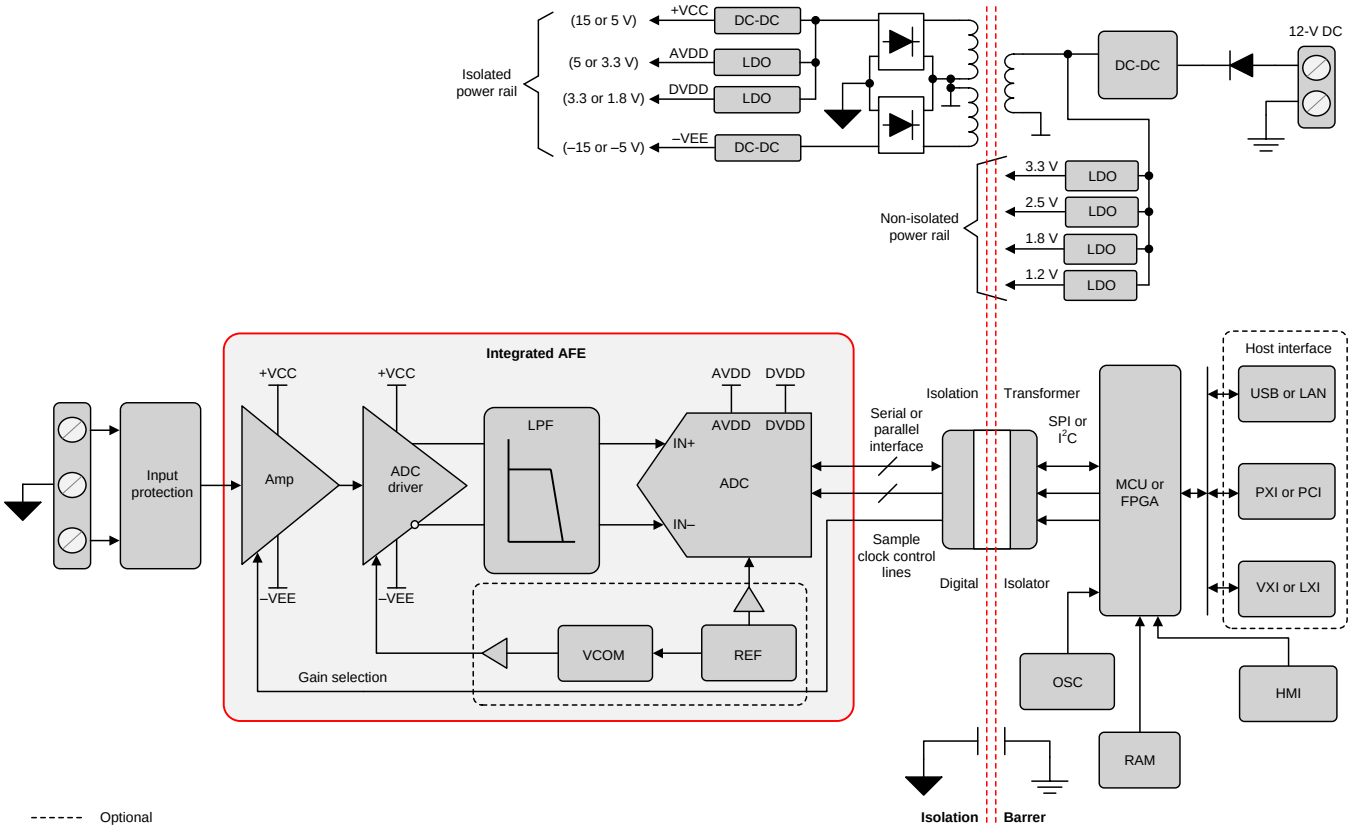


図 2. Isolated Analog Input DAQ Reference Diagram

In this example, the host or embedded controller interfaces with the ADC through a serial interface (for example, SPI or I^2C) in order to minimize the total number of required isolated channels. The controller will also support one or more interfaces to a central controller with either PXI, PCI, LXI, VXI, or USB protocols. A human machine interface (HMI) with an embedded GUI can also be included for local monitoring, data logging, and accessing. A local oscillator or clock and well as memory will normally be required.

Finally, isolated and non-isolated power DC-DC and LDO solutions are required to power the electronics on both sides of the isolation barrier. Normally, for sensitive analog inputs, both DC-DC and LDO solutions are required in order to maximize system power efficiency and noise immunity.

The following sections detail the timing challenges presented by the isolation barrier in terms of its effect on the ADC's data rate and SNR performance, and the challenges of synchronizing the sample clock with the host clock. When these performance limiting characteristics are understood, solutions using key features of TI's high performance AFE solutions for amplifiers, ADCs, and isolation devices are highlighted along with TI's power solutions for both isolated and non-isolated supplies. Furthermore, a novel design for synchronizing the ADC's sample clock with the host clock is also demonstrated.

For more background information on DAQ challenges and solutions, see the TIDA-00732 and TIDA-00164 designs.

1.2 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Number of channels	Single
Input type	Differential
Input range	±5 V fully differential
Input impedance	1 kΩ
Resolution	20 bit
SNR[1]	97 dB at 100-kHz signal input
	101 dB at 2-kHz signal input
THD[1]	–113 dB at 100-kHz signal input
	–127 dB at 2-kHz signal input
ENOB[1]	15.86 bits at 100-kHz signal input
	16.46 bits at 2-kHz signal input
Power supply isolation	250-V DC (continuous) basic insulation
	5000-V AC for 1 minute (withstand)
Digital channel isolation	5.7-kV_{RMS} isolation for 1 minute per UL 1577
Operating temperature	0°C to 60°C
Storage temperature	–40°C to 85°C
Connectors	60-pin Samtec high density connector for precision host interface (PHI) module interface
Power	12-V DC, 200 mA
Form factor (L × W)	110 mm × 80 mm

(1) See 表 21 for more details.

1.3 Block Diagram

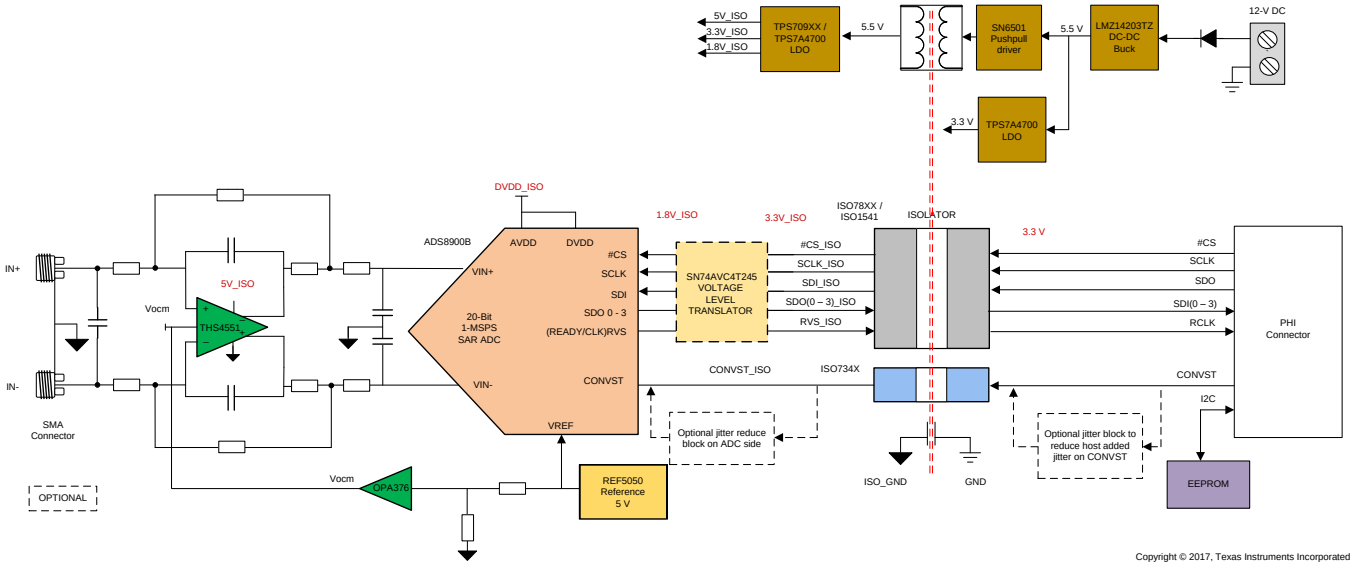


図 3. TIDA-01037 System Block Diagram

1.4 Highlighted Products

The system contains the following highlighted parts, which determine the overall system performance. These parts are grouped into these sub-blocks:

- Analog signal chain
- Clock
- Power

1.4.1 Analog Signal Chain

- *THS4551*: The THS4551 fully differential amplifier offers an easy interface, high precision, and a high-speed differential ADC. Very low DC error and drift support emerging 16- to 20-bit SAR ADC input requirement. With the exceptional DC accuracy, low noise, and robust capacitive load driving, this device is well suited for DAQ systems where high precision is required along with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.
- *ADS8900B*: The module has a single-channel differential analog input and uses the ADS8900B, 20-bit, 1-MSPS SAR ADC with an integrated reference buffer.
- *REF5050*: The onboard reference REF5050 (ultra-low noise, low drift, and high precision) followed by low noise, low temperature drift, and low output impedance buffer provides a 5-V reference to the ADC core.
- *ISO784x*, *ISO734x*, and *ISO1541*: The digital isolation for the host SPI and control signal is achieved using the ISO7840 and ISO7842 digital isolators. Sample clock isolation done with ISO7340 for low jitter requirement. The host controller communicates with the LMK61E2-SIAR (ultra-low programmable clock oscillator) through the ISO1541, which isolates the I^2C bus.

1.4.2 Clock

The LMK61E2 programmable oscillator has the following features:

- Ultra-low noise, high performance (90 fs RMS jitter at > 100 MHz)
- Frequency tolerance ±50 ppm
- Frequency output 10 MHz to 1 GHz
- I^2C interface

1.4.3 Power

図 4 illustrates the power supply tree of the TIDA-01037. The TIDA-01037 needs 12-V DC of power to generate the 5.5-V, 3.3-V non-isolated power rail and the 5.2-V, 3.3-V, and 1.8-V isolated power rail.

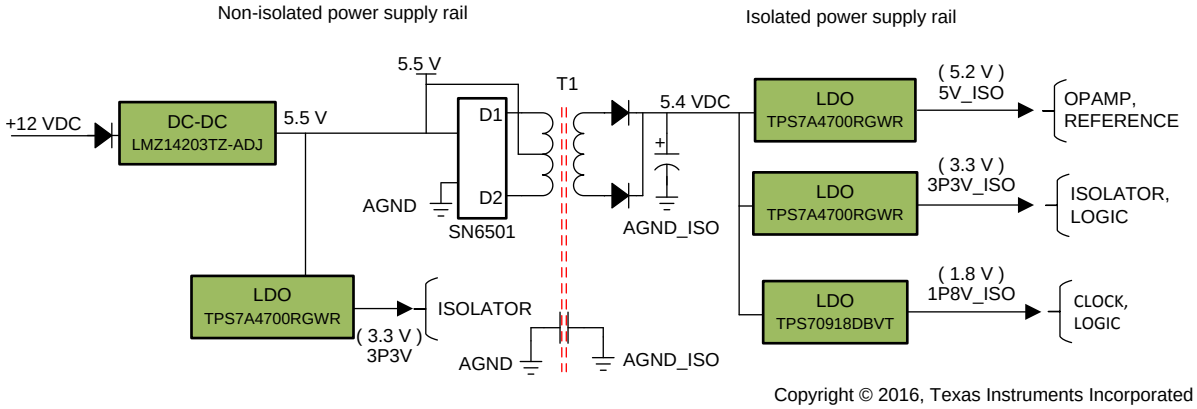


図 4. TIDA-01037 Power Supply Block

- *SN6501*: The isolated power supply power is generated using the SN6501, low-noise, low-EMI push-pull transformer driver.
- *DC-DC and LDO*: The power supply rail for both the isolated and non-isolated sections is generated by the DC-DC convertor and LDO, which are shown in 表 2.

表 2. Power Supply Rail

SERIAL NO	TYPE	PART NO	SUPPLY RAIL
1	DC-DC	LMZ14203	5.5 V
2	LDO	TPSA4700RGWR	5.2 V, 3.3 V
3	LDO	TPS70918DBVT	1.8 V

2 System Design Theory

Galvanic isolation is commonly used by DAQ systems in order to breaks ground loops and thereby improves measurement accuracy and safety. Isolation may be achieved within the analog domain prior to the ADC or in the digital domain after the ADC. Prior to this publication, digital isolation was the preferred embodied solution for systems requiring medium performance (resolution < 16 bits, sampling rates < 1 MSPS, and BW < 100 kHz). However, for higher resolution, higher speed solutions (> 18 bits, > 1 MSPS, and > 100 kHz), digital isolators will limit signal chain performance, dramatically reducing the DAQ's effective number of bits (ENOB). Digital isolators present two main design challenges:

1. Propagation delay in digital isolator (described in 2.1)
2. Additive jitter due to digital isolator (described in 2.2)

These challenges and a detailed analysis of their impact with examples are described in the following sections.

2.1 Isolated DAQ Signal Chain Design—Timing Analysis

In DAQ systems, isolation in the signal chain breaks ground loops and thereby improves measurement accuracy and safety. Isolation may be achieved within the analog domain prior to the ADC or in the digital domain, after the ADC. Digital isolation is preferred when higher sampling rates are required. However, for a higher resolution (> 16 bits) and higher speed (>1 MSPS), the propagation delay and jitter of the digital isolator limits the signal chain performance for higher input signal frequencies. The propagation delay reduces the sampling rate of the signal chain. The jitter introduced by the digital isolator degrades the SNR at higher input frequencies.

This design guide describes the performance impact of propagation delay and jitter associated with isolated DAQ systems, explains the theory, calculation, and design, and presents examples.

2.1.1 Effect of Propagation Delay on Sampling Rate

In a typical DAQ system, a serial peripheral interface (SPI) transfers data between the ADC and the host. 図 5 shows a generic SPI block diagram. The host is generally the SPI master that decides the sampling rate and data transfer rate. In a typical SPI Motorola® protocol, the host sends data at rising edge and receives data on the falling edge within the same clock cycle.

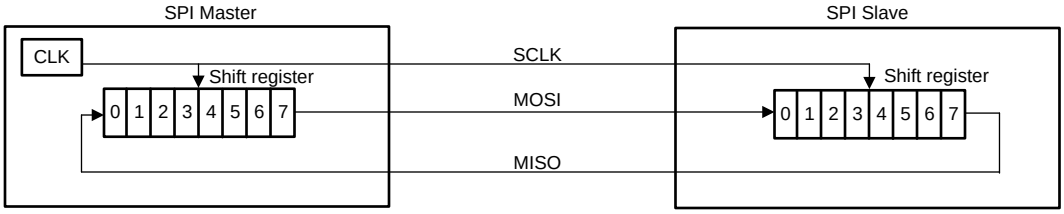


図 5. SPI Block Diagram

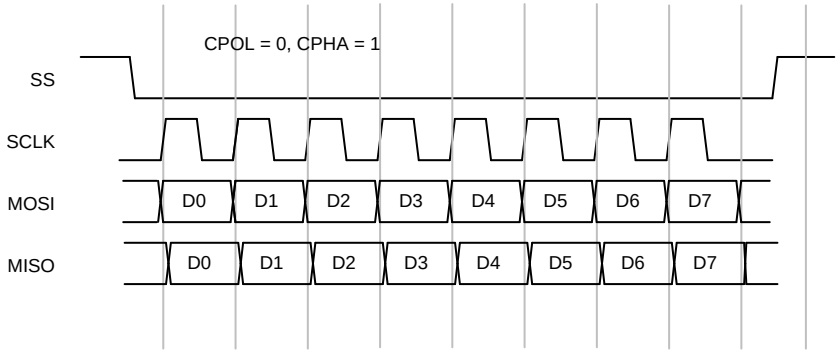


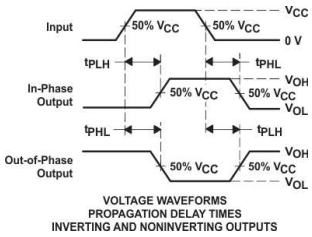
図 6. SPI Timing Diagram

As depicted in 図 6, the host expects valid data before the clock falling edge. The total round-trip propagation delay should be less than half the SCLK period to avoid missing bits. Hence, the theoretical maximum SPI clock can be calculated as:

$$SCLK_{max} = \frac{1}{2 \times t_{pd}} \quad (1)$$

式 1 assumes that there is no change in the waveform shape. However, digital signals become analog in nature as they have finite rise-fall times, which result in waveform deformities causing pulse width distortion (PWD) as they propagate through different digital signal chain elements. The pulse width of the clock or the data line changes due the different threshold voltages and rise-fall times of the digital devices in the path.

図 7 shows a datasheet example of propagation delay and PWD that can be found in various devices.



6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5	7.1	1	8.5	1	9.5	ns
t_{PHL}					5	7.1	1	8.5	1	9.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	1	13	ns
t_{PHL}					7.5	10.6	1	12	1	13	

図 7. Propagation Delay and PWD

A detailed timing analysis is required to calculate the maximum SPI clock rate by considering the SPI propagation delay and PWD.

2.1.2 Non-Isolated DAQ Timing Analysis

The timing analysis of a simple non-isolated DAQ system shown in 図 8 is first considered. The interface between the ADC and host is an SPI with a level translator. The analysis assumes that in each sampling interval, the ADC acquires a sample, converts it, and sends the serialized data to the host. The said assumption is critical for low latency systems.

The objective of the timing analysis is:

- Compute the maximum SPI clock rate (serialized data rate).
- Compute the maximum sampling rate of the ADC.

The maximum SPI clock is computed by estimating the total propagation delay and total PWD of the SPI. The ADC sampling rate is calculated from the SPI clock rate and ADC acquisition time. In this example, level translators or buffers are used in between the host and the ADC to make input and output voltage levels compatible and thus will add to the total round-trip delay that must be considered for timing analysis. 表 3 breaks down all the timing parameters in the ADC-host interface that is considered in this example.

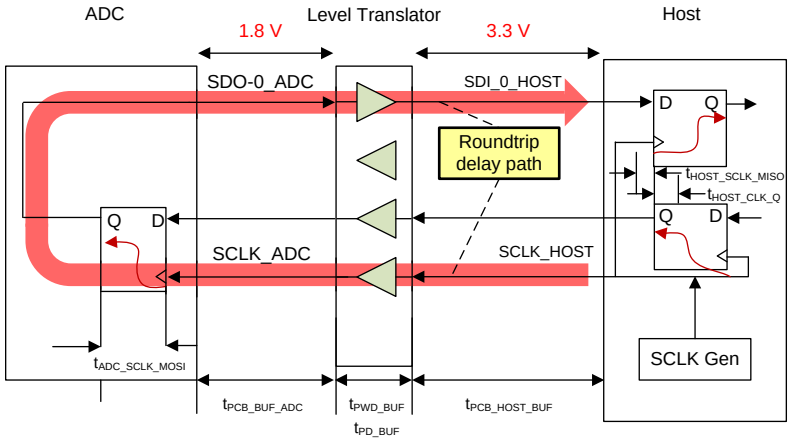


図 8. Simple Non-Isolated SPI ADC-Host Interface

表 3. Timing Parameter

PARAMETER	DESCRIPTION
t_{SCLK_min}	Minimum SCLK period
$t_{PCB\_HOST\_ISO}$	PCB trace delay between host and isolator
$t_{PCB\_HOST\_BUF}$	PCB trace delay between host and buffer
t_{PD_ISO}	Isolator propagation delay
t_{PD_BUF}	Buffer or level translator propagation delay
$t_{PCB\_BUF\_ADC}$	PCB trace delay between buffer and ADC
$t_{PCB\_ADC\_BUF}$	PCB trace delay between ADC and buffer
$t_{PCB\_BUF\_ISO}$	PCB trace delay between buffer and isolator
$t_{PCB\_ISO\_HOST}$	PCB trace delay between isolator and host
t_{SU_HOST}	Setup time of host MISO line
t_{PLHmax}	Maximum propagation delay from low to high
t_{PHLmin}	Minimum propagation delay from high to low
t_{PHLmax}	Maximum propagation delay from high to low
t_{PLHmin}	Minimum propagation delay from low to high
$t_{PWD\_BUF\_max}$	Maximum pulse width distortion of buffer or level translator
$t_{SCLK\_PH\_min}$	Minimum positive clock high period
$t_{PWD\_HOST\_max}$	Maximum host pulse width distortion
f_{SCLK_max}	Maximum SCLK frequency
$t_{PD\_HOST\_SCLK}$	Propagation delay of host SCLK at host end
$t_{ADC\_SCLK\_MOSI}$	ADC SCLK to MOSI output delay
$t_{HOST\_SCLK\_MISO}$	Host SCLK to MISO delay
t_{RTPD_max}	Maximum propagation round-trip delay
t_{OD_BUF}	Buffer output delay due impedance mismatch and loading effect of receiver
t_{OD_ISO}	Isolator output delay due impedance mismatch and loading effect of receiver

$$t_{RTPD\_max} = t_{PD\_HOST\_SCLK} + 2 \times t_{PD\_BUF} + t_{ADC\_SCLK\_MISO} + t_{HOST\_SCLK\_MISO} \quad (2)$$

2.1.2.1 Determining Maximum SPI Clock (SCLK)

In low latency system, the converted data should be made available to host system with minimum delay. A higher SCLK results in lower latency. The SPI clock should be computed for two cases:

1. SPI clock limited by ADC
2. SPI clock limited by round-trip delay

The minimum of these cases is the maximum SPI clock. 2.1.2.2 details the procedure to find the maximum SPI clock for a non-isolated SPI example.

$$SCLK_{max} = \min\left(SCLK_{max\_adc\_limited}, SCLK_{max\_rtpd\_limited}\right) \quad (3)$$

2.1.2.2 SPI Clock Limited by ADC

The maximum SPI SCLK is same as ADC_SCLK. However, the SPI SCLK duty cycle is affected by the PWD of the various digital devices it passes through. As a result, the maximum SPI SCLK limited by the ADC and digital device in the path is computed from $t_{SCLK\_ADC\_max}$ and $t_{PWD\_BUF\_max}$.

The system shown in 図 8 is used as an example with individual devices as listed in 表 4.

表 4. Devices Used in Non-Isolated and Isolated Interface Examples

SERIAL NO	DESCRIPTION	DEVICE
1	ADC	ADS8900B
2	LEVEL TRANSLATOR	74AVC4T245
3	ISOLATOR	ISO78XX
5	Flip-flop	SN74AUP1G80
4	PCB TYPE	FR4 - 4layer

Step 1: Estimating PWD of the Buffer

To find the PWD for the buffer 74AVC4T245, the max and min values of t_{PLH} and t_{PHL} are taken from the 74AVC4T245 datasheet.

$$t_{PWD\_BUF\_max} = \max\left(\left|t_{PLHmax} - t_{PHLmin}\right|, \left|t_{PHLmax} - t_{PLHmin}\right|\right) \quad (4)$$

$$t_{PWD\_BUF\_max} = \left(\left|4.5 - 0.1\right|, \left|4.5 - 0.1\right|\right)$$

$$t_{PWD\_BUF\_max} = 4.4\ ns$$

Step 2: Calculating Maximum ADC Clock

$$t_{SCLK\_PH} = t_{SCLK\_PH\_min} + t_{PWD\_BUF\_max} + t_{PWD\_HOST\_max} \quad (5)$$

表 5. Non-Isolated Interface Timing Parameters

PARAMETER	DELAY (ns)	REMARK
$t_{PWD\_HOST\_max}$	0	—
$t_{PWD\_BUF\_max}$ ($t_{PWD\_BUF} + t_{OD\_BUF}$)	4.40	No buffer or level translator in the TIDA-01037 round-trip path
$t_{SCLK\_PH\_min}$ ($0.45 \times t_{ADC\_CLK\_min}$)	5.99	—
t_{SCLK_PH}	10.39	—

$$f_{SCLK\_max} = \frac{1}{2 \times t_{SCLK\_PH}} = 48.1\ MHz \quad (6)$$

The maximum SCLK frequency supported by the ADC is 48 MHz.

2.1.2.3 SCLK Limited by Round-Trip Delay and Host SPI

The SCLK limited by round-trip delay is computed by finding the total propagation delay of the path that starts from the host MOSI and back to the host MISO through the ADC, which is marked as "round-trip" in 図 8.

$$t_{RTPD\_max} = t_{PD\_HOST\_SCLK} + 2 \times t_{PD\_BUF} + t_{ADC\_SCLK\_MISO} + t_{HOST\_SCLK\_MISO} \quad (7)$$

$$t_{RTPD\_max} = 0\ ns + 2 \times 4.5\ ns + 6.5\ ns + 1.2\ ns$$

$$t_{RTPD\_max} = 16.7\ ns$$

$$t_{SCLK\_min} \geq 2 \times t_{RTPD\_max} \quad (8)$$

$$t_{SCLK\_max} = \frac{1}{2 \times 16.7 \times 10^{-9}} \cong 30\ MHz \quad (9)$$

2.1.2.4 Determining Maximum ADC Sample Clock

The maximum ADC sampling clock assumes that in each sampling interval (or conversion cycle), the ADC performs sample acquisition, conversion, and data transfer. 図 9 shows a typical ADC timing diagram for one conversion cycle. The acquisition time and conversion time can be found in the ADC's datasheet. The data transfer time can be computed from the bits transferred and the SCLK period. However, acquisition and data transfer can happen at the same time. Hence the minimum conversion cycle time is:

$$t_{CONVST\_CYCLE\_min} = t_{CONV} + N \times t_{SCLK\_min} \quad (10)$$

For ADS8900B:

- t_{CONV} = 300 ns
- N = 20 for SDO0 only

注: The time requirement for the SCLK cycle varies depends on the resolution of the ADC resolution; see datasheets for the SPI mode of transfer.

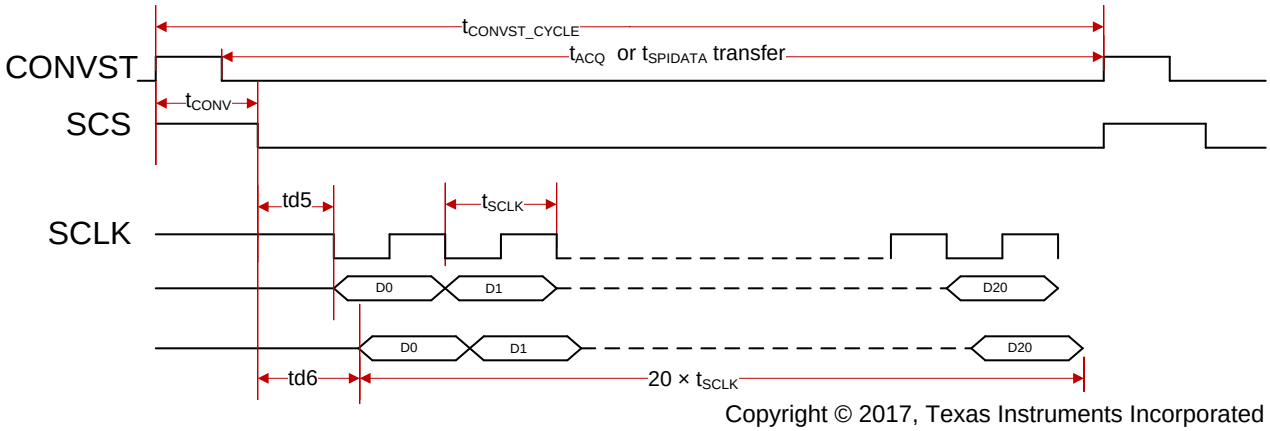


図 9. ADS8900B ADC Timing Diagram

表 6. ADS8900B Timing Parameter

PARAMETER	DESCRIPTION
t_{CONVST_CYCLE}	Time between two consecutive conversion start signal
t_{ACQ}	Acquisition time or SPI data transfer time
t_{CONV}	Conversion time

表 6. ADS8900B Timing Parameter (continued)

PARAMETER	DESCRIPTION
t_{SCLK}	SPI clock time period
td5	Minimum time required SCS low to SCLK low
td6	Time between SCS low to MISO change

The maximum ADC sampling clock frequency depends on the number of SDO lines and the maximum conversion time for the ADC. 式 11 shows the relationship between ADC sampling clock frequency and SDO line configuration. 表 7 lists the maximum SCLK frequency ($f_{ADC\_SAMPLECLK\_max}$) for various SDO lines calculated using 式 11.

$$f_{ADC\_SAMPLECLK\_max} = \left(\frac{1}{\left(N \times \frac{1}{f_{SCLK\_max}} \right) + t_{CONV}} \right) \quad (11)$$

表 7. SDO Lines versus ADC Sampling Frequency

SDOx	N	$f_{ADC\_SAMPLECLK\_max}$
SDO[0]	20	1 MHz
SDO[0..1]	10	1.6 MHz
SDO[0..3]	5	2.1 MHz

表 7 shows that a single SDO line is sufficient to achieve a 1-MSPS sampling rate in this non-isolated interface example.

2.1.3 DAQ Timing Analysis With Digital Isolator in Data Path

The isolated DAQ system shown in 図 10 is typical of such a system and is the subject of the next timing analysis example. The interface between the ADC and host is an SPI with a level translator and a digital isolator. Again, the analysis assumes that in each sampling interval, the ADC acquires the sample, converts it, and sends the serialized data to the host.

The objective of the timing analysis is:

- Compute the maximum SPI clock rate (serialized data rate).
- Compute the maximum sampling rate of the ADC.

As described in 2.1.2.1, the maximum SPI clock is computed by estimating the total propagation delay and total PWD of the SPI. The ADC sampling rate is calculated from the SPI clock rate and ADC acquisition time. 図 10 shows the timing parameter that is considered for this timing analysis example.

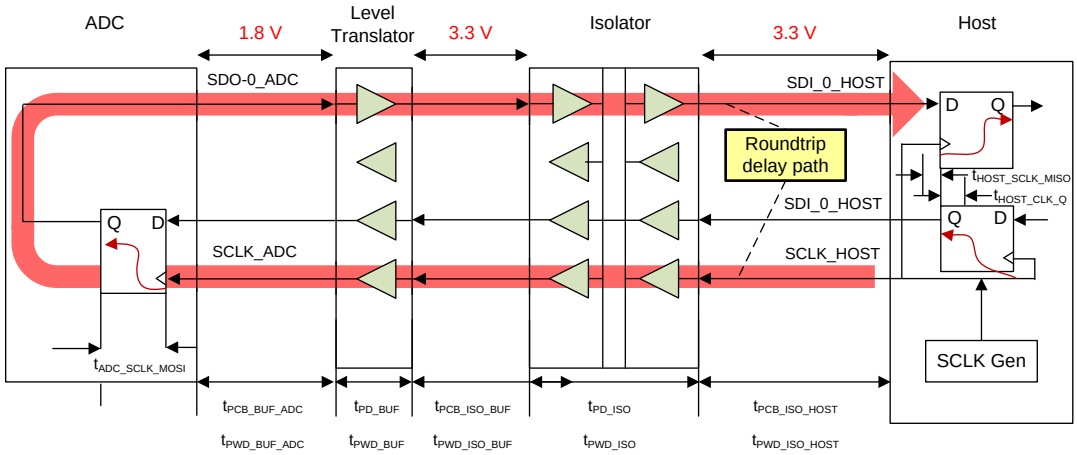


図 10. Isolated SPI ADC-Host Interface

2.1.3.1 Determining Maximum SPI Clock (SCLK)

As described in 2.1.2.1, in a low latency system, the converted data should be made available to the host system with minimum delay. Again, compute the SPI clock for two cases:

1. SPI clock limited by ADC
2. SPI clock limited by round-trip delay

The minimum of these cases is the maximum SPI clock. 2.1.3.2 details the procedure to find the maximum SPI clock for the isolated SPI example.

$$f_{SCLK\_max} = \min\left(f_{SCLK\_max\_adc\_limited},\ f_{SCLK\_max\_rtpd\_limited}\right) \quad (12)$$

2.1.3.2 Determining Maximum SCLK Limited by ADC

Computing the maximum SCLK limited by the ADC is similar to the procedure described in 2.1.2.2. 表 8 lists the associated timing parameter values taken from respective device datasheets. In this example, assume the level translator is not required and make the corresponding timing values zero.

表 8. Host to ADC Clock Path Timing

PARAMETER	DELAY (ns)	REMARK
$t_{PWD\_HOST\_max}$	0	Maximum PWD of host driver, typical value in tens of ps for FPGA
$t_{PWD\_BUF\_max}$ (t_{PWD_BUF} + t_{OD_BUF})	0	No buffer or level translator in the TIDA-01037
$t_{PWD\_ISO\_max}$ (t_{PWD_ISO} + t_{OD_ISO})	4.20	PWD of isolator (ISO7840)
$t_{SCLK\_PH\_min}$ (0.45 × 13.33)	5.99	High pulse time for 75-MHz clock with 45% duty cycle
$t_{SK\_BUF\_max}$	0	Buffer skew (no buffer in the TIDA-01037)
$t_{SK\_ISO\_max}$	2.50	Isolator skew
$t_{SCLK\_PH\_ISO}$	12.69	—

$$t_{SCLK\_PH\_ISO} = t_{SCLK\_PH\_min} + t_{PWD\_ISO\_max} + t_{SK\_ISO\_max} + t_{PWD\_BUF\_max} + t_{SK\_BUF\_max} + t_{PWD\_HOST\_max} \quad (13)$$

$$t_{SCLK\_PH\_ISO} = 12.69\ ns$$

$$f_{SCLK\_max\_adc\_limited} = \frac{1}{2 \times t_{SCLK\_PH\_ISO}} = \frac{1}{2 \times 12.69\ ns} = 39.4\ MHz \quad (14)$$

The maximum ADC-supported SCLK for an isolated system with an added isolator in data path is $f_{SCLK\_max\_adc\_limited} \cong 39$ MHz

2.1.3.3 SCLK Limited by Round-Trip Delay and Host SPI

The SCLK limited by round-trip delay computation for the isolated DAQ example is similar to the procedure detailed in 2.1.2.2. 表 9 lists all the timing parameter values in the round-trip path. The total round-trip delay is given by 式 15:

$$t_{RTPD\_ISO\_max} = t_{PD\_HOST\_SCLK} + t_{PCB\_HOST\_ISO} + 2 \times t_{PD\_ISO} + t_{PCB\_ISO\_BUF} + 2 \times t_{PD\_BUF} + t_{PCB\_BUF\_ADC} + t_{ADC\_CLK\_MISO} + t_{PCB\_ADC\_BUF} + t_{PCB\_BUF\_ISO} + t_{PCB\_ISO\_HOST} + t_{HOST\_SCLK\_MISO} \quad (15)$$

表 9. Timing Parameters in Isolated SPI Example

PARAMETER	DELAY (ns)	DESCRIPTION
$t_{PD\_HOST\_SCLK}$	0	Propagation delay host SCLK to output
$t_{PCB\_HOST\_ISO}$	1.5	PCB delay between host to isolator
$t_{PD\_ISO} \times 2$	32.0	Isolator propagation delay
$t_{PCB\_ISO\_BUF}$	0	PCB delay between Isolator to buffer or level translator
$t_{PD\_BUF} \times 2$	0	Buffer or level translator propagation delay
$t_{PCB\_BUF\_ADC}$	0	PCB delay between buffer to ADC
$t_{ADC\_CLK\_MISO}$	6.5	ADC clock to output delay
$t_{PCB\_ADC\_BUF}$	0	PCB delay between ADC to buffer
$t_{PCB\_BUF\_ISO}$	0	PCB delay between buffer to isolator
$t_{PCB\_ISO\_HOST}$	0	PCB delay between isolator to host
$t_{HOST\_SCLK\_MISO}$	1.2	Setup time of host MISO line
$t_{RTPD\_ISO\_max}$	41.2	—

The minimum SCLK period limited by the round-trip delay is:

$$t_{SCLK\_min\_rtpd\_limited} \geq 2 \times t_{RTPD\_ISO\_max}$$

$$f_{SCLK\_max\_rtpd\_limited} = \frac{1}{2 \times 41.2 \times 10^{-9}} \cong 12.1 \text{MHz} \quad (16)$$

Hence, f_{SCLK_max} = 12 MHz.

The round-trip delay limits the SPI SCLK to 12 MHz; any delay added in the round-trip path further reduces the maximum SCLK.

2.1.3.4 Determining Maximum ADC Sample Clock

The maximum ADC sampling clock rate computation procedure is same as described in 2.1.2.4, and 式 11 is repeated for reference:

$$f_{ADC\_SAMPLECLK\_max} = \left(\frac{1}{t_{CONVST\_CYCLE\_min}} \right) = \left(\frac{1}{t_{CONV} + N \times t_{SCLK\_min}} \right) \quad (17)$$

The ADC sampling clock rate for a different SDO line configuration is calculated using 式 17 and listed in 表 10.

表 10. Maximum ADC Clock and SDO Line Configuration

SDOx	N	$f_{ADC\_SAMPLECLK\_max}$
SDO[0]	20	508 kHz
SDO[0..1]	10	1.1 MHz
SDO[0..3]	5	1.4 MHz

These results shows the design needs at least two SDO lines to achieve a 1-MSPS sampling rate in this isolated SPI example.

2.1.4 Maximizing Sample Rate With Source-Synchronous Mode

Part of TI's family of high-performance SAR ADCs, both the ADS9110 and ADS8900B possess a source-synchronous feature that significantly overcomes the limitation of SCLK reduction due to round-trip propagation delay. The source-synchronous mode provides a clock output (on the RVS pin) synchronized to the output data (SDOx data lines). The host can receive the data with a slave SPI. The maximum ADC sampling clock frequency is determined by selecting the minimum of SCLK limited by ADC and RVS limited by the host.

$$f_{SCLK\_max} = \min\left(f_{SCLK\_max\_adc\_limited}, f_{SCLK\_max\_host\_limited}\right) \quad (18)$$

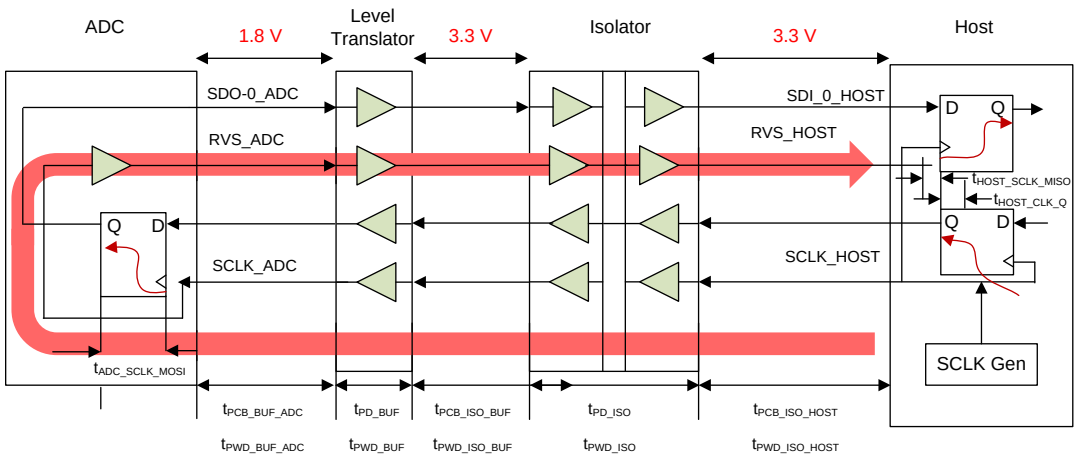


図 11. Isolated SPI in Source-Synchronous Mode

2.1.5 Determining Maximum SCLK Limited by ADC and Host

Computing the maximum SCLK limited by the ADC is described in 2.1.3.2. A level translator is not required, and corresponding timing values are made zero.

$$f_{SCLK\_max\_adc\_limited} = \frac{1}{2 \times t_{SCLK\_PH\_ISO}} = \frac{1}{2 \text{ x } 12.69 \text{ ns}} = 39.4 \text{ MHz} \quad (19)$$

Hence the maximum SCLK limited by ADC is:

$$f_{SCLK\_max\_adc\_limited} \cong 39 \text{ MHz}$$

Similarly, the SCLK limited by the host can be computed as:

$$t_{SCLK\_min\_host\_limited} = t_{RVS\_SCLKPH\_ISO} = t_{SCLK\_PH\_min} + t_{PWD\_BUF\_max} + t_{SK\_BUF\_max} + t_{PWD\_ISO\_max} + t_{SK\_ISO\_max} + t_{PWD\_ADC\_max} \quad (20)$$

表 11. ADC-to-Host Clock Path Timing

PARAMETER	DELAY (ns)	REMARK
$t_{SCLK\_PH\_min}$ (0.45 × 2 × 12.69)	11.4	High pulse time for $f_{SCLK\_max\_adc\_limited}$ clock with 45% duty cycle
$t_{PWD\_BUF\_max}$ (t_{PWD_BUF} + t_{OD_BUF})	0	No buffer or level translator in the TIDA-01037
$t_{SK\_BUF\_max}$	0	Buffer skew (no buffer in the TIDA-01037)
$t_{PWD\_ISO\_max}$ (t_{PWD_ISO} + t_{OD_ISO})	4.2	PWD of the isolator (ISO7840)
$t_{PWD\_ADC\_max}$	0	Maximum PWD of ADC SDO output lines
$t_{SK\_ISO\_max}$	2.5	Isolator skew
$t_{RVS\_SCLKPH\_ISO}$	18.1	—

$$t_{SCLK\_min\_host\_limited} = 18.1\,ns \quad (21)$$

$$f_{SCLK\_max\_adc\_limited} = \frac{1}{2 \times t_{SCLK\_min\_host\_limited}} = \frac{1}{2 \times 18.1\,ns} = 27.6\ MHz \quad (22)$$

The value of the PCB trace delay does not matter if the user can route RVS and SDOx at equal length and keep the differential length to a minimum. The differential length between RVS and SDOx results in skew, and that has to be considered for $t_{RVS\_SCLKPH\_ISO}$ calculation.

Hence with f_{SCLK_max} = 27.6 MHz, the maximum ADC sampling rate is computed for different SDOx line configuration and listed in 表 12.

表 12. Maximum ADC Sample Rate in Source-Synchronous Mode

SDOx	N	$f_{ADC\_SAMPLECLK\_max}$
SDO[0]	20	975 kHz
SDO[0..1]	10	1.5 MHz
SDO[0..3]	5	2.0 MHz

表 12 shows that it possible to achieve a sampling rate of 2 MSPS using source-synchronous mode and a multiSPI™ configuration.

2.1.6 Concluding Remarks

The document provides a comprehensive timing analysis for non-isolated and isolated ADC interfaces. The objective of the timing analysis is to determine the maximum ADC sampling rate and the maximum SPI clock to maximize ADC sample rate. The maximum SPI clock ensures minimum latency. Digital isolators have large propagation delays, which limit the maximum SPI clock. Source-synchronous mode and a multiSPI configuration makes it possible to achieve a high sampling rate with digital isolators.

2.2 Additive Jitter Due to Digital Isolator

The ADC SNR performance is a function of sampling clock jitter at a high input signal frequency. The digital isolator's additive jitter to the sample clock limits the signal chain SNR. To the first order, the jitter impact on SNR can be calculated as:

$$SNR = -20 \log (2\pi f_{in} \times t_{jitter}) + 10 \log (OSR) \quad (23)$$

where:

- f_{in} is the input signal frequency
- t_{jitter} is the total jitter of the ADC (internal clock + external clock)
- OSR is the over sampling ratio (only for sigma-delta ADC)

As can be seen in 図 12, the SNR impact from jitter increases with the signal frequencies because it results in a larger measurement error. Find more details in the TIDA-00732 design guide, *18-Bit, 2-MSPS Isolated Data Acquisition Reference Design for Maximum SNR and Sampling Rate* (TIDUB85).

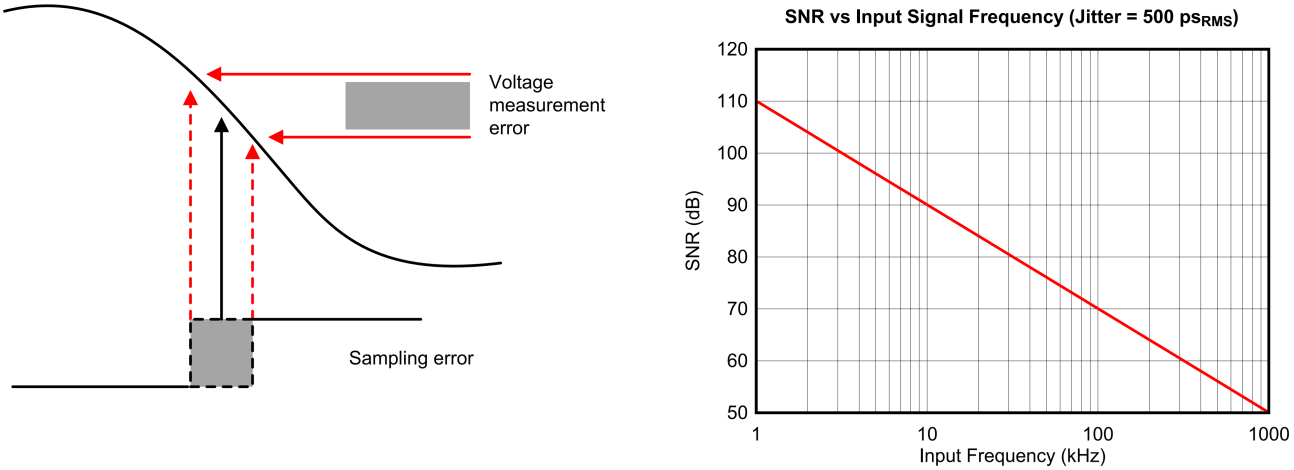


図 12. Error Due to Jitter on Sampling Clock

2.3 TIDA-01037 Solution

2.3.1 Compensating for Propagation Delay

The ADS8900B has a multiSPI digital interface that allows the host controller to operate at a slower SPI SCLK and still achieves the required sampling rate. The multiSPI module offers the following options to reduce SCLK speed:

- Option to increase the width of the output data bus - 1, 2, and 4 SDO lines
- ADC mater mode or source-synchronous mode

The multiSPI option allows the SPI SCLK to be reduced, which in turn reduces the impact on the sampling rate of the propagation delay. If the reduced SCLK rate is still above the loopback delay, then source-synchronous mode will be useful.

In ADC mater mode or source-synchronous mode, the SCLK from the host is looped back by the ADC along with the data. The clock and data are synchronous in source-synchronous mode; therefore, the propagation delay of the isolator has no impact on the data rate.

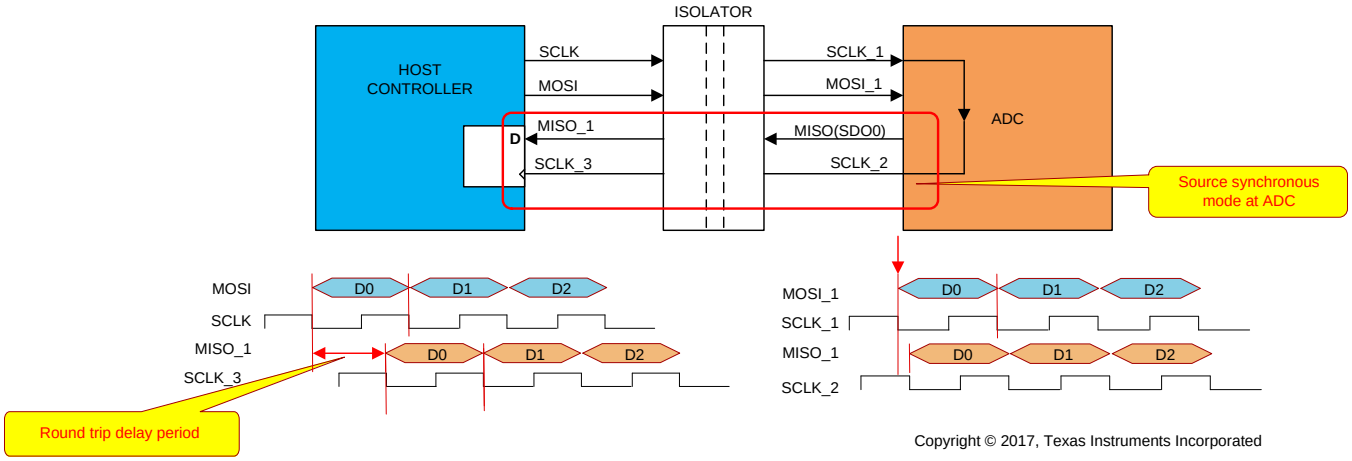


図 13. ADS8900B SPI Source-Synchronous Mode With Host and Slave End Timing Waveform

As illustrated in 図 13, in ADC-master or source-synchronous mode, the device provides an asynchronous output clock (on the RVS pin) along with the output data (on the SDO-x pins). The ADC-master or source-synchronous mode completely eliminates the effect of isolator delays and the clock-to-data delays, which are typically the largest contributors in the overall delay.

2.3.2 Mitigating SNR Degradation Due to Jitter

Any sample clock (CONVST) jitter will degrade ADC SNR performance at high input signal frequencies, which reduces system performance, as defined by 式 23 and outlined in detail by the TIDA-00723 TI Design. Generating a CONVST signal with a low-jitter oscillator will minimize mitigate jitter, improving SNR performance by nearly 12 dB as demonstrated by the TIDA-00732 and TIDA-01035 designs. However, such solutions may not be feasible for host-controlled sample clocks, but minimizing additive jitter while maximizing the sample clock is still desired.

In order to optimize performance, two isolators are used. The ISO734x family is used to isolate the jitter sensitive sampling clock because it possesses an adequate signaling speed and low jitter. Note that the sampling clock will always be a frequency (can be determined using 式 11) below SPI, and its isolator signaling speed is not normally a design constraint. However, isolator propagation delay and signaling directly impacts SPI data throughput (CS, SCLK, SDO, SDIx lines). SPI lines are jitter tolerant and the ISO784x is used to maximize data without additive jitter concerns. 表 13 highlights the ISO734x and ISO784x performance, and when used together, they can optimize the DAQ SNR and the sample rate.

表 13. Isolator Jitter From Datasheet

ISOLATOR	JITTER (pk-pk)	SPEED	PROPAGATION DELAY
ISO784x	900 ps at 3.3 V	100 Mbps	11 ns
ISO734x	130 ps at 3.3 V	25 Mbps	31 ns

図 14 illustrates the optimized DAQ design. A host-generated ADC sample clock (CONVST) is derived from the system clock, SYS_CLK, and uses the low-jitter signal path enabled by the ISO734x. High-speed signaling is achieved with the ISO784x for the SPI data lines (CS, SCLK, SDI, SDO[3:0], and RVS). Furthermore, the TIDA-01037 possesses an optional jitter cleaner circuitry that can be used to reduce host-generated CONVST jitter. This circuitry contains a low-jitter clock generator used to re-clock the CONVST (generated by the host) with SYS_CLK to remove the jitter added by the host.

図 14 shows the datasheet jitter specification of the isolator used in the TIDA-01037 design.

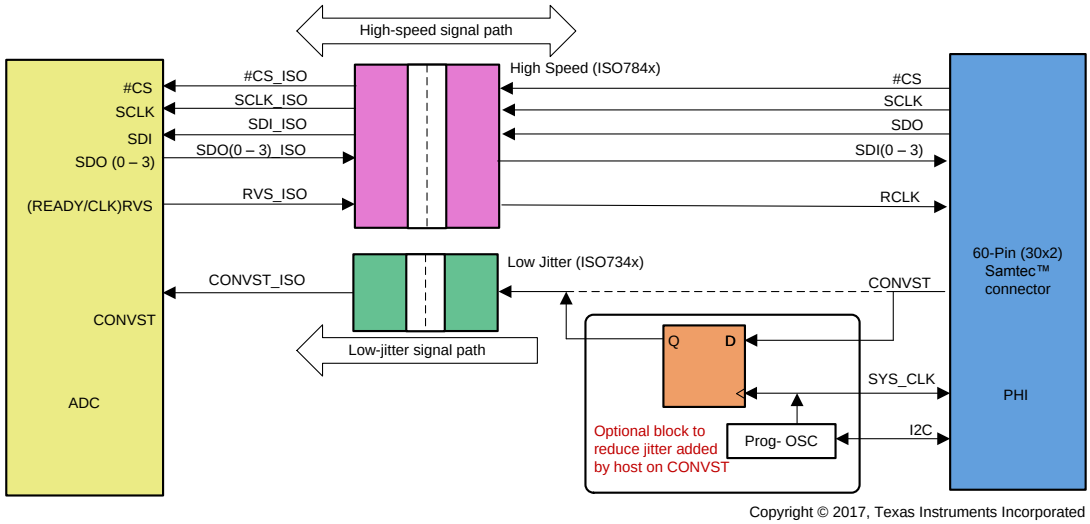


図 14. TIDA-1037 Optimized Block Diagram for Isolated DAQ

2.4 Circuit Design

To optimize the performance of the 20-bit, 1-MSPS DAQ system, the input buffer, anti-aliasing filter, and reference driver must be designed in such a way that the performance is equal to or greater than the ADC performance.

2.4.1 Analog Input Front End (Input Buffer and Anti-Aliasing Filter)

図 15 describes the TIDA-01037's AFE, which highlights the differential input filter, high output drive differential input buffer, and anti-aliasing filter. A high-speed, fully differential amplifier (FDA) with a programmable output common mode is well suited to drive the data converter due to its inherent nature to increase immunity to external common-mode noise and reduce even order harmonics.

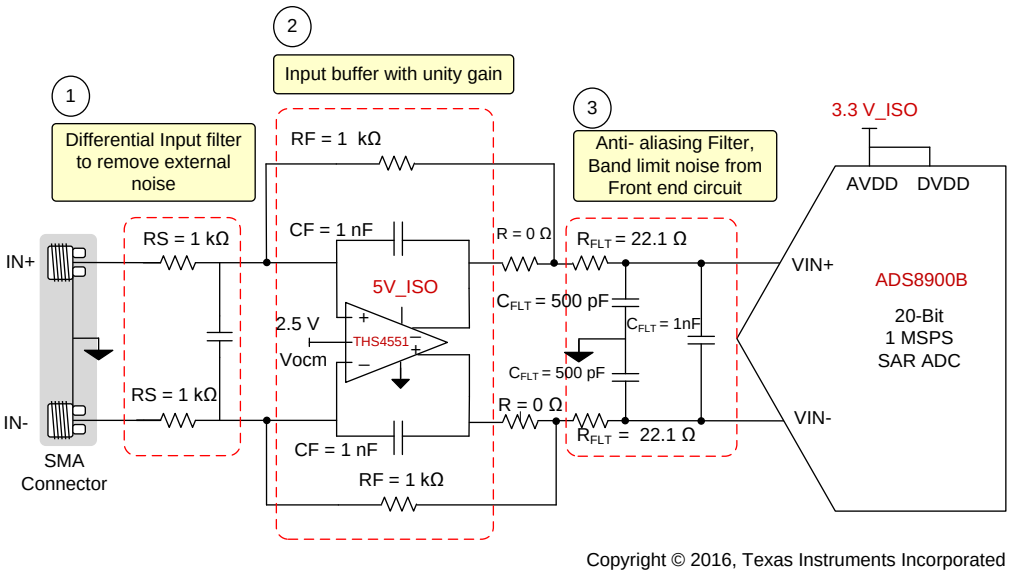


図 15. TIDA-01037 AFE

The TIDA-01037 is designed with the THS4551 FDA configured as an unity gain second-order active low-pass filter, which drives the 20-bit, 1-MSPS ADS8900B SAR ADC at full dynamic range. The transfer function of this filter is determined by 式 24:

$$\frac{V_{OD}}{V_{IN}} = \frac{RF}{RS} \times \left(\frac{1}{1 + j2\pi f \times RF\, C_F} \right) \times \left(\frac{1}{1 + j2\pi f \times 2 \times R_{FLT} C_{FLT}} \right) \quad (24)$$

The amplifier gain is determined by the RF and RS ratio and both were chosen to be 1 kΩ, so the FDA is configured as an unity gain buffer. In order to satisfy the design's targeted specifications of supporting 100-kHz input signals, the anti-aliasing filter cutoff frequency was designed to be ≅ 4 MHz. The differential mode capacitor added across the filter output helps remove high-frequency differential noise and increase THD performance. Take care to select passive components with minimum voltage and temperature coefficients to preserve THD performance for varying input and temperature conditions.

2.4.2 Reference Buffer Circuit

The reference driver circuit, illustrated in 図 16, generates a voltage of 5-V DC using a single 5.2-V supply. This circuit is suitable to drive the reference of the ADS8900B at higher sampling rates up to 1 MSPS. The reference voltage of 5 V in this TI Design is generated by the high-precision, low-noise REF5050 circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter formed by resistor R90 and capacitor C88.

The R_{BUF_FLT} is R93, and the C_{BUF_FLT} is C96 at the output of the reference driving ADC reference input. The value of R_{BUF_FLT} and C_{BUF_FLT} can be found using 式 25:

$$C_{BUF\_FLT} = \frac{I_{REF} \times T_{CONV\_MAX} \times 2^N}{V_{REF}} \quad (25)$$

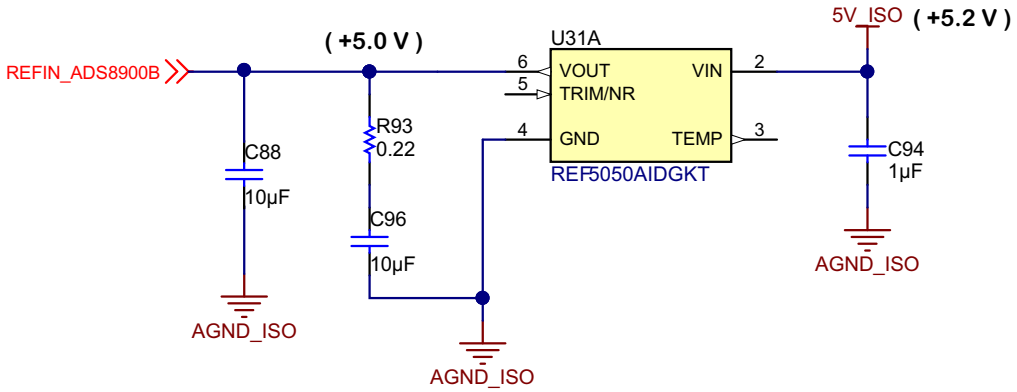


図 16. Reference Buffer Circuit

2.4.3 Common-Mode Voltage (VOCM)

The external REF5050 high-precision, ultra-low noise, low-drift voltage reference generates both ADC voltage reference and signal input common-mode to ensure the complete dynamic range of the is ADS8900B used. The voltage is at a value of 2.5 V (5 V / 2) by using the REF5050 and the OPA376 precision, low-noise amplifier as a buffer, as illustrated in 図 17.

The FDA common-mode voltage (VOCM) should be at mid-supply to achieve maximum output dynamic range. VOCM is derived from the supply voltage with resistive divider network. The VOCM voltage is buffered using the OPA376 op amp within the loop compensation method. This configuration has good stability when driving larger capacitive loads.

Resistor R96 is an isolation resistor that is connected in series between the op amp output and the capacitive load to provide isolation and avoid oscillations. Capacitor C95 between the op amp output and the inverting input becomes the dominant AC feedback path at higher frequencies. This configuration allows heavy capacitive loading while keeping the loop stable. The feedback resistor R94 helps to maintain the output DC voltage same as the non-inverting input of op amp.

The value of resistor R96 has chosen such that lowers than 10% of load. The combination of resistor R95 and capacitor C100 forms a low-pass filter with a cutoff frequency of 159 Hz. This filter will clean the ripple and noise.

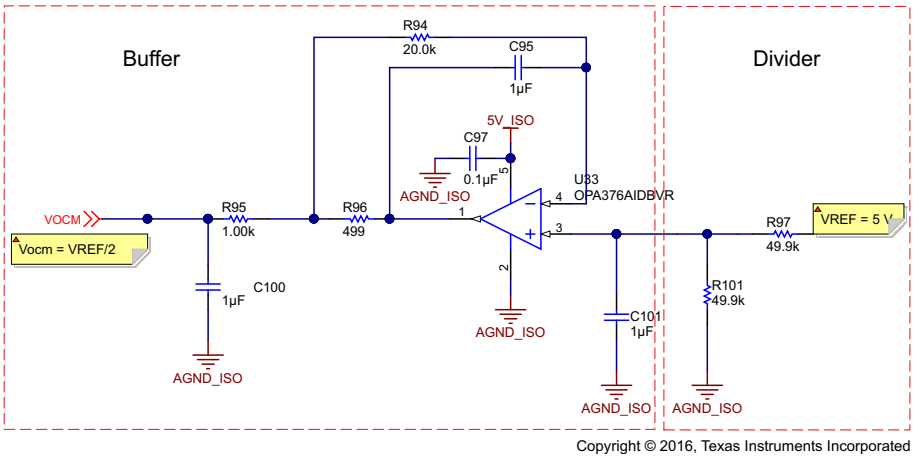


図 17. Common-Mode Voltage

2.4.4 Clock Design

The clock source is an essential component in signal chain design, specifically when driving the ADC sample clock. Clock jitter directly impacts ADC SNR performance and becomes proportionally greater at higher input signal frequencies. It is important that the jitter from the selected clocking source will be significantly less than the jitter introduced by the digital isolator.

This design has two master clock sources that can be used for ADC sample clock generation, jitter cleaner logic, and host interface synchronization. 表 14 shows how to select one of the sources by properly setting indicated resistor jumpers:

- Crystal oscillator (3.3 V, 125 MHz, 50 ppm, low jitter, 1.9-ps jitter)
- LMK61E2 - Programmable crystal oscillator (3.3 V, 150 MHz, 90-fs jitter)

表 14. Master Clock Selection

SERIAL NO	MASTER CLOCK	RESISTOR MOUNTING	REMARKS
1	Crystal oscillator	R14: Populate R17: Do not populate	3.3 V, 125 MHz, 50 ppm, low jitter, 1.9-ps jitter
2	Programmable crystal oscillator (LMK61E2)	R14: Do not populate R17: Populate	3.3 V, 150 MHz, 90-fs jitter (Frequency of oscillator must be programmed to 125 MHz through I^2C interface)

2.4.4.1 Programming LMK61E2

The LMK61E2 programmable crystal oscillator can be program using a USB2ANY programming cable with the CodeLoader4 software programming tool. The setup file of the LMK61E2 can be downloaded from the CodeLoader webpage.

図 18 shows the hardware setup of the TIDA-01037 with USB2ANY hardware. 表 15 lists connection definitions.

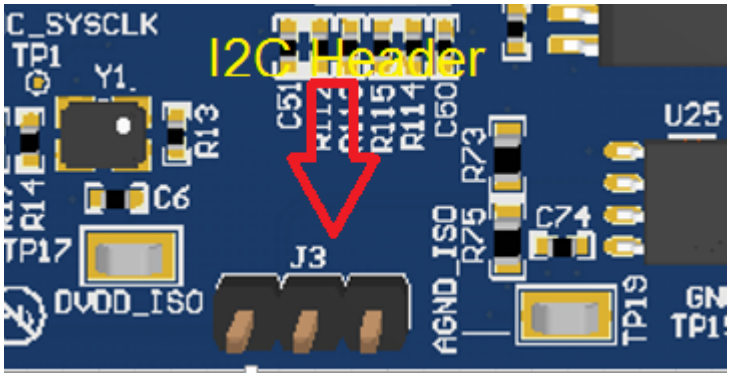


図 18. LMK61E2 Programming Setup

表 15. USB2ANY Connection

SIGNAL NAME	TIDA-01037	USB2ANY
SCL	Pin no 3 / J3	Pin no 2 /J4
SDA	Pin no 2 / J3	Pin no 1 /J4
GND	Pin no 1 / J3	Pin no 5 /J4

2.4.4.1.1 Programming Procedure

1. Open the CodeLoder4 programming tool and select the LMK61E2 device.

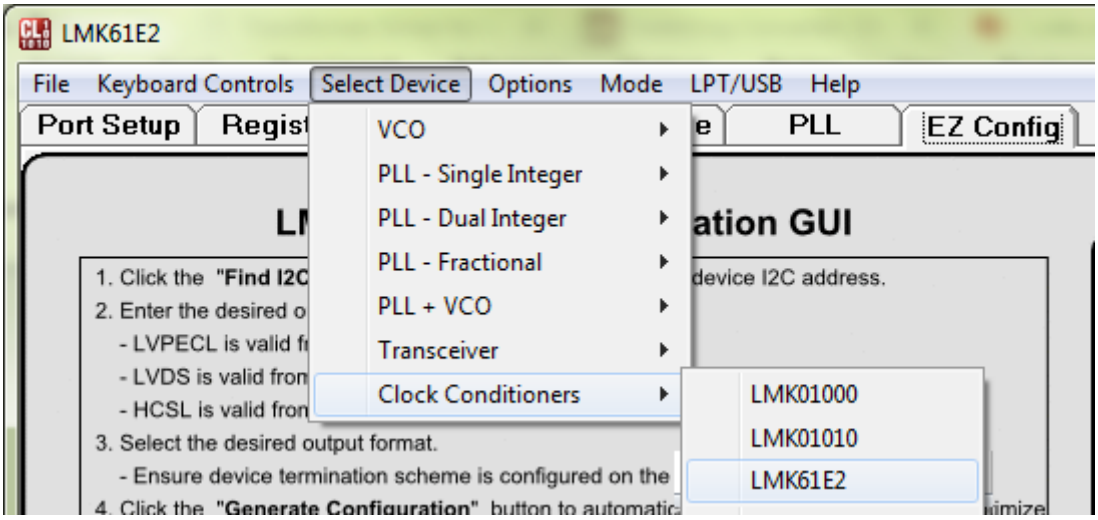


図 19. Select Device

2. Go to the EZ Config tab. Under *Output Configuration*, enter "45" for MHz and the output type as "LVDS". Then generate the configuration and click the Program EEPROM button. Follow these steps (1 to 5) as shown in 図 20.

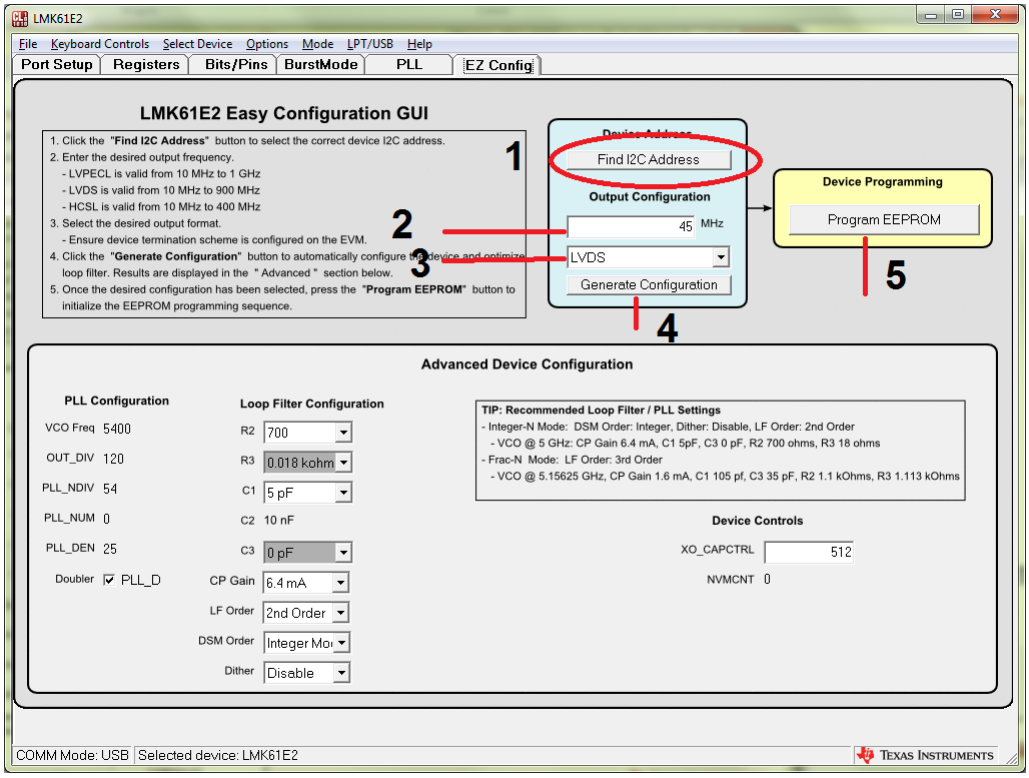


図 20. Steps to Configure LMK61E2 GUI

2.4.5 Isolator Design and Optimization

In order to provide the required system protection, the TIDA-01037 uses TI's ISO1541, ISO734x, and ISO784x family of high-performance isolated devices. The ISO784x series supports signaling rate up to 100 Mbps, has a low 11-ns propagation delay, and operates from a wide supply voltage (2.25 to 5.5 V). The ISO734x series operates from a 3.3- to 5.5-V supply, possesses a very low jitter (≈ 130 ps) signaling rate up to 25 Mbps, and a typical propagation delay of 35 ns. These isolators are reinforced with very high immunity possessing either a 3.0- or 5.7-kV_{RMS} isolation voltage. The digital interface requires six isolation channels for standard source-synchronous SPI communication and up to nine channels when four multiSPI outputs are used.

On the other hand, the ADC sampling clock requires just one ISO734x isolator channel. A single ISO1541 bidirectional isolator is used for I^2C communication to the optional jitter cleaner (see the TIDA-01035 TI Design for more information).

The TIDA-01037 demonstrates how an isolated analog input can be optimized using six to nine isolated channels. In this example, illustrated in 図 21, three digital isolators are required (one ISO734x and two ISO784x devices). More commonly, data converters lacking the source-synchronous mode and multiSPI features will require just two isolator devices (one ISO734x and one IS784x), as illustrated in 図 22.

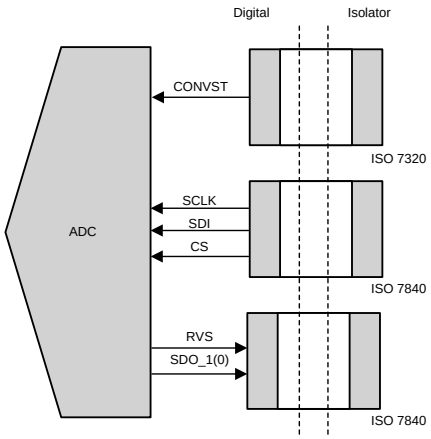


図 21. TIDA-01037 Isolated DAQ Solution Using TI's Source-Synchronous Mode

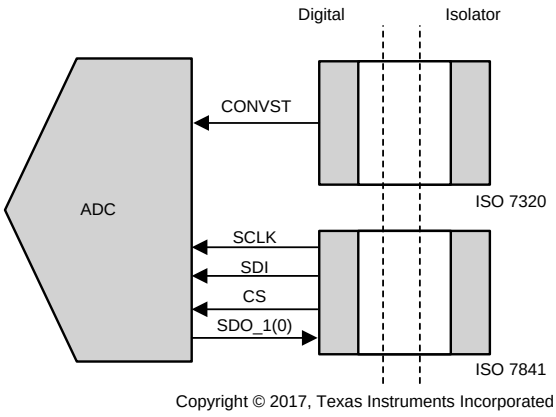


図 22. Typical Isolated DAQ Solution

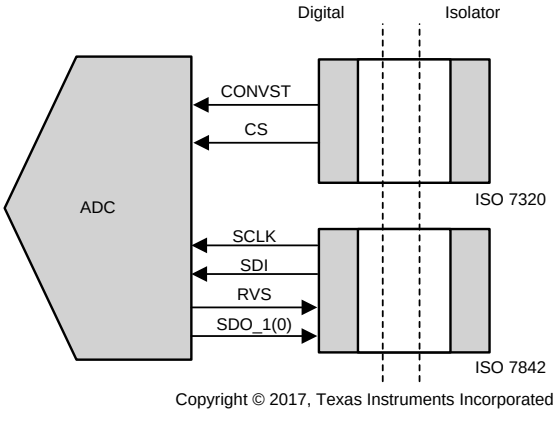


図 23. Isolated DAQ Solution Using TI's Source-Synchronous Mode and Only Two Isolators

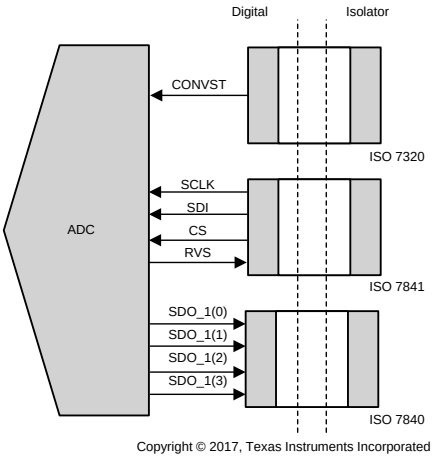


図 24. SNR and Sample Rate Optimized Isolated DAQ Solution

Studying 図 21, it is quickly realized that a more optimum solution would be able to move the CS signal to the ISO7340 channel and replace the ISO7840 with an ISO7842 so the other ISO7840 can be eliminated as shown in 図 23. Account for the propagation delay differences between the CS and other SPI signals (SCLK, SDI, and SDOx), and as a result, it may not practical. A more desirable and optimized solution for high-speed signaling is illustrated in 図 24. TI's multiSPI feature is used to minimize SPI frequency and maximize ADC sample rate across the isolation boundary where three additional SPI outputs (SDO1-3), and thus three additional isolated data channels, are required. However, this solution still requires only three digital isolators while maximizing the features provided by the ADC, resulting in better device utilization. Similar to the previous solution, take care to match the propagation delays between the ISO7841 and ISO7840 devices; however, they do both possess similar nominal propagation delays.

表 16. Required Number of Isolators for Common DAQ Systems

DATA LINES	ONE DATA LINE SDO(0)				TWO DATA LINES SDO(0:1)				FOUR DATA LINES SDO(0:3)			
ISO xxxx	7320/7340	7840	7841	Total	7320/7340	7840	7841	Total	7320/7340	7840	7841	Total
Single analog input	1	0	1	2	1	2	0	3	1	2	0	3
Dual analog input	1	3	0	4	1	3	0	4	1	4	0	5
Quad analog input	1	4	0	5	1	5	0	6	1	7	0	8
Eight analog input	2	8	0	10	2	10	0	12	2	14	0	16

表 17. Required Number of Isolators for DAQ Systems Using Source-Synchronous Mode

DATA LINES	ONE DATA LINE SDO(0)				TWO DATA LINES SDO(0:1)				FOUR DATA LINES SDO(0:3)			
ISO xxxx	7320/7340	7840	7841	Total	7320/7340	7840	7841	Total	7320/7340	7840	7841	Total
Single analog input	1	0	1	2	1	1	1	3	1	1	1	3
Dual analog input	1	1	2	4	1	1	2	4	1	2	2	5
Quad analog input	1	5	0	6	1	6	0	7	1	8	0	9
Eight analog input	2	10	0	12	2	12	0	14	2	16	0	18

2.4.6 Power Supply Solution

This TI Design requires isolated and non-isolated power rails to various components. The following section provides a detailed design procedure for the various power supply rails.

2.4.6.1 DC-DC

The LMZ14203TZ-ADJ simple switcher is capable of accepting a 6- to 46-V DC input and deliver a 0.8- to 6-V output with 90% efficiency. The undervoltage lockout is selected at 7.97 V, which helps to enable the LMZ4203TZ-ADJ.

To set a 5-V output voltage, the resistor R_{FBT} (R25) and R_{FBB} (R31 + R36) decide the output voltage of the LMZ14203TZ-ADJ. For a 5.6-V output:

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{5.6}{0.8}\right) - 1 \tag{26}$$

$$\frac{R_{FBT}}{R_{FBB}} = 6$$

$$R_{FBT} = \frac{5.62\,K}{6} = 932\,\Omega \tag{27}$$

Therefore, R25 = 5.62K , R31 = 931 Ω, and R36 = 1 Ω.

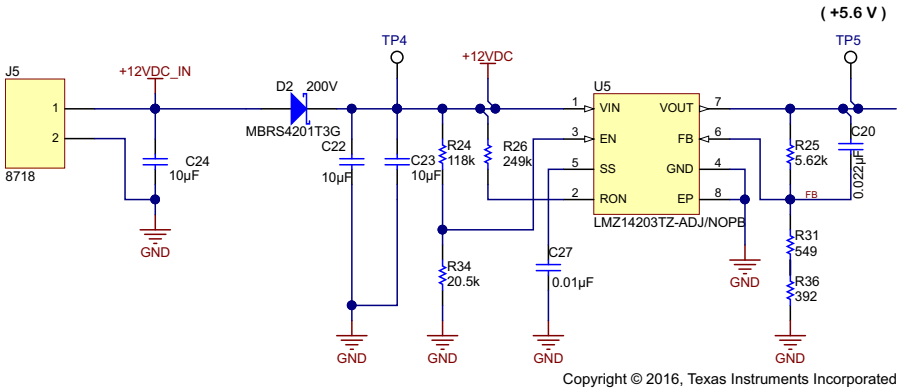


図 25. DC-DC Power Supply

2.4.6.2 LDOs

The TPS7A4700 is a positive voltage (36 V), ultra-low-noise (4 μV_{RMS}) LDO capable of sourcing a 1-A load. The TPS7A470x is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering op amps, ADCs, DACs, and other high-performance analog circuitry.

The TPS7A4700RGWR has ANY-OUT™ programmable pins to program the desired output voltage. The sum of the internal reference voltage (V_{REF} = 1.4 V) plus the accumulated sum of the respective voltage is assigned to each active pins. The ANY-OUT pins (Pin 8, Pin 1, and Pin 12) are programmed to active low to get 3.3 V at the output.

The TPS709 series of linear regulators are ultra-low quiescent current devices designed for power sensitive applications. A precision band gap and error amplifier provides 2% accuracy over temperature. The LDO can accept 2.7- to 30-V input voltages and deliver fixed output voltages 1.2 to 6.5 V with a maximum 200-mA output current. The TPS70918DBVT generates 1.8- from 5-V DC of the LMZ14203TZ-ADJ DC-DC converter.

2.4.6.3 Push-Pull Transformer

The SN6501 is a transformer driver designed for low-cost, small form-factor, isolated DC-DC converters using push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals that alternately turn on and off the two output transistors.

The SN6501 transformer driver is designed for low-power push-pull converters with input and output voltages in the range of 3 to 5.5 V. While converter designs with higher output voltages are possible, take care that higher turns ratios do not lead to primary currents that exceed the SN6501 specified current limits.

The TIDA-01037 uses the recommended transformer inform the SN6501 datasheet. For transformer selection and isolation power supply design, see the SN6501 datasheet. 表 18 shows key parameters of the transformer.

表 18. Transformer Specification

PARAMETER	VALUE
Voltage—time	11 µs
Turns ratio	1.1:1 ± 2%
Switching frequency	150 kHz min
Di electric	6250 rms, 1 second

3 Getting Started Hardware and Software

3.1 Host Interface

The system performance of the TIDA-01037 can be evaluated using TI's precision host interface (PHI) controller. PHI is TI's SAR ADC evaluation platform, which supports the entire TI SAR ADC family. By using PHI, the TIDA-01037 can easily communicate with the host PC using a USB interface. PHI supports the ADS8900B multiSPI and onboard configuration I^2C EEPROM interface. PHI GUI software can evaluate both the AC and DC parameters of the ADS8900B.

For more information on PHI, see the ADS8900B EVM-PDK.

3.2 Hardware Functional Block

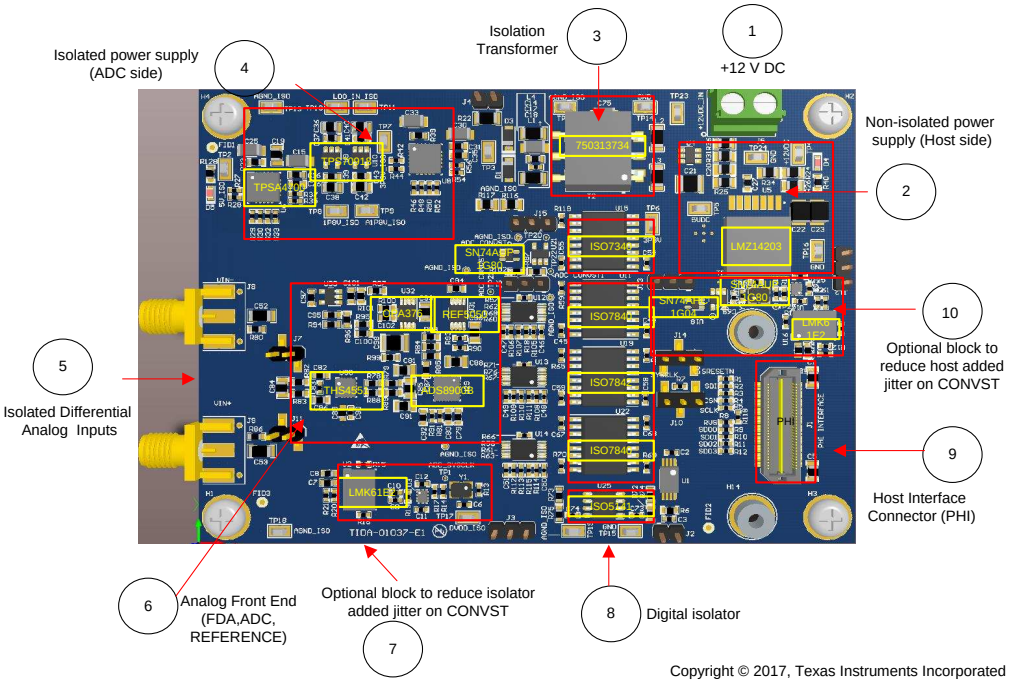


図 26. TIDA-01037 Hardware

図 26 shows various hardware functional blocks of the TIDA-01037 and function of each block:

1. 12-V DC power supply input connector that accepts 9- to 12-V DC input to power the TIDA-01037
2. Host-side DC-DC buck convertor that generates 5 V from the 12-V input
3. Isolation transformer for power supply isolation and isolated power that is generated with the SN6501 push-pull transformer driver
4. Isolated power supply rails block that generates 5-V, 3.3-V, and 1.8-V power rails
5. Differential analog inputs connector
6. AFE circuits (ADC ADS8900B, THS4551, and REF5050)
7. Optional jitter mitigation block to reduce jitter on ADC side
8. Digital isolator for data isolation (SPI and I^2C)
9. PHI interface connector, which uses the TIDA-01037 to communicate with the host PC through USB interface
10. Optional jitter mitigation logic block to reduce host added jitter on CONVST

3.2.1 Operation Mode

The TIDA-01037 hardware had provision to compare the performances of the low-jitter isolator and high-speed isolator using mode selection as illustrated in 図 27. 表 19 shows the jumper configuration for CONVST path selection.

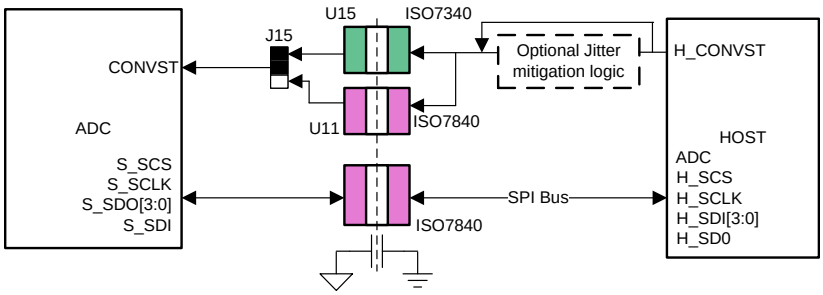


図 27. CONVST Isolator Path Jumper Selection

表 19. Operation Mode Jumper Setting

JUMPER SETTING	DESCRIPTION
J15—1, 2 Short	CONVST signal passed through ISO7840 isolator and connected to ADC sample clock input
J15—2, 3 Short	CONVST signal pass through ISO7340 isolator and connected to ADC sample clock input

3.3 Getting Started Application GUI

The PHI GUI software, which is based on the LabVIEW™ platform, validates the TIDA-01037. 図 28 shows the available test options in the PHI GUI.

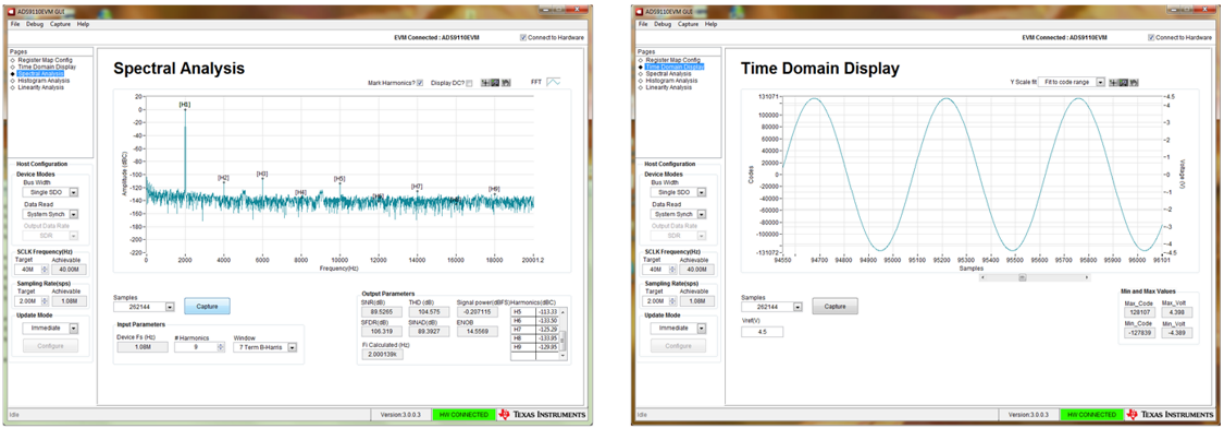


図 28. PHI GUI Demonstrate AC Parameter Analysis (Spectral and Time Domain)

The PHI GUI can be used to validate the following system key specifications:

1. Spectral analysis
   - SNR
   - THD
   - SFDR
   - SINAD
   - ENOB
2. Linearity analysis
   - DNL
   - INL
   - Accuracy
3. Histogram analysis
   - Effective resolution

Find the PHI GUI software at the ADS8900B product page.

4 Testing and Results

4.1 Test Setup

図 29 shows the TIDA-01037 test setup to validate complete signal chain performance of isolated high-speed, high SNR (20-bit, 1-MSPS) analog input DAQ module.

The test needs to evaluate the performance of a high-speed (1-MSPS) and high-resolution (20-bit) system that is compliant with testing requirements. The setup has a DS360, a standard research systems precision ultra-low distortion waveform generator, which is capable of generating a sine pattern with a signal frequency range of 10 MHz to 200 kHz. The device needs high precision with a very low ripple power supply to power the entire system. This TI Design requires 9- to 12-V DC at 250 mA with high precision and low ripple power. The 12-V DC voltage is generated using a Keithley triple output power supply (2230G). It is capable of generating up to 30 V with 0.03% voltage accuracy and 0.1% current accuracy with simultaneous voltage and current indication.

The data capturing is established using a USB 2.0 interface. The testing computer must have one USB port and must support USB 2.0 specification.

Sometimes, the signal source may also have noise on top of the signal while generating a sine wave with 100 kHz. To remove this unwanted noise, a 100-kHz differential band-pass filler is connected in between the signal source and the TIDA-01037 input connector. This filter will attenuate input noise at a 100-kHz band.

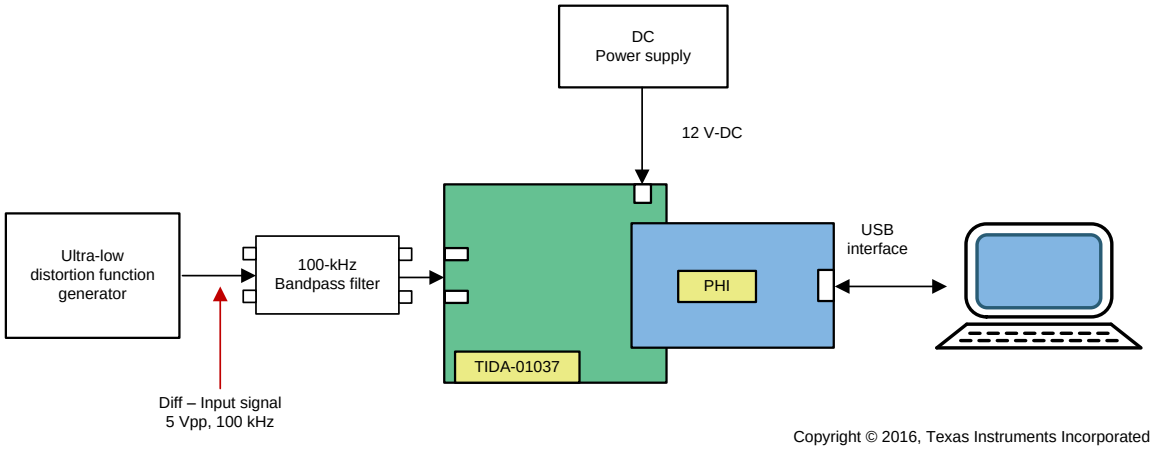


図 29. TIDA-01037 Test Setup

Install the PHI GUI software in the host computer before testing:

1. Plug the PHI interface board into the Samtec connector (J1).
2. Configure the operation mode using programmable resistor jumper (see 3.2.1).
3. Connect 12-V DC of power to the J5 connector. Ensure the positive terminal is connected to the positive input (Pin 2 of J5) and the negative terminal is connected to the negative input (Pin 1 of J5).
4. Connect the differential output of function generator to the differential input terminal (J8 and J9 SMA connector) of the TIDA-01037 board (for a 100-kHz input signal frequency, connect the 100-kHz band pass filter in between the signal source and the TIDA-01037 board). Also, make sure both differential signals are balanced and configured as shown in 図 29.
5. Connect the PHI module to the PC or laptop using a micro USB cable.
6. Switch on the power supply.
7. Switch on the signal source and set the signal source parameter. Then, enable the output.

8. Run the PHI GUI software, go to the spectrum analysis tab, and capture result (SNR, THD, and ENOB) with various input signal frequencies.
9. The test results taken for both 2-kHz and 100-kHz input frequency for both mode of operation as described in 3.2.1.

表 20. Signal Source Test Conditions

PARAMETER	VALUE
Pattern	Sine
Voltage	7.23 Vpp (adjust to cover full input dynamic range)
Frequency	2 kHz and 100 kHz
Source impedance	600 Ω
Power supply	12-V DC at 250 mA

The test results are taken for both 2-kHz and 100-kHz input frequency with and without jitter cleaner mode.

注:

1. While testing with a 100-kHz input signal frequency, a bandpass filter is used in between the signal source and the TIDA-01037 module.
2. Populated corresponding resistor jumper for with or without jitter mitigation mode.

4.2 Performance Test Results

Measured results for both 2-kHz and 100-kHz inputs are summarized in 表 21 and 図 30. These results are compared to ADS8900B data sheet which is used as an ideal performance goal. Measured results clearly indicate the benefits used both isolator families as part of a comprehensive solution. For example, the signal chain will realize nearly a 14-dB gain, 2.25-bit ENOB improvement when using both the ISO7340 and ISO7840 devices for a 100-kHz input signal. Furthermore, using the ADC multiSPI feature allows requires only a maximum clock of 45 MHz while still operating the ADS8900B at its maximum 1 MSPS sample rate.

表 21. Performance Test Result

PARAMETER	ADS8900B DATASHEET SPECIFICATION	TIDA-01037	
		ISO7840 ONLY SOLUTION	ISO7340 and ISO7840 SOLUTION
Fin (kHz) = 2			
SCLK (MHz)	45		
Sample rate (MSPS)	1		
SNR (dB)	104.00	100.72	101.12
THD (dB)	–125.00	–121.62	–122.60
ENOB	17.00	16.43	16.50
Fin (kHz) = 100			
SCLK (MHz)	45		
Sample rate (MSPS)	1		
SNR (dB)	99.50	83.70	97.37
THD (dB)	–110.00	–112.60	–113.00
ENOB	16.20	13.61	15.86

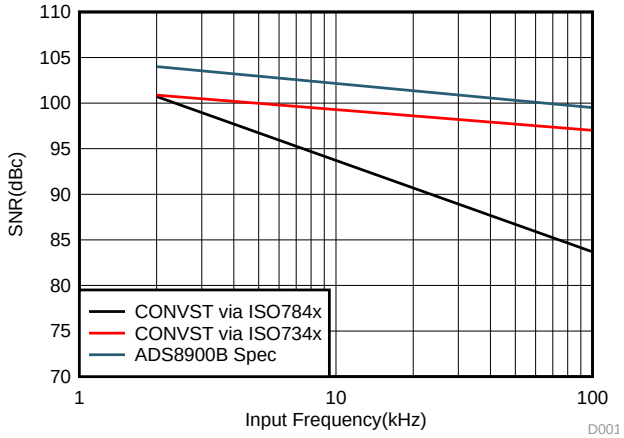


図 30. TIDA-01037 SNR Performance Graph

図 31. 2-kHz Spectrum—ISO7840 Only Solution

図 32. 2-kHz Spectrum—ISO7340 and ISO7840 Solution

図 33. 100-kHz Spectrum—ISO7840 Only Solution

図 34. 100-kHz Spectrum—ISO7340 and ISO7840 Solution

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01037.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01037.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01037.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01037.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01037.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01037.

6 Software Files

To download the software files, see the design files at TIDA-01037.

7 Related Documentation

1. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report (SLVA043)
2. Texas Instruments, *Fully-Differential Amplifiers*, Application Report (SLOA054)
3. Texas Instruments, *Op Amp Noise Theory and Applications*, Excerpted from *Op Amps for Everyone* (SLOA082)
4. Texas Instruments, *18-Bit, 2-MSPS Isolated Data Acquisition Reference Design for Maximum SNR and Sampling Rate*, TIDA-00732 Design Guide (TIDUB85)

7.1 商標

8 About the Authors

ANBU MANI is a systems engineer in the Industrial Systems Engineering team at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Anbu has fifteen years of experience in analog circuit design and digital circuit design for the Automatic Test Equipment in Modular platform. He is also engaged with the design and development of embedded products. Anbu earned his bachelor of engineering (BE) in electronic and communication from the Anna University, Chennai.

SANKAR SADASIVAM is a system architect in the Industrial Systems Engineering team at Texas Instruments, where he is responsible for architecting and developing reference design solutions for the industrial systems with a focus on Test and Measurement. Sankar brings to this role his extensive experience in analog, RF, wireless, signal processing, high-speed digital, and power electronics. Sankar earned his master of science (MS) in electrical engineering from the Indian Institute of Technology, Madras.

HARSH MISRA is a project trainee in the Industrial Systems Engineering team at Texas Instruments, where he is learning developing reference design solutions for the industrial systems with a focus on Test & Measurement. Harsh is a final-year student pursuing a bachelor of engineering (B.E. hons) in electrical and electronics engineering from Birla Institute of Technology & Sciences (BITS), Pilani.

リビジョンAの改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年12月発行のものから更新 **Page**

- 現行のスタイルガイドに合わせた表現と画像に 変更 1

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。