参考資料

TI Designs: TIDA-01480
Xilinx® Zynq® UltraScale+™ ZU2CG–ZU5EV MPSoC用の統合電源のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、Xilinx® Zynq® UltraScale+™ (ZU+)ファミリのMPSoCデバイスに電力を供給するように設計された、スケーラブルな電源です。このデザインは、標準のDC電源から電力を受け取り、適切に定義されたSamtecソケット端子ストリップ接続により、Xilinxチップセットと DDRメモリのすべてのレールに電力を供給します。このスケーラブルなデザインは、デュアル・コア Arm® Cortex®-A53アプリケーション・プロセッサとデュアル・コア Arm Cortex-R5リアルタイム・プロセッサを持つ、最も基本的なZU2CGデバイスから、グラフィック処理(GPU)を追加したZUxEG製品、さらにビデオ・コーデックと最大16個の16.3Gbpsトランシーバ(MGTH)を含むZU5EVデバイスまで、幅広く対応できます。

リソース

TIDA-01480	デザイン・フォルダ
TPS65023	プロダクト・フォルダ
TPS56C215および TPS568215	プロダクト・フォルダ
TPS62067	プロダクト・フォルダ
TPS51200	プロダクト・フォルダ

TI E2E™ Community

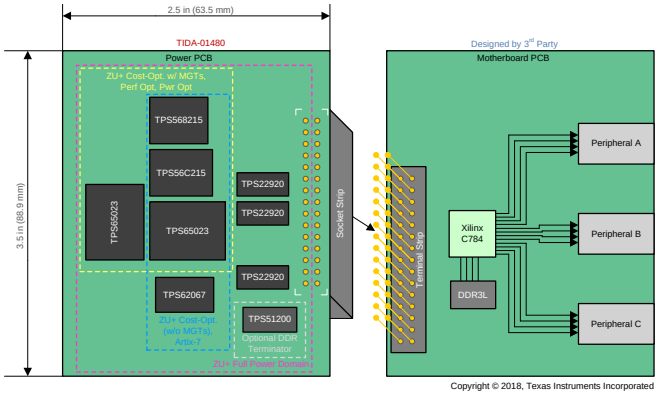
E2E™エキスパートに質問

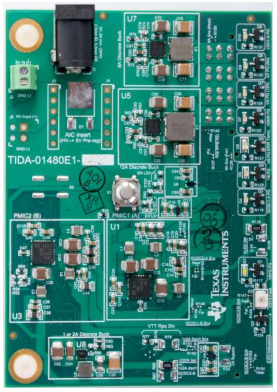
特長

- 17のハードウェア構成可能な電源レール
  - 9つの降圧コンバータ、4つのLDO、3つの負荷スイッチ、1つのDDRターミネータ
- すべての出力電圧をハードウェアで簡単に変更可能
  - ソフトウェアやカスタムEEPROM/OTPは不要
- 必要な入力電圧は5V、6A (30W)の1つのみ
- 次のXilinx製品に理想的な電源:
  - Zynq Ultrascale+ MPSoC (ZU2CG、ZU3CG、ZU4CG、ZU5CG、ZU2EG、ZU3EG、ZU4EG、ZU5EG、ZU4EV、ZU5EV)
- プロトタイピング・ツールとして使用するための、小型の3.5インチ×2.5インチのPCB

アプリケーション

- 産業用 - ファクトリ・オートメーションおよび制御
  - プログラマブル・ロジック・コントローラ(PLC): CPU (PLCコントローラ)
  - マシン・ビジョン: ビジョン・コンピュータ
  - 産業用ロボット: CPU基板
- 産業用 - 医療、保健、フィットネス
  - イメージング: 超音波スキャナ
- 車載用 - 先進運転支援システム
  - ADASカメラ: サラウンド・ビューのECU





1 System Description

This reference design is intended to be used as a prototyping tool for developing innovative applications using the Xilinx Zynq Ultrascale+ (ZU+) MPSoC devices. The 10 ZU+ products that can be powered from this reference design, ZU2CG-ZU5EV, are all available in a C784 package (784-pin, 28 rows by 28 columns of pins, 23 mm × 23 mm, 0.8-mm pitch BGA).

Prior to Xilinx developing the ZU+ MPSoC, the ability to manufacture SoCs combining multi-core processors and FPGAs was limited to companies with a lot of money to invest in product development. The Xilinx ZU+ MPSoCs significantly reduces this monetary barrier to entry and a wide variety of designers benefit as a result. Although the cost of MPSoCs has reduced, it can be difficult to design a PCB with a device having a large number of pins. The power supply is not the highest priority, but a reliable power supply is important to release a final product to market.

The flexibility of the Xilinx ZU+ devices can be overwhelming to a designer who wants to develop rapid prototypes of new products. This reference design is designed specifically to solve the problem of designing a power supply for the flexible yet complex ZU+ devices. Board designers can focus on routing critical high-speed data and peripheral connections to the ZU+ MPSoC and let this reference design resolve concerns related to power supply design for the many required rails of the ZU+ MPSoC. The board on which the Xilinx ZU+ device is mounted, or the *motherboard*, simply needs to use the specified Samtec connectors and the designer can wire his or her PCB using Xilinx terminology. The designer can combine this reference design with their newly designed Xilinx ZU+ motherboard prototype, plug in an AC/DC (5 V, 6 A out) adapter to the barrel jack of this reference design, and begin testing.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER(1)	SPECIFICATIONS	DETAILS
Input power source	DC 5 V, 6 A (30 W); applied by a 2.5-mm ID, 5.5-mm OD barrel jack or screw terminals	YU0506 (3.1)
VCCINT(2), VCCINT_IO(3), VCCBRAM(3)	0.85 V/0.9 V, ±3%, ≤ 9.1 A	TPS56C215 (2.3.2)
VPS_MGTRAVCC	0.85 V, ±3 %, 300 mA	Third TPS22920 load switch (2.3.4)
VCC_PSINTFP, VCC_PSINTFP_DDR	0.9 V, ±5%, up to 5.75 A	TPS568215 (2.3.2)
VCCINT_VCU(3)	0.9 V, ±3%, 3 A	TPS54318
VCCO_PSDDR,VDD(4), VDDQ(4)	1.1 V to 1.5 V (user-defined), ±V_{DRR}%, > 500 mA	TPS62067 (2.3.3)
VMGTAVTT (GTH), VMGTAVTT (GTY), VCC_VCU_PLL(3)	1.2 V, ±3%, up to 1.35 A	First TPS65023 DCDC1 (2.3.1)
VCC_PSPLL	1.2 V, ±3%, 100 mA	First TPS22920 load switch (2.3.4)
VCC_PSAUX, VCC_PSADC	1.8 V, ±5%, 520 mA	First TPS65023 DCDC2 (2.3.1)
VCCO_PSIO[3..0]	User-defined; shown combined as 1.8 V to 3.3 V, ±5%, 100 mA × 4	First TPS65023 DCDC3 (2.3.1)
VCC_PSDDR_PLL	1.8 V, ±5%, 100 mA	First TPS65023 LDO1 (2.3.1)
VMGTAVCC (GTH), VMGTAVCC (GTY)	0.9 V, ±3%, 1.3 A	Second TPS65023 DCDC1 (2.3.1)
VCCAUX, VCCAUX_IO, VCCADC	1.8 V, ±3%, 820 mA	Second TPS65023 DCDC2 (2.3.1)
VMGTVCCAUX (GTH), VMGVCCAUX (GTY)	1.8 V, ±3%, 100 mA	Second TPS22920 load switch (2.3.4)
VCC_PSINTLP	0.85 V, ±5%, 400 mA	Second TPS65023 DCDC3 (2.3.1)
VPS_MGTRAVTT	1.8 V, ±3%, 100 mA	Second TPS65023 LDO1 (2.3.1)
HDIO VCCO	1.2 V to 3.3 V (user-defined), ±3 %, ≤ 500 mA	Multiple options

(1) Parameters are listed for Variant 005. All other variants combine rails together or do not require certain rails.
(2) VCCINT can also operate when provided a 0.72-V power rail, as shown in 2.1.4.
(3) This parameter is an independent rail for some Xilinx product variants depending on the feature set used in the application.
(4) VDD and VDDQ are common names for the primary DDR memory power supply and not connections on the Xilinx device.

表 1. Key System Specifications (continued)

PARAMETER[1]	SPECIFICATIONS	DETAILS
HPIO VCCO	1 V to 1.8 V (user-defined), ±3 %, ≤ 500 mA	Multiple options
VTT, VREFCA (VDDQ/2)	Mid-rail reference voltage for DDR memory	TPS51200 (2.3.5)
Operating temperature	–40°C to +85°C	2.3
Solution size (area)[5]	Variant 001: 1.337 in^2 (863 mm^2); Variant 005: 1.894 in^2 (1222 mm^2)	2.1.5
Form factor (x-y dimensions)	2.5 in × 3.5 in (63.5 mm × 88.9 mm) PCB	2.2

(5) A DDR terminator is optional and a voltage divider can be substituted depending on the DDR memory IC used. The TPS51200 is not included in solution size measurements.

2 System Overview

2.1 Block Diagrams

There are five (5) assembly variants of this reference design. The variants of this reference design are intended to power the Zynq UltraScale+ family and are named according to the desired optimization of the ZU+ device and whether or not the multi-Gigabit transceivers (MGTs) are used. The names used for these board variants are consistent with Xilinx nomenclature. For additional information, refer to the Xilinx references in 5.

2.1.1 Variant 001: Always-On, Cost-Optimized (No MGTs)

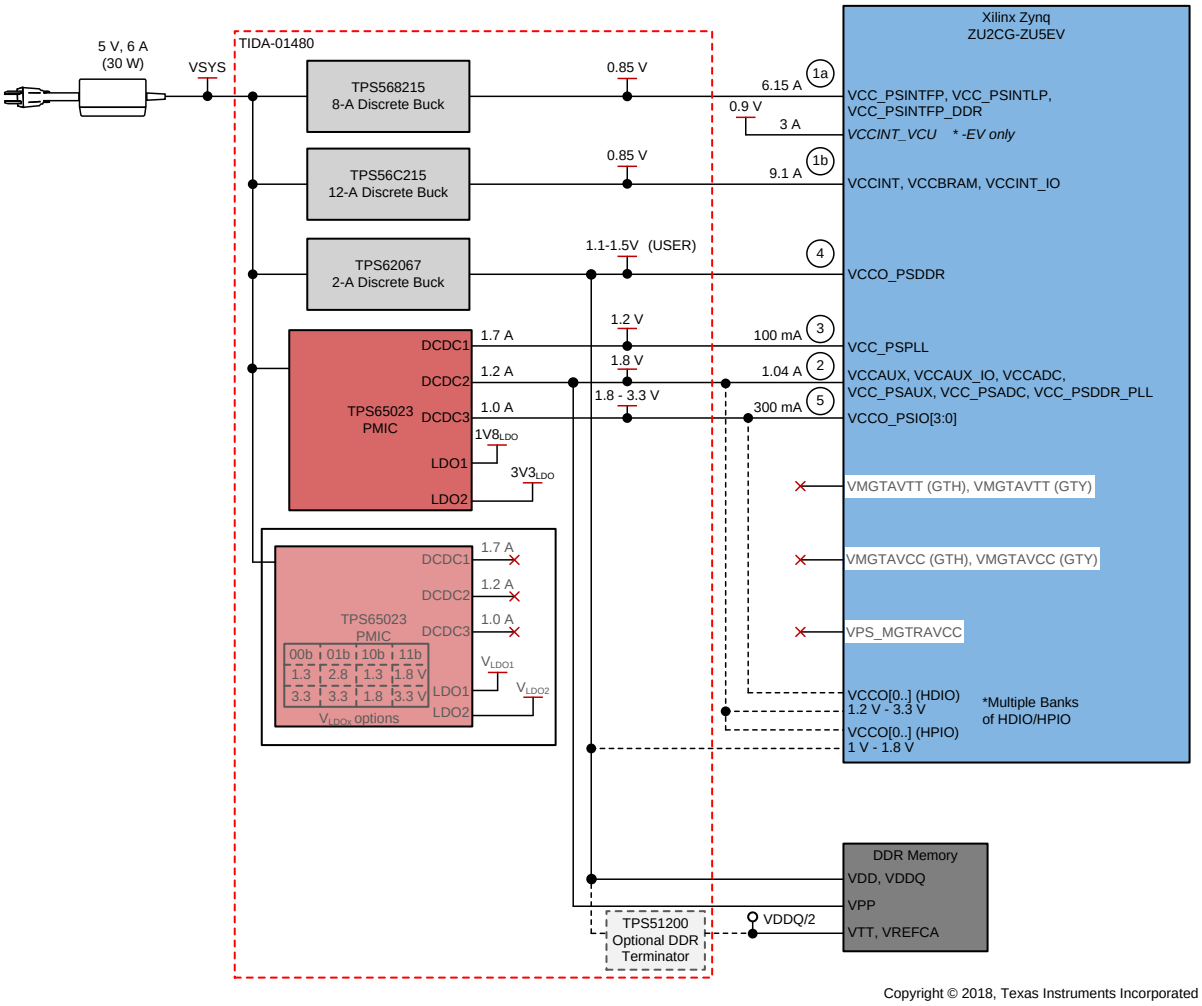


図 1. Block Diagram of Design Variant 001

Notes about Variant 001:

- Use case titled *Always On: Cost-Optimized with Only Five Power Regulators (CG or EG Devices)* in Xilinx document UG583.
- The second TPS65023 PMIC is not required in this reference design.
- Xilinx power rails containing *VMGT* refer to the MGTs and are not used in this assembly variant of the reference design.

- When -EV Xilinx devices are used, VCCINT_VCU requires a separate, dedicated 0.9-V supply. The TPS54318 (3-A discrete buck) can be added to the design to support VCCINT_VCU.
- Solution size = 1.337 in^2 (863 mm^2)

2.1.2 Variant 002: Always-On Cost-Optimized (With MGTs)

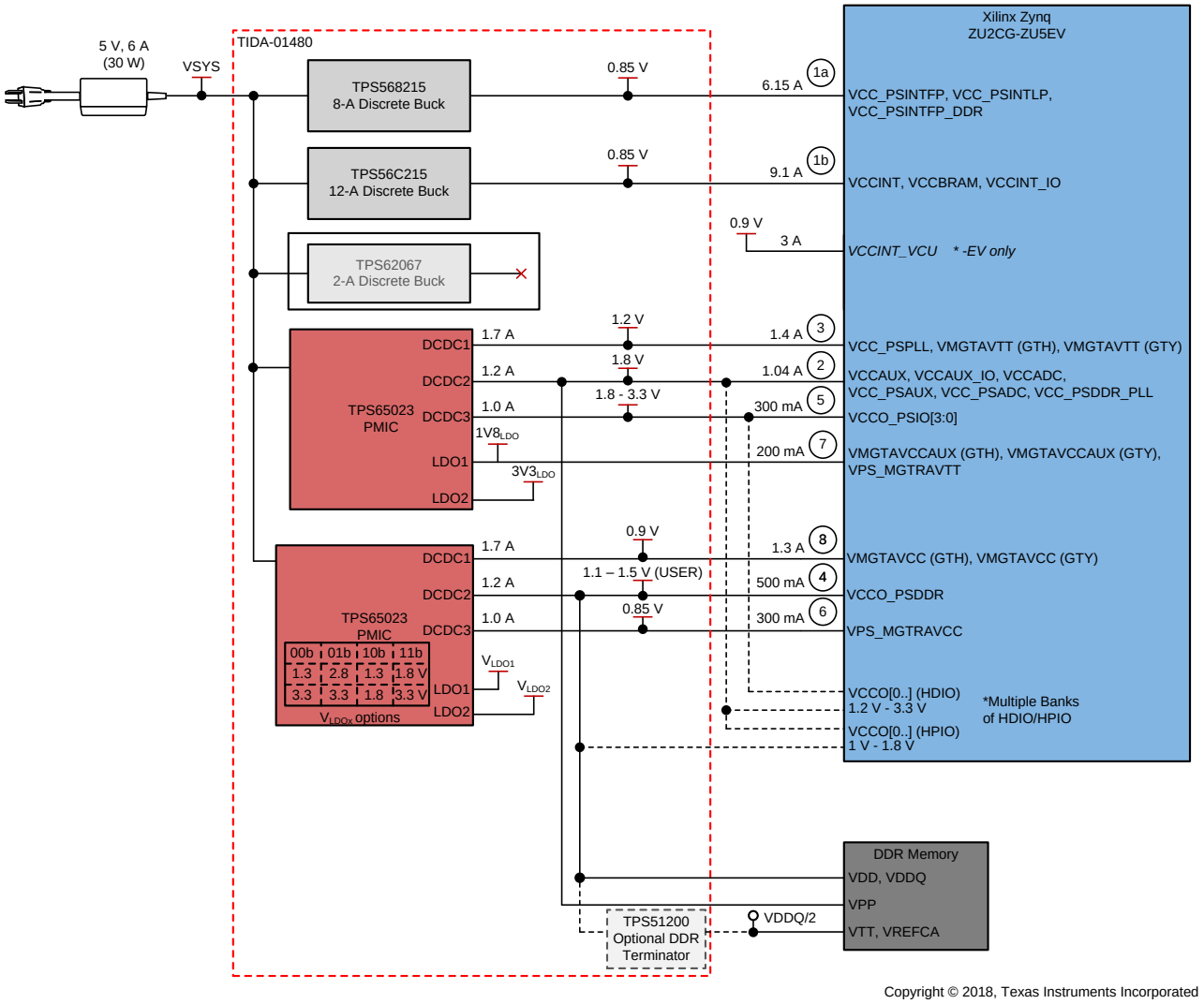


図 2. Block Diagram of Design Variant 002

Notes about Variant 002:

- Use case titled *Always On: Cost-Optimized Power Rail Consolidation* in Xilinx document UG583.
- The second TPS65023 PMIC is added in this variant of the reference design. If the *VCCO_PSDDR* Xilinx rail current added to the DDR Memory current requirements are less than 1.2 A, then the TPS62067 can be omitted from this design. In this case, the power rail named *VCCAUX* would alternately be wired to *VCCO_PSDDR* on the Xilinx motherboard.
- Xilinx power rails containing *VMGT* refer to the MGTs and are added in this variant of the reference design.
- When -EV Xilinx devices are used, VCCINT_VCU requires a separate, dedicated 0.9-V supply. The

TPS54318 (3-A discrete buck) can be added to the design to support VCCINT_VCU.

- Solution size = 1.614 in^2 (1041 mm^2)

2.1.3 Variant 003: PL Performance-Optimized (Rail Consolidation)

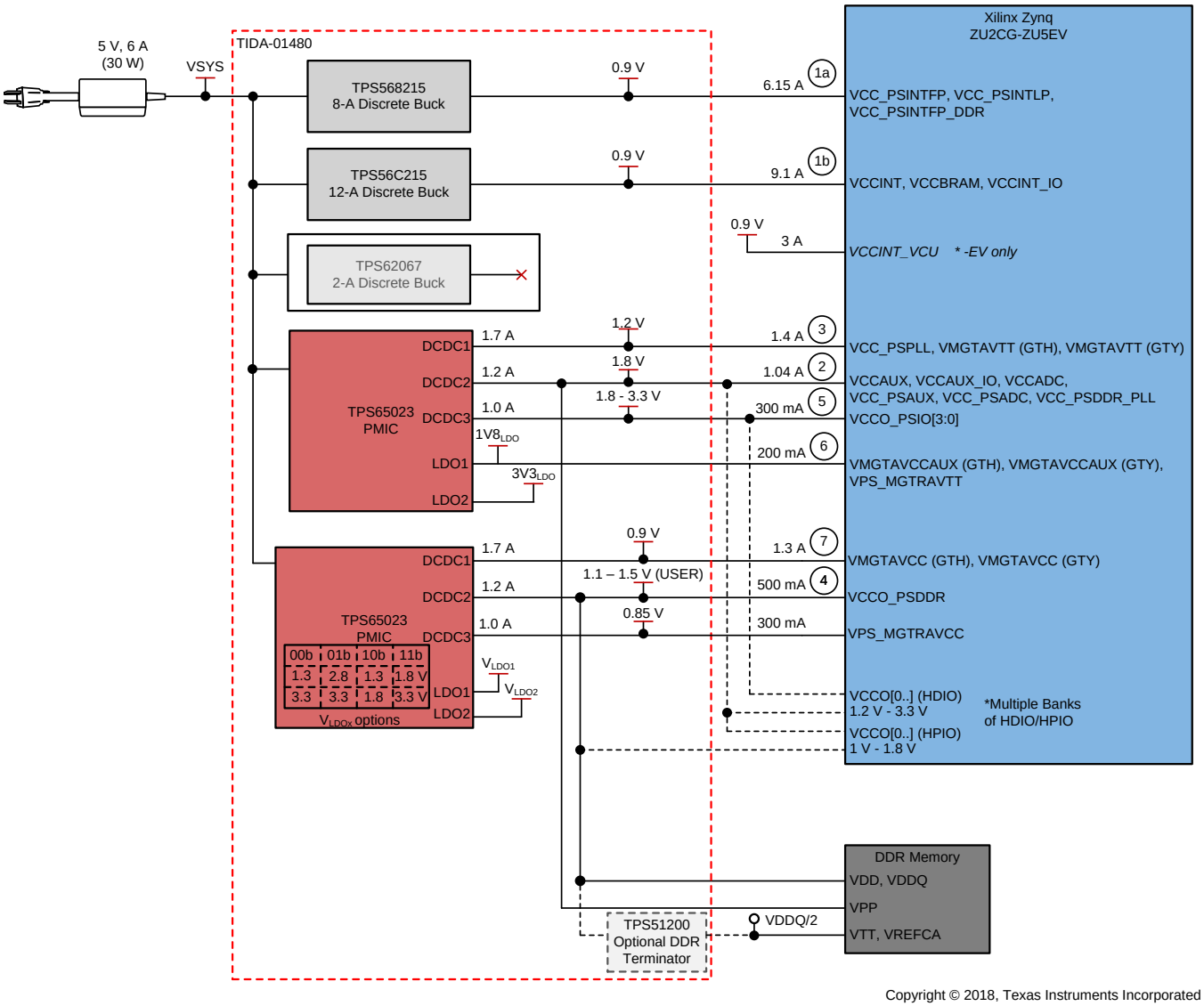


図 3. Block Diagram of Design Variant 003

Notes about Variant 003:

- Use case titled *Always On: PL Performance-Optimized Rail Consolidation* in Xilinx document UG583.
- The number of power rails in this variant of the reference design is consolidated for performance optimization. If the DDR memory does not require a DDR terminator to sink and source current from the VTT (VDDQ/2) reference node, then the TPS51200 can be omitted from this design. In this case, the rail named *VCC_PSINTLP* would alternately be wired to *VCCO_PSDDR* on the Xilinx motherboard.
- When -EV Xilinx devices are used, VCCINT_VCU requires a separate, dedicated 0.9-V supply. The TPS54318 (3-A discrete buck) can be added to the design to support VCCINT_VCU.
- Solution size = 1.614 in^2 (1041 mm^2)

2.1.4 Variant 004: Always-On, Power-Efficiency Optimized

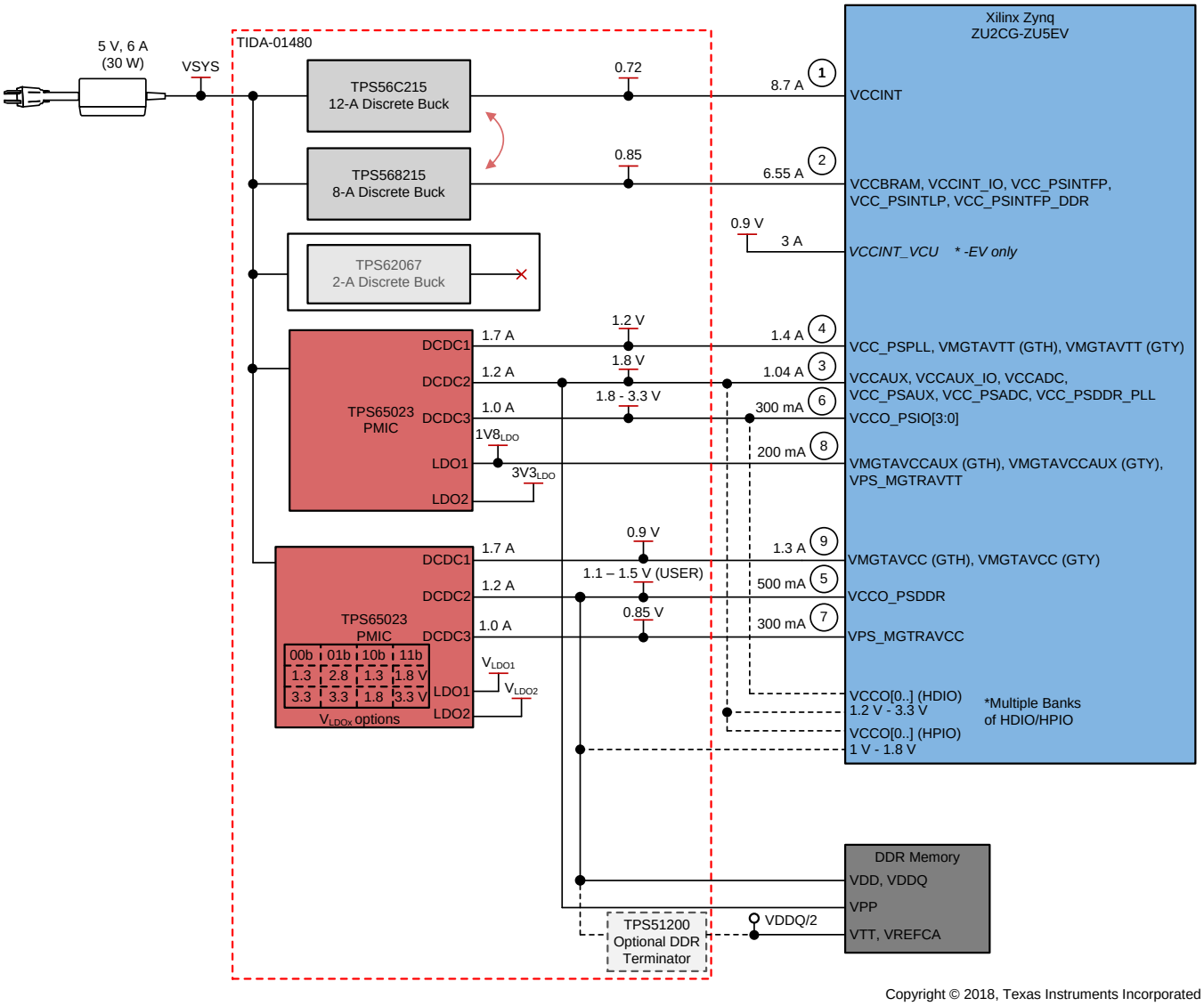


図 4. Block Diagram of Design Variant 004

Notes about Variant 004:

- Use case titled *Always On: Power and/or Efficiency-Optimized Power Rail Consolidation for Low-Power Devices* in Xilinx document UG583.
- Similarly to Variant 002, the second TPS65023 PMIC is added in this variant of the reference design. If the *VCCO_PSDDR* Xilinx rail combined with the DDR Memory current requirements are less than 1.2 A, then the TPS62067 can be omitted from this design. In this case, the power rail named *VCCAUX* would alternately be wired to *VCCO_PSDDR* on the Xilinx motherboard.
- When power-efficiency is optimized, the lowest voltage is used for each rail.
- When -EV Xilinx devices are used, VCCINT_VCU requires a separate, dedicated 0.9-V supply. The TPS54318 (3-A discrete buck) can be added to the design to support VCCINT_VCU.
- Solution size = 1.614 in^2 (1041 mm^2)

2.1.5 Variant 005: Full Power Domain

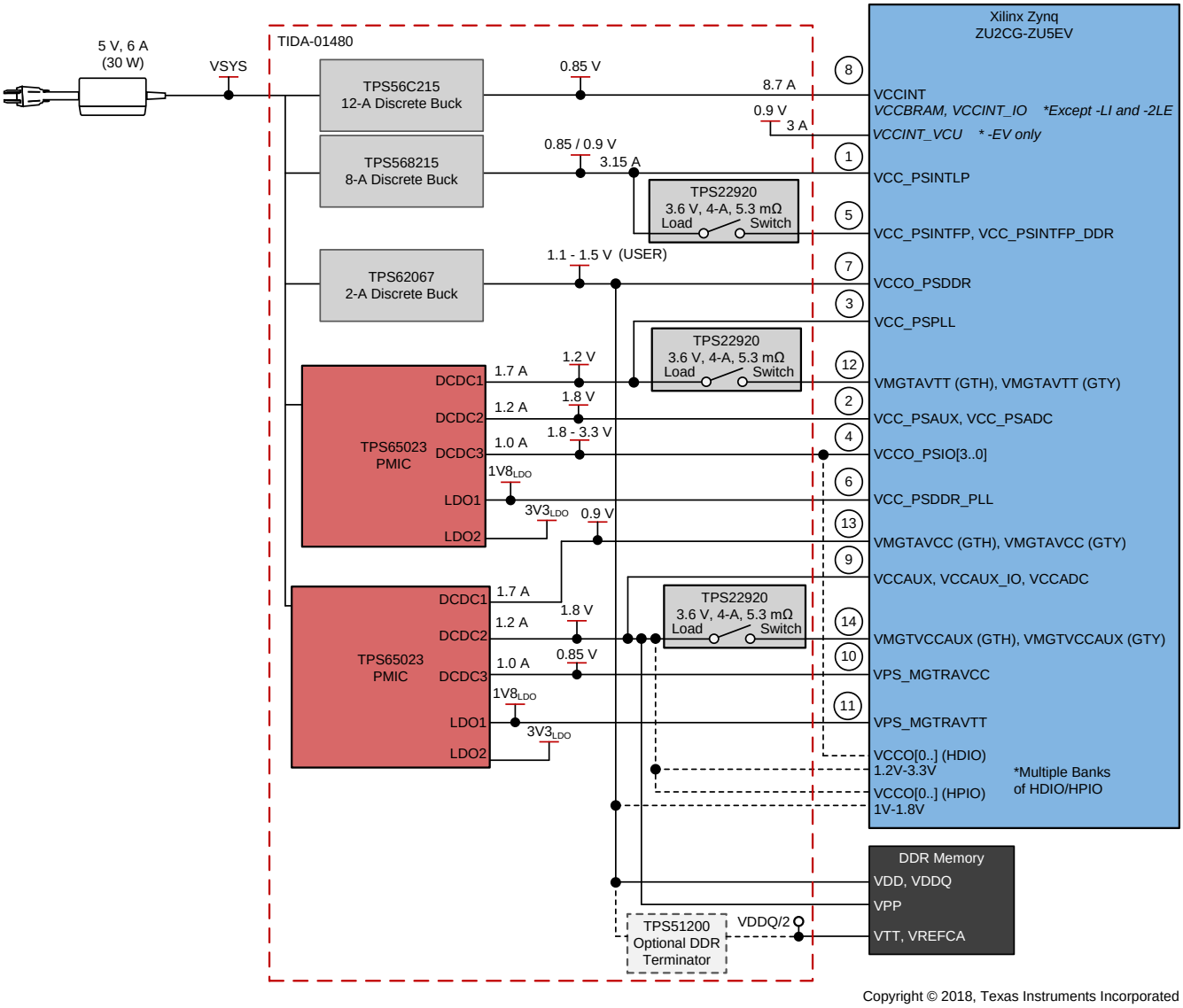


図 5. Block Diagram of Design Variant 005

Notes about Variant 005:

- Use case titled *Full Power Domain Flexibility Consolidation* in Xilinx document UG583.
- All Xilinx power rails are wired individually, and all components are assembled in this variant of the reference design. As a result, this variant is the standard assembly of this reference design, and all other variants can be derived from this version by removing components from the PCB.
- Rail 14 for VMGTVCCAUX (GTH and GTY) may require additional filtering to meet the 3% tolerance requirement because rail 9 for VCCAUX, VCCAUX_IO, and VCCADC are less sensitive and only require 5% tolerance
- When -EV Xilinx devices are used, VCCINT_VCU requires a separate, dedicated 0.9-V supply. The TPS54318 (3-A discrete buck) can be added to the design to support VCCINT_VCU.
- Solution size = 1.894 in^2 (1222 mm^2)

2.2 Design Considerations

This reference design is intended to be used during the prototyping phase for any application of a Zynq UltraScale+ ZU2CG-ZU5EV device. To begin prototyping, first select the part in the Zynq family of devices that meets the needs of the application. The next step is to design a motherboard PCB containing the Xilinx MPSoC and the correct Samtec connectors to mate with this reference design. When the motherboard PCB is built, connect the two boards through the Samtec connectors and apply a barrel jack to this reference design to use it as a power supply for the motherboard. Refer to 3.1 for more details on the Samtec connectors.

Although intended for prototyping, the overall solution size can be critical for designers. As a result, the entire reference design (including power devices, passive components, connectors, and indicator LEDs) fits on a 3.5 in × 2.5 in PCB. The design is scalable to meet the needs of a variety of Xilinx power profiles; as a result, close attention is paid to silkscreen labeling, highlighting the area used by each device block, and top-side placement of critical power components.

For the solution size of each variant, refer to 2.1.

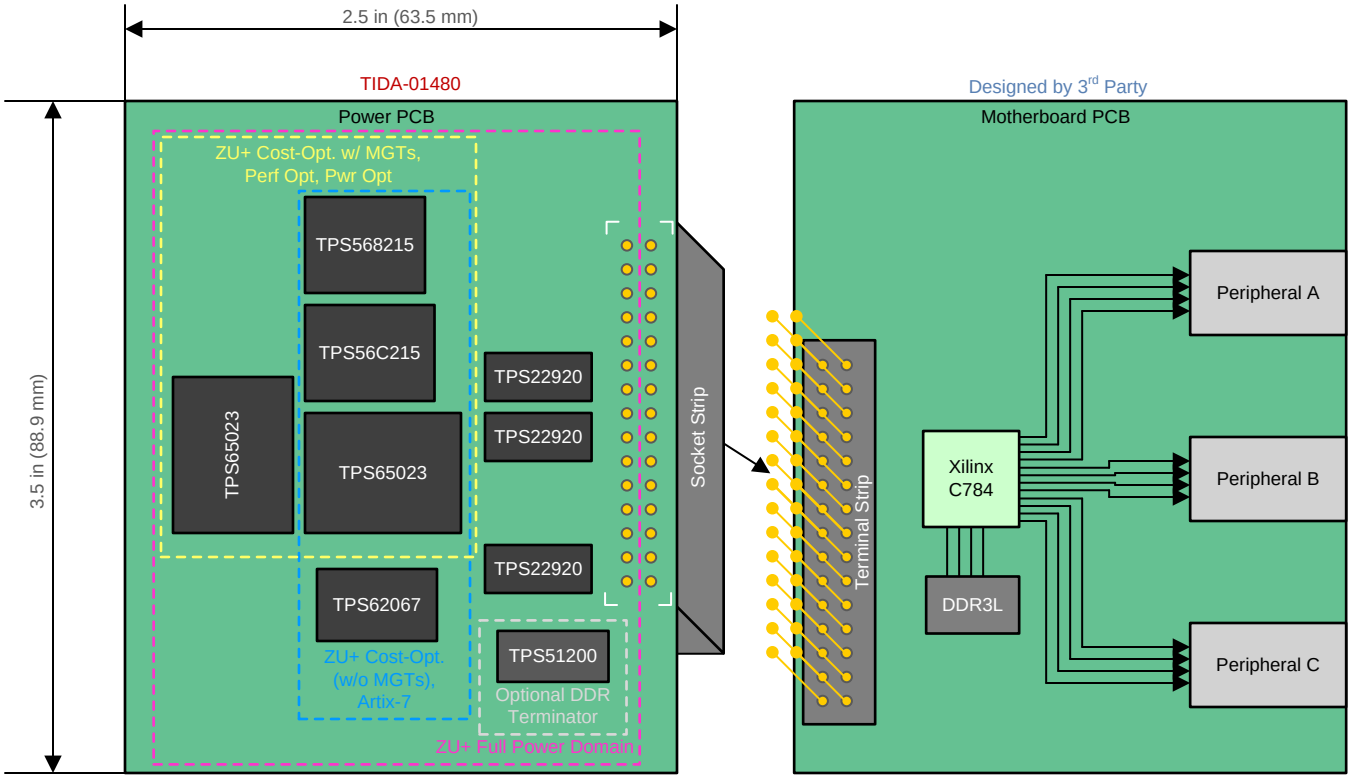


図 6. TIDA-01480 Form Factor Conceptual Drawing

2.3 Highlighted Products

2.3.1 TPS65023

The TPS65023 device is an integrated power management device for applications that require multiple power rails (see 図 7). The TPS65023 provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O, and memory rails in a processor-based system. The core converter allows for on-the-fly voltage changes through a serial interface, allowing the system to implement dynamic power savings. All three step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents.

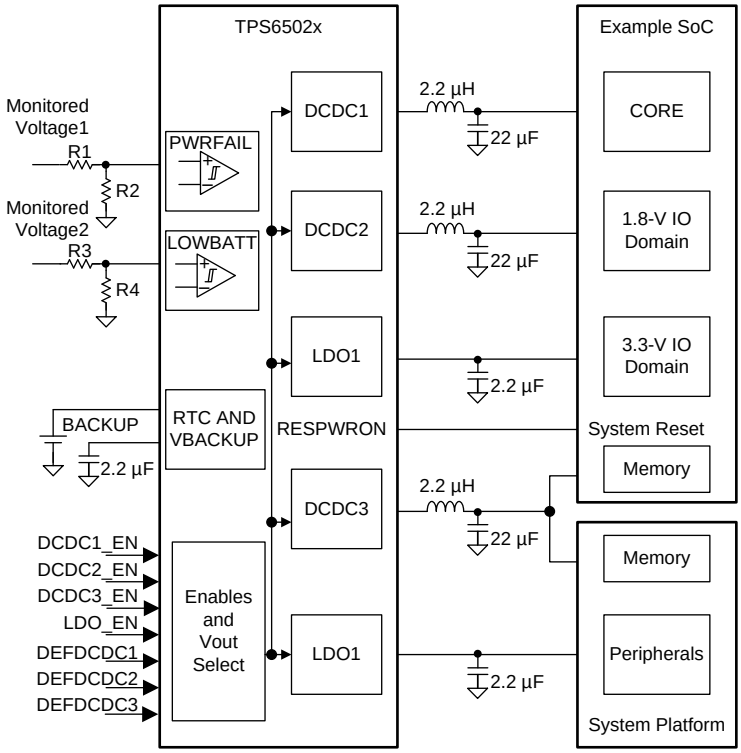


図 7. TPS65023 Simplified Application Circuit

The TPS65023 is chosen for this reference design because it is a densely integrated power management device that provides a high number of power rails in a small package, which is critical to achieve the desired solution size. The Xilinx ZU+ MPSoCs are flexible and can be used in a variety of applications, and the TPS65023 output voltages can be set in hardware for scalability and flexibility in the power supply.

This reference design uses the B revision of the TPS65023, TPS65023B, for its improved I^2C performance over the previous version of the device.

For automotive applications requiring AEC-Q100 qualification, consider using the TPS65023-Q1 in the assembly of this design.

For more relevant information on this device, see *TPS65023x Power Management IC for Li-Ion and Li-Polymer Powered Systems* .

2.3.2 TPS56C215 and TPS568215

The TPS56C215 is TI's smallest monolithic, 12-A synchronous buck converter with an adaptive on-time D-CAP3™ Control Mode (see 図 8). The device integrates low $R_{DS(on)}$ power MOSFETs that enable high efficiency and offer ease-of-use with a minimum external component count for space-conscious power systems. Competitive features include a very accurate reference voltage, fast load transient response, auto-skip mode operation for light load efficiency, adjustable current limit, and no requirement for external compensation. A forced continuous conduction mode helps meet tight voltage regulation accuracy requirements for performance DSPs and FPGAs. The TPS56C215 is available in a thermally enhanced 18-pin HotRod™ QFN package.

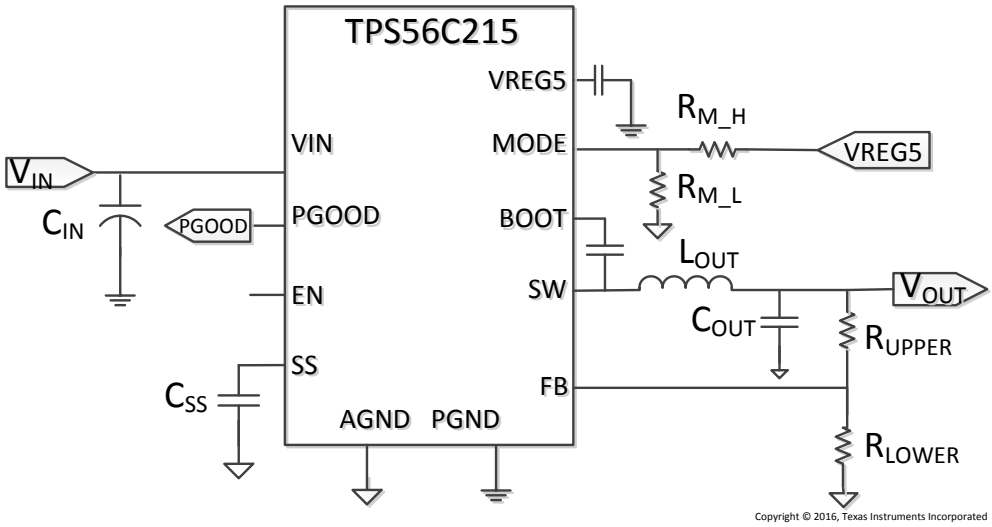


図 8. TPS56C215 Simplified Application Circuit

The TPS56C215 is chosen for this design to deliver high current (up to 12 A) to the core rail of the Xilinx ZU+ MPSoC. The core rail, VCCINT, requires up to 8.7 A of current for the ZU5xx variant. When a ZU2xx-ZU4xx Xilinx variant is used, two TPS568215 devices can be used instead to reduce overall cost. The end designer can use any combination of one or two TPS5x215 devices required to meet the current needs of the application because the two buck converters are pin-to-pin equivalent.

The *C* in TPS56C215 is hexadecimal notation, where 0xC converts to decimal 12, meaning that the TPS56C215 is rated for up to 12 A of current at the output. The TPS568215 has an identical simplified application circuit, and the TPS568215 data sheet indicates that this device rated for up to 8 A of current at the output. The circuitry for both devices in this reference design is the same, except that the TPS56C215 requires a physically larger inductor for lower DC resistance and a higher rated current capability. As a result, only the device designated as U5 on this reference design can deliver up to 12 A of continuous current.

For more relevant information on this device, see *TPS56C215 4.5-V to 17-V Input , 12-A Synchronous Step-Down SWIFT™ Converter* .

2.3.3 TPS62067

The TPS62067 is a highly efficient, synchronous step-down DC/DC converter (see 図 9). This device provides up to 2 A of output current. With an input voltage range of 2.9 V to 6 V, the device is a perfect fit for power conversion from a 5-V or 3.3-V system supply rail. The TPS62067 operates at a 3-MHz fixed frequency and enters power save mode operation at light load currents to maintain high efficiency over the entire load current range. The power save mode is optimized for low output voltage ripple. The TPS62067 provides an open drain power good output. The TPS62067 converter is optimized for operation with a tiny 1-µH inductor and a small 10-µF output capacitor to achieve smallest solution size and high regulation performance.

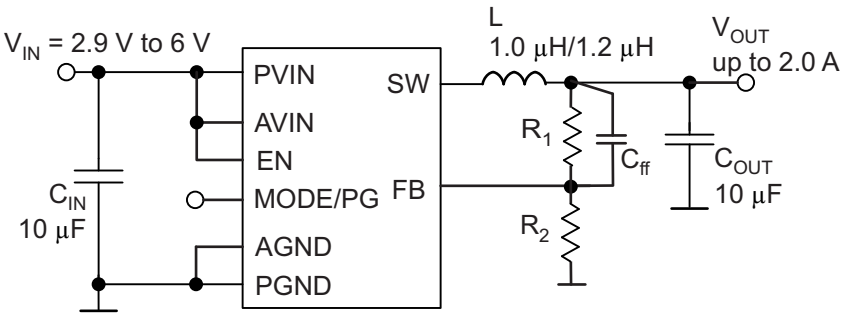


図 9. TPS62067 Simplified Application Circuit

Certain applications of the Xilinx ZU+ MPSoCs require an additional dedicated rail to provide power to DDR memory's VDD (VDDQ) power input. For these applications, the TPS62067 is chosen to supply up to 2 A of current with a hardware-configurable output voltage to support DDR2, LP-DDR2, DDR3, LP-DDR3, or DDR4. The default assembly of this reference design sets this voltage to 1.35 V for LP-DDR3.

For automotive applications requiring AEC-Q100 qualification, consider using the TPS62067-Q1 in the assembly of this design.

The TPS62067 features the power-good (PG) output function on pin 6 and is used in this reference design. To use the MODE function (input) on pin 6 to force PWM at a fixed switching frequency (instead of the PG ability), use the TPS62065 and modify the schematic accordingly to change the wiring of the PG output to an input for MODE selection. The AEC-Q100 automotive qualified version of this device, TPS62065-Q1, is also available.

For more relevant information on this device, see *TPS6206x 3-MHz, 2-A, Step-Down Converter in 2-mm × 2-mm SON Package* .

2.3.4 TPS22920

The TPS22920 is a small, space-saving load switch with controlled turn-on to reduce inrush current (see 図 10). The device contains a N-channel MOSFET that can operate over an input voltage range of 0.75 V to 3.6 V and switch currents up to 4 A. An integrated charge pump biases the NMOS switch to achieve a minimum switch ON resistance (R_{ON}). The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. The TPS22920 has a 1250-Ω on-chip resistor for quick output discharge when the switch is turned off, which ensures that the output is not left floating. The TPS22920 has an internally controlled rise time to reduce inrush current. The TPS22920 is available in an ultra-small, space-saving 8-pin CSP package.

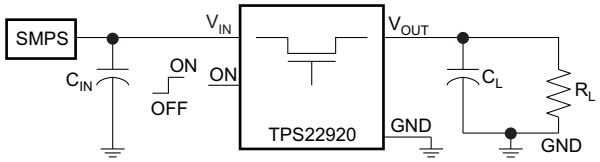


図 10. TPS22920 Simplified Application Circuit

This device is chosen for this reference design for two reasons:

1. It is tiny—smaller than the 0603 capacitors at the input and output used in this design.
2. Less wiring—the integrated charge pump means the 5-V system input voltage does not need to be routed to a secondary bias input of the load switch.

For automotive applications requiring AEC-Q100 qualification, consider using the TPS22965-Q1 in a modified version of this reference design. The TPS22965-Q1 is not pin-to-pin compatible with the TPS22920 because the small Die-Size Ball Grid Array (DSBGA) package used for the TPS22920 is not commonly used in automotive applications.

For more relevant information on this device, see *TPS22920x 3.6-V, 4-A, 5.3-mΩ On-Resistance, Integrated Load Switch with Controlled Turn-on* .

2.3.5 TPS51200

The TPS51200 device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space is a key consideration (see 図 11). The TPS51200 maintains a fast transient response and requires a minimum output capacitance of only 20 µF. The TPS51200 supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT bus termination. In addition, the TPS51200 provides an open-drain PGOOD signal to monitor the output regulation and an EN signal that can be used to discharge VTT during S3 (suspend to RAM) for DDR applications.

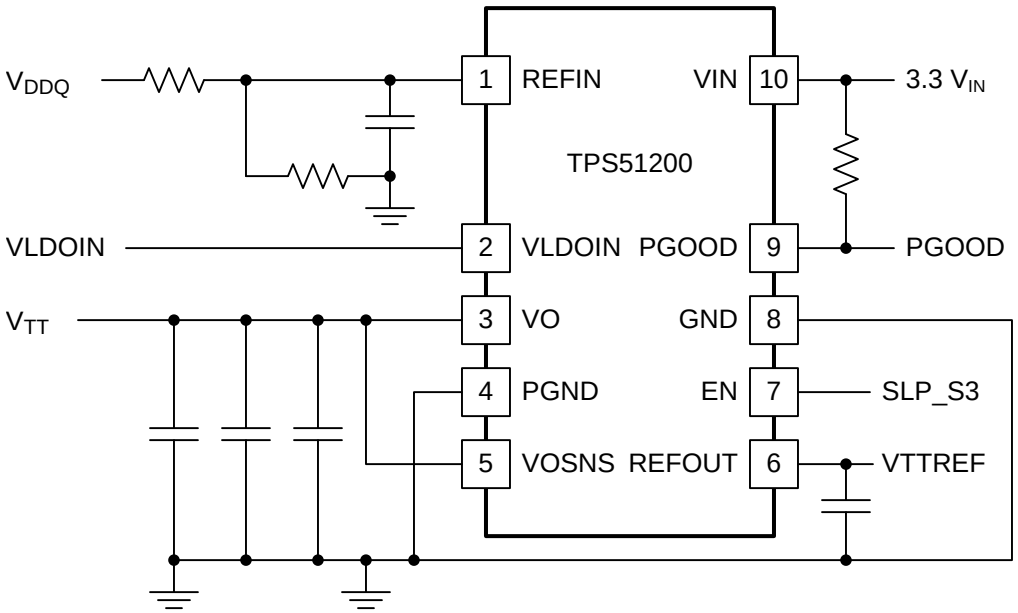


図 11. TPS51200 Simplified DDR Application Circuit

If a DDR terminator is required by the application, the TPS51200 is used in the reference design because it simply and reliably produces an output voltage at the VO pin (V_{TT} node) that is equal to the voltage at the REFIN pin (half of the voltage labeled VDDQ) by either sinking or sourcing current into the V_{TT} node.

For more relevant information on this device, see *TPS51200 Sink and Source DDR Termination Regulator* .

2.4 System Design Theory

2.4.1 Buck Converter Output Voltages

All DC/DC buck converters set the output voltage using the same principle. A resistor divider is connected from the output voltage to GND, and the center node of the two resistors is connected to the feedback pin of the converter. Although the name of the feedback pin and the terminology for its voltage can differ from device to device, the same general equation is used to set the voltage for all of the buck converters in this reference design.

The feedback voltage (commonly referred to as V_{FB} or V_{REF}) is a constant for each buck converter and can easily be found in the data sheet for that device. For the TPS65023, the feedback voltage for the DC/DC buck converters is called $V_{DEFDCDCx}$. V_{OUT} is the desired output voltage for the buck converter. Generally speaking, R_2 is selected first and is treated as a constant to solve for R_1 using 式 1.

$$R1 = R2 \times VOUTVFB - R2 \quad (1)$$

After two resistors are selected from the component library and placed in the schematic, the output voltage can be calculated using 式 2 to ensure the voltage is within the desired supply voltage range.

$$VOUT = VFB \times R1 + R2R2 \quad (2)$$

図 12 shows an example of how to set the output voltage for DCDC3 of the TPS65023 using an external resistor divider. This example is shown because wiring the TPS65023 is the most complex in this reference design and the same theory is used for all buck converters.

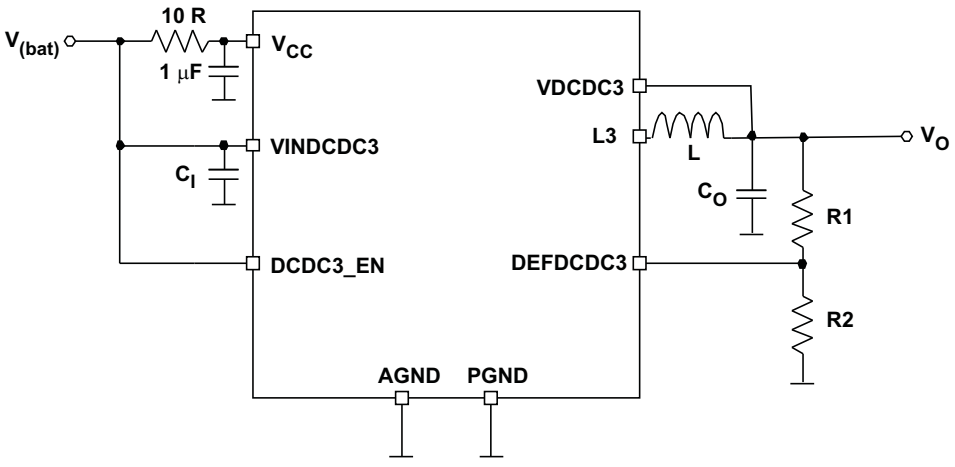


図 12. TPS65023 External Resistor Divider for DCDC3

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

The only hardware required to power on this reference design at full load is a DC power supply capable of delivering 5 V at a current of at least 6 A. The simplest way to apply this power is by connecting a barrel jack plug of an AC/DC adapter into the receptacle J1 with an inner diameter (ID) of 2.5 mm and an outer diameter (OD) of 5.5 mm, where the internal *tip* has positive (+) polarity and the external *sleeve* has negative (–) polarity. An AC/DC adapter with generic part number *YU0506* is commonly available and meets these requirements.

If an AC/DC adapter meeting these specific requirements is not available, a DC power supply in a lab can be connected to screw terminal J2 by connecting the "+" terminal to pin 1, labeled *5V IN*, and the "-" terminal to pin 2, labeled *GND*.

When the design is used for prototyping an application of the Xilinx Zynq UltraScale+ MPSoC, the mating Samtec connectors for J6 and J7 must be used and must be mounted with relative positions to each other matching the placement of J6 and J7 on the bottom of this board.

- J6 (MPS-04-7.70-01-L-V) mates with MPT-04-6.30-01-L-V:
  - Pin 1 of J6 has X,Y coordinates of 1900 mil, 2472 mil (48.26 mm, 62.789 mm)
- J7 (BSE-060-01-L-D-A) mates with BTE-060-09-L-D-A:
  - Pin 1 of J7 has X,Y coordinates of 1944.25 mil, 197 mil (49.383 mm, 5.004 mm)

The distance from the center of pin 1 on J6 to the center of pin 1 on J7 is +44.74 mil (1.136 mm) horizontally on the X-axis and –2275 mil (57.785 mm) vertically on the Y-axis.

3.2 Testing and Results

3.2.1 Test Setup

A handheld digital multimeter measures the DC output voltages of each power rail output provided by this reference design. 図 13 shows the setup for this test and highlights the measurement locations probed with the multimeter.

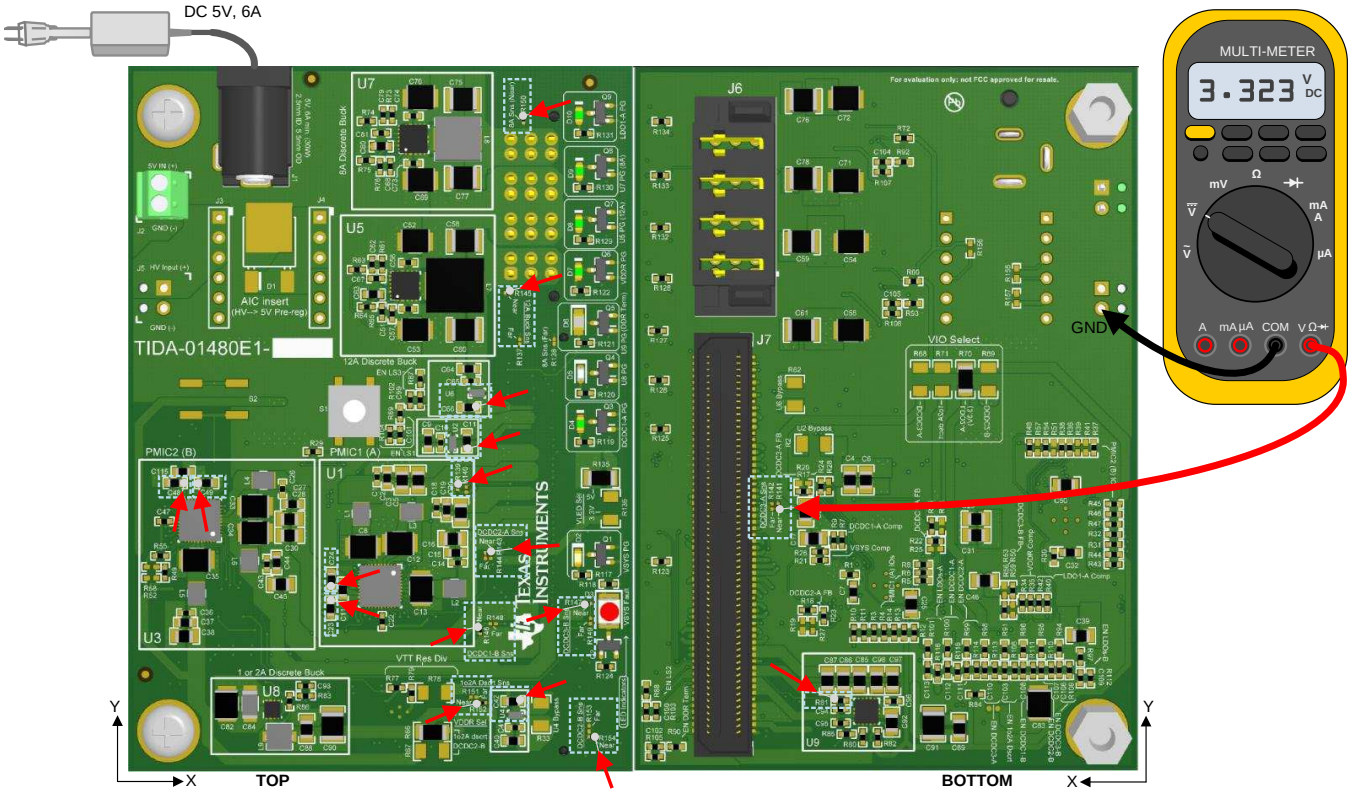


図 13. Setup and Measurement Locations for DC Voltage Measurements

表 2 lists the results of these simple measurements.

A standard DC power supply, an electronic load, and an oscilloscope are used to take load measurements on the output power rails. The voltage is measured at the output capacitor of the DC/DC switching regulator where the output voltage is being sensed by the device. 図 14 shows the setup for these tests . The VCC_12A rail provided by the TPS56C215 is shown as an example of how the load is applied and how the measurement is taken with the oscilloscope probe. A current probe (not depicted) is also used to monitor the load current and slew rate during load steps.

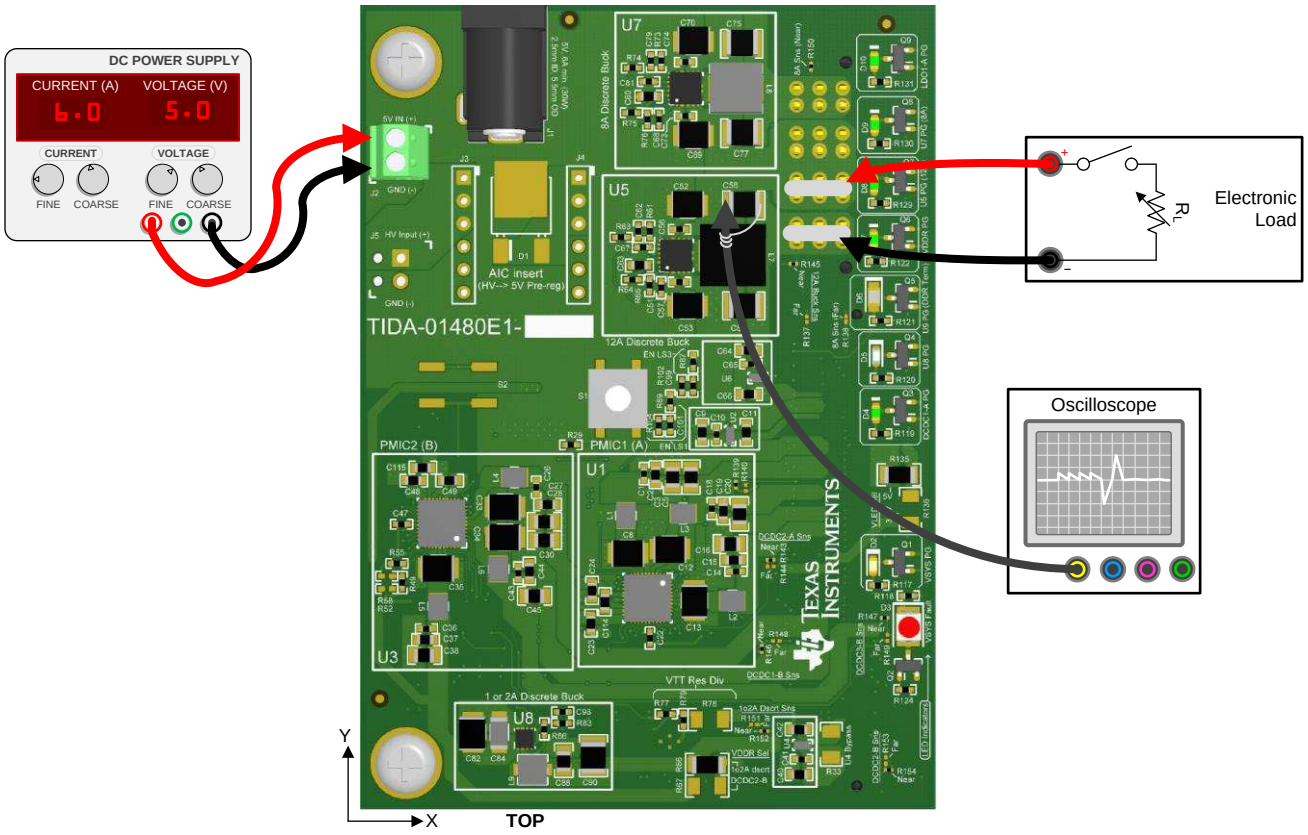


図 14. Setup for Measuring Output Voltages with Load Applied

3.2.2 Test Results

表 2 lists the power rails measured for DC output voltage using the default component values populated on this reference design. The measurements are done at no load with a handheld multimeter and the component designator, where the measurement is taken, is also listed.

表 2. DC Output Voltage Measurements

POWER RAIL NAME	DEVICE COMPONENT DESIGNATOR	MEASUREMENT COMPONENT DESIGNATOR	DESIRED VOLTAGE (V)	MEASURED VOLTAGE (V)
VDCDC1_A	U1	R139	1.2	1.204
VDCDC2_A	U1	R143	1.8	1.804
VDCDC3_A	U1	R141	3.3	3.323
VLDO1A_1V8	U1	C23	1.8	1.802
VLDO2A_3V3	U1	C24	3.3	3.301
VDCDC1_B	U3	R146	0.9	0.902
VDCDC2_B	U3	R154	1.8	1.806
VDCDC3_B	U3	R147	0.85	0.862
VLDO1_B	U3	C48	1.8	1.797
VLDO2_B	U3	C49	3.3	3.293
VDCDC1_A_LS1	U2	C11	1.2	1.204
VDCDC2_B_LS2	U4	C42	1.8	1.806
VCC_12A	U5	R145	0.9	0.896
VCC_8A	U7	R150	0.9	0.894
VCC_1or2A	U8	R152	1.36	1.378
VCC_12A_LS3	U6	C66	0.9	0.896
VTT_DDR	U9	R81	0.68	0.689

図 15 shows the test results measuring the output voltage of VDCDC1_A with no load applied. Note that PFM mode is entered automatically by the TPS65023B device. This feature can be disabled by writing to the device with I^2C commands.

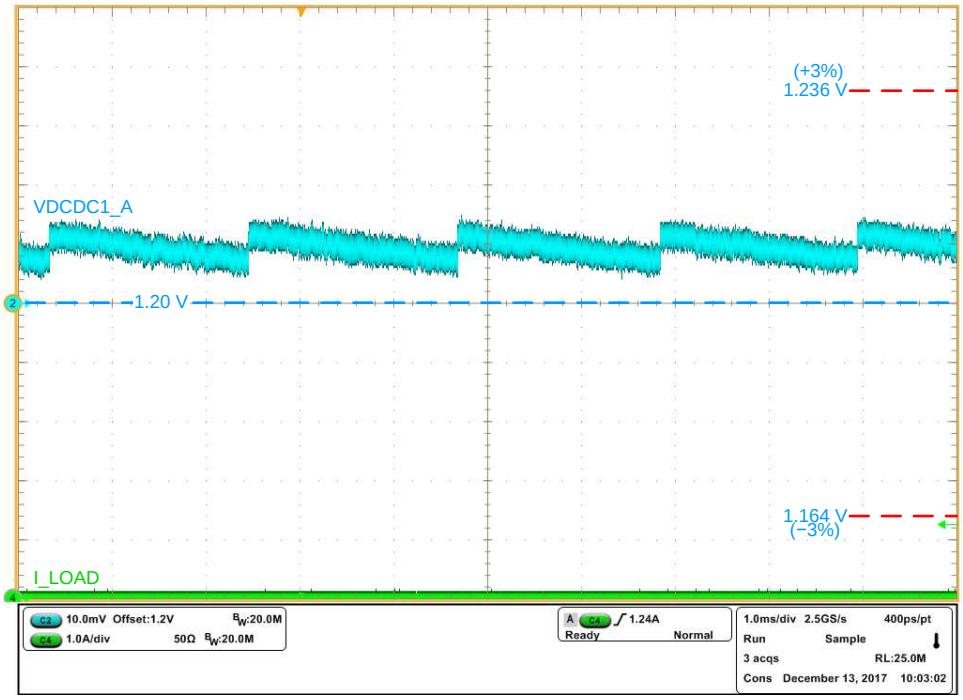


図 15. VDCDC1_A No Load Test

図 16 shows the test results measuring the output voltage of VDCDC1_A with a full load of 1.7 A applied. Note that the TPS65023B device is in PWM and switching continuously.

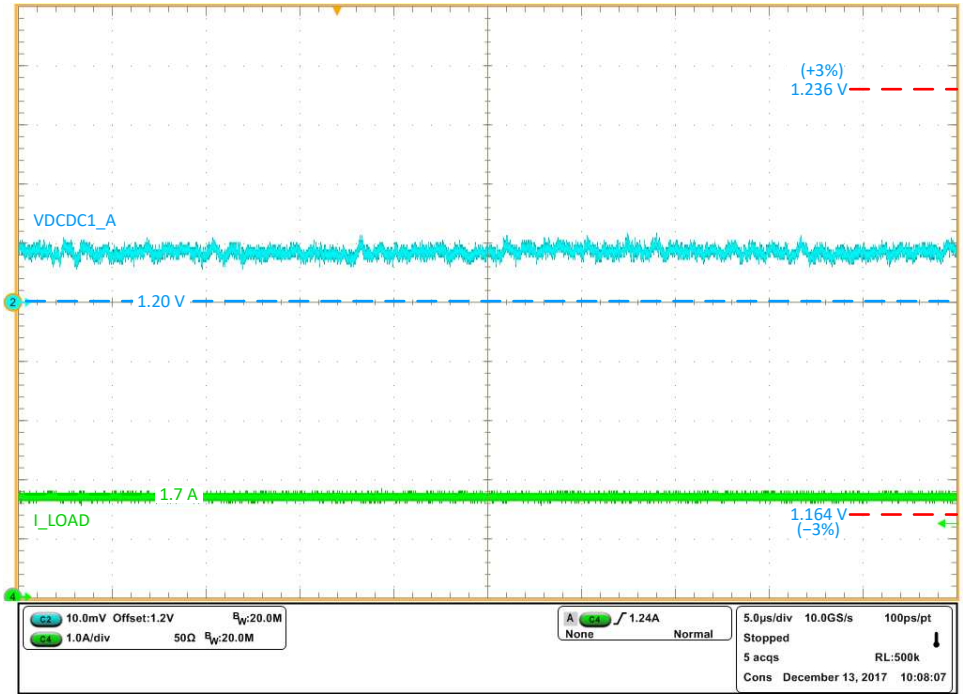


図 16. VDCDC1_A Full Load Test

図 17 shows the test results measuring the output voltage of VDCDC1_A with a load step from 0 A to 1.7 A (100%) applied. Note that the electronic load is set to the maximum slew rate of 25 A/µs, but this slew rate is not fully achieved because of the soft-start feature of the TPS65023B device and the large output capacitance of the power rail.

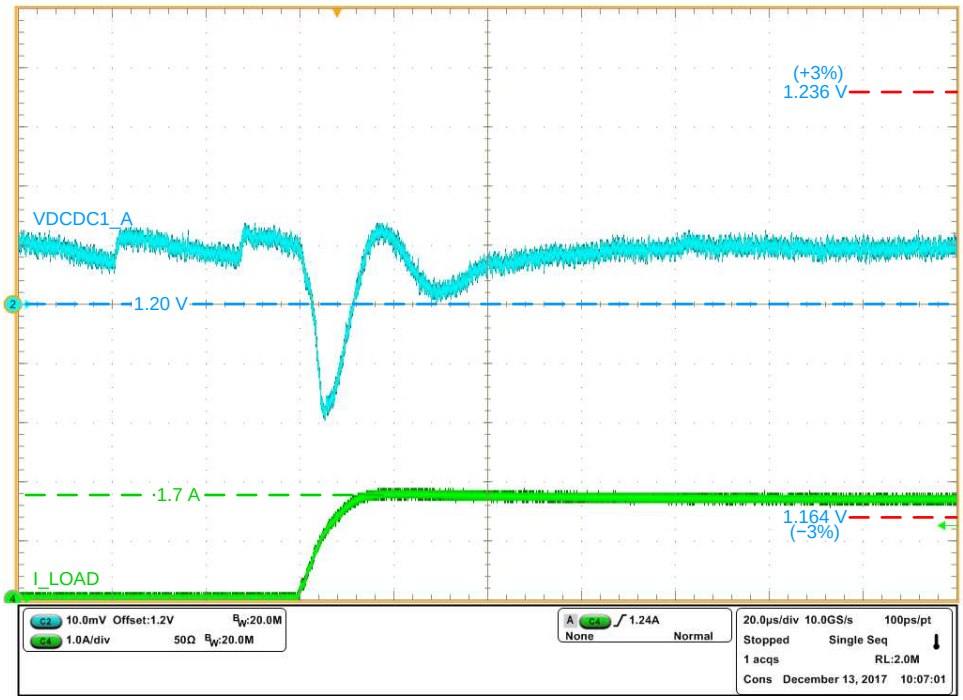


図 17. VDCDC1_A Load Step Test

図 18 shows the test results measuring the output voltage of VCC_8A with no load applied. Note that PFM mode is entered automatically by the TPS568215 device. This feature can be disabled by changing the resistor divider connected to the MODE pin of the device.

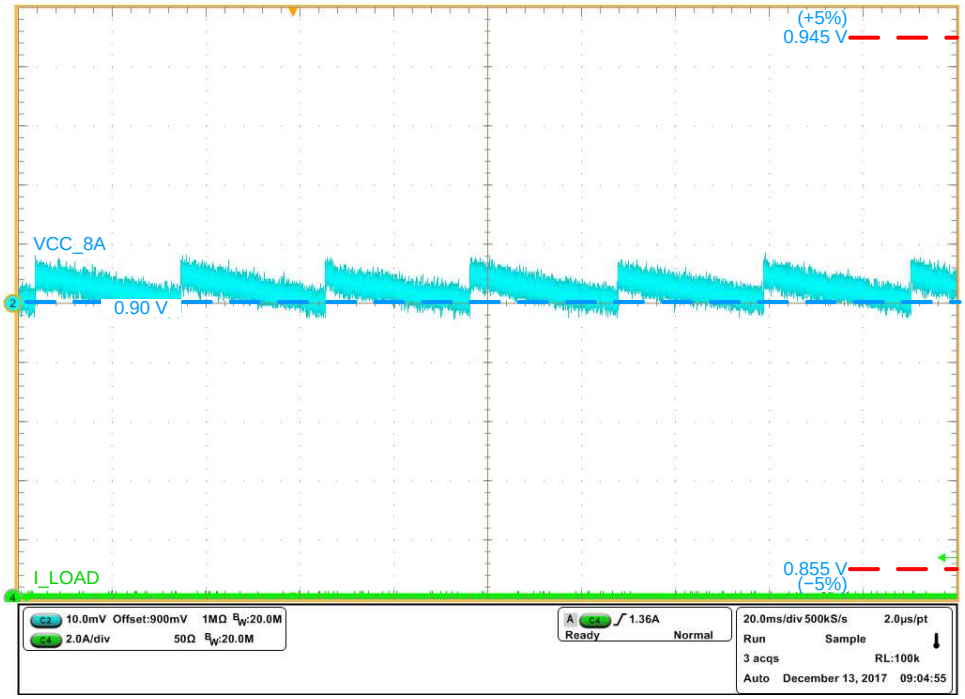


図 18. VCC_8A No Load Test

図 19 shows the test results measuring the output voltage of VCC_8A with a full load of 6.55 A applied as required by the application. Note that the TPS568215 device is in PWM and switching continuously.

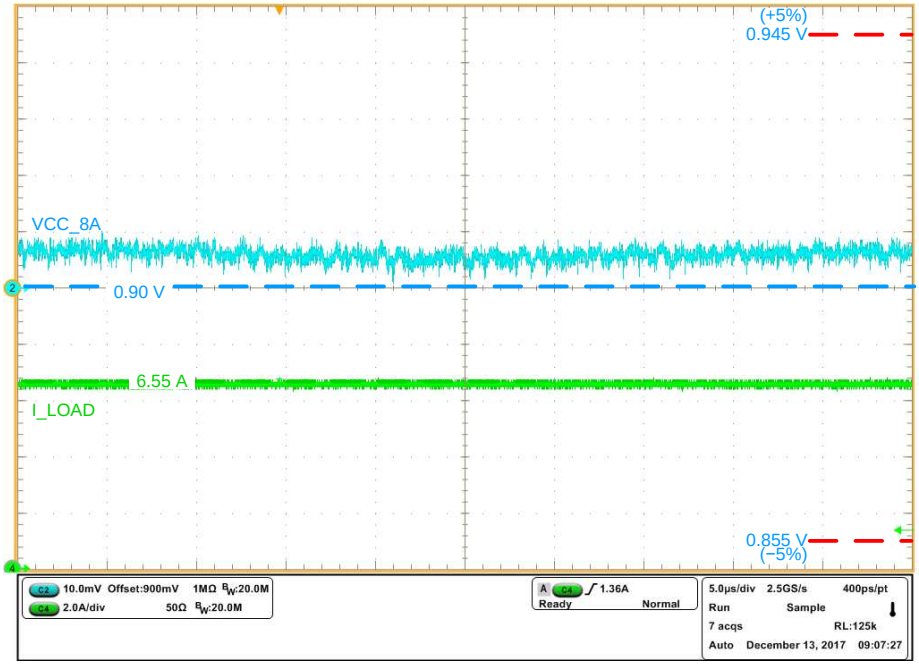


図 19. VCC_8A Full Load Test

図 20 shows the test results measuring the output voltage of VCC_8A with a load step from 0 A to 6.55 A (100%) applied. The application only requires 25% of full load but the TPS568215 is capable of staying in regulation with a full 100% load step. Note that the electronic load is set to the maximum slew rate of 25 A/µs, but this slew rate is not fully achieved because of the soft-start feature of the TPS568215 device and the large output capacitance of the power rail.

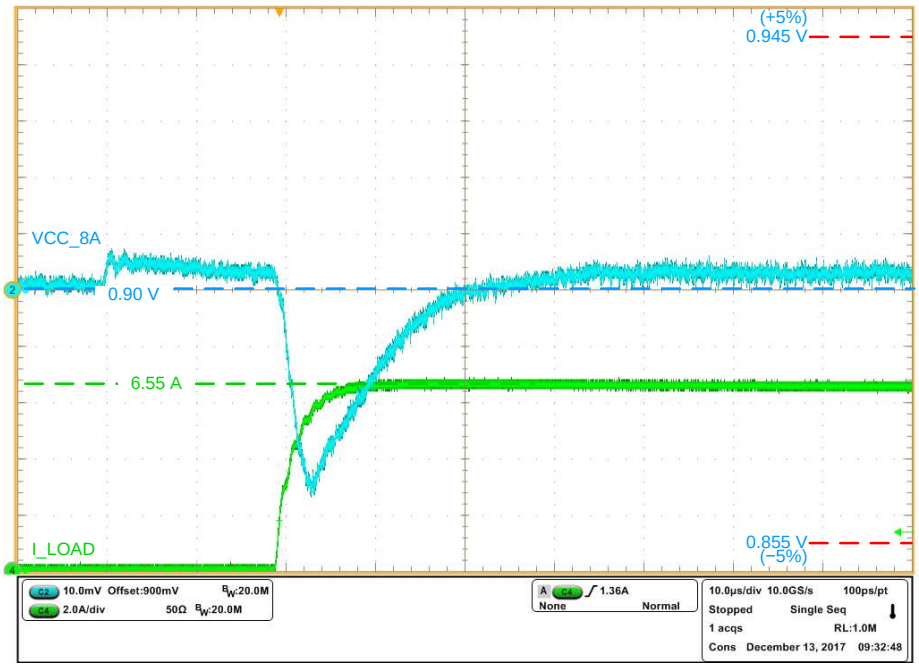


図 20. VCC_8A Load Step Test

図 21 shows the test results measuring the output voltage of VCC_12A with no load applied. Note that PFM mode is entered automatically by the TPS56C215 device. This feature can be disabled by changing the resistor divider connected to the MODE pin of the device.

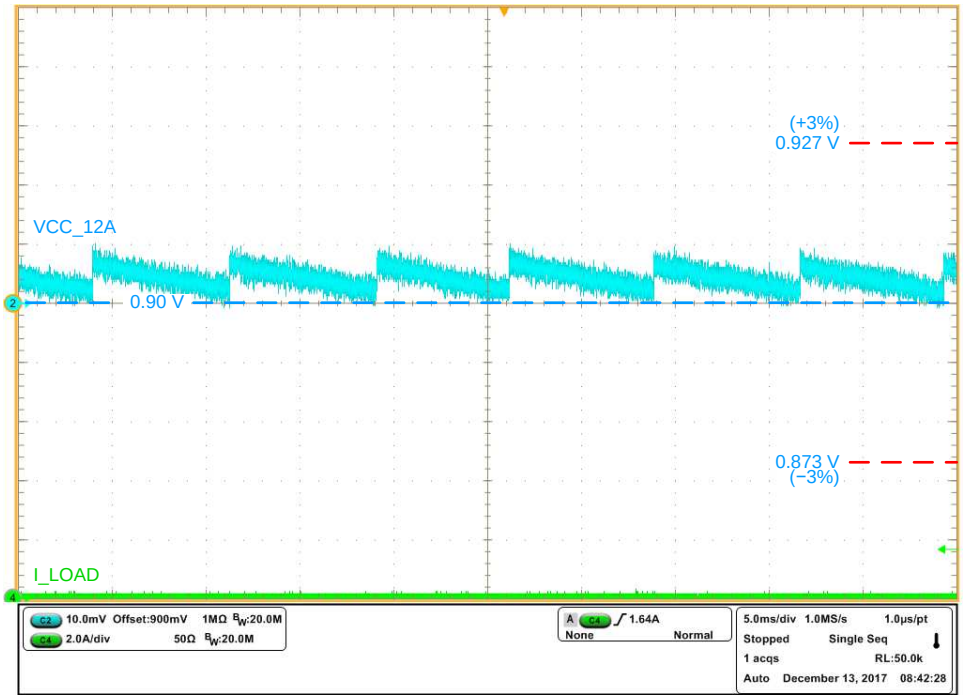


図 21. VCC_12A No Load Test

図 22 shows the test results measuring the output voltage of VCC_12A with a full load of 9.1 A applied as required by the application. Note that the TPS56C215 device is in PWM and switching continuously.

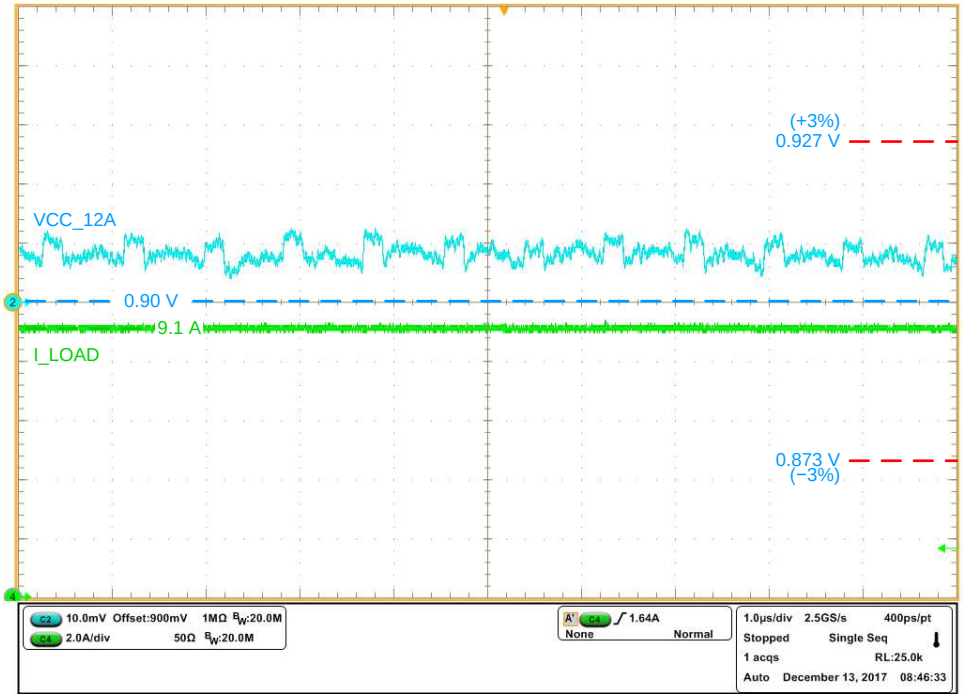


図 22. VCC_12A Full Load Test

図 23 shows the test results measuring the output voltage of VCC_12A with a load step from 5.28 A to 9.1 A (58% to 100%) applied. The application only requires 25% of the full load, and the load step measurement depicted is the largest range that consistently meets the desired 3% tolerance of the output voltage. Note that the electronic load is set to the maximum slew rate of 25 A/µs, but this slew rate is not fully achieved because of the soft-start feature of the TPS56C215 device and the large output capacitance of the power rail.

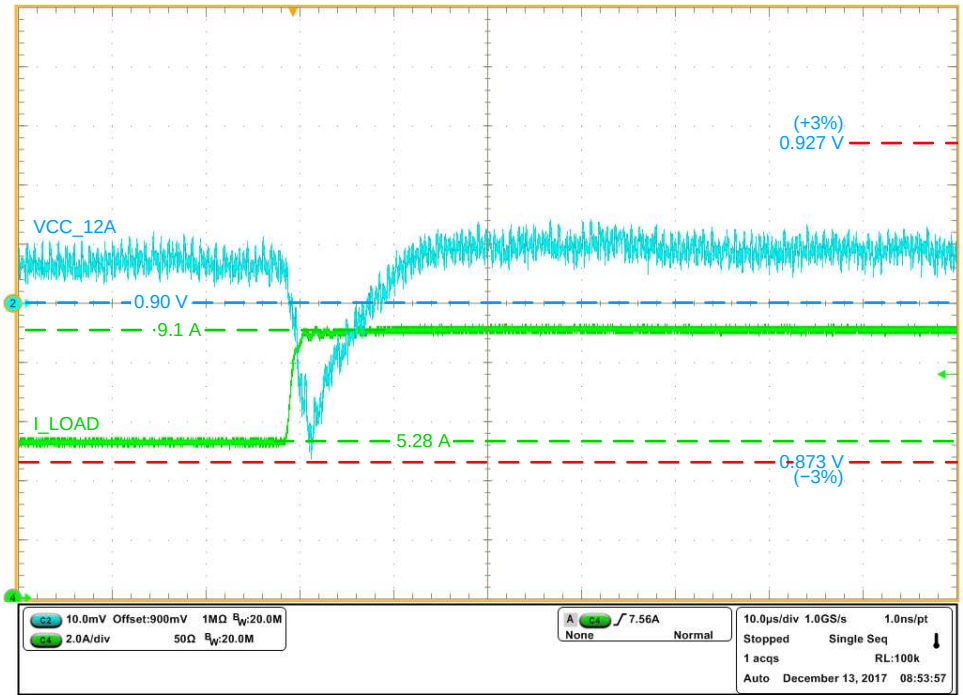


図 23. VCC_12A Load Step Test

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01480.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01480.

4.3 PCB Layout Recommendations

The layout guidelines in each device's data sheet are used as a starting point for placement of critical components for the respective buck converter. For additional guidance on layout, see the EVM User's Guides consulted in 5.

This reference design is a six (6) layer PCB with 1-oz. copper thickness and a total thickness of 62 mils. The top (first) and bottom (sixth) layers are used for component placement and for routing signals and power. The second and fifth layers are solid copper GND planes. The innermost layers (third and fourth) are reserved for routing low-speed digital signals and low-current power traces. An example of a low-current power trace would be any of the 200-mA LDOs for the two TPS65023 devices, which have an average trace width of 30 mils.

The shortest routing distance from input to output is for the TPS56C215 12-A converter and for the TPS568215 8-A converter. For these two high-current rails, the input power from VSYS is connected by a solid copper polygonal pour directly to both sets of input capacitors with an approximate distance of 750 mils (19 mm). The output inductor is connected by a solid copper pour directly to the blade of J6 with an approximate distance of 150 mils (3.8 mm). The total worst-case distance from input (VSYS) to output (VCC_12A or VCC_8A), including the device, is less than 2 inches with all routing on the top layer.

All buck converters have at least one pin named AGND, and all components that must connect to AGND (sensitive analog signals such as feedback resistors, comparator resistors, and mode selection resistors) are connected to the AGND pin of the device using a *star-point* connection. These AGND star-points connect to the GND plane with a single via connected to the GND net and these vias are located near an AGND pin for each device (five AGND-to-GND vias total, one for each device designated as U1, U3, U5, U7, and U8).

To save space, large bypass capacitors that appear in sets of two (2, 4, 6, or 8) alternate placement on top and bottom layers of the PCB with multiple vias placed around the capacitor pad to allow current flow to and from opposite layers of the board. For example, U5 (TPS56C215) requires four output bypass capacitors. C58 and C60 are placed on the top layer while C59 and C61 are placed on the bottom layer with five vias surrounding each pad.

Other than thermal relief vias for devices and drill holes for through-hole components, all vias have a hole size of 7.9 mils and a 14-mil diameter (3-mil annular ring). The minimum trace width for low-speed low-current signal routing is 4 mils around the TPS65023 devices and 6 mils anywhere else on the board.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01480.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01480.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01480.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01480.

5 Related Documentation

1. Texas Instruments, *TPS65023B/TPS650231EVM User's Guide*
2. Texas Instruments, *TPS56C215EVM-762 12-A, SWIFT™ Regulator Evaluation Module User's Guide*
3. Texas Instruments, *TPS568215EVM-762 8-A, SWIFT™ Regulator Evaluation Module User's Guide*
4. Texas Instruments, *TPS62065/TPS6206567EVM User's Guide*
5. Texas Instruments, *TPS22920EVM-002/TPS22920L User's Guide*
6. Texas Instruments, *Using the TPS51200 EVM Sink/Source DDR Termination Regulator User's Guide*
7. Xilinx, *Zynq UltraScale+ MPSoC Product Tables and Product Selection Guide*
8. Xilinx, *UltraScale Architecture PCB Design, UG583*

5.1 商標

6 About the Author

BRIAN BERNER joined Texas Instruments as an applications engineer in 2011 after earning his bachelor of science and master of science degrees in electrical engineering from Lehigh University. Prior to joining the Integrated Power Management team, Brian worked as an applications engineer supporting customers using the TPS6598x family of USB Type-C and PD Port Controllers while developing technical content to aid in product development.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (March 2018) から **Revision B** に変更 **Page**

- new row in the *Key System Specifications* table for independent VCCINT_VCU rail, which must be 0.9 V and separate but is only required in ZU4EV and ZU5EV Xilinx devices 追加 2
- Created separate rail for VCCINT_VCU needed for Xilinx -EV devices for each variant in the *Block Diagrams* section ... 5
- Modified wiring of power outputs to Xilinx rails numbered 1, 5, 10, 12, 3, 9, and 14 in the *Block Diagram of Design Variant 005* figure to improve sequencing accuracy and to create a separate rail needed for VPS_MGTRAVCC 8

2017年12月発行のものから更新 **Page**

- ドキュメントのすべてのセクションで、Artix-7 (現在はTIDA-050000 TI Designでサポート)への言及を 削除 1
- Corrected typos and updated the solution sizes for each variant in the *Block Diagrams* section 4

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