参考資料

TI Designs: TIDA-01520
車載ヘッドライト用のプリ昇圧制御付き50Wデュアル段LEDドライバのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインでは、車載用フロント・ライト・アプリケーション用の2つのLEDストリングを駆動する方法と、マイクロコントローラ(MCU)を使用せずにプリ昇圧電圧を自動的に調整する方法を示す、デュアル段のソリューションについて詳説します。

このデザインは、昇圧コントローラ(LM5122-Q1)と、それに続く2つの降圧LEDドライバ(TPS92515HV-Q1)を使用します。適応型プリ昇圧制御と呼ばれる回路により、LEDストリング全体の電圧を測定し、昇圧コントローラの帰還に電流を注入して、LEDストリングの長さ、およびLED順方向電圧の温度差異に基づいて、昇圧電圧を調整します。これによって、スイッチング損失が減少し、総合的なシステム効率が最大化されます。

このリファレンス・デザインには、いくつかのベンチ結果と、CISPR 25仕様に従ったEMC測定結果も示されています。

リソース

TIDA-01520	デザイン・フォルダ
LM5122-Q1	プロダクト・フォルダ
TPS92515HV-Q1	プロダクト・フォルダ
OPA348-Q1	プロダクト・フォルダ

TI E2E™ Community

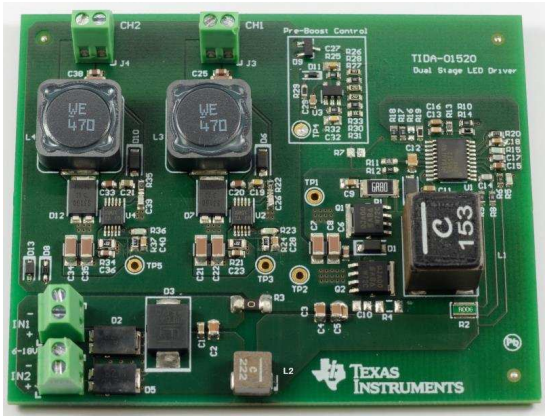
E2E™エキスパートに質問

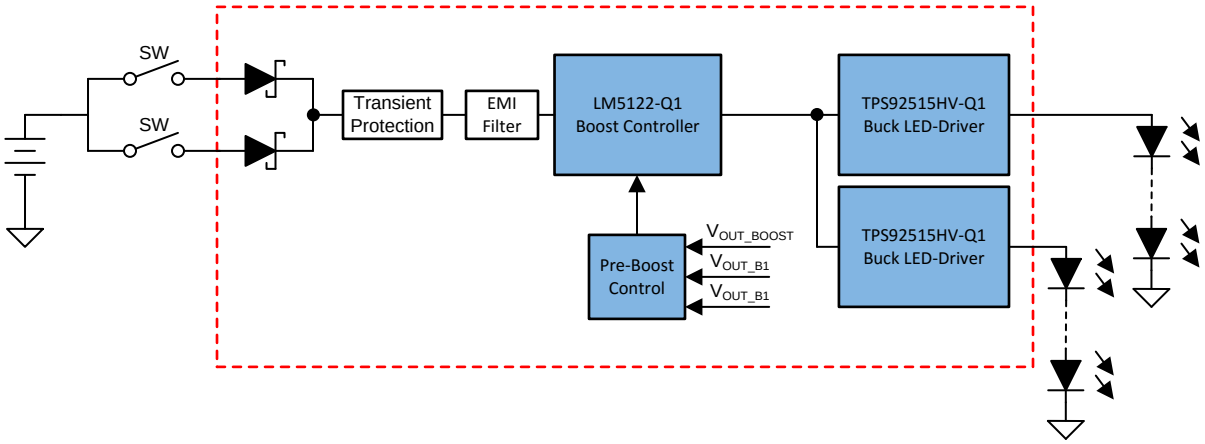
特長

- デュアル段: 昇圧 + 2つの降圧LEDドライバ
- ストリングの長さと温度差異に応じて昇圧電圧を自動的に調整
- 動的な負荷をサポート(マトリクスおよび調光)
- 各チャネルは最大14のLEDで25W
- CISPR 25を満たすことをテスト済み

アプリケーション

- 外部照明 - ヘッドライト
- 外部照明 - フォグライト





1 System Description

This reference design showcases a two-channel LED driver for automotive front light applications. The design uses a dual-stage approach consisting of one boost controller (LM5122-Q1) and two buck LED drivers (TPS92515HV-Q1). The boost controller provides a intermediate voltage rail that connects the LED drivers. With this architecture, the system can operate during cold crank and load dump conditions where the battery voltage is varying. This architecture also enables a flexible number of LEDs per string. The buck LED drivers are based on a hysteretic control, which is ideal to support dynamic loads. This control is specifically required for shunt dimming and matrix-based front light applications.

This reference design also includes a circuit called adaptive pre-boost control. This circuit measures the boost voltage and the voltage across the LED strings. Based on the difference, a current gets injected into the feedback node of the boost controller to adjust the boost voltage based on the length of the LED string and the temperature variations of the LED forward voltage. This maximizes the overall system efficiency by reducing the switching losses of the boost controller and the buck LED drivers.

This dual-stage LED driver is designed with the following points in consideration:

- Each channel up to 25 W
- 1-A LED current
- Operation during cold cranking condition
- Maximum of 14 LEDs per string
- Adaptive pre-boost voltage control

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range of operating DC	6 V to 18 V	2.3.4
Maximum string length per channel	14 LEDs at 3-V forward voltage (42 V)	2.3.5
Default LED current	1 A	2.3.5
Output power	25 W per channel	2.3.5
PCB form factor	75 mm × 60 mm	2.3.1

2 System Overview

2.1 Block Diagram

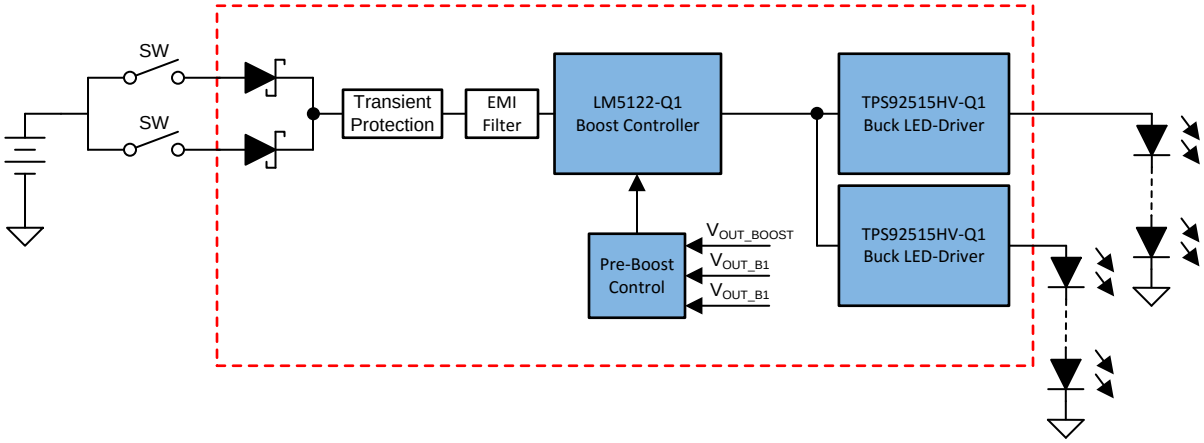


図 1. Block Diagram of TIDA-01520

2.2 Highlighted Products

2.2.1 LM5122-Q1

The LM5122 device is a multiphase-capable synchronous boost controller intended for high-efficiency synchronous boost regulator applications. The control method is based upon peak current mode control. Current mode control provides inherent line feedforward, cycle-by-cycle current limiting, and ease of loop compensation.

The switching frequency is programmable up to 1 MHz. Higher efficiency is achieved by two robust, N-channel MOSFET gate drivers with adaptive dead-time control. A user-selectable diode emulation mode also enables discontinuous mode operation for improved efficiency at light load conditions.

An internal charge pump allows 100% duty cycle for high-side synchronous switch (bypass operation). A 180º phase-shifted clock output enables easy multiphase interleaved configuration. Additional features include thermal shutdown, frequency synchronization, hiccup mode current limit, and adjustable line undervoltage lockout.

図 2 shows the functional block diagram of the LM5122-Q1 boost controller.

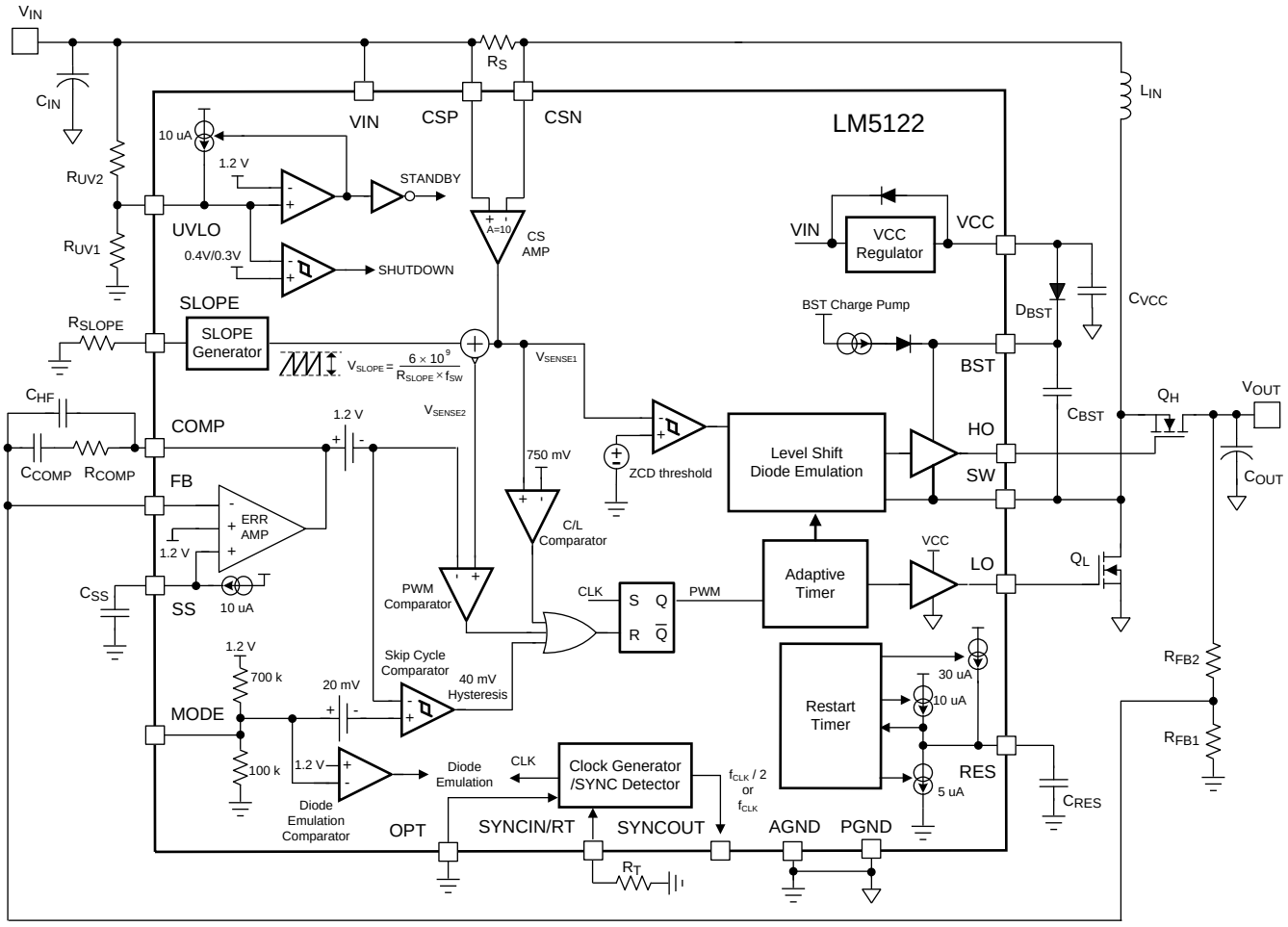


図 2. Functional Block Diagram of LM5122-Q1 Boost Controller

2.2.2 TPS92515HV-Q1

The TPS92515 family of devices are compact monolithic switching regulators integrating a low-resistance N-channel MOSFET. The devices are intended for high-brightness LED lighting applications where efficiency, high bandwidth, PWM or analog dimming (or both), and small size are important.

The regulator operates using a constant off-time, peak current control. The operation is simple: after an off-time based on the output voltage, an on-time begins. The on-time ends once the inductor peak current threshold is reached. The TPS92515 device can be configured to maintain a constant peak-to-peak ripple during the ON and OFF periods of a shunt FET dimming cycle. This ripple is ideal for maintaining a linear response across the entire shunt FET dimming range.

Steady-state accuracy is aided by the inclusion of a low-offset, high-side comparator. LED current can be modulated using either analog or PWM dimming, or both simultaneously. Other features include undervoltage lockout (UVLO), wide input voltage operation, inherent LED open operation, and wide operating temperature range with thermal shutdown.

図 3 shows a block diagram of the TPS92515HV-Q1 buck LED driver.

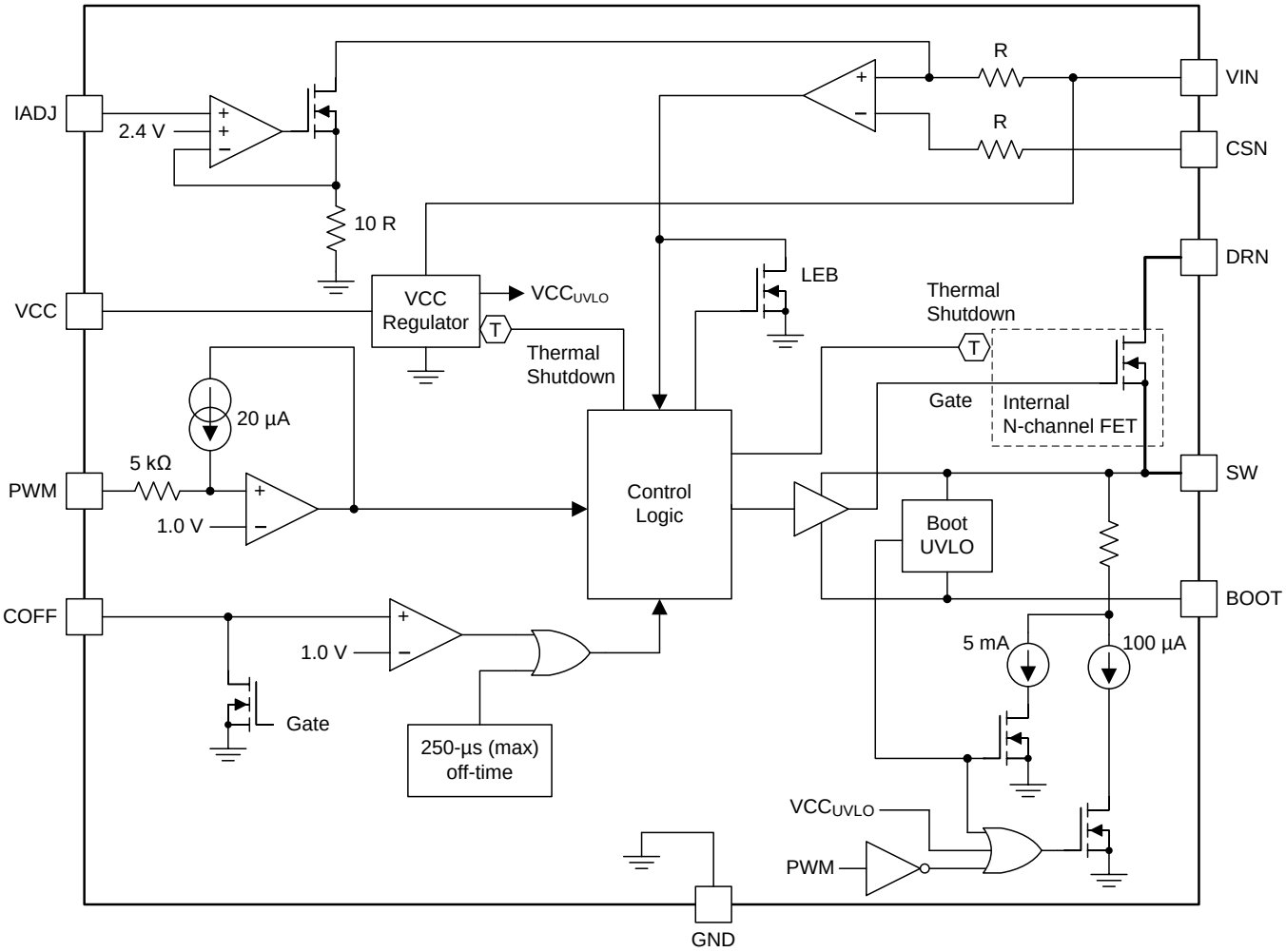


図 3. Functional Block Diagram of TPS92515HV-Q1 Buck LED Driver

2.2.3 OPA348-Q1

The OPA348-Q1 device is a single-supply, low-power CMOS operational amplifier. Featuring an extended bandwidth of 1 MHz and a supply current of 45 µA, the OPA348-Q1 device is useful for low-power applications on single supplies of 2.1 V to 5.5 V.

図 4 shows a block diagram of the OPA348-Q1 operational amplifier.

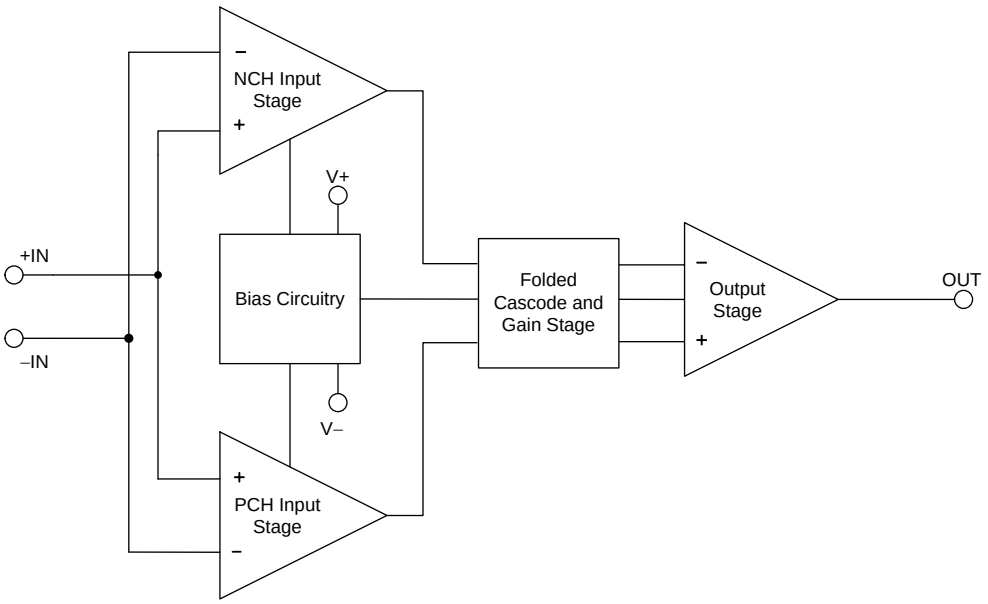


図 4. Functional Block Diagram of OPA348-Q1 Operational Amplifier

2.3 System Design Theory

2.3.1 PCB and Form Factor

This reference design uses a two-layer printed circuit board (PCB) where all components are placed on the top layer. The PCB is not intended to fit any particular form factor and has a dimension of 75 mm × 60 mm. The primary objective of the design with regards to the PCB is to make a solution that is compact while still providing a way to test the performance of the board. In a final-production version of this reference design, the size of the solution can be further reduced. 図 5 shows a 3D rendering of the PCB.

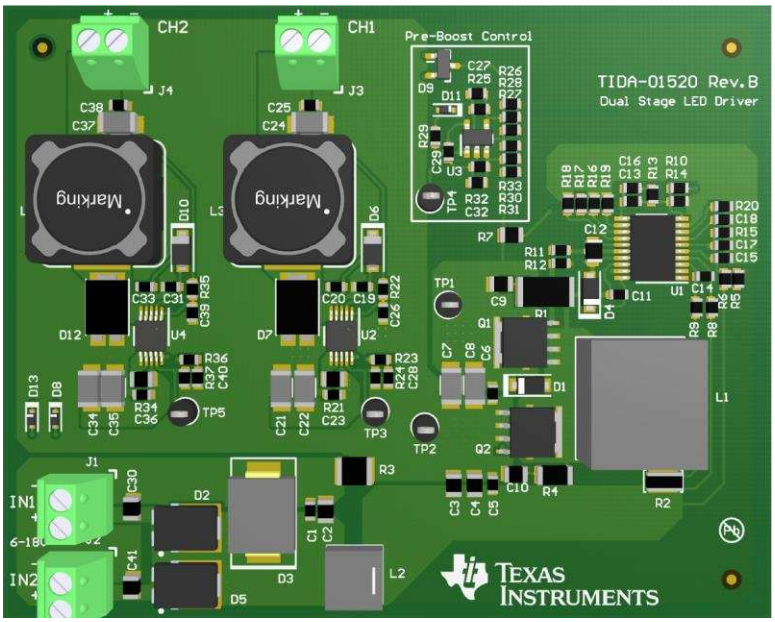


図 5. 3D Render of TIDA-01520 PCB

2.3.2 Input Protection and OR-ing

In this reference design, reverse polarity protection is implemented by using Schottky diodes D2 and D5 on the input lines as shown in 図 6. The diodes are acting as an OR-ing circuit, which implies independent function of the output channels by applying power to its input supply line.

Using Schottky diodes for reverse polarity protection is a very simple and common implementation; however, for high current levels, the power dissipation in the diodes gets very high (see 3.2.7). Smart diode controllers like the LM5050-1-Q1 or LM74700-Q1 can be used instead to reduce the power dissipation to a minimum.

For transient protection, a transient voltage suppressor (TVS) diode D3 is placed at the input after the reverse polarity protection.

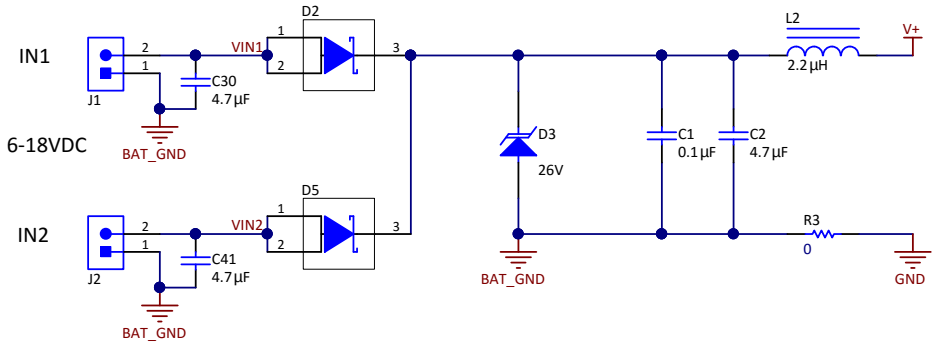


図 6. Schematic of Input Protection + EMI Filter

2.3.3 EMI Filter

A LC low-pass filter is placed on the input of the boost controller to attenuate conducted differential mode noise generated by the system. The filter consists of C1, C2, and L2 as shown in 図 6. For more details, see *Simple Success With Conducted EMI From DC-DC Converters*.

2.3.4 LM5122-Q1 Boost Controller

表 2 shows the default design parameters for the boost controller.

表 2. Design Parameters of Default Boost Controller

DESIGN PARAMETERS	VALUE
Output voltage range	18 V to 45 V
Output power	55 W
Minimum input voltage (DC)	6 V
Typical input voltage (DC)	13.5 V
Maximum input voltage (DC)	18 V
Switching frequency	330 kHz

For the maximum boost ratio (6 V to 45 V), the switching frequency of the LM5122-Q1 is limited by a forced off-time. Based on 式 1, the frequency in the default configuration is set to 330 kHz.

$$f_{SW(MAX)} = \frac{V_{IN(MIN)}}{V_{OUT} \times t_{LO\_OFF}} = \frac{6\ V}{45\ V \times 400\ ns} = 333\ kHz \quad (1)$$

図 7 shows the default LM5122-Q1 boost controller schematic of this reference design.

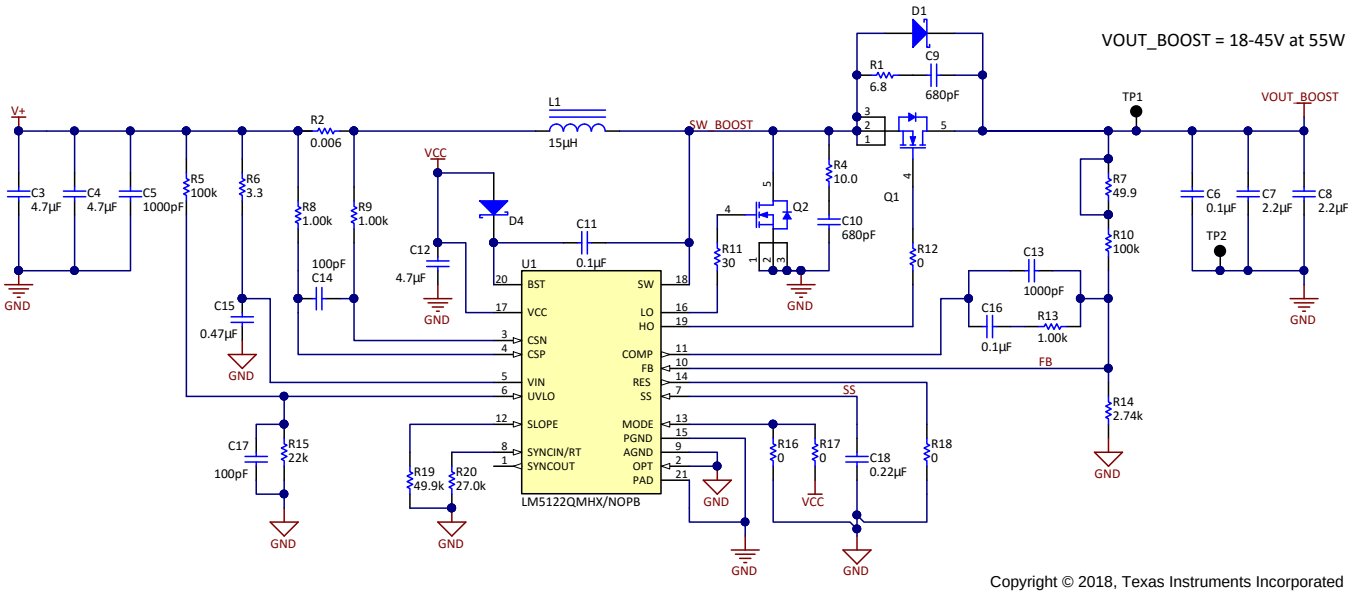


図 7. Schematic of LM5122-Q1 Boost Controller

The main components of the boost stage are selected by following the Detailed Design Procedure section in the data sheet *LM5122 Wide-Input Synchronous Boost Controller With Multiple Phase Capability*.

R20 sets the switching frequency whereas R19 programs the slope compensation. The desired startup voltage and the hysteresis are set by the voltage divider R5, 15. For this reference design, the startup voltage is 6.7 V with a hysteresis of 1 V, which results in a 5.7-V shutdown voltage. The inductor L1 has a value of 15 µH with a saturation current rating above the maximum expected inductor current of 9.7 A at a minimum input voltage of 6 V. For this example, a ripple ratio (RR) of 0.5, 50% of the input current is chosen. Based on this input current capability, a value of 6 mΩ is selected for the current sense resistor R2. R8, R9, and C14 form a filter for the current sensing. The slope compensation resistor R19 is set to 49.9 kΩ.

The output capacitors C6, C7, and C8 smooth the output voltage ripple and provide a source of charge during transient loading conditions. Also the output capacitors reduce the output voltage overshoot when the load is disconnected suddenly. Ripple current rating of output capacitor must be carefully selected. In a boost regulator, the output is supplied by discontinuous current and the ripple current requirement is usually high, which makes ceramic capacitors a perfect fit. The output voltage ripple is dominated by ESR of the output capacitors. Paralleling the output capacitor is a good choice to minimize effective ESR and split the output ripple current into capacitors. This example uses two 2.2-µF ceramic capacitors and one 0.1-µF ceramic capacitor with a voltage rating of 100 V. A higher output voltage ripple in this reference design is not a concern for the buck LED drivers, which are connected to the boost output voltage.

Input capacitors C3, C4, and C5 smooth the input voltage ripple. This reference design uses small-sized 4.7-µF ceramic capacitors with a voltage rating of 50 V. R6 and C15 form an RC filter, which helps to prevent faults caused by high-frequency switching noise injected into the VIN pin. The bootstrap capacitor C11 between the BST and SW pins supplies the gate current to charge the high-side N-channel MOSFET device gate during each cycle's turnon and also supplies recovery charge for the bootstrap diode D4. The VCC capacitor C12 is used to supply the peak transient currents of the LO driver and bootstrap diode as well as provide stability for the VCC regulator. A value of 4.7 µF is selected. R10 and R14 set the output voltage to 45 V. C18 forms the soft-start capacitor.

The high-side and low-side power switches Q1 and Q2 are 60-V rated N-channel MOSFETs in a PowerPAK® package. An additional Schottky diode D1 is placed in parallel with the high-side switch Q1 to improve efficiency and reduce ringing. Usually, the power rating of this parallel Schottky diode can be less than the power rating of the high-side switch because the diode conducts only during dead-times. R11 and R12 are gate resistors that can limit the rise and fall times of the switch node voltage. A resistor-capacitor snubber network (R1 and C9) across the high-side N-channel MOSFET Q1 reduces ringing and spikes at the switching node. For how to calculate these values, see *Power Tips: Calculate an R-C snubber in seven steps*. The optional snubber network (R4 and C10) for the low-side switch is not used.

R13, C16, and C13 configure the error amplifier gain and phase characteristics to produce a stable voltage loop. R7 is not populated but can be used when measuring the loop transfer function of the LM5122-Q1 controller. For more details, see *How to Measure the Loop Transfer Function of Power Supplies*.

See 4.3 for layout guidelines for the boost controller in this reference design.

2.3.5 TPS92515HV-Q1 Buck LED Driver

表 3 shows the default design parameters for the buck LED drivers.

表 3. Design Parameters of Default Buck LED Driver

DESIGN PARAMETER	RANGE	DEFAULT VALUE
Input voltage	18 V to 45 V	28 V
LED forward voltage		3 V
Number of LEDs in series	1 to 14	8
Output current range	0.2 A to 1.2 A	1 A
Output voltage	3 V to 42 V	24 V
Output power per channel	25 W max	24 W
Inductor current ripple		0.1 A
Switching frequency		350 kHz

図 8 shows the default TPS92515HV-Q1 LED driver schematic of this reference design.

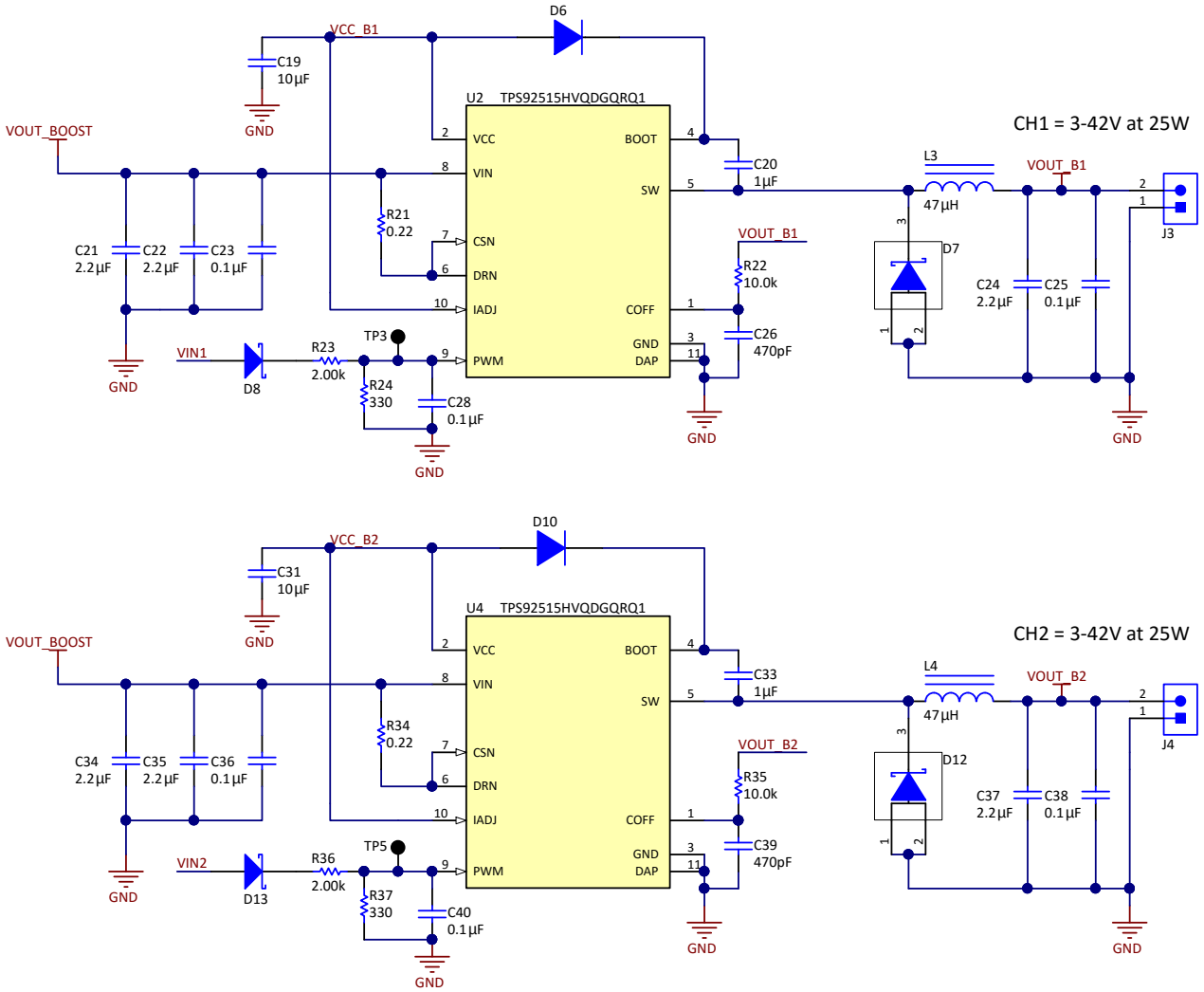


図 8. Schematic of TPS92515HV-Q1 Buck LED Driver

The main components of the buck LED drivers are selected by following the Detailed Design Procedure section in *TPS92515x 2-A, Buck LED Driver with Integrated N-channel FET, High-Side Current Sense, and Shunt FET PWM Dimming Capability*.

Components R22, R35, C26, and C39 are used to program the off-time of the hysteretic LED drivers to 0.2 µs. With the default configuration, the LED current is set to 1 A with a inductor ripple current of 0.1 A. When selecting an inductor ensure the ratings for both peak and average current are adequate. For the inductors L3 and L4, a value of 47 µH is selected. Based on the output current capability, a value of 220 mΩ is selected for the current sense resistors R21 and R34. R23, R24, R36, and R37 program the startup and UVLO level. C28 and C40 at the UVLO pin are placed for noise immunity. Capacitors C20 and C33 tied to the switch node (SW pin) and the diodes D6 and D10 connected to the VCC supply power the

BOOT pin to ensure proper operation of the internal MOSFET. The 10-µF VCC capacitors C19 and C31 supply current for the device operation as well as additional power for external circuitry. The low-side rectifier diodes D7 and D12 are 3-A rated, low-leakage, Schottky diodes in a PowerDI5 package. Diodes D8 and D13 provide reverse polarity protection to the PWM pin because the signal is coming from the input voltage. With a voltage higher than 1 V on the PWM, the device starts operation.

The input capacitors C21, C22, C23, C34, C35, and C36 provide a low impedance source for the discontinuous input current of the buck LED drivers. The output capacitors C24, C25, C37, and C38 in parallel with the LED load reduce the ripple current on the LEDs.

See 4.3 for layout guidelines for the TPS92515HV-Q1 in this reference design.

2.3.6 Adaptive Pre-Boost Control

This section describes how the adaptive pre-boost control circuit is working and how to select the right components.

表 4 shows the default design parameters for adaptive pre-boost control.

表 4. Design Parameters of Default Adaptive Pre-Boost Control

DESIGN PARAMETER	VALUE
VCC voltage	5 V
V_{FB} (boost controller)	1.2 V
Voltage offset (between pre-boost voltage and highest LED driver voltage)	10%

図 9 shows the default adaptive pre-boost control schematic of this reference design. The circuit is based on an operational amplifier configured as a differential amplifier, which measures and compares the buck LED driver voltages and the boost controller output voltage. Diode D9 is used for OR-ing functionality for the buck LED driver voltages. Depending on the number of connected LEDs, the circuit automatically regulates the pre-boost voltage to a level, which is higher than the buck LED driver voltage, by sourcing current into the pre-boost feedback node. The offset between pre-boost and buck voltage can be set such that the output voltage of the adaptive pre-boost control circuit reaches optimal operating voltage. This voltage results in increased overall efficiency by reducing the switching losses of the boost controller as well as the buck LED drivers.

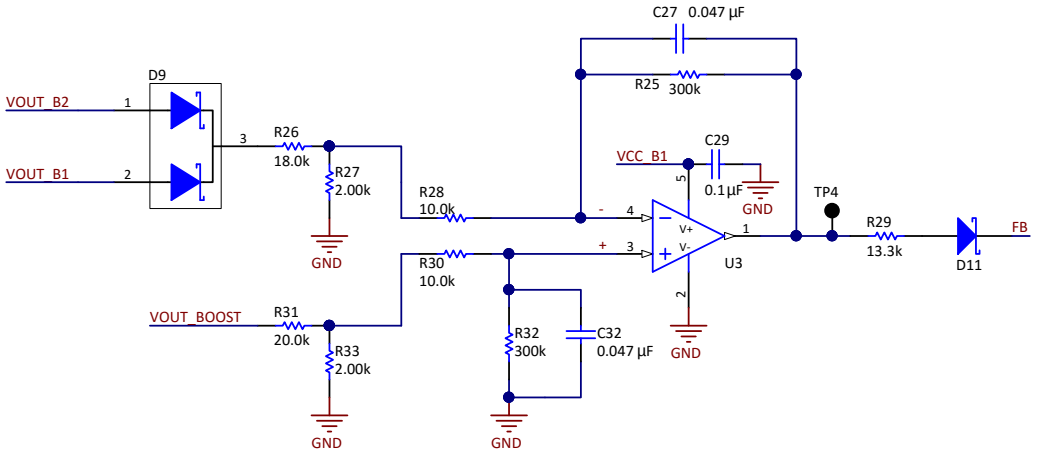


図 9. Schematic of Adaptive Pre-Boost-Control

The OPA348-Q1 operational amplifier can operate from a 2.1-V to 5.5-V supply. This reference design uses the 5-V VCC supply rail of the TPS92515HV-Q1 buck LED driver. The LED driver can allow up to 500 µA to be drawn from the VCC rail in addition to the device load. Resistor dividers reduce the measured voltages on the amplifiers input to a recommended level below 5.2 V. R26 and R27 reduce the LED driver voltage by a factor of 10, which result in a voltage level smaller than 4.2 V on the negative input of the amplifier. By keeping the same bottom resistor R27 = R33 = 2 kΩ and a 10% offset between the pre-boost voltage and the LED driver voltage. Use 式 2 to calculate the top resistor R31 of the boost voltage resistor divider.

$$R31 = (R26 + R27) \times (1 + \text{offset}) - R33 = (18\ \text{k}\Omega + 2\ \text{k}\Omega) \times (1 + 0.1) - 2\ \text{k}\Omega = 20\ \text{k}\Omega$$

- offset = 10% (2)

To calculate the gain of the operational amplifier, define the maximum error between boost voltage and LED driver voltage. In this example, the error must be smaller than 2 V. The maximum operational amplifier output voltage (V_{OPmax}) is 5 V, which is the VCC supply voltage level. 式 3 calculates the required gain.

$$\text{Gain} = \frac{V_{OPmax} \times \left(\frac{R31}{R33} + 1\right)}{\text{error}} = \frac{5\ \text{V} \times \left(\frac{20\ \text{k}\Omega}{2\ \text{k}\Omega} + 1\right)}{2\ \text{V}} = 27.5$$

- V_{OPmax} = maximum output voltage of the operational amplifier (3)

In this example, resistors R25, R28, R30, and R32 set the gain to 30. By increasing the gain, the maximum error can be reduced. Note that the loaded voltage dividers and the diode D9 create an additional error.

The output voltage of the boost controller is programmed with the feedback divider consisting of R10 and R14 (see 図 7). To vary the boost output voltage, an additional resistor R29 is connected to the boost controller feedback divider to enable feeding current into the boost feedback node (for more details, see *PMP9796 - 5V Low-Power TEC Driver Reference Design*). The feedback voltage V_{FB} of the boost controller is regulated to a constant value of 1.2 V (see *LM5122 Wide-Input Synchronous Boost Controller With Multiple Phase Capability Data Sheet*). Depending on the control voltage V_{CON}, which is the output voltage of the operational amplifier V_{OP}, minus the diode drop of D11 defines the current flowing through R29. Diode D11 prevents sink current into the output of the amplifier. Therefore, the circuit can only reduce the boost output voltage. In this example, the minimum control voltage V_{CONmin} is 1.2 V, the maximum control voltage V_{CONmax} is 4.8 V, and the resistance of R10 is selected to a value of 100 kΩ.

式 4 calculates an appropriate value for the resistance of R29.

$$R29 = R10 \times \left(\frac{V_{CONmax} - V_{CONmin}}{V_{OUT\_BOOSTmax} - V_{OUT\_BOOSTmin}}\right) = 100\ \text{k}\Omega \times \left(\frac{4.8\ \text{V} - 1.2\ \text{V}}{45\ \text{V} - 18\ \text{V}}\right) = 13.3\ \text{k}\Omega \quad (4)$$

Finally, the bottom feedback resistor R14 of the boost controller is calculated using 式 5:

$$R14 = \frac{V_{FB} \times R10 \times R29}{R29 \times V_{OUT\_BOOSTmax} + R10 \times V_{CONmin} - V_{FB} \times (R10 + R29)} = \frac{1.2\ \text{V} \times 100\ \text{k}\Omega \times 13.3\ \text{k}\Omega}{13.3\ \text{k}\Omega \times 45\ \text{V} + 100\ \text{k}\Omega \times 1.2\ \text{V} - 1.2\ \text{V} \times (1}$$

- V_{FB} = 1.2 V (5)

For this reference design, verify that the quiescent current of the amplifier plus the current through R29 needs to be smaller than 500 µA, which is the maximum allowed current to be drawn from the TPS92515HV-Q1 VCC rail.

$$\frac{V_{CONmax} - V_{FB}}{R29} + I_Q \le 500\ \mu\text{A} \quad (6)$$

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

図 10 shows the default test setup of this reference design.

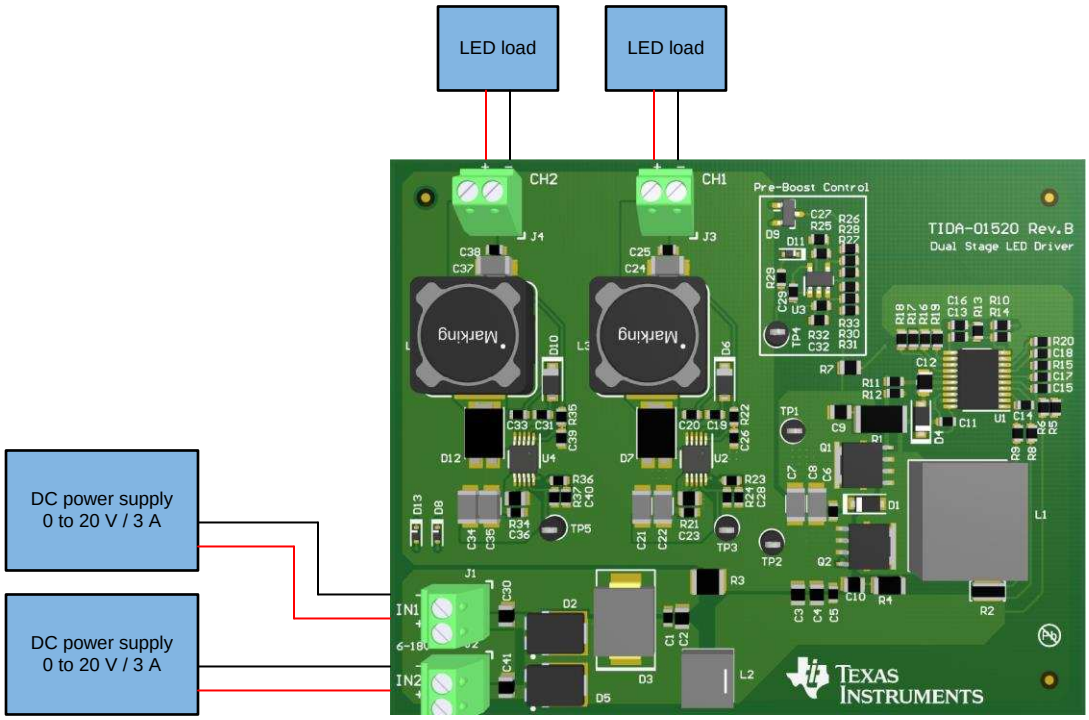


図 10. Default Test Setup

Connect a DC power supply to each input terminal (J1, J2) and the LED strings to the output terminals (J3, J4). By providing power to one of the inputs, the respective output channel gets active.

The PCB of this reference design implements several test points, which are described in 表 5. Use these test points to measure signals on the reference design.

表 5. Test Point Descriptions

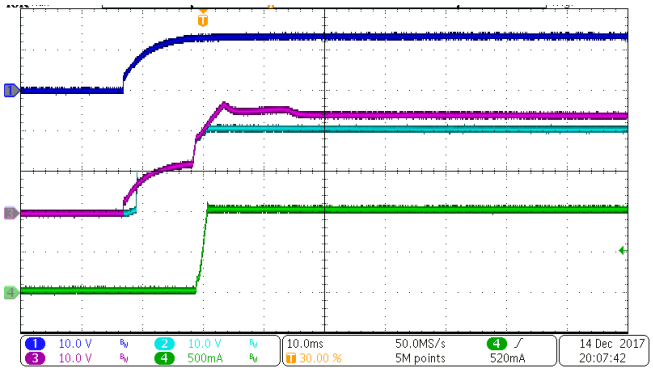
TEST POINT	DESCRIPTION
TP1	Boost output voltage
TP2	Power ground
TP3	PWM pin of LED driver (CH1), can be used to enable or disable the device or for dimming functionality
TP4	PWM pin of LED driver (CH2), can be used to enable or disable the device or for dimming functionality
TP5	Operational amplifier output

3.2 Testing and Results

All tests in this section are performed in the default configuration where the input voltage is 13.5 V and the LED current is set to 1 A on each channel.

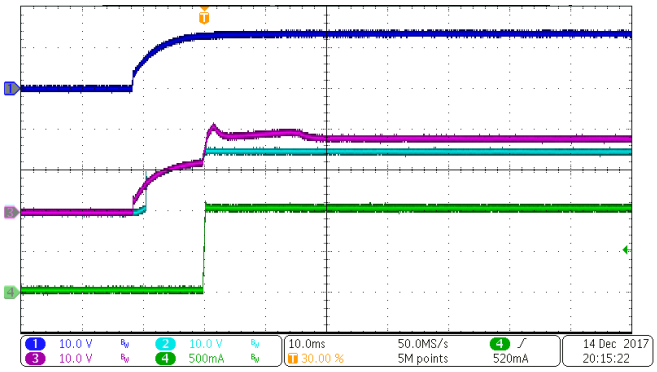
3.2.1 Startup/Shutdown

図 11 through 図 14 show the startup and shutdown behavior of the reference design. During startup, the adaptive pre-boost control starts acting and regulates the boost output voltage to the set level.



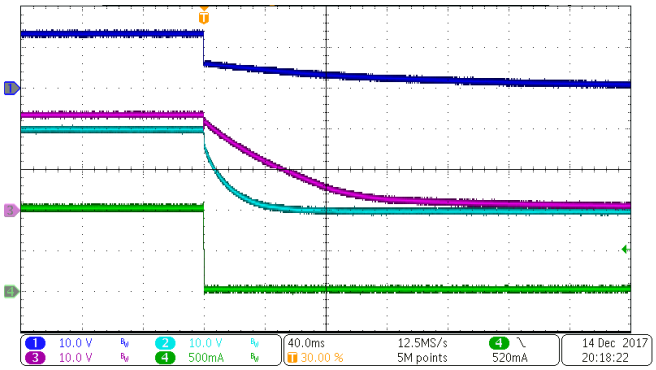
CH1: VIN, CH2: VOUT LED driver , CH3: VOUT boost, CH4: LED current

図 11. Startup (CH1 at Eight LEDs)



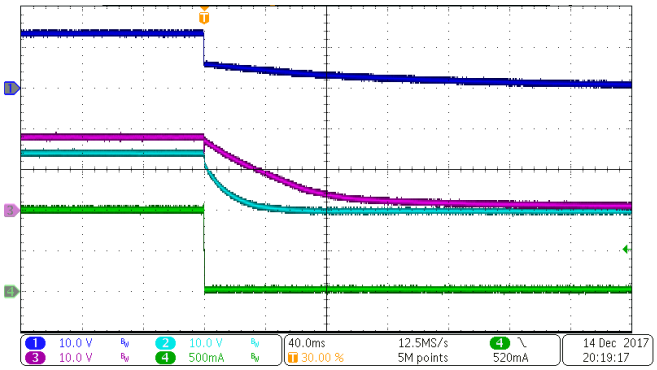
CH1: VIN, CH2: VOUT LED driver , CH3: VOUT boost, CH4: LED current

図 12. Startup (CH1 at Six LEDs)



CH1: VIN, CH2: VOUT LED driver , CH3: VOUT boost, CH4: LED current

図 13. Shutdown (CH1 at Eight LEDs)

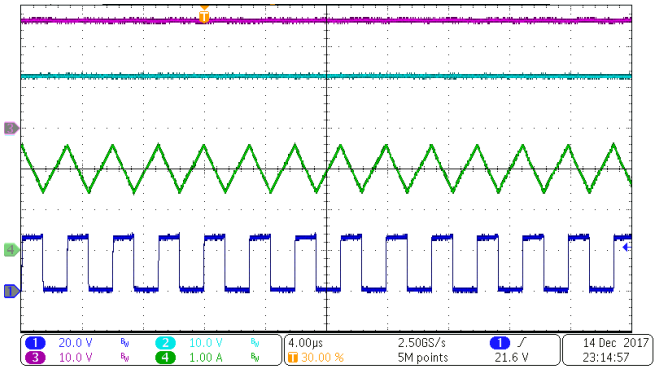


CH1: VIN, CH2: VOUT LED driver , CH3: VOUT boost, CH4: LED current

図 14. Shutdown (CH1 at Six LEDs)

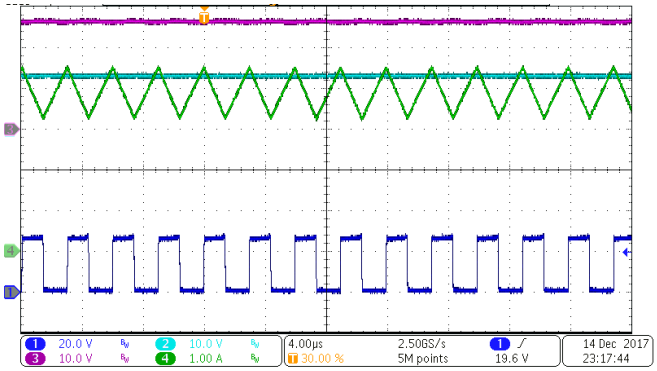
3.2.2 Steady State Operation

図 15 through 図 18 show the steady state operation of the LM5122-Q1 boost controller. With 8 LEDs connected, the boost controller operates with nearly a 50% duty cycle.



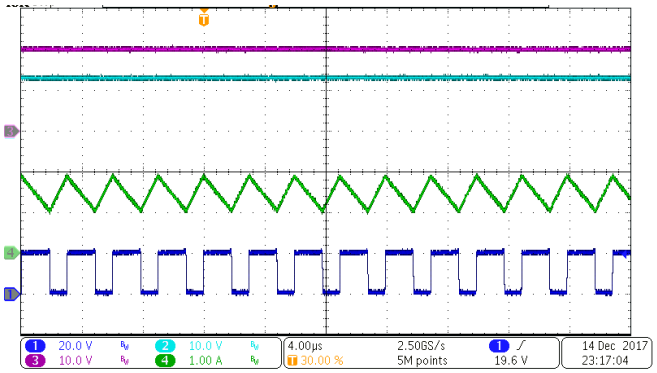
CH1: SW boost, CH2: VIN, CH3: VOUT boost, CH4: IL boost

図 15. Boost Operation (CH1 at Eight LEDs)



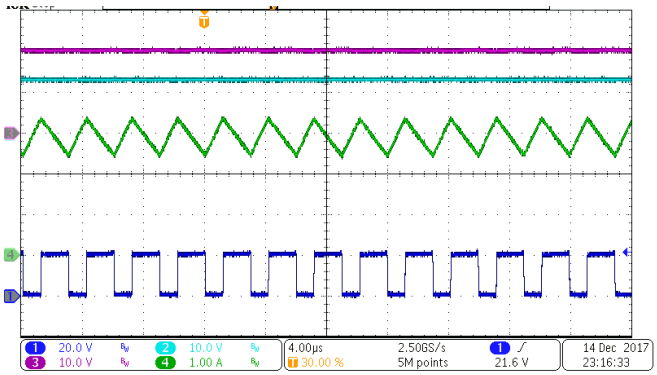
CH1: SW boost, CH2: VIN, CH3: VOUT boost, CH4: IL boost

図 16. Boost Operation (CH1 + CH2 at Eight LEDs)



CH1: SW boost, CH2: VIN, CH3: VOUT boost, CH4: IL boost

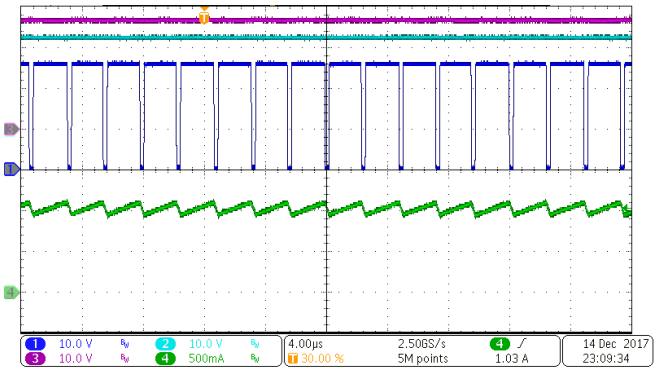
図 17. Boost Operation (CH1 at Six LEDs)



CH1: SW boost, CH2: VIN, CH3: VOUT boost, CH4: IL boost

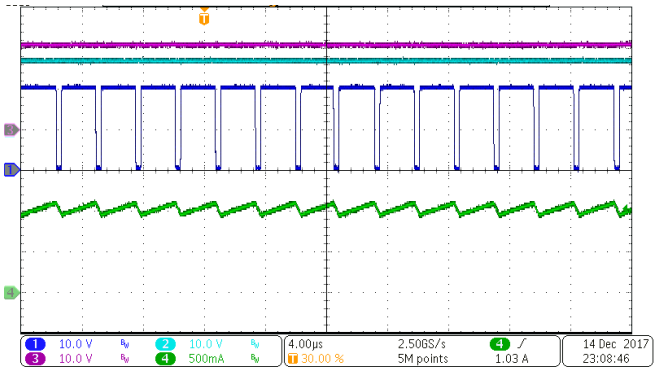
図 18. Boost Operation (CH1 + CH2 at Six LEDs)

図 19 and 図 20 show the steady state operation of the TPS92515HV-Q1 buck LED driver.



CH1: SW LED driver, CH2: VOUT LED driver, CH3: VOUT boost, CH4: IL LED driver

図 19. LED Driver Operation (CH1 at Eight LEDs)

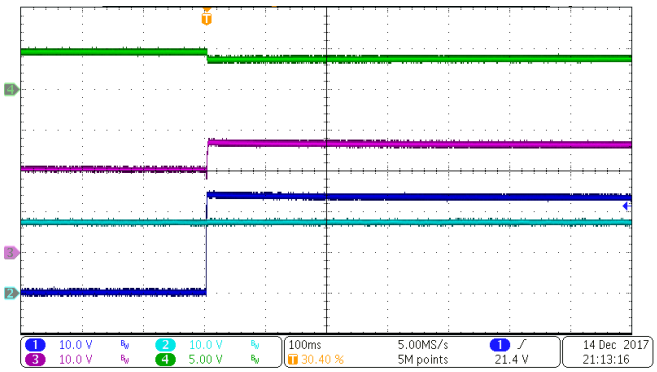


CH1: SW LED driver, CH2: VOUT LED driver, CH3: VOUT boost, CH4: IL LED driver

図 20. LED Driver Operation (CH1 at Six LEDs)

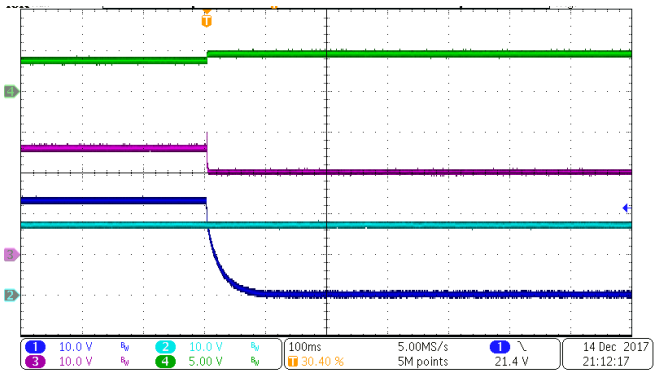
3.2.3 Adaptive Pre-Boost Control

図 21 and 図 22 show the operation of the adaptive pre-boost control. When a channel with a higher LED forward voltage gets activated, the adaptive pre-boost control regulates the boost voltage to a higher value. The circuit also regulates the boost voltage down once the channel get switched off.



CH1: VOUT LED driver (8 LEDs), CH2: VOUT LED driver (6 LEDs), CH3: VOUT boost, CH4: VOUT operational amplifier

図 21. Adaptive Pre-Boost Control Operation (up)



CH1: VOUT LED driver, CH2: VOUT LED driver, CH3: VOUT boost, CH4: VOUT operational amplifier

図 22. Adaptive Pre-Boost Control Operation (Down)

3.2.4 Efficiency

表 6 shows the efficiency of the design in different conditions. To achieve a total efficiency of 91%, each stage (boost and buck) operates with an efficiency of ≈ 95%.

表 6. Efficiency of TIDA-01520

CONDITION	EFFICIENCY
TIDA-01520 DESIGN	
CH1 + CH2 at eight LEDs	88.4%
CH1 + CH2 at six LEDs	88.3%
CH1 at eight LEDs	87.7%
CH1 at six LEDs	89.6%
TIDA-01520 DESIGN EXCLUDING LOSSES OF REVERSE PROTECTION DIODES D2, D5	
CH1 + CH2 at eight LEDs	91.2%
CH1 + CH2 at six LEDs	91.1%

3.2.5 Stability

図 23 shows the bode diagram of the LM5122-Q1 boost controller in this reference design. For a stable operation over all conditions, the control loop is designed more conservatively. If a higher bandwidth is needed, the external compensation can be changed.

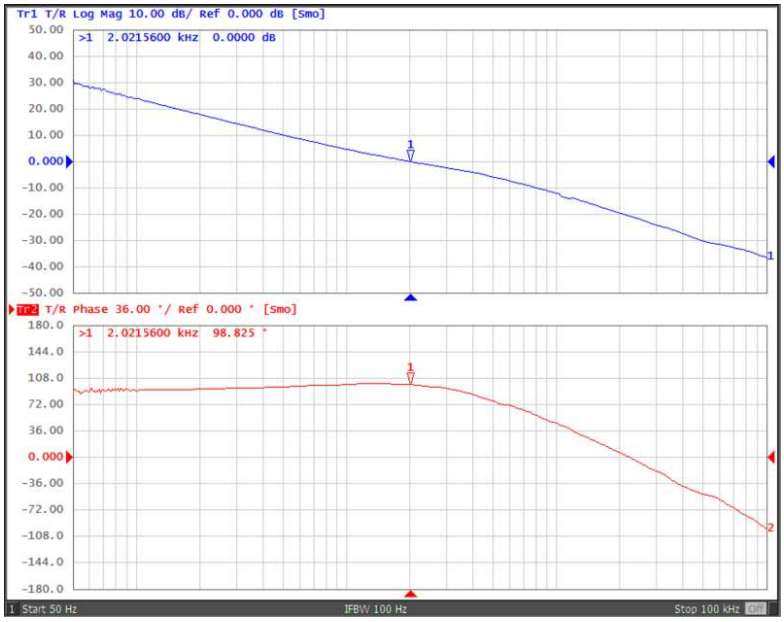


図 23. Frequency Response: CH1 + CH2 at Eight LEDs (≈ 48 W)

3.2.6 Electromagnetic Compatibility (EMC)

All test in this section are performed according to the CISPR 25 standard. 図 24 to 図 26 show the different setups. Note that the test setup for conducted emissions is a worst case scenario where the LED driver PCB is placed 5 cm above the reference ground plane. In a real application housing, the distance from the LED driver PCB to the reference ground plane will be higher; thus, the common-mode noise coupling will be lower.

図 24. CISPR 25 Conducted Emissions Setup

図 25. CISPR 25 Radiated Emissions Setup (Monopole)

図 26. CISPR 25 Radiated Emissions Setup

3.2.6.1 Conducted Emissions

図 27 and 図 28 show the conducted emissions at a power level of approximately 36 W (CH1 + CH2 at 6 LEDs) where the design is passing class 3. From 150 kHz to 30 MHz, the design is passing class 5.

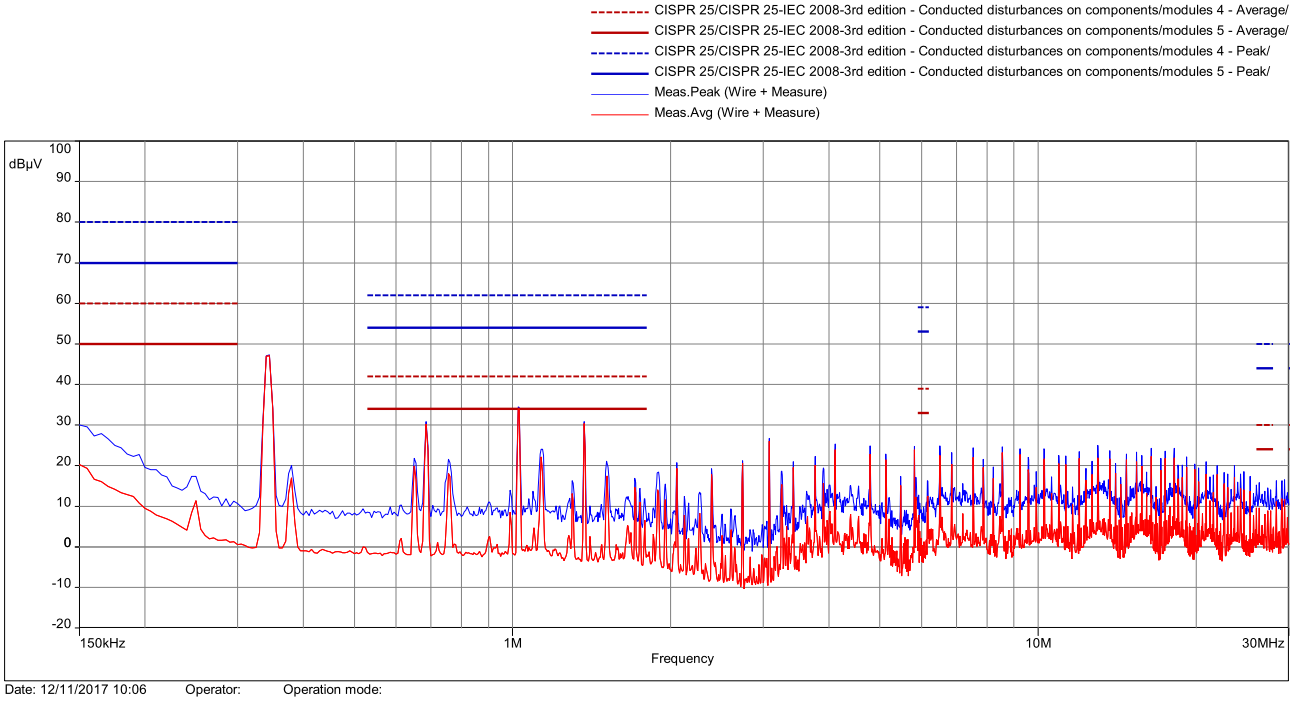


図 27. Conducted Emissions: 0.15 MHz to 30 MHz, CH1 + CH2 at Six LEDs (≈ 36 W)

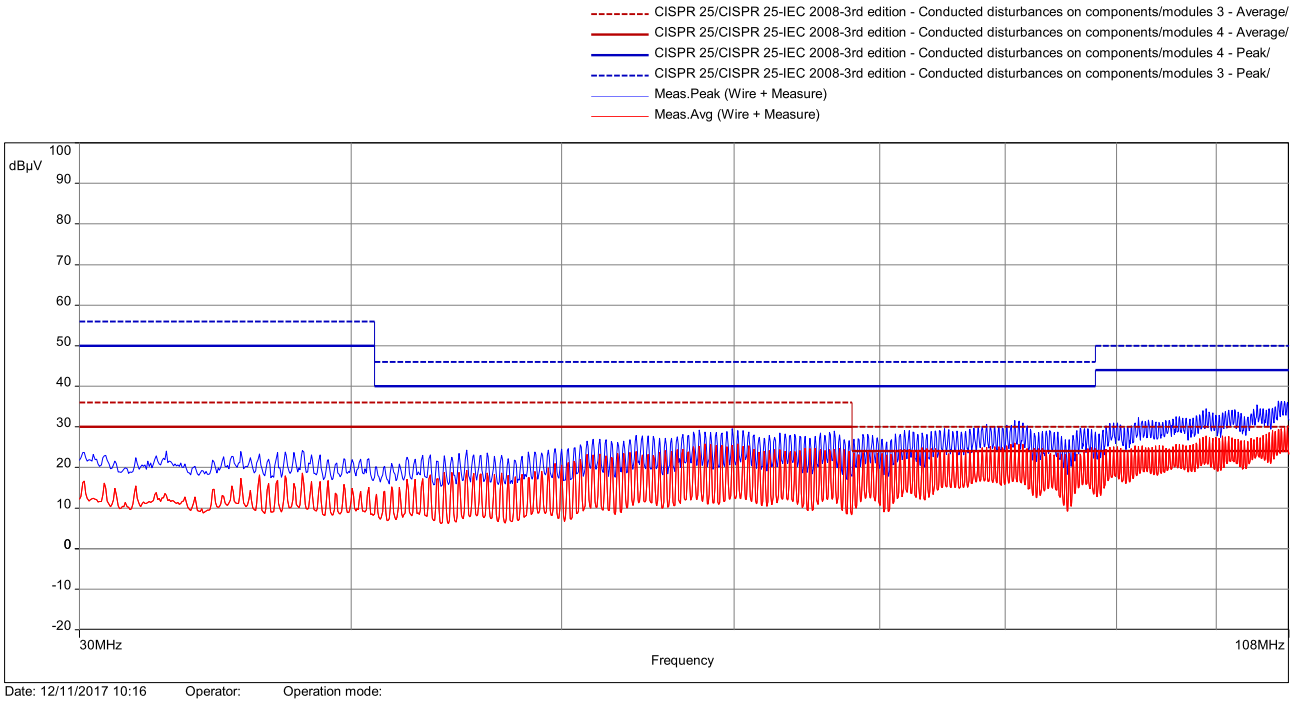


図 28. Conducted Emissions: 30 MHz to 108 MHz, CH1 + CH2 at Six LEDs (≈ 36 W)

図 29 and 図 30 show the conducted emissions at a power level of approximately 24 W (CH1 at 8 LEDs) where the design is passing class 4.

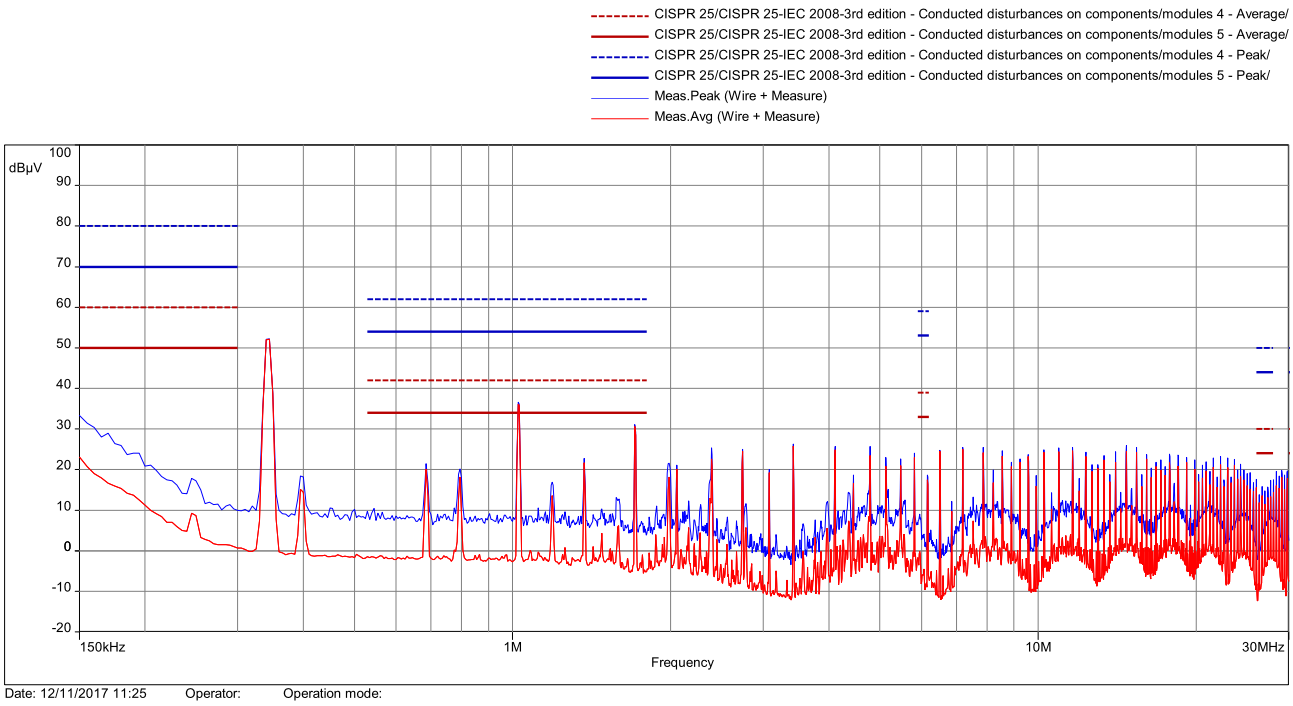


図 29. Conducted Emissions: 0.15 MHz to 30 MHz, CH1 at Eight LEDs (≈ 24 W)

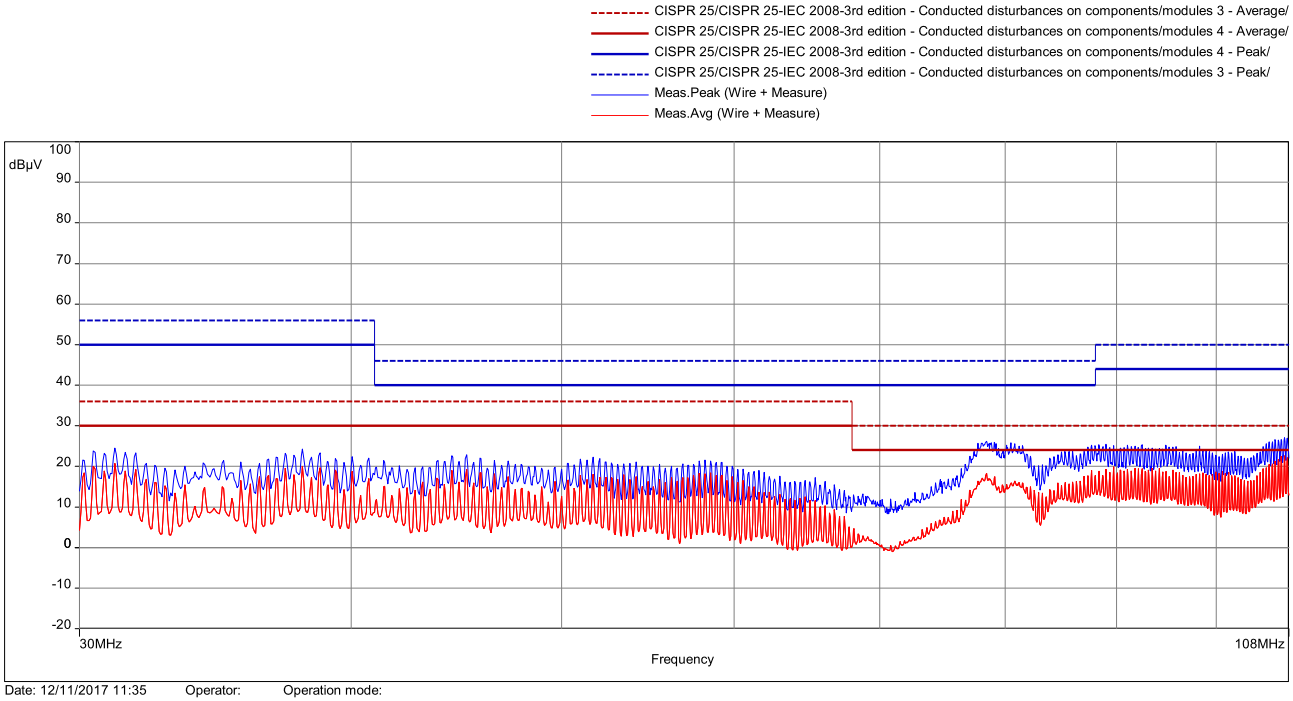


図 30. Conducted Emissions: 30 MHz to 108 MHz, CH1 at Eight LEDs (≈ 24 W)

図 31 and 図 32 show the conducted emissions at a power level of approximately 48 W (CH1 + CH2 at 8 LEDs) where the design is not passing class 3 in the high frequency range. From 150 kHz to 30 MHz, the design is passing class 4.

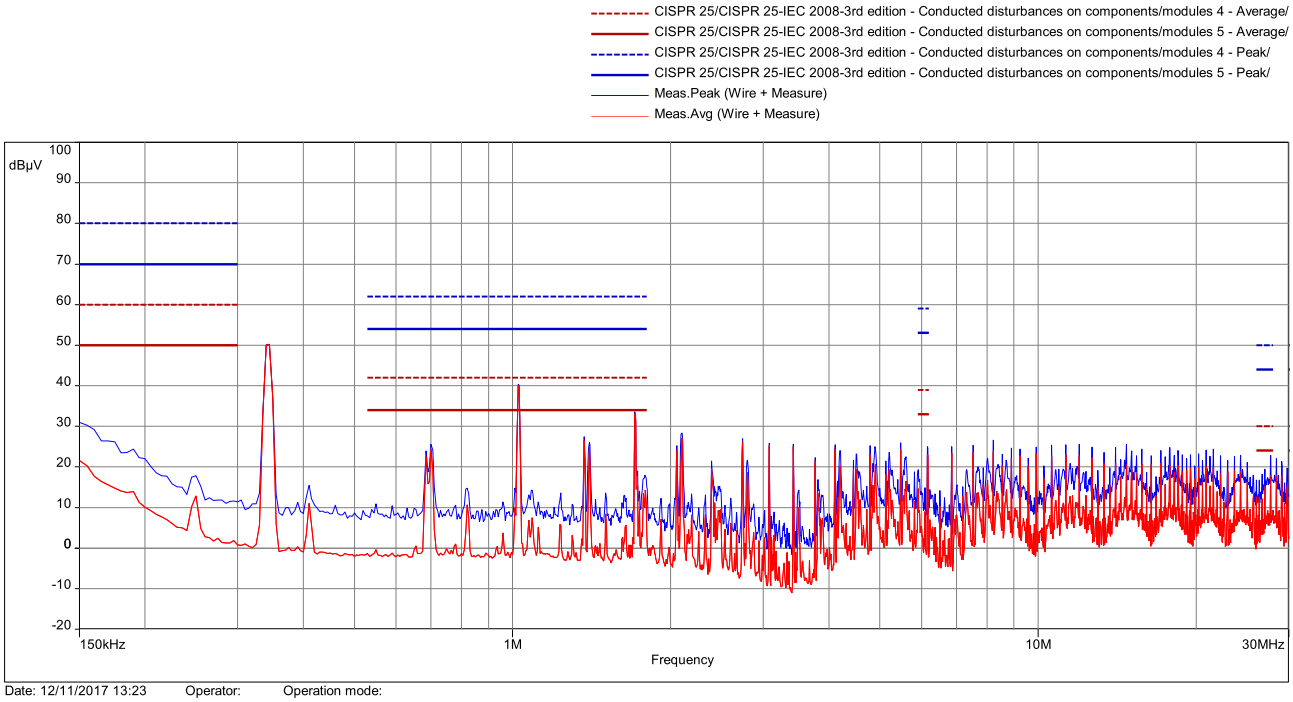


図 31. Conducted Emissions: 0.15 MHz to 30 MHz, CH1 + CH2 at Eight LEDs (≈ 48 W)

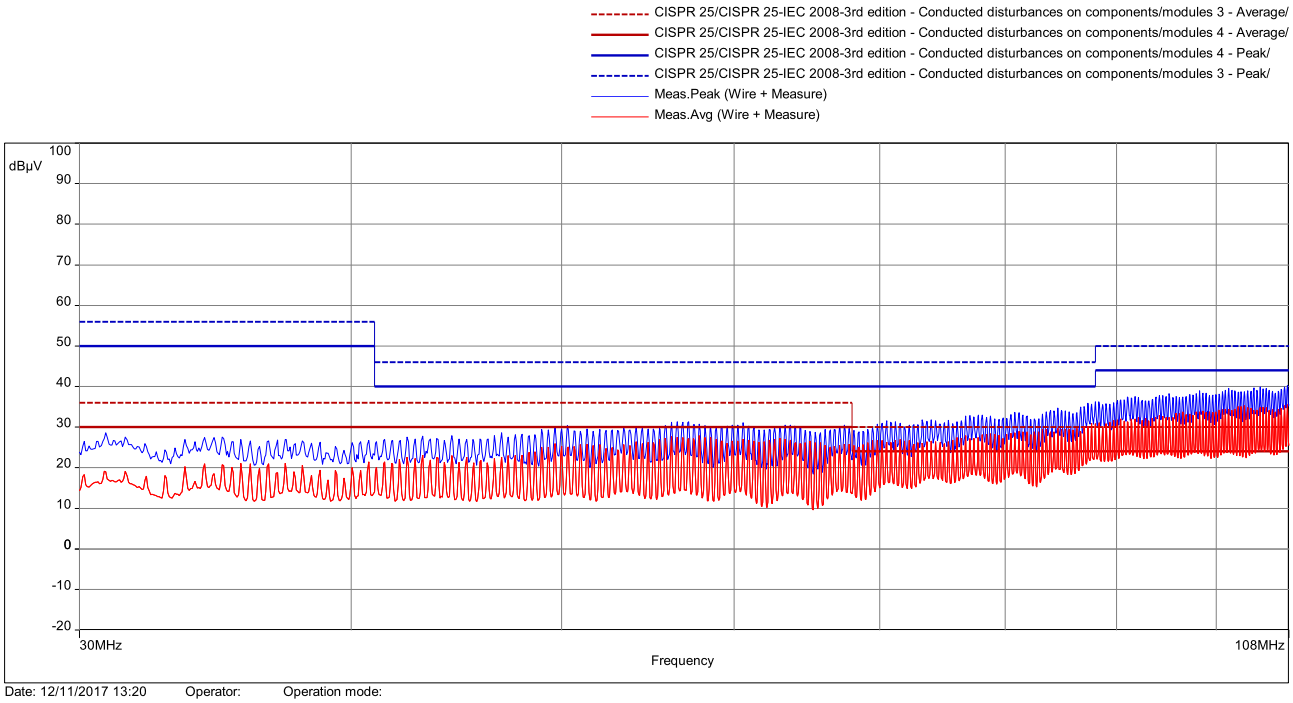


図 32. Conducted Emissions: 30 MHz to 108 MHz, CH1 + CH2 at Eight LEDs (≈ 48 W)

To further reduce the emissions in the higher frequency range, use a metal shielding or common-mode filter. 図 33 shows the conducted emissions from 30 MHz to 108 MHz at a power level of approximately 48 W (CH1 + CH2 at 8 LEDs) where a metal plate (10 × 10 cm) is placed below the reference design PCB. Now the design is passing class 3.

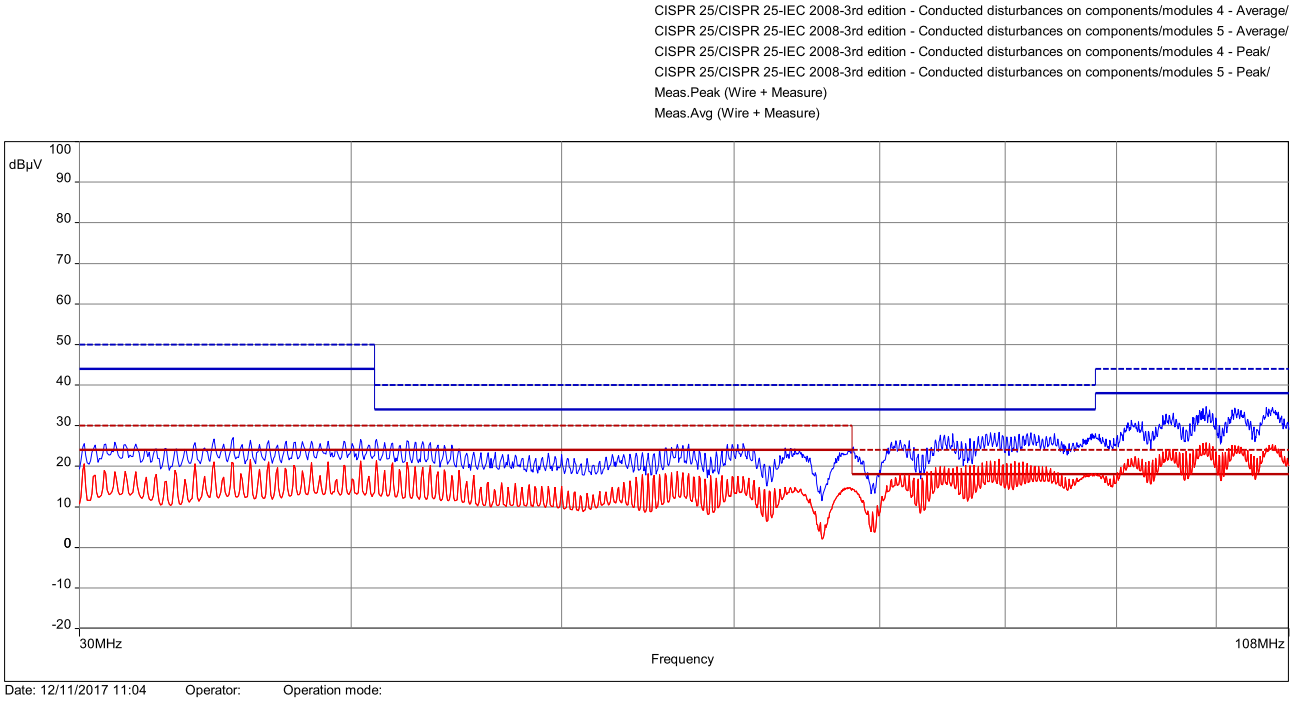


図 33. Conducted Emissions: 30 MHz to 108 MHz, CH1 + CH2 at Eight LEDs (≈ 48 W) + Shielding

図 34 shows the conducted emissions from 30 MHz to 108 MHz at a power level of approximately 48 W (CH1 + CH2 at 8 LEDs) where a common-mode choke (PLT10HH1026R0PNL) is used at the input connector of the reference design PCB. Now the design is passing class 5.

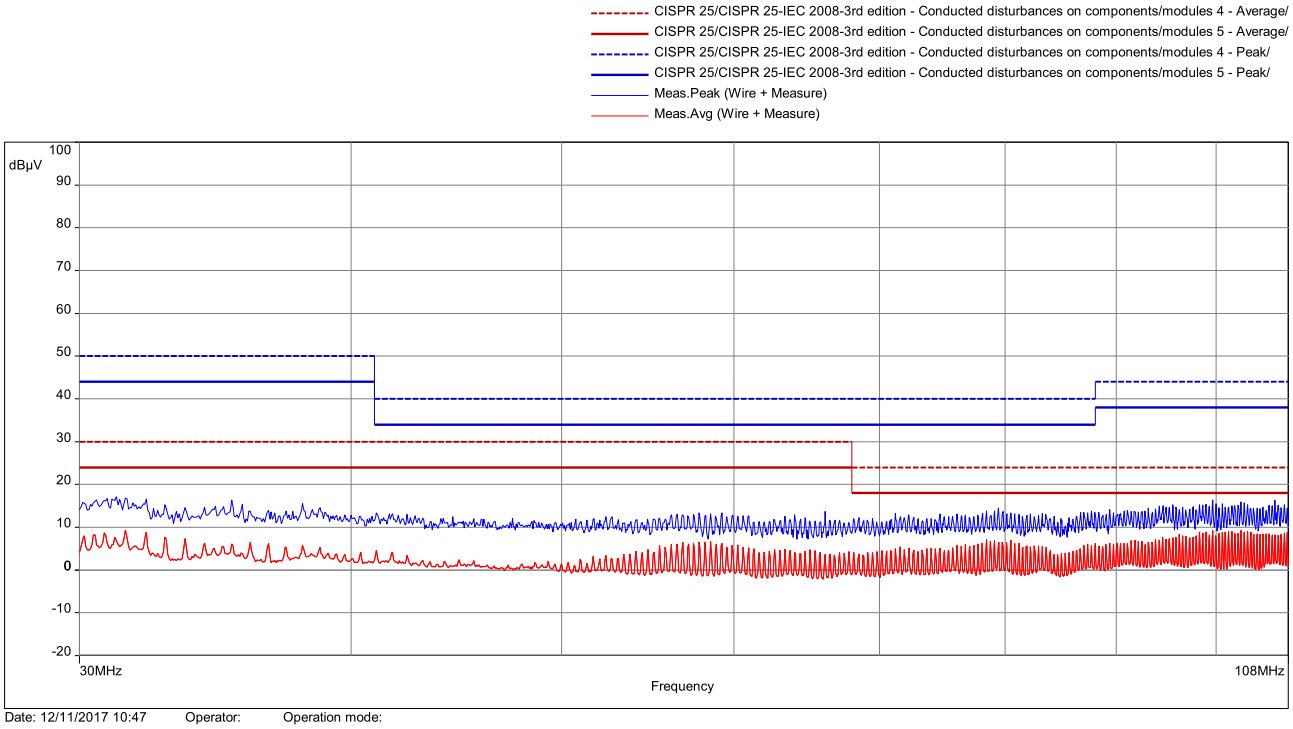


図 34. Conducted Emissions: 30 MHz to 108 MHz, CH1 + CH2 at Eight LEDs (≈ 48 W) + CM Choke

3.2.6.2 *Radiated Emissions*

図 35 and 図 36 show the radiated emissions at a power level of approximately 36 W (CH1 + CH2 at 6 LEDs) where the design is passing class 3. From 30 MHz to 1 GHz, the design is passing class 4.

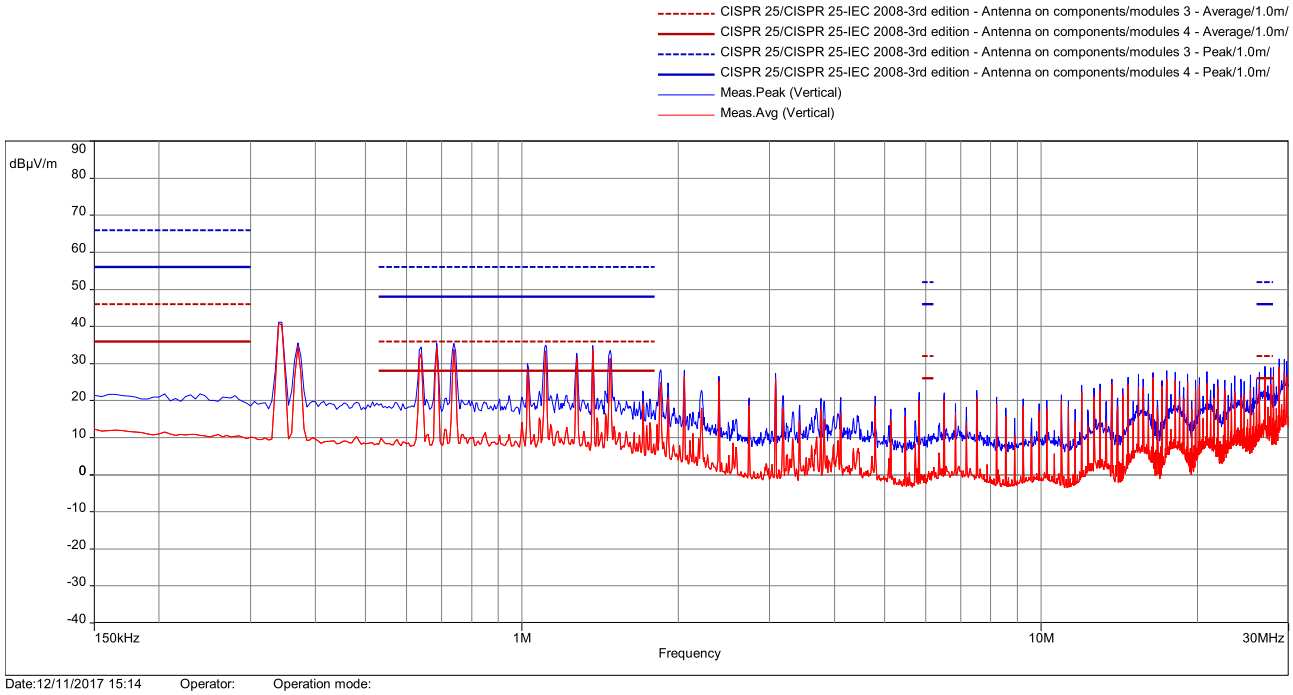


図 35. Radiated Emissions: 0.15 MHz to 30 MHz, CH1 + CH2 at Six LEDs (≈ 36 W)

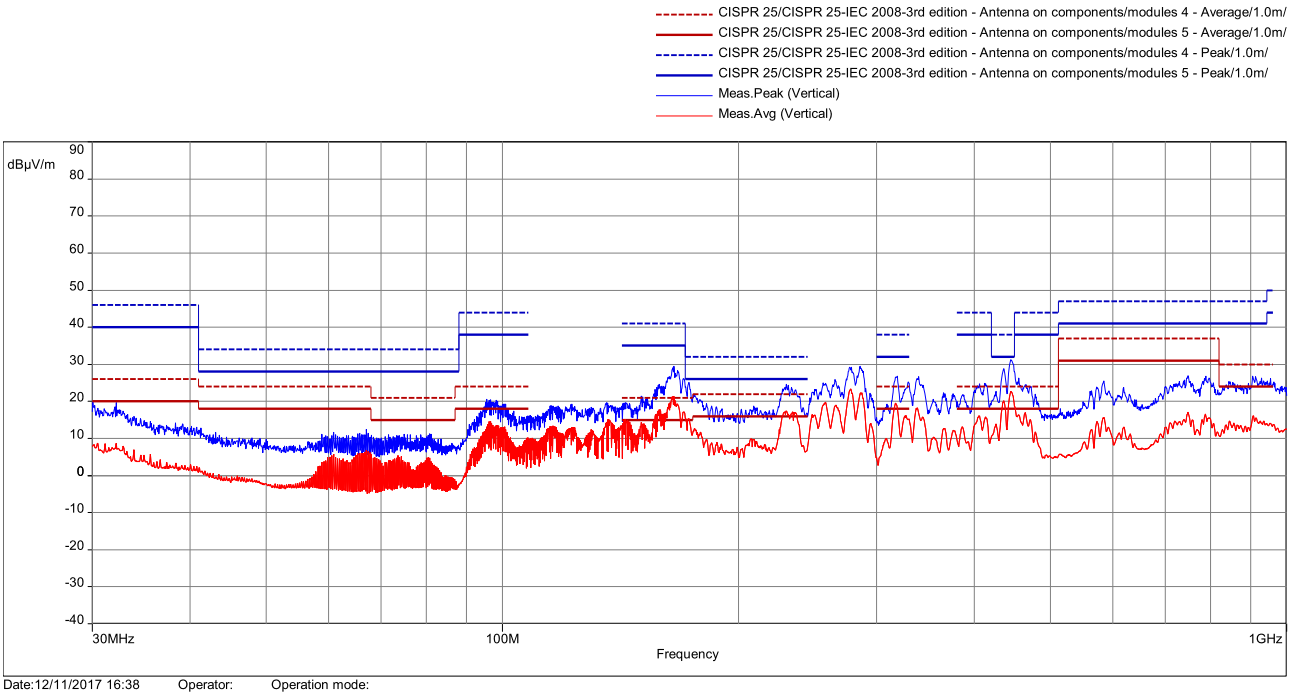


図 36. Radiated Emissions: 30 MHz to 1 GHz, CH1 + CH2 at Six LEDs (≈ 36 W)

図 37 and 図 38 show the radiated emissions at a power level of approximately 48 W (CH1 + CH2 at 8 LEDs) where the design is passing class 3. From 30 MHz to 1 GHz, the design is passing class 4.

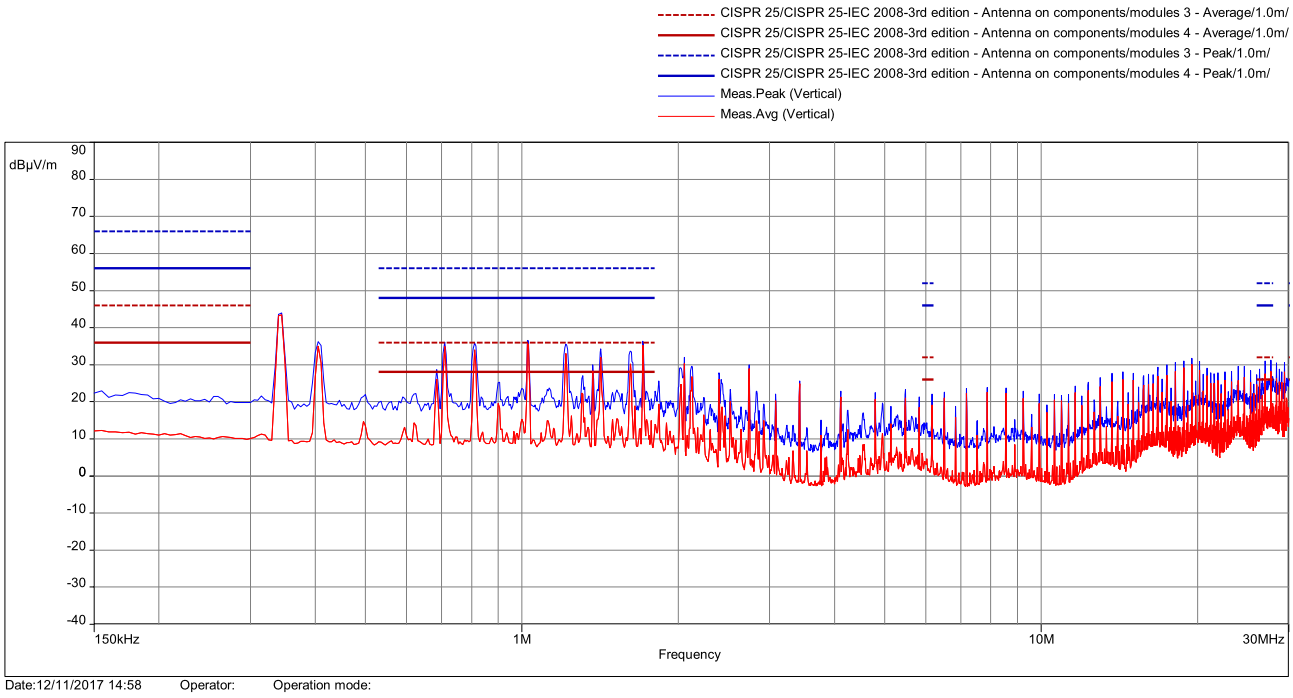


図 37. Radiated Emissions: 0.15 MHz to 30 MHz, CH1 + CH2 at Eight LEDs (≈ 48 W)

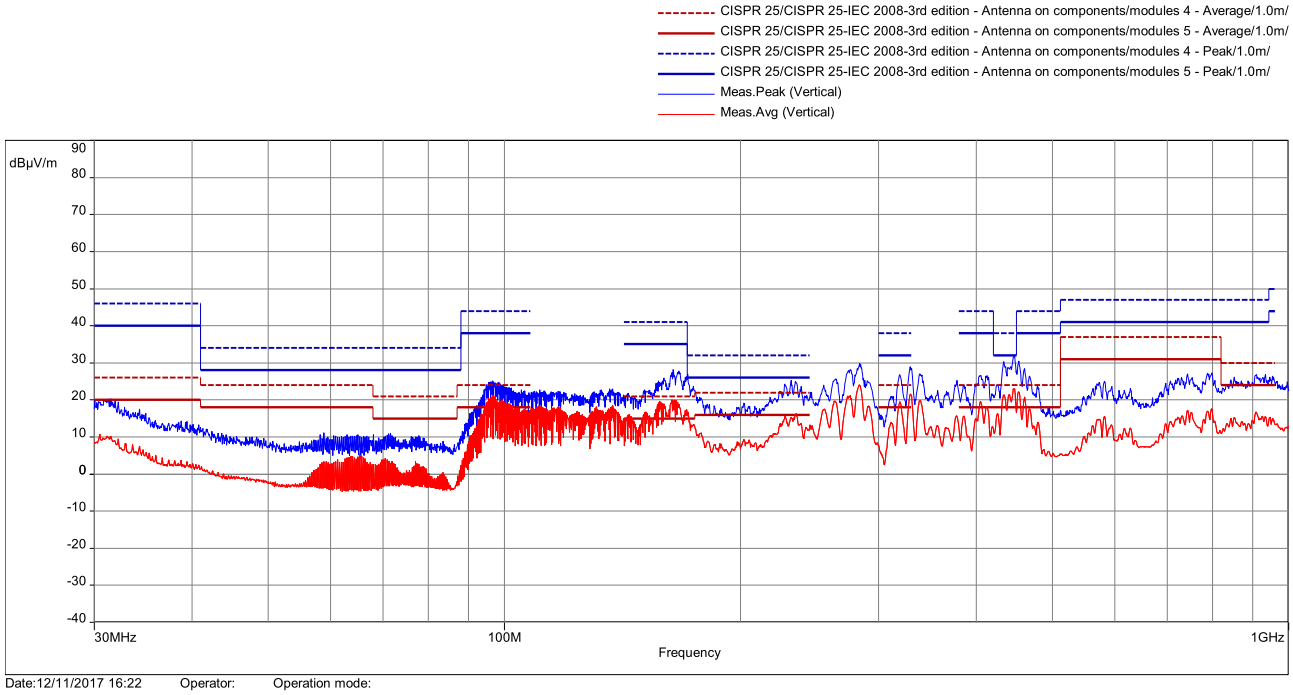


図 38. Radiated Emissions: 30 MHz to 1 GHz, CH1 + CH2 at Eight LEDs (≈ 48 W)

3.2.7 Thermal Performance

図 39 through 図 42 show the thermal behavior for different conditions. The highest temperature is on the input protection diodes. As described in 2.3.2, smart diode controllers such as the LM5050-1-Q1 or LM74700-Q1 can be used, which result in lower power losses. To improve the thermal performance of the whole board, consider implementing the following items:

- Add more layers on the PCB
- Increase the PCB size
- Increase the copper thickness to 2 oz
- Adding a heat sink

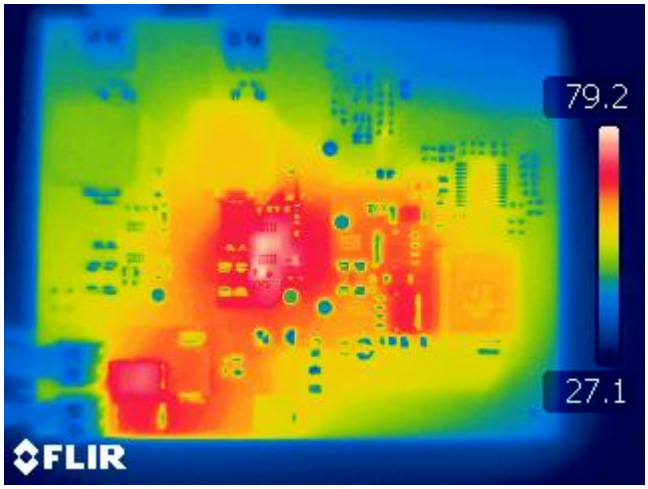


図 39. Thermal Image: CH1 at Eight LEDs (≈ 24 W)

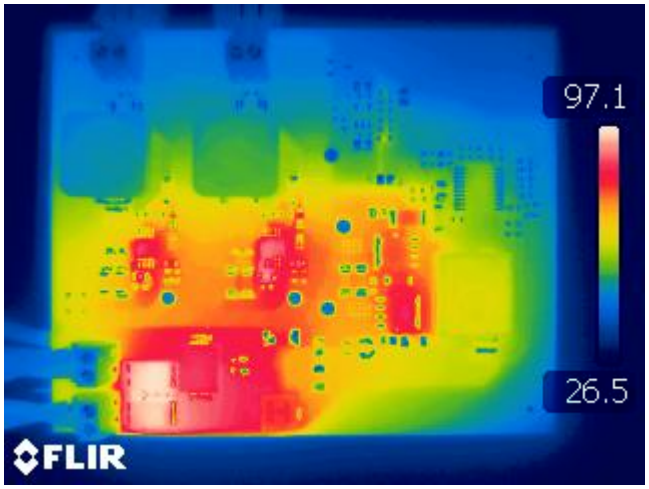


図 40. Thermal Image: CH1 + CH2 at Eight LEDs (≈ 48 W)

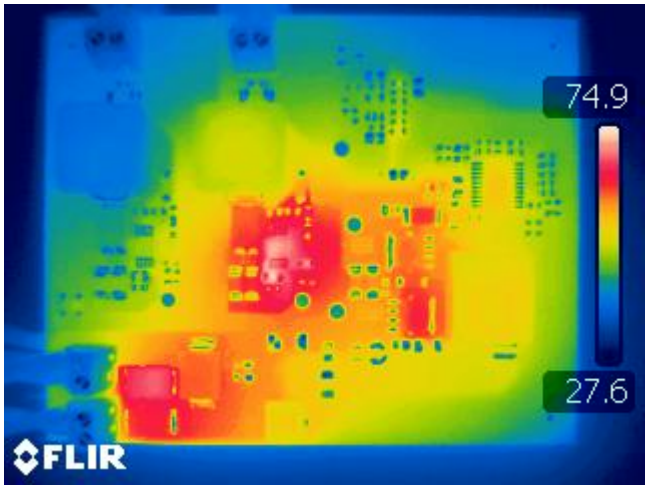


図 41. Thermal Image: CH1 at Six LEDs (≈ 18 W)

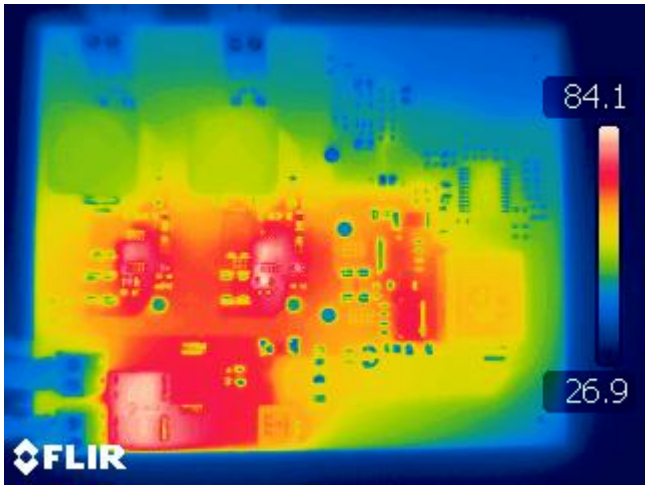


図 42. Thermal Image: CH1 + CH2 at Six LEDs (≈ 36 W)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01520.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01520.

4.3 PCB Layout Recommendations

The layout of the boost controller as shown in 図 43 is created by following the layout example and guidelines in the Layout section of *LM5122 Wide-Input Synchronous Boost Controller With Multiple Phase Capability*.

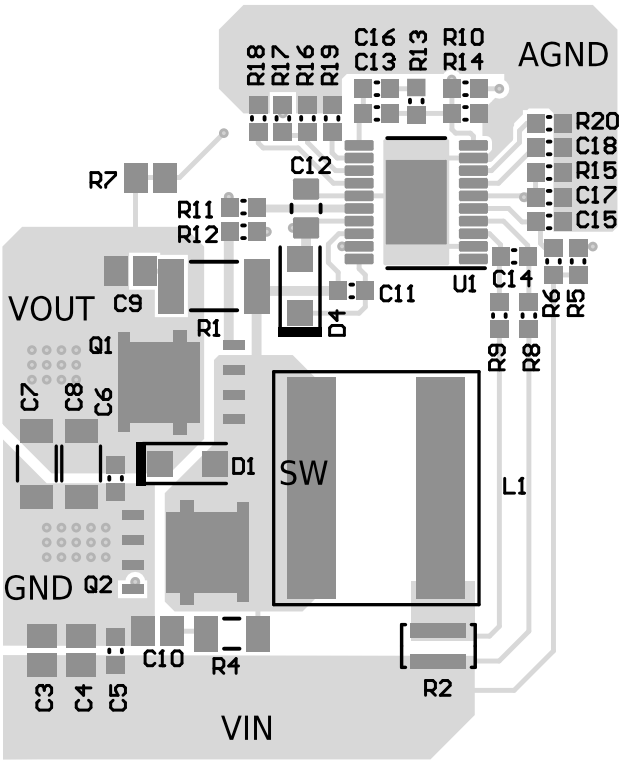


図 43. LM5122-Q1 Boost Controller Layout (Top Layer)

The layout of the boost controller as shown in 図 44 is created by following the layout example and guidelines in the Layout section of *TPS92515x 2-A, Buck LED Driver with Integrated N-channel FET, High-Side Current Sense, and Shunt FET PWM Dimming Capability*.

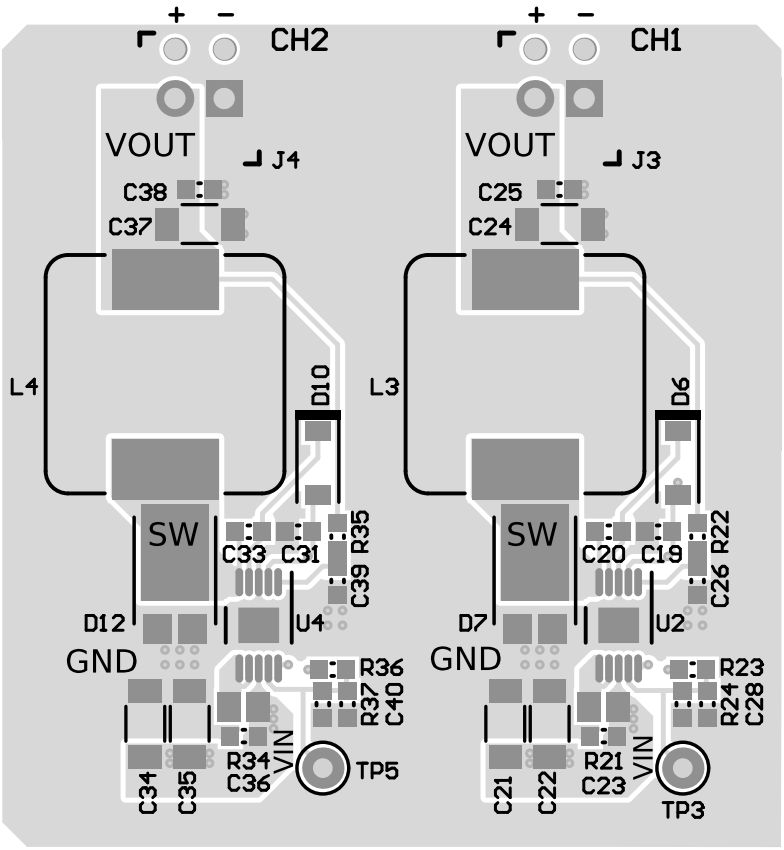


図 44. TPS92515HV-Q1 Buck LED Driver Layout (Top Layer)

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01520.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01520.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01520.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01520.

5 Related Documentation

1. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters Application Report*
2. Texas Instruments, *LM5122 Wide-Input Synchronous Boost Controller With Multiple Phase Capability Data Sheet*
3. TI E2E Community, *Power Tips: Calculate an R-C snubber in seven steps*
4. Texas Instruments, *AN-1889 How to Measure the Loop Transfer Function of Power Supplies Application Report*
5. Texas Instruments, *TPS92515x 2-A, Buck LED Driver with Integrated N-channel FET, High-Side Current Sense, and Shunt FET PWM Dimming Capability Data Sheet*
6. Texas Instruments, *PMP9796 - 5V Low-Power TEC Driver Reference Design*

5.1 商標

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