参考資料

TI Designs: TIDA-01638
バックアップ電源のシームレスな切り替えのリファレンス・デザイン

概要

このTIリファレンス・デザインでは、冗長化電源との電源多重化を紹介します。1つの電源に障害が発生した場合、システムはバックアップ電源に切り替わり、下流の負荷に対して電力を途切れなく供給する必要があります。電源の冗長性により、1つの電源に障害が発生しても、システムは自動的に他の電力レールに切り替わり、データの消失防止を保証できます。TIDA-01638統合リファレンス・デザインは、電圧レール間でシームレスに切り替えを行い、出力電圧ディップを最小化できます。アクティブな電流制限、過電圧保護、および常時オンの逆電流保護により、システムのストレスや、予期しない逆電流条件も防止できます。このデザインは、光ライン・カード、ネットワーク接続ストレージ、および冗長化電源の間でシームレスな移行を必要とする電源システムなどのアプリケーションに有用です。

リソース

TIDA-01638	デザイン・フォルダ
TPS2121	プロダクト・フォルダ
REF3325	プロダクト・フォルダ
TPS2595	プロダクト・フォルダ
TPS564201	プロダクト・フォルダ

TI E2E™ Community

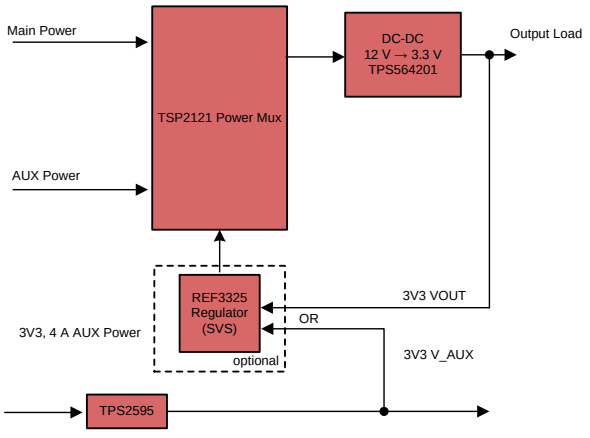
E2E™ エキスパートに質問

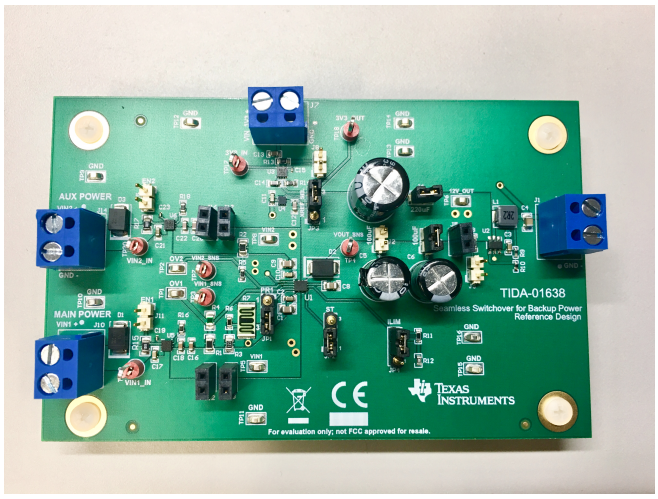
特長

- 5µsの移行時間と外部基準電圧によりシームレスな切り替えを実現
- 優先電源の選択
- 過電圧保護と電流制限
- ホット・プラグ保護
- 入力セトリング、ソフト・スタート制御
- ステータス出力の表示

アプリケーション

- アドイン・カード
- ネットワーク・インターフェイス・カード
- ソリッド・ステート・ドライブ(SSD) - エンタープライズ
- IPネットワーク・カメラ
- シングル・ボード・コンピュータ





1 System Description

Redundant power is critical in systems that require uninterrupted sources of power. If the output voltage were to dip on these systems, this could cause the downstream load to reset or enter an undervoltage lockout condition. Therefore, if the main power source were to fail, the system needs to switchover to a backup power source without interrupting normal operation. To minimize the voltage dip on the output, the system needs to detect whenever the main supply begins to drop and quickly switchover to the backup source. When the main power source is restored, the system switches back to the main power source.

This reference design showcases seamless switchover between two 12-V power supplies. Priority is given to IN1, the main power rail, and switches over to the backup rail, IN2, whenever IN1 dips past a specified threshold. To minimize the offset when comparing the voltages between the two rails, an external comparator breakout (CP2) is used. By connecting an external precision voltage reference (XREF) to CP2, this minimizes the voltage error while switching between VIN1 and VIN2. The ST pin also provides adjustable hysteresis when comparing the voltage on VIN1 to CP2.

The reference design is a straightforward, compact design that fully integrates priority power mux operation. Additional features include over-voltage protection, fast reverse current blocking, active current limiting, and soft start control. Large input capacitors are suggested if switching between high current rails. During fast switchover, a sudden change in current, di/dt (4 A / 5 µs), could strain the input supplies. The capacitors help to provide a temporary power source for fast switchover. Furthermore, the TPS2595 eFuses on the input channels allow for fast input capacitor charging. If the system is tested with long inductive cables, the sudden changes in current could cause spikes on both input channels. The TPS2595 eFuses are not necessary on the final design, but allow for testing with longer cables that would otherwise limit fast switchover due to inductive ringing. Finally, the downstream DC/DC replicates common power architectures that have downstream converters powering various voltage rails.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	V_{IN}	12.1 V +/- 3%
Output voltage range	V_{OUT}	12 V +/- 5%
Load Current	I_{OUT}	2.5 A(1)
Output Capacitance	C_{OUT}	320 µF
Fast-Switchover Time	t_{SW}	5 µs
On-Resistance	R_{ON}	56 mΩ

(1) 2.5 A at 12-V output of the TPS2121, if DC/DC is enabled the max load current will be less due to I_{MAX} from the converter

2 System Overview

2.1 Block Diagram

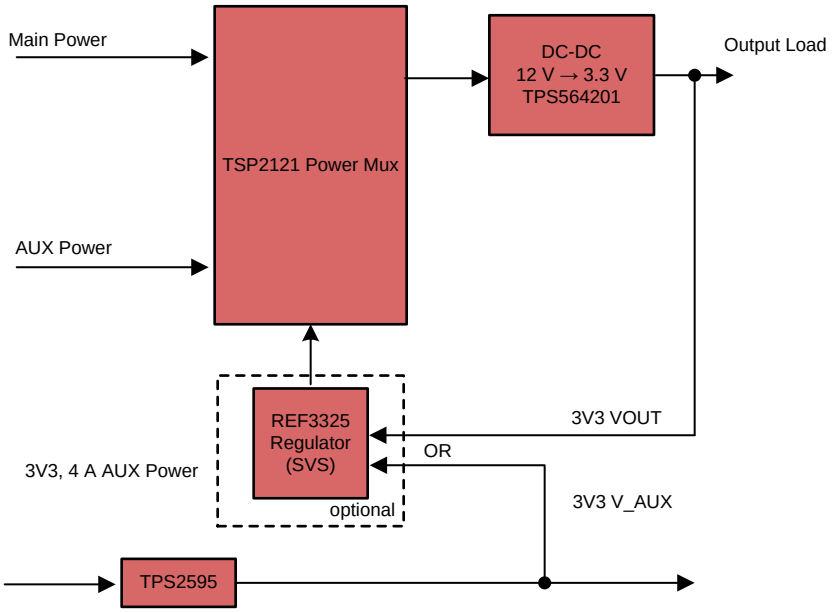


図 1. TIDA-01638 Block Diagram

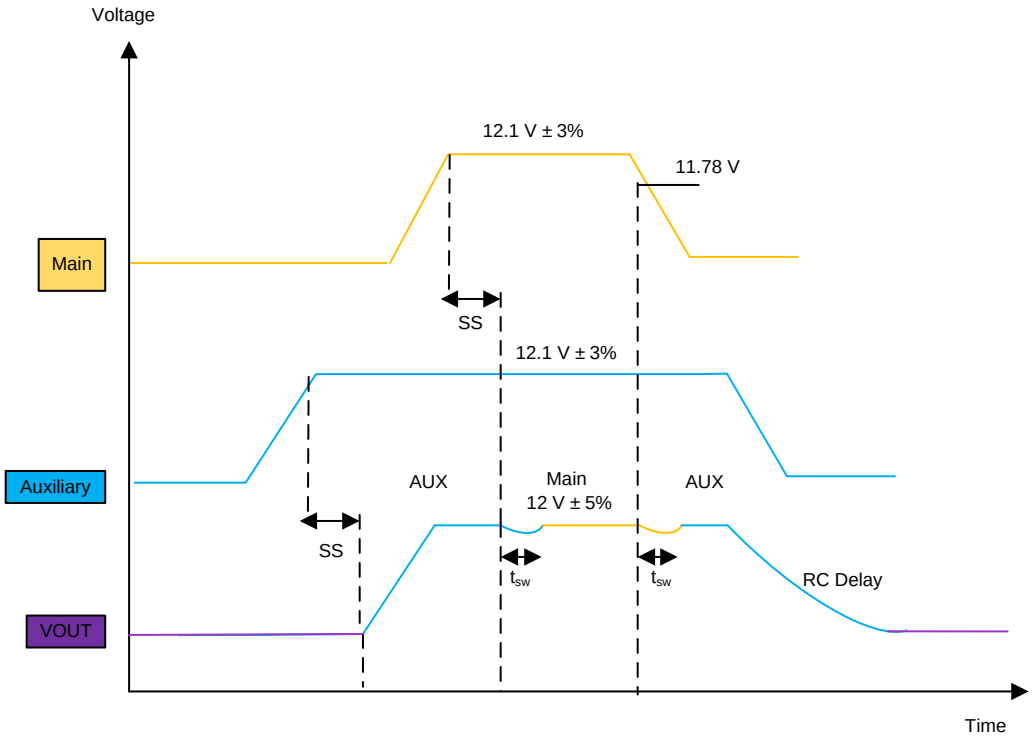


図 2. Seamless Switchover Timing Diagram

2.2 Design Considerations

2.2.1 External Voltage Reference Control Scheme (XREF)

An external comparator breakout (CP2) can be used to reduce the switchover voltage error for a more seamless switchover. This is also called External Voltage Reference Control Scheme (XREF). To enable the XREF configuration, the voltage on the CP2 pin needs to be higher than the internal voltage reference, VREF, (typically 1.06 V). When the CP2 voltage is higher than VREF, the pins can be considered "high". When the CP2 pin is high, priority is given to PR1 (IN1) or CP2 (IN2) depending on which pin contains the higher voltage. In other words, if the voltage on PR1 is 2.6 V while the voltage on CP2 is 2.5 V, then IN1 will be given priority. Once the voltage on PR1 drops below 2.5 V, the device will check if a reverse current condition exists. If not, then the TPS2121 will fast switchover to IN2. Each channel has always on reverse current blocking. If the output falls within V_{RCB} of one of the inputs, 25mV (typ), the device will quickly switch channels to prevent reverse current.

The CP2 pin can be connected to an external voltage source to provide a more accurate voltage comparison against PR1. The pin can be connected to a precision voltage reference or even the output of the device. In this design, the REF3325 provides an external reference of 2.5 V ± 0.15% (2.50375V). If the voltage on PR1 is higher than this external reference, priority will be given to IN1. If an accurate external voltage comparison is not required, CP2 can be connected to IN2 using a resistor divider, or a different supply. However, the voltage won't be as precise as the external voltage reference, and could vary depending on the input supply, resistor tolerances, and input parasitics.

The system specifications detail the input voltage range for 12.1 V ± 3%. The desired operation is to switch to IN2 when IN1 falls outside of its normal operating range. Therefore, the resistor divider on PR1 must be configured so the pin dips below 2.50375V (CP2) before IN1 crosses 11.73 V (12.1 V - 3%). Once this occurs, the design will start fast switchover to IN2 within 5 us.

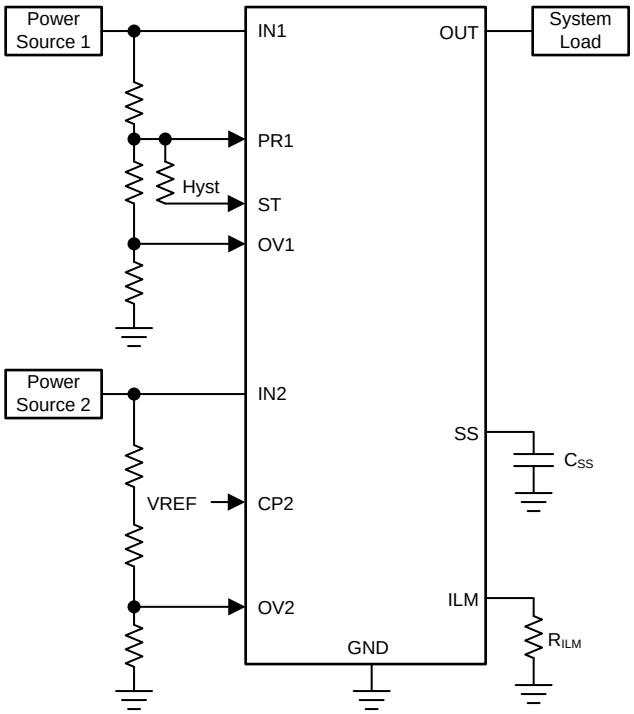


図 3. XREF Configuration Example

2.2.2 Adjustable Hysteresis

During normal operation, the switchover between IN1 and IN2 occurs whenever the voltage on PR1 is greater than or less than the voltage on CP2. For systems that require precise switchover, such as this reference design, the voltage on PR1 needs to remain close to the voltage on CP2 during normal operation. On this reference design, the voltage on PR1 is determined using a simple resistor divider.

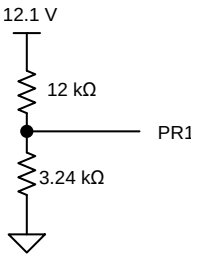


図 4. V_{PR1} Calculation

With the REF3325 connected to CP2, the voltage on CP2 is 2.5 V ± 0.15%. Switchover from IN2 to IN2 will occur when the voltage on PR1 is lower than CP2. From the design specifications, this occurs at 12.1 - 3%. Therefore, at 11.73 V, the voltage on PR1 needs to be lower than 2.5034 (2.5 V ± 0.15% from the REF3325) in order for the switchover from IN1 to IN2 to occur. 式 1 shows that the voltage on PR1 will be lower than the CP2 voltage at 11.73 V.

$$V_{PR1} = 11.73\ V \times \frac{3240\ \Omega}{3240\ \Omega + 12\ k\Omega} = 2.493\ V \quad (1)$$

However, if IN1 were to remain at 11.73 V due to system conditions or the input supplies being affected, any transient event or system noise could slightly raise and lower the voltage on the PR1 pin. This would cause the device to switch between IN1 and IN2 repeatedly, potentially degrading system performance and the input supplies. For example, if 50 mV of noise was introduced into the system while IN1 was at 11.73 V, the voltage on PR1 would raise to 2.504, switching the input supply back to IN1.

By connecting an extra resistor from PR1 to the ST pin, this can be used to provide precise, adjustable hysteresis. When the device uses IN2 as the output supply, the ST pin is pulled to GND. Therefore, if an extra resistor was connected from PR1 to ST, it will slightly lower the resistance on PR1, R_{PR1}. This will slightly lower the voltage on PR1. Therefore, if IN2 is the output supply while IN1 remains at 11.73 V, the voltage on PR1 will be slightly lower than if IN1 were the output supply. This will prevent small transients from causing accidental switchover. 図 5 shows the configuration used in the reference design.

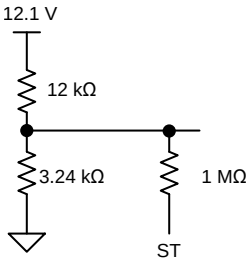


図 5. External Pull-down Resistor

Using the following resistor network, the resistors were configured to achieve the necessary voltage on the PR1 pin.

R_{PR1} Calculation

$$R_{PR1} = \frac{1\,M\Omega \times 3.24\,k}{1\,M\Omega + 3.24\,k} = 3229.54\ \Omega \quad (2)$$

V_{PR1} Calculation

$$V_{PR1} = 11.73\ V \times \frac{3229.54\ \Omega}{3229.54\ \Omega + 12\,k\Omega} = 2.487\ V \quad (3)$$

After adding hysteresis from ST to PR1, this prevents slight transients or noise from accidentally switching the input back to IN1. Adding to the previous example, if a 50-mV transient event occurred on IN1 at 11.73 V while IN2 was powering the output, the voltage on PR1 would rise to 2.5044 without adding hysteresis, causing the device to switch back to IN1. However, if an external 1MΩ resistor is added for hysteresis, the voltage on PR1 becomes 2.497, which is below the CP2 threshold.

By adding the external 1-MΩ resistor, when IN1 returns to 11.73 V the voltage on PR1 becomes 2.497V. Therefore, the device won't switch back to IN1 until the voltage on IN1 reaches 11.81 V. Compared to 2.5034V on CP2, the external resistor adds 0.26% hysteresis before switching over.

2.2.3 Output Voltage Dip and Fast Switchover

After input settling and soft start time, the reference design utilizes a fast switchover to minimize output voltage dip. Nominal fast switchover time is 5 μs. The amount of voltage drop on the output is dependent on the output load current (I_{OUT}), and the load capacitance (C_{OUT}). The minimum output voltage ($V_{OUT,MIN}$) during switchover can be found using the following equations:

$$V_{OUT,MIN} = V_{SW} - V_{DIP} \quad (4)$$

$$V_{DIP} = t_{SW} \times \left(\frac{I_{OUT}}{C_{OUT}} \right) \quad (5)$$

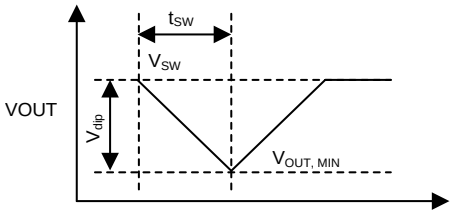


図 6. Graph of V_{DIP}

V_{DIP} will occur after the device recognizes the voltage on PR1 crosses the CP2 voltage. For this reference design, V_{DIP} will occur while switching from IN1 to IN2 after the voltage on IN1 reaches 11.78 V.

The maximum output dip (V_{DIP}) and output load current (I_{OUT}) are dependent on system specifications, as shown below. These values can be predetermined and adjusted by varying the load capacitance of the system. For this reference design, the calculations are shown in 式 6 and 式 7:

Nominal V_{DIP} Calculation

$$V_{DIP} = 5\ \mu s \times \left(\frac{2.5\ A}{320\ \mu F} \right) = 0.04\ V \quad (6)$$

Therefore, the output of the reference design will dip to 11.73 V before starting fast switchover, and then drop an additional 0.04 V while switching between IN1 and IN2.

In a worst-case scenario, fast switchover can occur in 15 µs. Using this information, the maximum voltage dip is calculated to be 0.12-V dip. In a worst case scenario, the voltage on the ouput can dip to 11.61 V before switching to the other 12-V supply. This still remains within the system specifications for maximum V_{OUT} drop, which was set at 12 V +/- 5% (11.4 V).

Worst-Case V_{DIP} Calculation

$$V_{DIP} = 15\ \mu s \times \left(\frac{2.5\ A}{320\ \mu F} \right) = 0.12\ V \tag{7}$$

2.2.4 Overvoltage Calculations

Output overvoltage protection is available for both IN1 and IN2 if either applied voltage is greater than the maximum supported load voltage. The VREF comparator on the OV1 / OV2 pins allows for the overvoltage protection threshold to be adjusted independently. When overvoltage is engaged, the corresponding channel will turn off immediately if the pin reaches 1.1 V. The reference design will also fast switchover to the other input if it is a valid voltage.

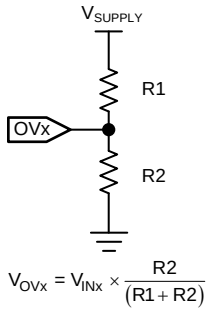


図 7. OV Resistors

In this reference design, overvoltage on both channels is programmed at 12 V+15% (~13.8 V). The OV Resistor Calculations is shown in 式 8:

$$1.1\ V = V_{INx} \times \left(\frac{5\ k\Omega}{5\ k\Omega + 57.6\ k\Omega} \right) = 13.77\ V \tag{8}$$

2.2.5 Total Solution Size

As designs are continually getting smaller and sleeker, designs require a more space-conscious layout. By using the integrated power mux device, the system can remain as compact and space efficient as possible.

A priority power mux solution traditionally requires a multi-chip design. To seamlessly switch between input rails and minimize voltage dip, many configurations contain OR-ing controllers alongside fuses and diodes for protection. This reference design can provide seamless switchover with only an external voltage source, which reduces solution size, cost, and number of components.

図 8 below shows an example of the total solution size. This boxed-off area contains the external reference voltage (REF3325) and the TPS2121.

注: The reference design contains a larger solution size to test multiple configurations.

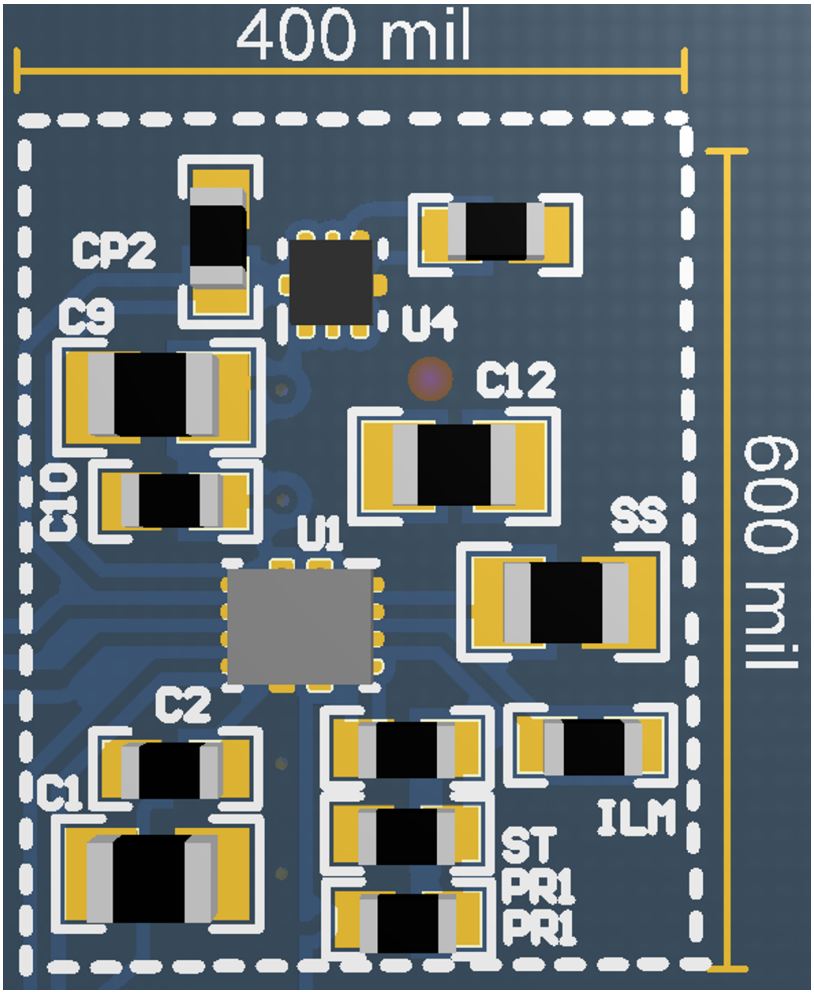


図 8. TPS2121 Example Solution Size

2.3 Highlighted Products

2.3.1 TPS2121

The TPS2121 is a dual input, single-output Power Multiplexer that will automatically detect, select, and seamlessly transition between available inputs. Active current limting protects against overcurrent events, and always-on reverse current protection blocks reverse current. Priority can be automatically given to the highest input voltage or manually assigned to a lower voltage to support both ORing and Source Selection Operation.

2.3.2 REF3325

The REF3325 is a low-power, precision, low-dropout voltage reference device. Small size and low power consumption (5-µA max) make the REF3325 ideal for a wide variety of portable and battery-powered applications. The REF33xx can be operated at a supply voltage 180 mV above the specified output voltage under normal load conditions. All models are specified for the wide temperature range of –40°C to +125°C.

2.3.3 TPS2595

The TPS2595x family of eFuses is a highly-integrated circuit protection and power management solution in a small package. The devices use few external components and provide multiple protection modes. They are a robust defense against overloads, short circuits, voltage surges, and excessive inrush current. Current limit level can be set with a single external resistor. Over-voltage events are limited by internal clamping circuits to a safe fixed maximum, with no external components required. Applications with particular inrush current requirements can set the output slew rate with a single external capacitor.

2.3.4 TPS564201

The TPS564201 is a simple, easy-to-use, 4-A synchronous step-down converter in SOT-23 package. These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low-equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components. The TPS564201 operates in pulse skip mode, maintaining high efficiency during light load operation. The TPS564201 is available in a 6-pin 1.6-mm × 2.9-mm SOT (DDC) package, and specified from a –40°C to 125°C junction temperature

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 System Overview

The Seamless Switchover Reference Design can be configured in multiple modes of operation to accommodate different system requirements. The main configuration, XREF, can accommodate systems that require fast switchover between input power sources while minimizing the output voltage dip. This reference design can also support other modes of operation, including VCOMP and VREF. VCOMP simply compares the voltages on both channels and gives priority to the channel with higher voltage. VREF gives priority between power sources without fast switchover.

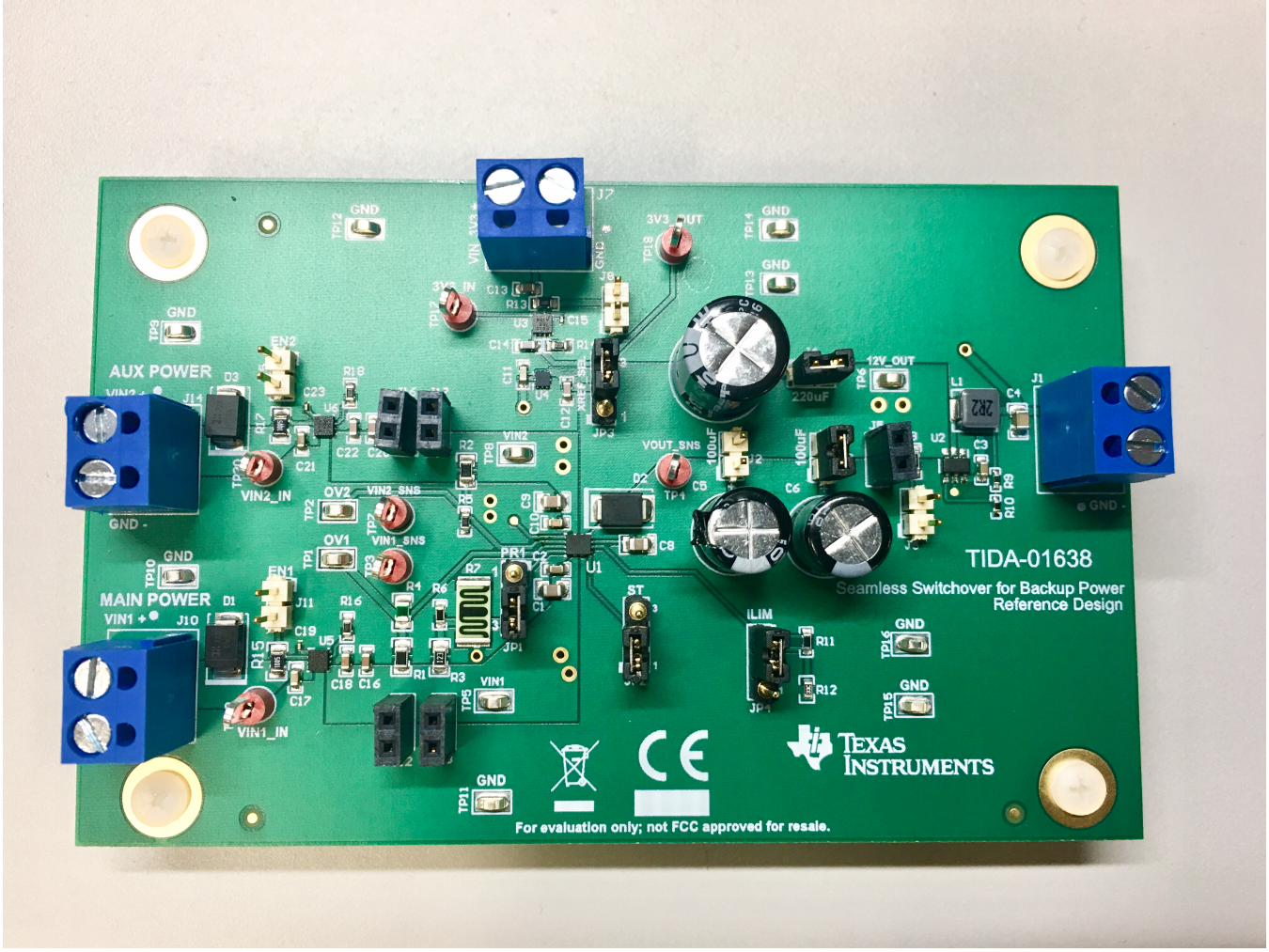


図 9. TIDA-01638 Reference Board

表 2. Jumper / Connector Summary

Input	Connector	Label	Description
Main Power (VIN1)	J11	EN1	Enable for eFuse (U5)
	J12, J13	-	Female headers for attaching input capacitance
	JP1	PR1	Selects between Priority Control and GND Position 1-2 sets GND Position 2-3 sets Priority
	JP2	ST	Enables / Disables Adjustable Hysteresis Position 1-2 disables hysteresis Position 2-3 enables hysteresis
AUX Power (VIN2)	J15	EN2	Enable for eFuse (U6)
	J16, J17	-	Female headers for attaching input capacitance
XREF	J8	-	Enable for XREF TPS2595 U3
	JP3	XREF_SEL	Selects between either 3.3-V input Position 1-2 sets 3.3 V from output of DC/DC Position 2-3 sets 3.3 V from external header VIN_3V3
Output (VOUT)	J2, J3, J4	100 µF, 100 µF, 220 µF	Output Capacitance
	J5	-	Female header for attaching output capacitance
	J6	-	Enable for DC/DC
	JP4	ILIM	Current Limit Control Position 1-2 sets 4.5-A max Position 2-3 sets 2- max No jumper sets 1.5-A max

3.2 Testing and Results

3.2.1 Test Setup

To configure the reference design for XREF, connect the jumpers as shown in 表 3. Make sure to include input capacitors on both input channels (J12, J13, J16, J17) if longer inductive cables are being used. Also ensure that PR1 jumper, JP1, and XREF_SEL, JP3, are configured properly for XREF. The ST Jumper, JP2, is pulled up using pins 1 and 2 for adjustible hysteresis. ILIM is connected R12, creating a overcurrent threshold of 4.52 A.

表 3. XREF Configuration Setup

Description	Jumper / Connector	Value
IN1	-	12.1 V
IN2	-	12.1 V
VOUT	-	12 V at 2.5 A
Input Capacitors	J12, J13, J16, J17	200 uF total
Output Capacitors	J2, J3, J4	320 uF
CP2	JP3	Pins 1 and 2
ST	JP2	Pins 2 and 3
ILIM	JP4	Pins 2 and 3
eFuse Enables	EN1, EN2, J8	OFF
DC/DC Enable	J6	OFF

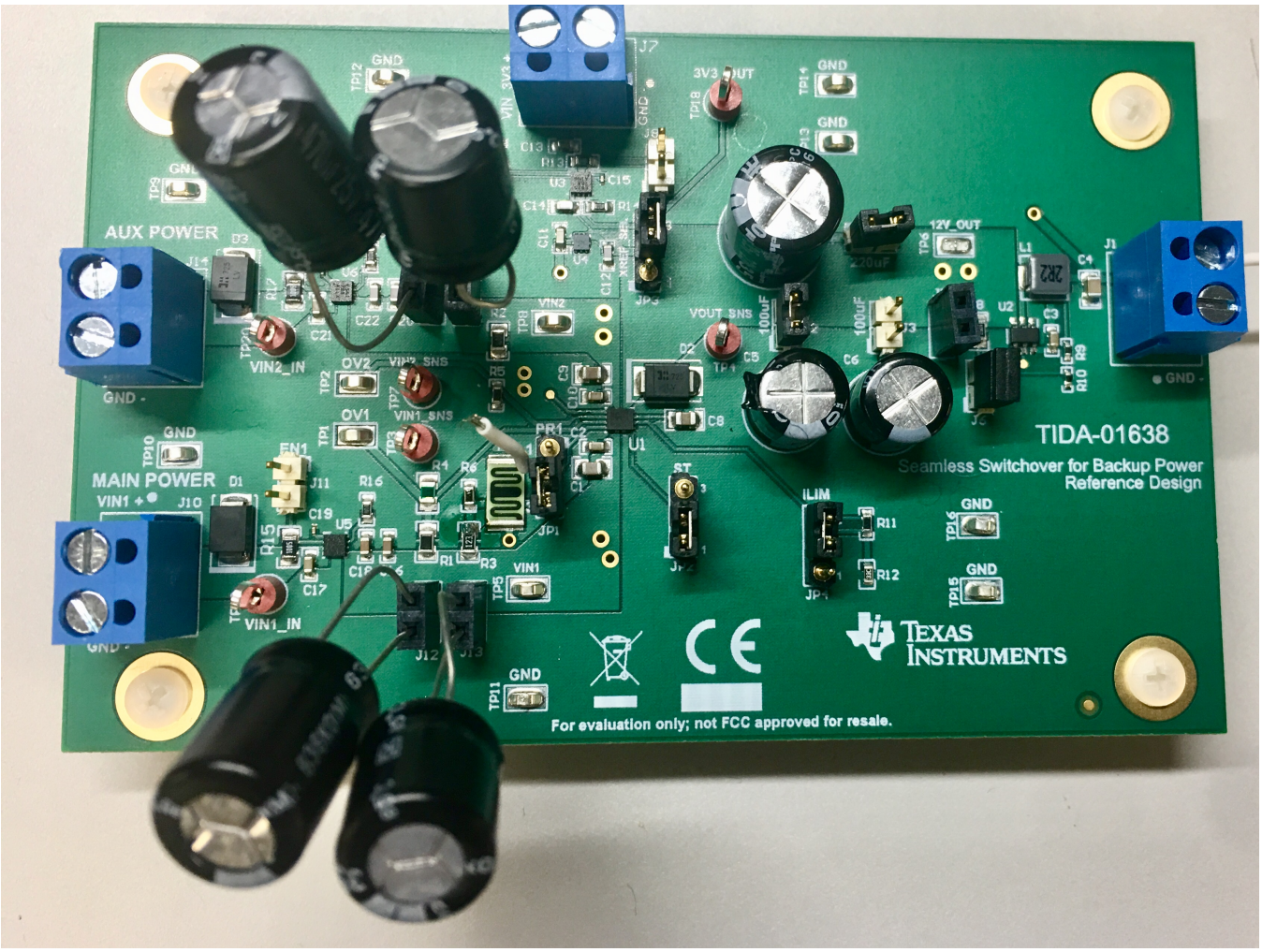


図 10. XREF Configuration

3.2.2 Test Results

3.2.2.1 Seamless Switchover from Main Power(IN1) to Backup Power (IN2)

The first scenario showcases when main power (IN1) is removed from the system, resulting in fast switchover to backup power (IN2). The reference design will start fast switchover when the voltage on PR1 drops below the voltage on CP2 (2.50375V). This will occur when the voltage on IN1 is approximately 11.78 V. Looking at the scope shot below, IN1 is dark blue, IN2 is light blue, VOUT is purple, and PR1 is green.

図 11 depicts this configuration. The total time for switching between IN1 and IN2 is roughly 180 µs.

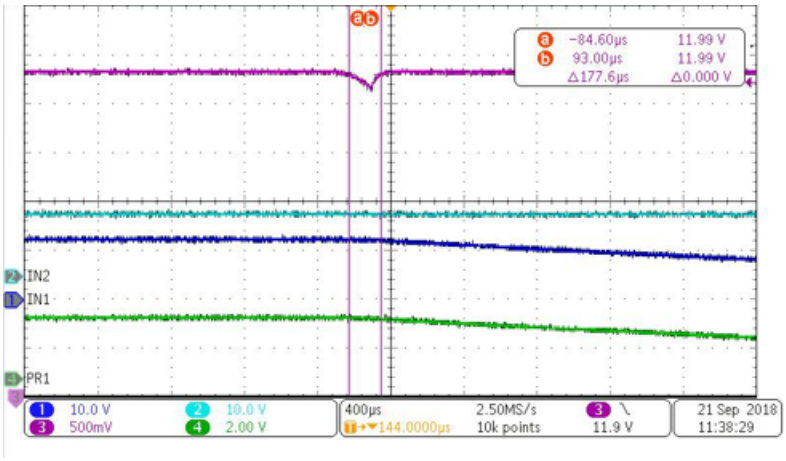


図 11. Seamless Switchover from IN1 to IN2

Zooming in on this scope shot in 図 12, as the voltage on IN1 dips below 11.78 V, fast switchover starts and VOUT switches to IN2 in approximately 3.1 µs. In total, the voltage on the output dips from 12 V to 11.72 V, resulting in a 0.27-V dip during switchover, a 2.39% dip.

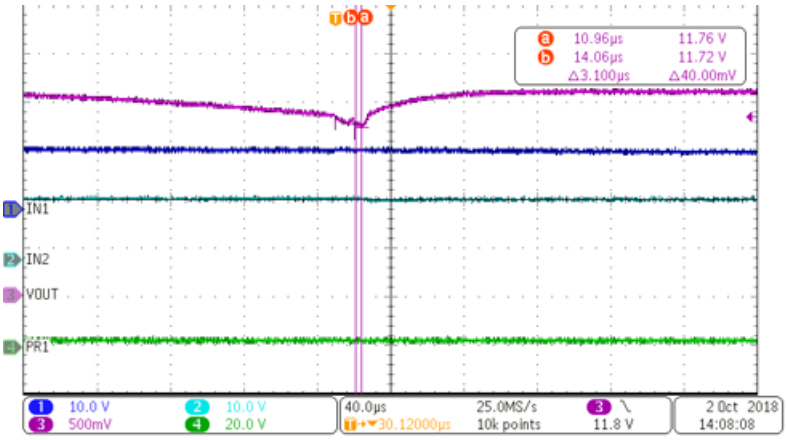


図 12. Seamless Switchover from IN1 to IN2

3.2.2.2 Seamless Switchover from Backup Power (IN2) to Main Power(IN1)

In this scenario, main power (IN1) is being reapplied to the system, while backup power (IN2) is supplying downstream components with power. The reference design starts fast switchover from IN2 to IN1 when the voltage on PR1 exceeds 2.5034V. During this scenario, since the voltage on IN1 is only 11.83 V when PR1 exceeds 2.5034V, fast switchover won't occur until the voltage on IN1 reaches within a threshold voltage of IN2 (V_{RCB}). Otherwise, since IN2 is higher than IN1 for a short period of time, reverse current would flow from IN2 to IN1. In the TPS2121 datasheet, V_{RCB} value is specified as 25 mV typically. Therefore, the design will not switch back from IN2 to IN1 until the voltage on IN1 reaches IN2 - V_{RCB}, at 11.975. At this point, fast switchover will occur.

In the scope shot provided below, the voltage on IN2 is 12.03 V. Therefore, the device will not switchover from IN2 to IN1 until the voltage on IN1 reaches 12.005V. In total, the voltage on the out dips from 12.03 V to 11.99 V, resulting in a 0.33% dip during switchover. The total time for switching between IN1 to IN2 is roughly 6 µs.

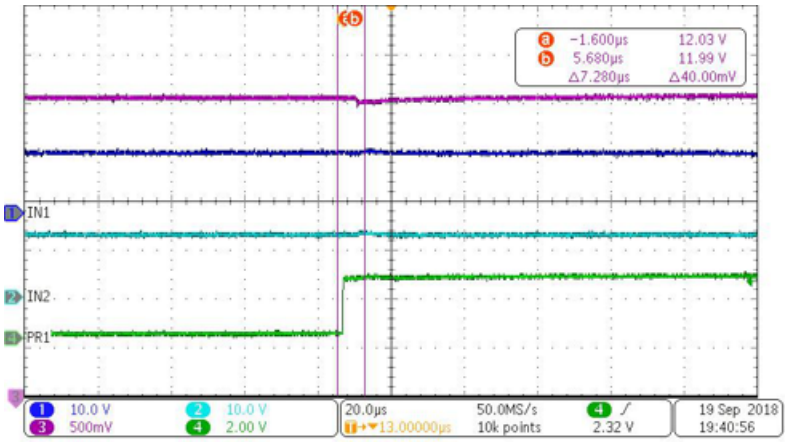


図 13. Fast Switchover from IN2 to IN1

3.2.2.3 *Seamless Switchover from Main Power (IN1) to Backup Power (IN2), Without External Voltage Reference*

Seamless Switchover can still occur without using an external voltage reference. The purpose of the external reference is to provide an external precise voltage source for the CP2 (2.5 V ± 0.15%). If a precise comparison isn't required, seamless switchover can still occur by providing the CP2 pin with the necessary voltage, in this case 2.5 V. In the configuration below, 2.5 V is given to CP2 through a separate power supply. Since the PSU cannot provide the CP2 pin with a precise value compared to the external voltage reference, seamless switchover occurs slower and with more dip on the output. As shown in 図 14, the output dipped to 11.66 V, with a total switchover time of approximately 250 µs.

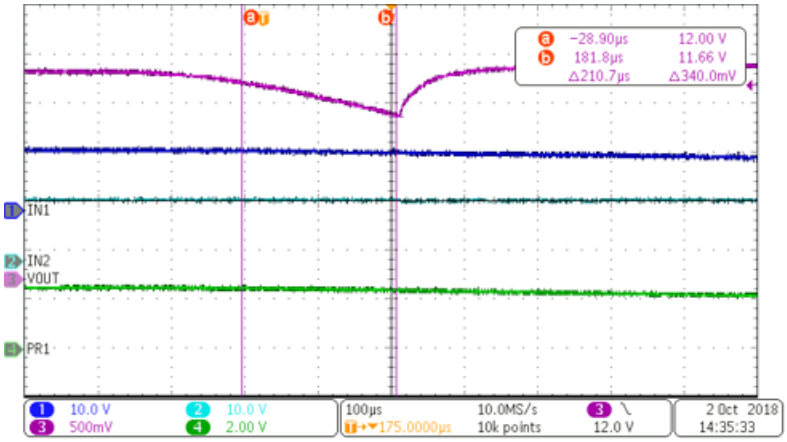


図 14. Fast Switchover without Voltage Source

3.2.2.4 *Slow Switchover fron IN1 to IN2*

The oscilloscope shot below demonstrates slow switchover on the reference design. By pulling CP2 to GND, this disables the fast switchover functionality. The switchover will occur when the voltage on PR1 drops below VREF (1.06 V). The total switchover time in this setup is approximately 800 us, with a voltage dip from 12.07 V to 11.51 V, a 5% dip.

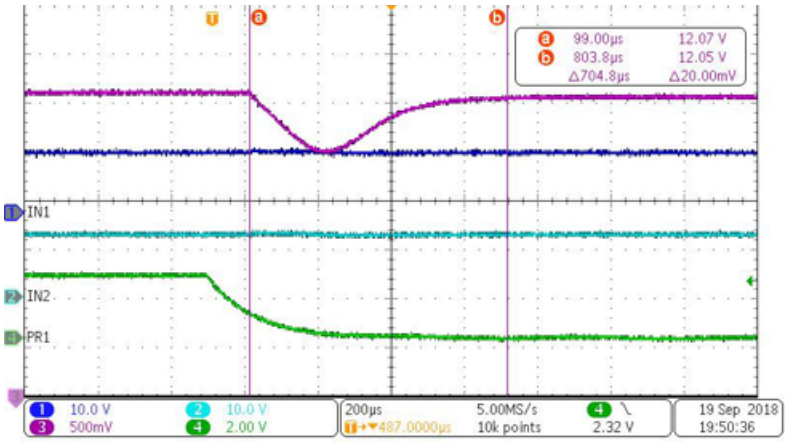


図 15. Slow Switchover from IN1 to IN2

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01638.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01638.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01638.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01638.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01638.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01638.

5 Software Files

To download the software files, see the design files at TIDA-01638.

6 Related Documentation

1. *Power Multiplexing Using Load Switches and eFuses*

6.1 商標

重要なお知らせと免責事項

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