Application Brief

Deep Dive into IEC 61000-4-5 Surge Immunity Testing of the TMCS1143 Hall-Effect Current Sensor

Introduction

The IEC 61000-4-5 standard defines surge immunity testing procedures, simulating the effects of lightning strikes or switching transients on electrical/electronic equipment. This paper details a comprehensive investigation into the surge current immunity performance of the TMCS1143 (information presented here can be applied to the TMCS114x family of devices in the DVF package), a popular Hall-effect current sensor used in diverse applications (especially Energy Infrastructure), under the stringent conditions specified by IEC 61000-4-5. This paper will explore the test setup, parameters, observed behavior, and ultimately, provide a clear assessment of the device's capability to withstand surge events (up to 20kA) as defined by this critical standard.

Understanding IEC 61000 4-5 and Surge Phenomena

IEC 61000-4-5 simulates surges caused by direct or indirect lightning strikes, as well as switching transients within a power system. These surges are characterized by:

- **High Voltage and Current:** The surge represents a dramatic and temporary increase in voltage and current.
- **Fast Rise Time:** Surges rise to peak values very rapidly, challenging the transient response of components
- **Short Duration:** While intense, surges are typically very short-lived, lasting only microseconds.
- **Polarity:** Surges can be positive or negative in polarity, reflecting both types of real-world events

The standard specifies various surge waveforms and test levels based on the expected exposure environment and the port being tested (power, signal, control). Key parameters include surge voltage (typically 0.5kV to 4kV peak), surge current (typically 0.5kA to 8kA peak), rise time (typically 50ns to 1.2µs) and pulse width (typically 50µs to 230µs). Failing to adequately protect against surges can lead to component damage, system malfunction, and data loss. Therefore, surge immunity testing, as defined by IEC 61000-4-5, is essential for validating the robustness of electronic equipment.

Test Levels and Considerations

TMCS1143 devices were subjected to a range of test levels:

- **Current Levels:** Surge currents applied started at 12kA, and units were tested at every 1kA level up to 20kA, with sample devices being tested at each current level.
- **Repetition Rate:** Surges were applied in a series of 5 repetitions at each test level, both positive- and negative-going, for a total of 10 pulses, with a time interval of about one minute between pulses.
- **Operating Conditions:** The TMCS1143 was tested with no supply voltage and at room temperature.
- **Current Waveform and Duration:** The 8/20µs current waveform defined by IEC 61000-4-5 exhibits a front time of approximately 8µs and a time to half-value of approximately 20µs, as shown in Figure 1. A sample of the actual test waveforms are shown in Figure 2.

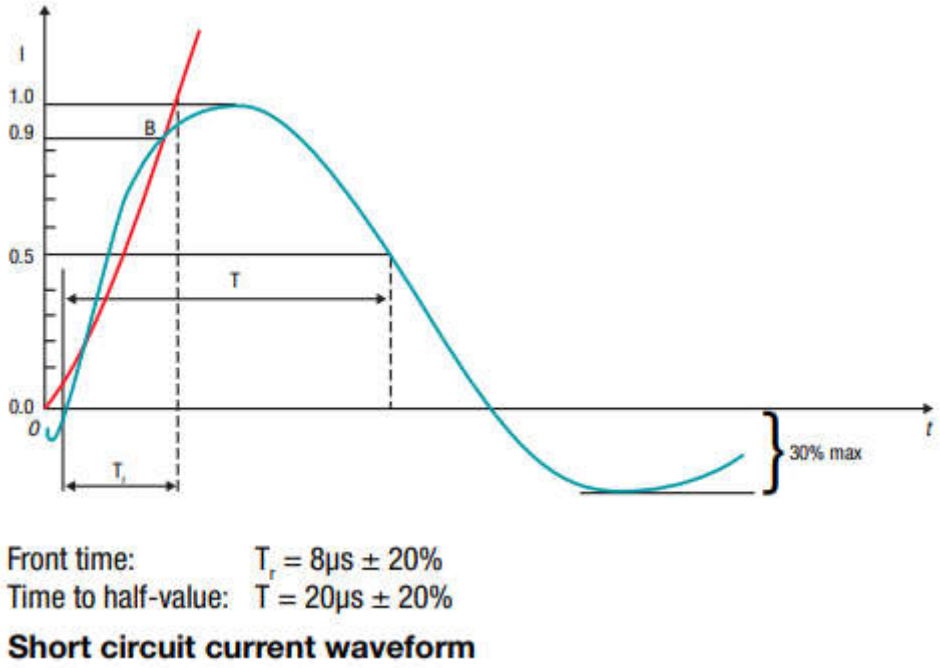

Figure 1. Surge Current Waveform

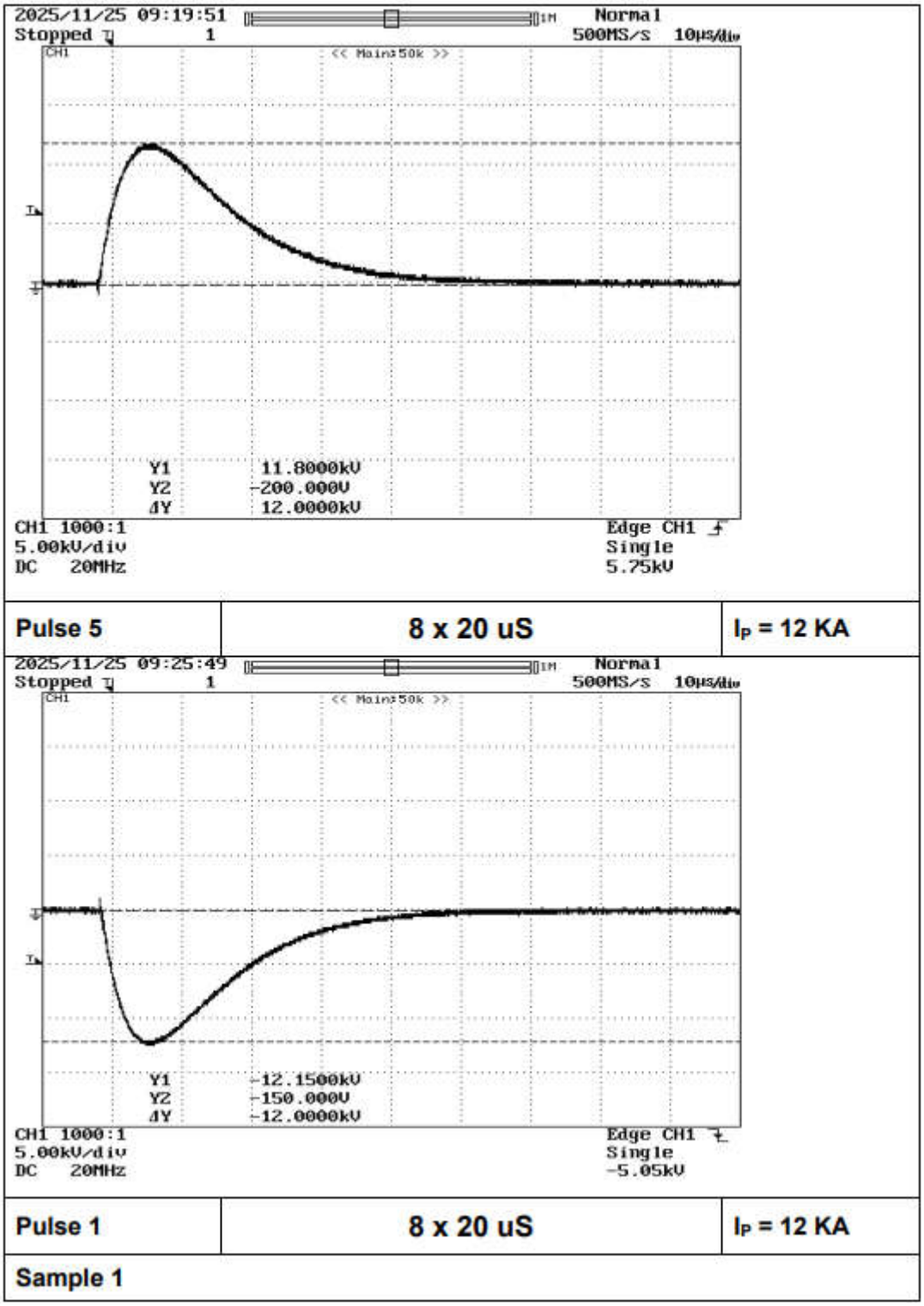

Figure 2. Actual Test Waveform

Test Setup and Methodology

The surge immunity testing of the TMCS1143 was conducted in a controlled laboratory environment, adhering to the current waveforms defined by the IEC 61000-4-5 specification. The test set up block diagram is shown in Figure 3. A standardized test setup was employed, consisting of the following key components:

- **Surge Generator:** A calibrated surge generator capable of producing the waveforms defined in IEC 61000-4-5, including the 8/20µs current wave.
- **Test Board:** The TMCS1143 was mounted on the standard TMCS1143 EVM with no specific regard to minimizing parasitic inductance and capacitance. This board provided connection points for the surge generator and monitoring equipment.
- **Monitoring Equipment:**
  - **Oscilloscope (Yokogawa DL7100):** Used to monitor the surge waveform (voltage and current) injected into the device-under-test (DUT).
  - **Current Probe (Pearson 5664):** Used to measure the current flowing through the input pins of the TMCS1143.
- **Device Testing:** Prior to stressing the TMCS1143 devices, they were mounted on test boards and verified on an automated test design. The pre-stress data was logged and saved for comparison to post-stress data. During stress, the surge current was applied to the IN+ pin of the device.

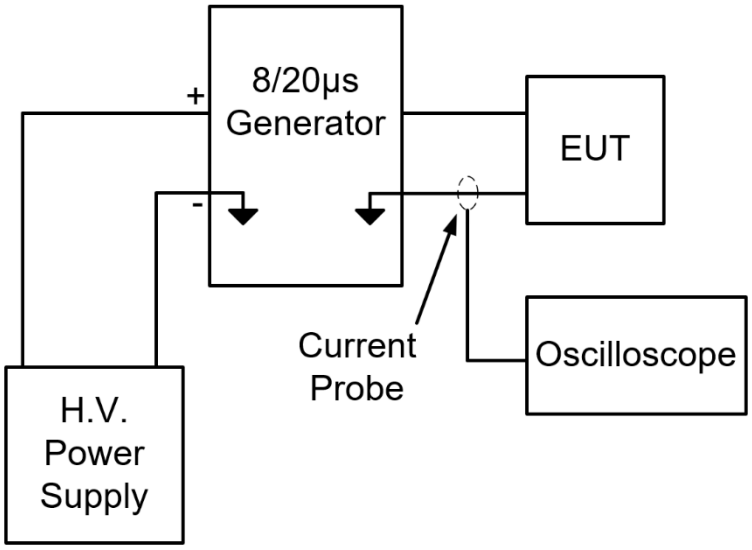

Figure 3. Surge Current Test Setup Block Diagram

Test Observations

The surge immunity testing revealed important insights into the TMCS1143's performance:

- **Physical Damage:** No observable physical damage was evident on any device tested at any of the current levels applied. Both pre- and post-stress images of each device were taken with no visible differences between the two. Pre- and post-stress images of a sample device are shown in Figure 4.

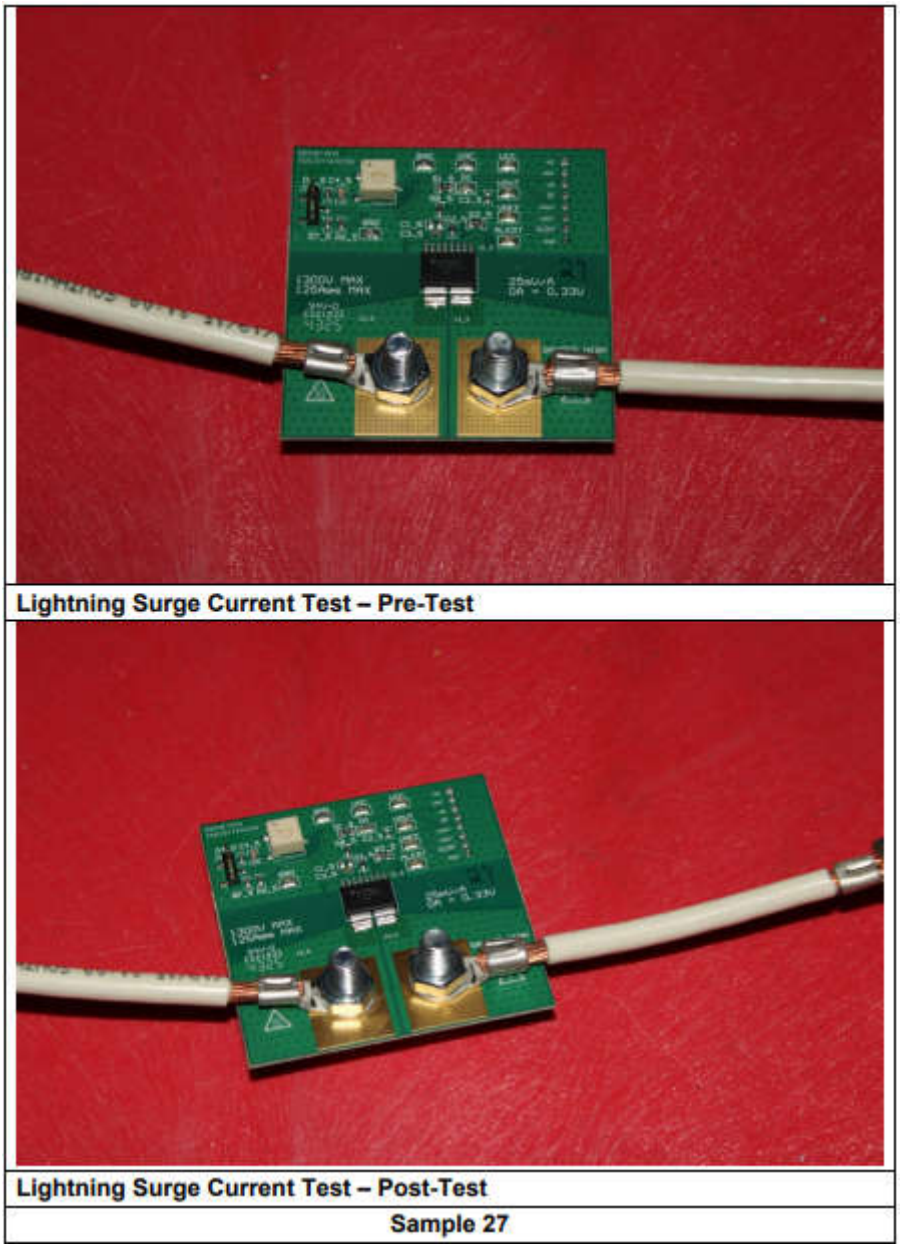

Figure 4. Pre- and Post-Stress PCB Images

- **Electrical Performance:** The most drastic performance changes between pre- and post-stress data were observed on the input conductor resistance (which includes the DUT lead frame as well as the adapter card, solder, cables, hardware, and interconnectors), sensitivity error, and offset error, with the largest changes occurring on the units stressed at 20kA. While there were definite changes across these parameters (especially at the 20kA test level), all devices still performed within the specification limits during post-stress testing and there were no significant changes observed to any other parameters tested between pre- and post-stress testing. The average measurements of the sample units collected from both pre- and post-stress at each tested surge current level can be found in Table 1.

Table 1. Pre- and Post-Stress Test Data

Surge Level (kA)	Units	Input Conductor Resistance (mΩ)		Sensitivity Error (%)		Offset Error (mV)	
		Pre	Post	Pre	Post	Pre	Post
12	1-3	70.69	74.04	-0.16	-0.13	-0.23	-0.24
13	4-6	70.68	77.25	-0.16	-0.11	-0.37	-0.37
14	7-9	72.50	74.73	-0.15	-0.17	-0.04	-0.09
15	10-12	72.28	72.55	-0.11	-0.11	-0.02	-0.07
16	13-15	72.02	82.72	-0.12	-0.16	-0.23	-0.30
17	16-18	73.45	87.17	-0.09	-0.10	-0.24	-0.26
18	19-21	72.31	83.44	-0.10	-0.14	-0.04	-0.09
19	22-24	75.87	90.48	-0.10	-0.09	-0.30	-0.28
20	25-27	75.50	93.65	-0.11	0.43	-0.04	0.19

Mitigation Strategies and Design Considerations

To enhance the surge immunity of systems incorporating the TMCS1143, the following mitigation strategies are recommended:

- **External Surge Protection:** Employing external surge protection devices (SPDs), such as Metal Oxide Varistors (MOVs) or Transient Voltage Suppressors (TVS diodes), at the input of the system can effectively shunt the surge current before it reaches the TMCS1143. Choosing an appropriate SPD with sufficient surge current handling capability is vital. A basic block diagram on how to implement these devices is shown in Figure 5. For a deeper dive and information on designing with surge protection devices, see section 5 in Design Considerations of Using In-Package Hall-Effect Current Sensors in Solar Systems.

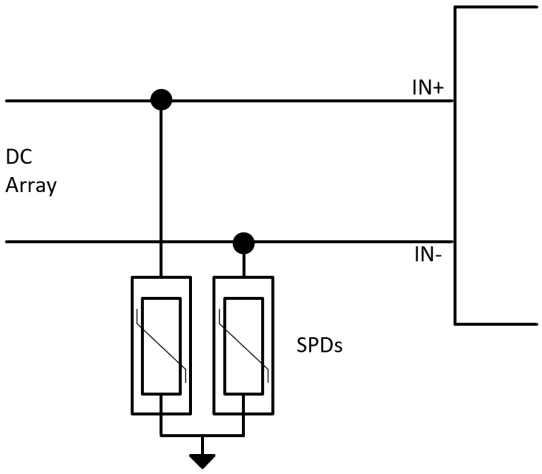

Figure 5. SPD Example Circuit Block Diagram

- **Snubber Network:** A snubber network across inductive loads helps absorb energy from the inductive kickback, reducing the stress on the TMCS1143 during surge events.
- **Proper Grounding and Shielding:** Implementing a robust grounding scheme and utilizing shielded cables minimizes the effects of electromagnetic interference (EMI) and improves surge immunity.

Conclusion

The IEC 61000-4-5 surge immunity testing of the TMCS1143 reveals a level of robustness preferred for many applications, specifically up to 20kA current levels commonly seen in Energy Infrastructure applications, such as Solar Inverters and Power Conversion Systems. By incorporating appropriate surge protection techniques – including external SPDs, snubber networks, and robust grounding practices – system designers can significantly improve the overall surge immunity of systems using the TMCS1143 and verify reliable operation in challenging electrical environments. A clear understanding of the devices' limitations under specific stress conditions allows for more informed design choices and helps with long-term performance.

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