Application Note

TUSB2E221 Repeater Design and Configuration Guide

Ryan Kitto

ABSTRACT

This application note will cover how to configure the TUSB2E221 eUSB2 repeater to match a system's design requirements. That includes how to configure the TUSB2E221 for pin-strap mode or I2C configuration, how to configure the USB2 and eUSB2 PHYs of the TUSB2E221, and recommendations for designing the layout of a system based on repeater configuration.

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Trademarks

1 Introduction

The USB2.0 standard has been long-standing in the industry for decades now, with it being used across a wide range of products and applications.

However, as the industry moves forward, the size of platforms and processors continues to grow smaller, leading to stricter requirements in power and size while still needing the same USB2.0 functionality that is expected with any USB host or device today. USB2.0 has some of the higher voltage signaling amplitudes in the industry, requiring up to 3.3V for LS or FS functionality, and in an industry where power and size is more of a concern, 3.3V signaling just isn't possible. In response to this, the USB-IF established the Embedded USB2 (eUSB2) Physical Layer Supplement, a spec meant to enable USB2.0 functionality at lower amplitudes without impacting any of the functionality that's used today. As a part of this spec, USB-IF also introduced the eUSB2 repeater.

An eUSB2 repeater is an IC meant to enable the lower voltages of eUSB2 signaling (1.0V or 1.2V) to interface with the standard USB2.0 signaling voltages of up to 3.3V without any difficulty being caused by the difference in amplitude, and the TUSB2E221 is one of those repeaters. TUSB2E221 enables this communication by being able to simultaneously interface with eUSB2 signaling on one side of the repeater and translate that to output USB2 signaling at the expected voltage, and vice-versa with USB2 to eUSB2 signaling. Additionally, these repeaters are also able to help compensate for loss in the signal that can come from the eUSB2 or USB2 trace, as well as adjust the amplitude or emphasis of the USB2 or eUSB2 signaling.

This document aims to introduce the different ways the TUSB2E221 can be implemented and configured in a system. That includes how to configure the TUSB2E221 for either pin-strap or I2C mode, recommended settings in pin-strap mode, and how to configure the TUSB2E221 in I2C mode. Additionally, it will also cover how to design the layout of an application to properly utilize the functionality of the TUSB2E221.

2 Different ways to configure the TUSB2E221

There are two ways to configure the TUSB2E221: I2C configuration and pin-strap settings. Both options are viable and can be used, however they both have their benefits.

With an I2C configuration, both the eUSB2 PHY and the USB2 PHY can be configured at the same time, allowing for specific combinations of configurations depending on the system's design. Additionally, I2C adds a few more settings to certain registers that are not available when using the repeater in pin-strap mode.

With a pin-strap configuration, repeater implementation is much simpler, only allowing either the eUSB2 PHY or the USB2 PHY to be configured, not both at once. This allows one side of the repeater to follow set guidelines based on which PHY is being configured. Pin-strap mode also removes the requirement of an I2C bus to properly configure the TUSB2E221, using only the three EQ pins and SDA/SCL pins to determine PHY configuration.

2.1 I2C Configuration

In order to use I2C to configure the TUSB2E221, certain pins need to be configured to set the TUSB2E221 to I2C mode:

Table 2-1. I2C Mode Pin Configuration

Pin Name	Pin Configuration
EQ0	Pulled-down to GND or floating.
EQ1	Pulled-down to GND or floating.
EQ2/INT	Floating, or connected to the GPIO of the host with a 10Kohm PU for open-drain mode.
SCL	PU to Vio using a 1Kohm resistor.
SDA	PU to Vio using a 1Kohm resistor.

If the above pins are configured as listed in Table 2-1, then the repeater will be set to I2C mode, with port 0 and port 1 of the repeater set to USB repeater mode.

Once in I2C mode, the following bits can be modified to adjust the performance of either the eUSB2 or USB2 PHY.

Table 2-2. TUSB2E221 Configuration Bits

Register	Description
E_EQ_Px	Controls the RX EQ of the eUSB2 pins. This allows for loss compensation from 0.34dB up to 4.07dB.
E_HS_TX_AMPLITUDE_Px	Controls the TX amplitude of the signal output by the eUSB2 pins of the repeater. This configures the output of the eUSB2 pins to be between 360mVpp and 500mVpp
E_HS_TX_PRE_EMPHASIS_Px	Controls pre-emphasis on the output of the eUSB2 pins. This pre-emphasis can range from 0dB up to 3.86dB.
U_EQ_Px	Controls the RX EQ of the USB2 pins. This allows from loss compensation from 0.06dB up to 3.35dB.
U_SQUELCH_THRESHOLD_Px	Controls the squelch threshold of the USB2 pins. This allows USB2 HS signals as low as 85mV to be detected or requires signals to be at least 130mV to be detected.
U_DISCONNECT_THRESHOLD_Px	Controls the disconnect threshold of the USB2 connection. This sets the range that determines whether a HS signal amplitude is too high, starting from a 525mV minimum up to 825mV minimum.
U_HS_TX_AMPLITUDE_Px	Controls the TX amplitude of the signal output by the USB2 pins of the repeater. This configures the output of the USB2 pins to be between 740mVpp up to 1040mVpp.
U_HS_TX_PRE_EMPHASIS_Px	Controls pre-emphasis on the output of the USB2 pins. This pre-emphasis can range from 0.5dB up to 4.0dB.

By adjusting the above bits, the performance of the TUSB2E221 can be adjusted to better suit a system's constraints. For example, in a system where the USB2 trace between the repeater and the USB2 connector is longer in terms of length, the U_EQ_Px and U_HS_TX_AMPLITUDE_Px bits can be adjusted to higher values to improve the performance of the USB2 side of the repeater, allowing the USB2 signal output from the repeater to have a stronger drive strength while improving the USB2 signal as it is received.

Additionally, while in I2C mode, these configuration bits have more settings available than they would in pin-strap mode. While these settings are not needed for typical applications, in extreme design cases, they can be used to further improve performance of a system.

In summary, I2C mode allows for further configuration of the TUSB2E221 than what is immediately available in pin-strap mode, while at the cost of ease of configuration that is offered in pin-strap mode.

2.2 Pin-strap Configuration

As opposed to I2C configuration, pin-strap mode does not require any software or external programming, using the three EQ pins of the TUSB2E221 (EQ0, EQ1, EQ2) and the SDA/SCL pins to select the level of compensation for either the eUSB2 PHY or the USB2 PHY. This allows for a simple solution to select the compensation level that best suits a systems design, as opposed to using I2C to control both the USB2 and eUSB2 PHYs.

One thing to point out is that depending on how SDA and SCL are configured in pin-strap mode, which PHY is being configured will change. Table 2-3 below lists which PHY can be configured based on the setting of the SCL/SDA pins.

Table 2-3. Pin-Strap PHY Selection

SCL	SDA	EQ0	EQ1	EQ2
Low/Floating	Low/Floating	USB2 PHY Configuration		
High	Low/Floating	eUSB2 PHY Configuration		High-Z

2.2.1 USB2 PHY Configuration

If both the SDA and SCL pins are pulled low or floating, then the TUSB2E221 will allow for the USB2 PHY to be configured via the three EQ pins. These pins allow for up to 8 different configurations, each one tailored towards certain amounts of Equivalent Series Resistance, or ESR, on the USB2 data lanes from the repeater to the USB2 connector.

However, while there are eight options available, only three of these options need to be reviewed for a typical application:

Table 2-4. USB2 PHY Pin-strap Configuration

EQ0	EQ1	EQ2	USB2 PHY Compensation Level	USB ESR
Low/Float	Low/Float	Low/Float	Level 0	USB A: 2.5Ω USB B: 2.5Ω
High	Low/Float	Low/Float	Level 1	USB A: 10Ω USB B: 10Ω
Low/Float	High	Low/Float	Level 2	USB A: 17.5Ω USB B: 17.5Ω

Of the eight settings available, these three are commonly selected as they set both USB2 lanes to the same compensation level. The other five settings are designed to allow for USB2 lanes with different ESR values but are not typically used.

By determining the ESR of the USB2 side of the eUSB2 repeater, the correct compensation settings can be selected via the EQ pins to ensure that the USB2 signal is properly compensated. For example, in a system where the distance between the repeater and the USB2 connector is minimal and there are no components in the data path, it would be best to configure the eUSB2 repeater for USB2 PHY Compensation level 0.

Additionally, if I2C is used beforehand, table 5-4 of the TUSB2E221 can be used to determine which pin-strap settings for the EQ pins best match the register values used for the registers listed in Table 2-2. Table 5-4 can also be used to illustrate exactly how the registers are being tuned based on which pin-strap compensation level is being used.

2.2.2 eUSB2 PHY Configuration

If SCL is pulled high while SDA is pulled low or floating, then the TUSB2E221 will allow for eUSB2 PHY configuration. In eUSB2 PHY configuration mode, the EQ pins are used to select between four different eUSB PHY compensation levels:

Table 2-5. eUSB PHY Pin-strap Configuration

EQ0	EQ1	EQ2	eUSB PHY Compensation Level	eUSB ESR
Low/Float	Low/Float	Low/Float	Level 0	eUSB0: 2.5Ω eUSB1: 2.5Ω
High	Low/Float	Low/Float	Level 1	eUSB0: 7.5Ω eUSB1: 7.5Ω
Low/Float	High	Low/Float	Level 2	eUSB0: 15Ω eUSB1: 15Ω
High	High	Low/Float	Level 3	eUSB0: 25Ω eUSB1: 25Ω

Depending on the ESR of the eUSB2 data lanes between the repeater and the host/device, the EQ pins in pin-strap mode should be configured to match the ESR of the eUSB2 data lanes as closely as possible. For example, in the case where there are some components along the eUSB2 data lanes or the length of the trace between the repeater and the host/device is 10 inches, eUSB PHY Compensation level 3 would be the best level to configure for.

If I2C was used beforehand, table 5-6 of the TUSB2E221 datasheet can be used to determine what pin-strap settings best match the settings used for the eUSB registers listed in table 2-2. Table 5-6 can also be used to determine how exactly the eUSB2 PHYs are being configured based on which pin-strap settings are used.

3 Layout Guidelines

Depending on how the eUSB2 PHYs and USB2 PHYs are configured, the recommended length of eUSB2 and USB2 data lanes can vary. It's important to keep both settings and trace length in mind when determining the settings of a repeater. It's best to either design the trace with a certain compensation setting in mind based on required components, I.E ESD, CMCs, or to configure the repeater based on the trace length from the host/device to the repeater, and from the repeater to the connector.

3.1 Layout Guidelines for Pin-strap mode

If the TUSB2E221 is being designed with pin-strap mode in mind, it's important to keep in mind that depending on which PHY is being configured, the recommend trace length of the eUSB2 and USB2 traces will change accordingly.

If the TUSB2E221 is set to configure the USB2 PHY of the repeater, then we recommend that the eUSB2 trace between the host/device and the repeater be a maximum of 5 inches. This is because the eUSB2 PHY is configured by default to account for the loss typically seen in a 5-inch trace. Depending on the settings selected for the USB2 PHY, we recommend a max of up to 11 inches for the USB2 trace, with the max length being used in relation to the max USB2 PHY compensation level listed in table 2-4.

If the TUSB2E221 is set to configure the eUSB2 PHY of the repeater, then we recommend keeping the distance between the repeater and the USB connector as short as possible, to ensure the USB2 signal can pass through the USB cable without too heavily impacting signal integrity before arriving at the repeater. Depending on how the eUSB2 PHY is configured, the eUSB2 trace can be either 2.5, 5, 7.5, or 10 inches, following the compensation levels in table 2-5 respectively.

3.2 Layout Guidelines for I2C configuration

For I2C mode, the trace length of both the eUSB2 trace and the USB2 trace can change depending on how their respective PHYs are configured. By following table 5-3 through table 5-6 of the TUSB2E221 datasheet, the recommended trace length of the USB2 and eUSB2 data lanes can be approximated based on the set register values.

4 Miscellaneous Pin Configuration

Aside from the EQ, DP/DN and eDP/eDN pins, other pins of the TUSB2E221 also need to be configured to ensure proper functionality of the eUSB2 repeater.

4.1 Power Pins

The TUSB2E221 uses both a 3.3V and 1.8V power rail to power the internal eUSB2 and USB2 PHYs in the repeater. Configuration of these pins is straightforward, as there is no power supply sequencing requirements. The max amount of time it takes both pins to reach their minimum required supply voltage is 2ms, so make sure that requirement is met.

Otherwise, the only other concern is Decoupling capacitors. Assuming both VDD3V3 will use the same rail, there should be a 1uF pull-down capacitor is connected to each power rail, with an 100nF capacitor recommended per power pin, so two 100nF capacitors for the VDD3V3 rail, and one 100nF capacitor for the VDD1V8 rail. If following a provided specification for eUSB2 repeaters, it is recommended to follow that specification.

4.2 Control Pins

The TUSB2E221 features three additional pins for repeater control and functionality, the RESETB, VIOSEL, and CROSS pins.

The VIOSEL pin is used to control the voltage thresholds of the IO pins (EQ, CROSS, INT, SDA/SCL, RESETB) depending on how it is configured. For 1.8V high IO signaling, the VIOSEL pin should be pulled-up to 1.8V. For 1.2V high IO signaling, the VIOSEL pin should be pulled down to VSS/GND.

The RESETB pin is an active low reset that controls whether the TUSB2E221 is enabled or not. When the RESETB pin is pulled low, the TUSB2E221 will be disabled and have no functionality, disabling the USB2 lane. When the RESETB pin is pulled high, the TUSB2E221 will be enabled and place the eUSB2 PHYs into default mode, waiting for configuration from the eDSPr or eUSPr. We typically recommend pulling the RESETB pin up to the VIO selected by the VIOSEL pin with a 1Kohm resistor, with a 100nF cap connecting to GND.

Finally, if the DSBGA package of the TUSB2E221 is being used, there will be an additional CROSS pin which controls an internal crossbar mux inside the TUSB2E221. This internal mux controls the routing of the DP/DN A/B ports, and the eDP/eDN 0/1 ports. If the CROSS pin is pulled low at startup, eUSB0 will route to USBA, and eUSB1 will route to USBB. If the CROSS pin is pulled high at startup, eUSB0 with route to USBB, and eUSB1 will route to USBA. In most cases where this crossbar mux isn't needed, it's best to leave the CROSS pin pulled-down and route the signals across the repeater. For the QFN package of the TUSB2E221, this mux is not accessible and is pulled-down by default.

5 Summary

The TUSB2E221 allows for both simple and extensive configuration depending on a systems need. By tuning the TUSB2E221 to your system's needs and designing around it, implementing eUSB2 into a system can be easily done.

6 References

1. TUSB2E221 Datasheet: https://www.ti.com/lit/gpn/tusb2e221
2. TUSB2E221QFN Evaluation Module User's Guide: https://www.ti.com/lit/pdf/snlu354

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