Application Report

Current Sense Amplifier Considerations for Driving SAR ADCs

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ABSTRACT

Often in analog current sense amplifier (CSA) applications, there is a need to move the measurement information into the digital realm via an analog to digital converter (ADC). Based on the various needs of the converter, a question often investigated is whether the current sense amplifier is capable of driving the ADC in its own right. This paper investigates and discusses the feasibility of these implementations, limitations that make a buffer recommended or necessary, and the implementation of a drivable charge bucket filter from the stance of stability using the output impedance of the amplifier.

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Trademarks

1 Introduction

In many modern applications, the focus in signal chain often begins with the analog to digital converter (ADC) and its specifications. The designer begins by defining the resolution needs of the their specifications and works backwards to select a suitable driver that will provide the specifications necessary to deliver the desired throughput, resolution, and noise specifications required by the system.

When working with sensors, however, the opposite is quite often the case: the designer has chosen a specific sensor, such as a current sensing amplifier (CSA), to meet a specific requirement in their respective system, and therefore the desire is to find a way to capture the maximum throughput starting from the input side of the signal chain and moving forward. This application report aims to perform this type of analysis, examining the INA293 as the chosen sensor of interest, and discussing techniques to maximize throughput. Output impedance is examined to discern when a device may be capable of driving an ADC on its own, and when a buffer would be required to ensure optimal performance.

2 The SAR ADC Switching Model

When digitizing an analog signal via an ADC, the typical goal is to drive the signal to within 1/2 an LSB inside a specified period of acquisition time. This is due to the fact that the best case error that can be achieved in an ADC is limited to this value, due to the phenomenon commonly called quantization noise.

When choosing an input driver for the front end of an ADC, to meet this goal, typically three major criterion from the ADC govern the beginning focus area of analysis: acquisition time, ADC resolution, and desired sampling rate. These factors all contribute to the needs of the driver to properly drive the inputs.

2.1 Acquisition Time

When examining the sampling scheme for a SAR ADC, it is broken down into two specific time frames: acquisition time, and conversion time. The relative flow of the capture of a single sample is shown in Typical ADC Single Acquisition Cycle , and the input structure of the ADS8860 is shown in ADS8860 Input Sampling Stage Equivalent Circuit, Hold Mode below.

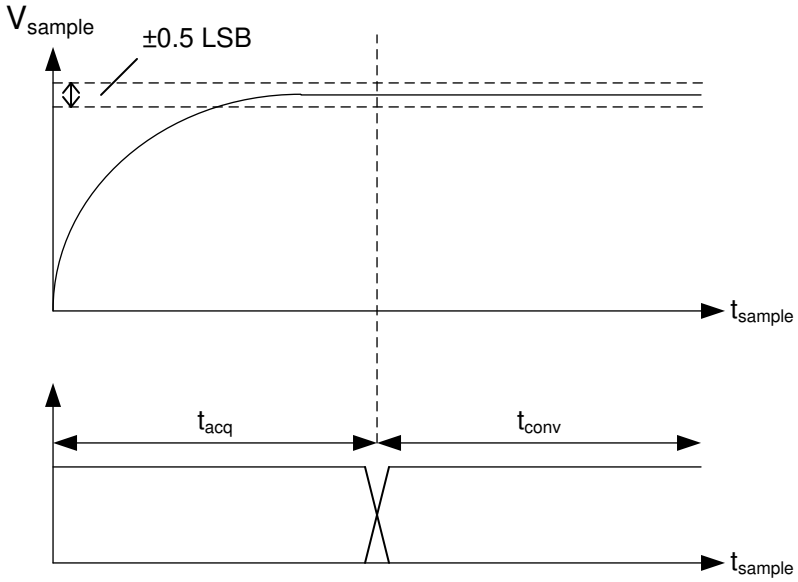

Figure 2-1. Typical ADC Single Acquisition Cycle

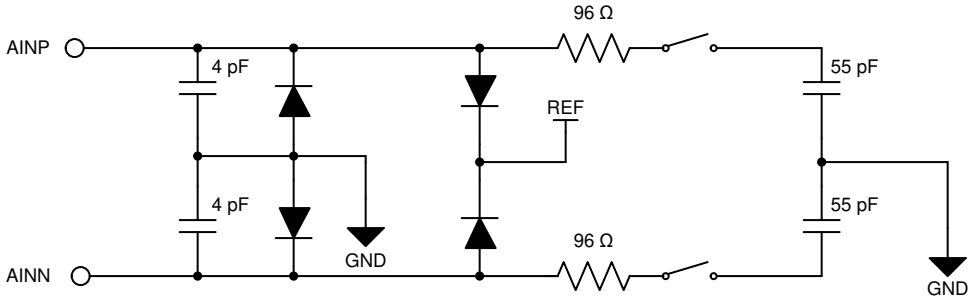

Figure 2-2. ADS8860 Input Sampling Stage Equivalent Circuit, Hold Mode

At the beginning of the acquisition phase, the switches of the sample and hold input structure close allowing the sample and hold capacitor, C_{SH}, to charge. This capacitor will continue to charge until it either settles to a final value, or the end of the acquisition period is reached, at which point the switch re-opens and conversion begins. The goal of a successful design is to ensure that this sample is sufficiently charged within the acquisition window of the ADC, to prevent any additional error greater than the quantization noise of the ADC on the measurement.

Immediately following the acquisition time, the ADC begins operation on the sampled value and digitizes the information. The time in which this occurs is called the conversion time. This is the time required by the ADC to convert the measured result into a digital value. Once this value is completed, it is delivered to the host processor, and the next sample and hold cycle begins.

The conversion time for any ADC is typically a fixed value inherent to the device, and remains fixed regardless of the value of the sampling clock.

2.2 ADC Resolution

ADC resolution creates a similar challenge to that of acquisition time, but on the opposing axis of quantization. When analog information is digitized, quantization error is often a primary source of error, and the magnitude of this error becomes smaller as resolution increases. However, as the error target is now smaller, the ADC is further challenged to settle to a more precise value within the acquisition time of the device. Quantization Error as a Percentage of FSR provides a quick glance at quantization error for various common ADC bit resolutions.

Table 2-1. Quantization Error as a Percentage of FSR

ADC Resolution	1 LSB, FSR = 4.096V	Quantization Error, % of FSR
0	4 mV	.049%
12	1 mV	.0122%
16	62.5 µV	.000763%
18	15.625 µV	.000190%
20	3.90625 µV	.000048%
24	244.14 nV	.00000298%

Because of this relationship, as the resolution of the ADC is increased, the amount of settling time needed is increased in turn.

2.3 Sample Rate

While not as vitally important as acquisition time or resolution, a third important parameter that merits discussion here is sample rate. Sample rate is the effective throughput of the device in terms of digitized samples, and is often determined with various design goals in mind, such as Nyquist criterion, additional resolution from oversampling, or even power considerations. In general, the maximum sampling rate of a device can be determined by adding the conversion time and the acquisition time of the device and taking the inverse of this total time, or

$$f_{SAMPLE} = \frac{1}{t_{SAMPLE}} = \frac{1}{(t_{ACQ} + t_{CONV})} \quad (1)$$

An important factor here, although not true of all ADCs, is that while conversion time for an ADC is a fixed quantity, the acquisition time of many devices can be altered by relaxing the sampling clock of the device, effectively widening the sampling window. This is an important feature when attempting to directly drive the ADC with a lower bandwidth sensor, as it will allow the amplifier to optimize achievable throughput once a stable filter is designed.

3 The ADC Charge Bucket Filter

While it is possible for an amplifier to directly drive the inputs of an ADC by itself in certain situations, in most cases, a charge bucket filter is needed, connected as shown in Charge Bucket Filter, Single-Ended ADC with Ground Sense Configuration below.

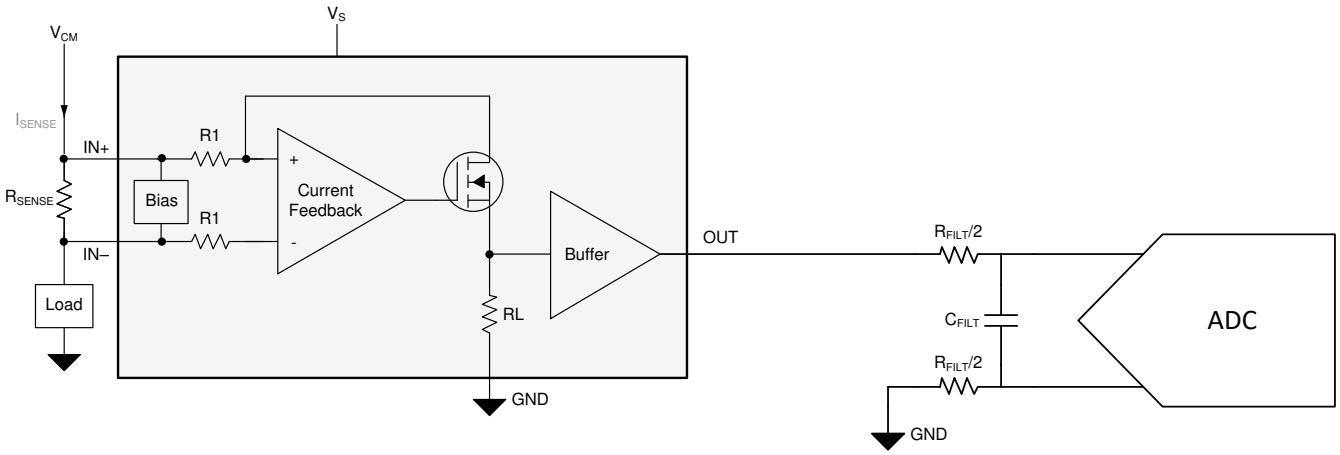

Figure 3-1. Charge Bucket Filter, Single-Ended ADC with Ground Sense Configuration

The purpose of this filter is not necessarily to provide anti-aliasing capabilities (although there may be potential to design to this), but rather to provide a *bucket* of additional energy to help charge the sample and hold node of the ADC to within 1/2 LSB inside of the acquisition window. This filter also helps to maintain stability in the system, as each sample in the sequence requires an inrush of charge, and often the amplifier cannot directly drive the input sampling structure for this requirement. In applications where this *is* possible, additional challenges such as spiking or droop on the signal can occur, and often require even higher bandwidths from the amplifier to properly recover, resulting in additional power needs from the amplifier, including higher quiescent current as a direct consequence of the higher bandwidth. An illustration of analog simulated outputs of both an unfiltered signal and a filtered signal are compared in Unfiltered vs. Filtered Output Signal.

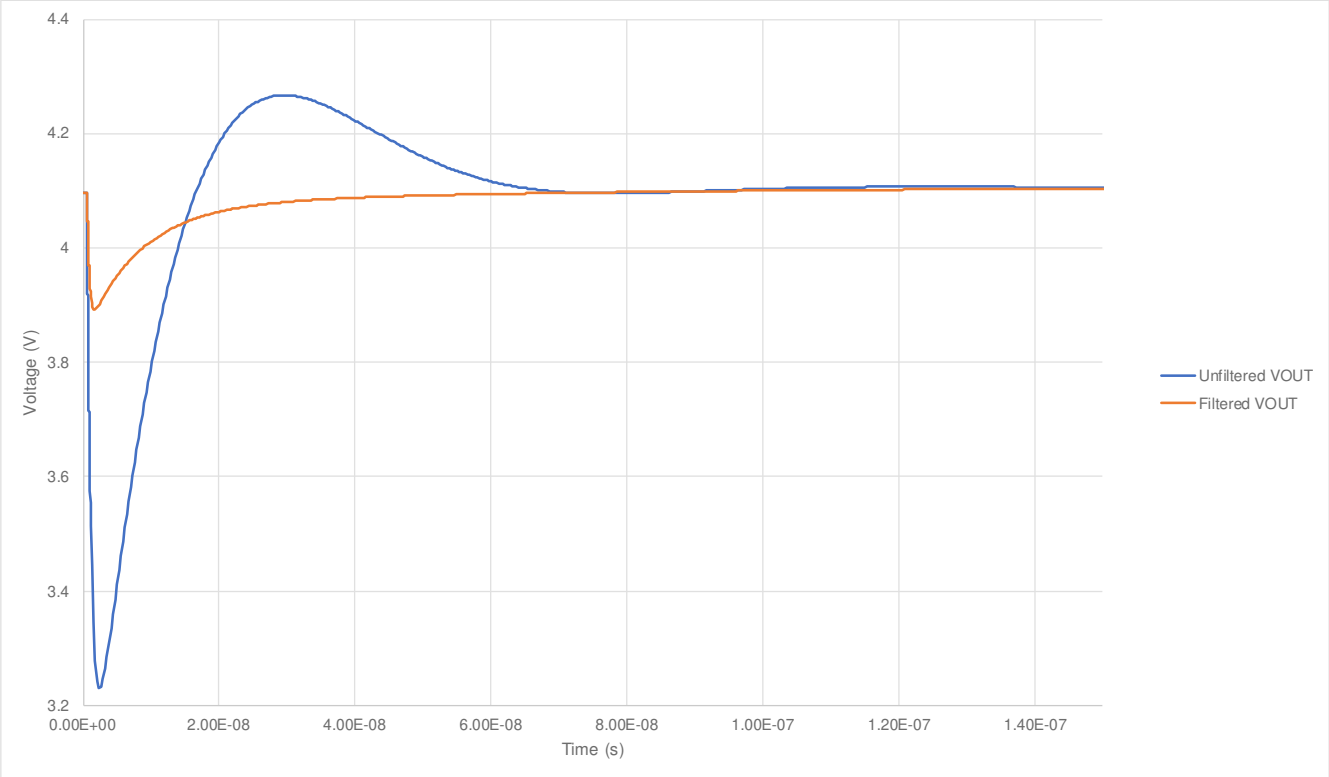

Figure 3-2. Unfiltered vs. Filtered Output Signal

As discussed in Math Behind R-C Component Selection, the following derivations and discussion are not found in textbook, but rather are approximations made based on assumptions from data over multiple designs. This approach combines the best aspects of multiple methods based on data, and provides an algorithm for circuit optimization. The assumptions made for the following analysis are:

- VIN = 100% FSR for worst case settling
- Total droop of the voltage allowed on the filter node (V_{FILT}) is 100mV
- Error Target = 1/2 LSB
- Current Sense Amplifier is approximated as a second order system
- The Current Sense Amplifier is 4 times faster than the filter

3.1 The Filter Capacitor, C_{FILT}

Recall that for a capacitor, the charge stored is equal to the voltage present on the capacitor multiplied by the capacitance. Then, for the sample and hold capacitor internal to the ADC, it can be expressed that

$$Q_{SH} = V_{FSR} \times C_{SH} \tag{2}$$

Using this expression, C_{SH} is defined as the internal sample and hold capacitance value of the ADC, and V_{FSR} as the maximum possible voltage of the full scale range across C_{SH}. The corresponding Coulumb product then gives us the maximum possible Coulombs that C_{SH} could need to charge to within a single acquisition cycle.

When the switch of the sample and hold structure closes, charge from the current sense amplifier as well as charge held on the filter capacitor both move to charge the sample and hold structure. It can threrefore be epxressed that

$$Q_{SH} = Q_{CSA} + Q_{C_{FILT}} \tag{3}$$

While the charge delivered by the amplifier comes from its output stage, charge from the filter capacitor is depleted, and causes the voltage on the node to droop. Here, the assumption is made that half of the charge needed to charge C_{SH} is sourced from the filter capacitor. The general form of this equation is given as

$$\Delta Q_{C_{FILT}} = N \times Q_{SH}, \quad 0 \leq N \leq 1 \tag{4}$$

where here, N = 0.5. As the capacitance of the chosen filter capacitor is a fixed value, we can then attribute the change in charge to the droop in voltage as

$$\Delta Q_{C_{FILT}} = \Delta V_{FILT} \times C_{FILT} \tag{5}$$

Combining these expressions, and solving for C_{FILT}, a final expression is derived of

$$C_{FILT} = \left(\frac{N \times V_{FSR}}{\Delta V_{FILT}}\right) C_{SH} \tag{6}$$

By the assumptions of V_{FSR} = 4.096V ≅ 4V, and V_{DROOP} = ΔV_{FILT} = 100mV, the parenthetical term reduces to a coefficient that provides a sizing relationship for the filter capacitor of

$$C_{FILT} = 20 \times C_{SH} \tag{7}$$

This implies that for the given sample and hold capacitance of an ADC operating at a full scale range of 4V, to maintain less than 100mV droop on the input node, a filter capacitor 20 times the size of sample and hold capacitance should be mounted, provided the amplifier is capable of supplying the remaining charge. If this is not the case, the droop may be greater than the assumed 100mV, which may or may not be acceptable based on system specifications.

A capacitor of this magnitude will often be difficult to implement, as amplifiers typically cannot drive large capacitive loads on their own and maintain stability. Current sense amplifiers are no exception here, so ways to ensure stability will need to be examined to successfully drive this type of load.

3.2 Output Filter Resistor, R_{FILT}

The immediate solution to the above problem is to isolate this capacitance from the output node of the amplifier via additional resistance. The interactions between the output impedance of the amplifier and this RC network are discussed in Output Filter Discussion and Design, but it is beneficial to explore the nature of this filter as it relates to the ADC input stage. Examining the voltage on the filter capacitor, recall that for a typical RC network in the time domain, the voltage charges as a function of the RC time constant, given as

$$V_{FILT} = (V_{INIT} - V_{FINAL}) \times e^{\frac{-t}{\tau_C}} + V_{FINAL} \tag{8}$$

where V_{INIT} is the initial charge on the filter capacitor prior to the beginning of the sample and hold cycle, V_{FINAL} is the final voltage that the capacitor charges to, and τ_C is the total time constant for the system with which the node will charge that includes contributions from both the RC network as well as the amplifier. The addition of resistance on the output reduces the amount of the current that can be delivered by the amplifier, and also filters higher frequency components of the signal based on the cutoff frequency formed by the RC response with C_{FILT}. The goal then, is to ensure that for the given C_{FILT}, the system is still able to settle to within 1/2 LSB within the sample and hold cycle of the ADC. For the above expression, this equates to

$$0.5 \times LSB = V_{FINAL} - V_{FILT} \tag{9}$$

It can also be observed that the maximum magnitude between V_{INIT} and V_{FINAL} is simply V_{DROOP}, or

$$V_{INIT} - V_{FINAL} = V_{DROOP} \tag{10}$$

Rearranging and substituing these into the RC equation, it can then be expressed that

$$0.5 \times LSB = (V_{DROOP}) \times e^{\frac{-t}{\tau_C}} \tag{11}$$

Solving this expression for τ_C, the relationship of V_{FILT} is then expressed in terms of settling as

$$\tau_C = \frac{-t_{ACQ}}{\ln(\frac{0.5 * LSB}{V_{DROOP}})} \quad (12)$$

However, since the CSA also contributes to this charge, an expression relating τ_C to both of these is needed. Since the CSA is approximated as a second order system, the shared contribution of both of these can be approximated using an root-mean-square (RMS) approach, or

$$\tau_C = \sqrt{(\tau_{RC})^2 + (\tau_{CSA})^2} \quad (13)$$

And given the assumption that the CSA is 4 times as fast as the RC network,

$$\tau_C = \sqrt{(4\tau_{CSA})^2 + (\tau_{CSA})^2} \quad (14)$$

Solving this equation for τ_{CSA} yields

$$\tau_{CSA} = \frac{\tau_C}{\sqrt{17}} \quad (15)$$

And substituting this back into the relationship for the RC time constant gives

$$\tau_{RC} = 4 \times \frac{\tau_C}{\sqrt{17}} \quad (16)$$

This approximation again allows the rendering of a ratiometric relationship between the RC network, the CSA, and the total network allowing the system to be solved. R_{FILT} is then given as

$$R_{FILT} = \frac{\tau_{RC}}{C_{FILT}} \quad (17)$$

However, given the nature of the approximations above, an optimal value of R_{FILT} may fluctuate slightly from this calculated value, so a range of values is examined, typically from $0.25*R_{FILT} < R_{FILT} < 2*R_{FILT}$.

Finally, with values for R_{FILT} and C_{FILT} determined, the bandwidth needed by the amplifier can be determined. Expressing the bandwidth of the amplifier in terms of frequency, and relating this to the RC time constant, this is given as

$$BW = \frac{1}{2 \times \pi \times \tau_{CSA}} = \frac{1}{2 \times \pi \times \frac{\tau_{RC}}{4}} = \frac{2}{\pi \times R_{FILT} \times C_{FILT}} \quad (18)$$

This reveals that if the bandwidth determined here is greater than the bandwidth of the current amplifier, adjustments must be made to ensure accurate settling.

Note

The mathematics discussed to this point are those performed in the "SAR ADC Drive" section of TI's Analog Engineer's Calculator. Therefore, discussion to this point is mainly for the reader's benefit to understand the theory behind these values, and quick calculation of these values may be easily obtained by use of this tool. The tool can also be utilized to help trim these values to determine an optimal acquisition time and filter for the amplifier's given bandwidth.

4 Output Filter Discussion and Design

With the above approximations, we now have a range of values for potential resistances, R_{FILT}, and capacitances, C_{FILT}, that can be used to design the charge bucket filter for a given acquisition time. The challenge now set is the design of a filter that allows convergence to 1/2LSB, but also maintains system stability. With this information, we can design a filter that optimizes to this criterion by examining the output impedance of the amplifier in question, and how that amplifier will interact with the attached filter to drive the sampling node.

Here, we will examine the design of the INA293 with the ADS8860, a 16-bit, 1MSPS true differential input device. This device was chosen to examine potential maximization of sampling rate for the INA293, as lower resolution, or lower acquisition time would result in relaxed design constraints here.

Using the ADS8860 data sheet, we can determine the following parameters as shown in ADS8860 Key Specifications.

Table 4-1. ADS8860 Key Specifications

Parameter	Value
ADS8860 Resolution	16 bits
ADS8860 Conversion Time (maximum)	710 ns
ADS8860 Acquisition Time (minimum)	290 ns
Sample and Hold Capacitance, C_{SH}	59 pF

Beginning with these values, and using the expressions derived in the previous section, the following calculated values are shown in Analog Engineer's Calculator Results.

Table 4-2. Analog Engineer's Calculator Results

Parameter	Value
1/2 LSB, FSR = 4.096V	31.25 µV
$C_{FILT, MIN} = 10*C_{SH}$	590 pF ≅ 600 pF
$C_{FILT, NOM} = 20*C_{SH}$	1180 pF ≅ 1200 pF
$C_{FILT, MAX} = 30*C_{SH}$	1770 pF ≅ 1800 pF
τ_C, min	35.93 ns
τ_{RC}	34.86 ns
$R_{FILT, MIN}$	7.4 Ω
$R_{FILT, NOM}$	29.55 Ω
$R_{FILT, MAX}$	59.1 Ω
Bandwidth Required, Nominal	18.3 Mhz

Examining the calculated values, it can immediately be observed that the required estimated bandwidth is much larger than the 1.2MHz offered by the INA293, and therefore, this ADC is most likely not able to be correctly driven at its 1MSPS default sampling rate by the INA293. Therefore, the sampling rate will need to be relaxed. However, this paper will continue to examine this design flow to provide context to the reader as to the behavior such a design will exhibit prior to correcting this, as iteration in a design such as this is key in optimizing the design for the given application.

Using the techniques discussed in Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT, a good starting place is to examine the output impedance of the INA293. Examining the INA293 spice model, it can be confirmed Using a small signal input placed at the output of the device that the model contains model parameters for the output impedance of the device, and can therefore be used to perform simulations, such as examining device stability, and examining the amplifier's ability to properly drive the ADC sample and hold circuitry. An example of this circuit and its corresponding output are shown in INA293 Z_{OUT} Test Circuit and INA293 Z_{OUT} Output Impedance below.

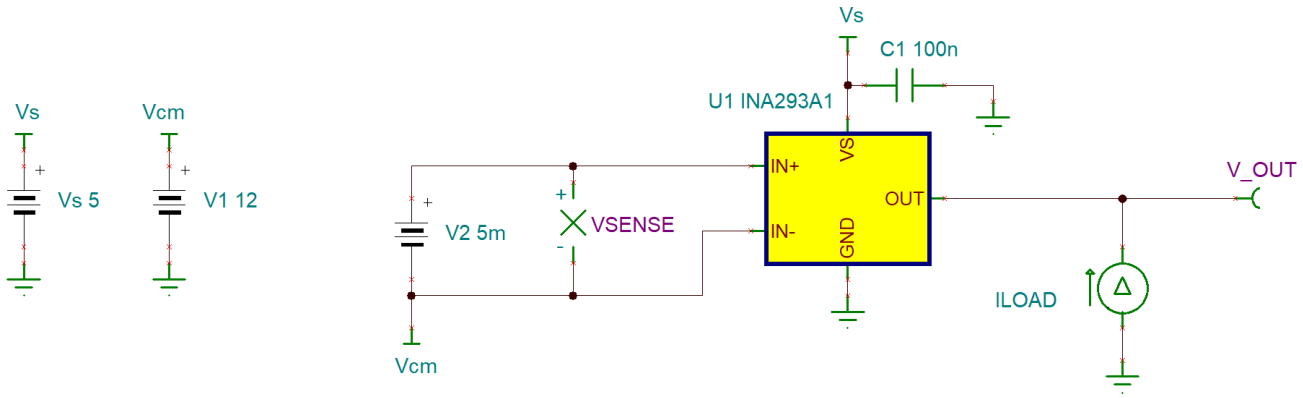

Figure 4-1. INA293 Z_{OUT} Test Circuit

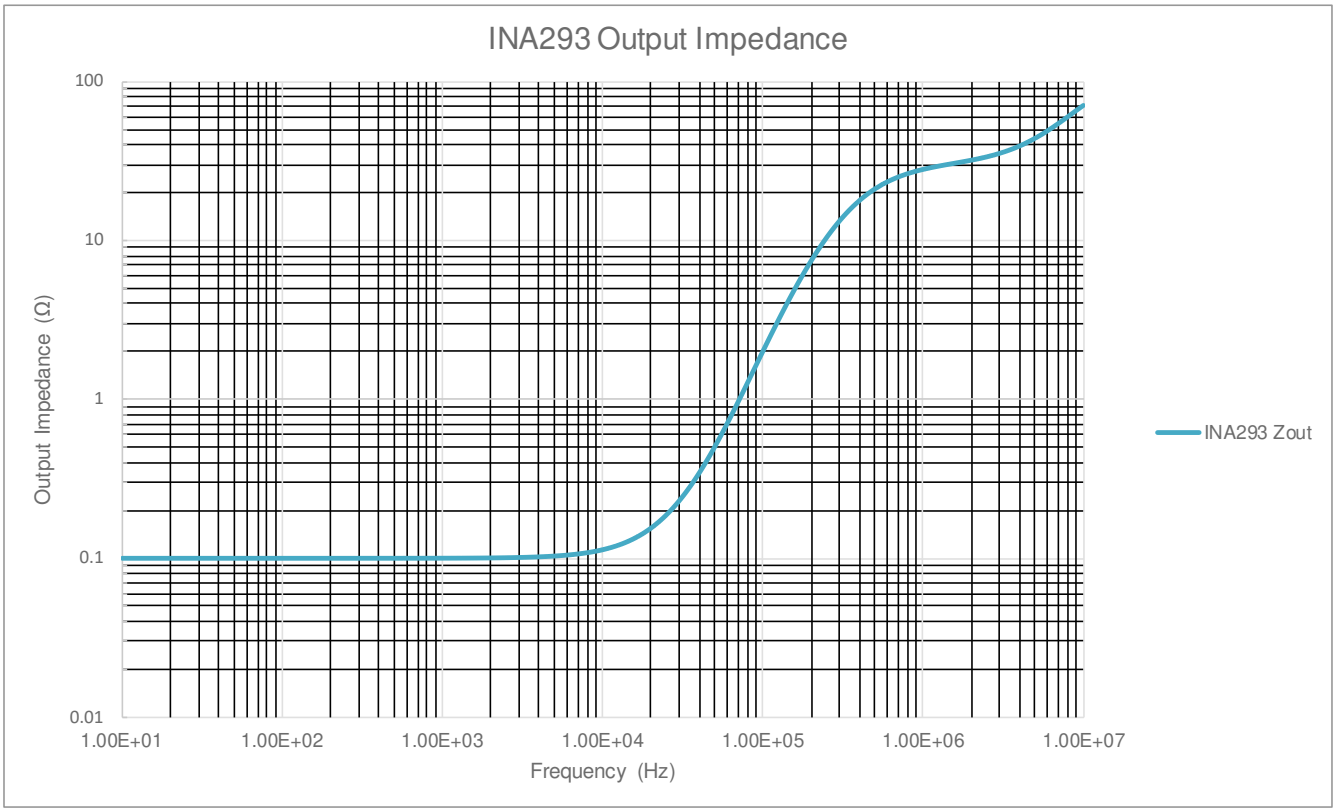

Figure 4-2. INA293 Z_{OUT} Output Impedance

Next, examining the presence of a non-isolated capacitive load on this output for each of the filter capacitance options renders the following output for each of these loads as shown in Z_{EQ} for Various C_{FILT}.

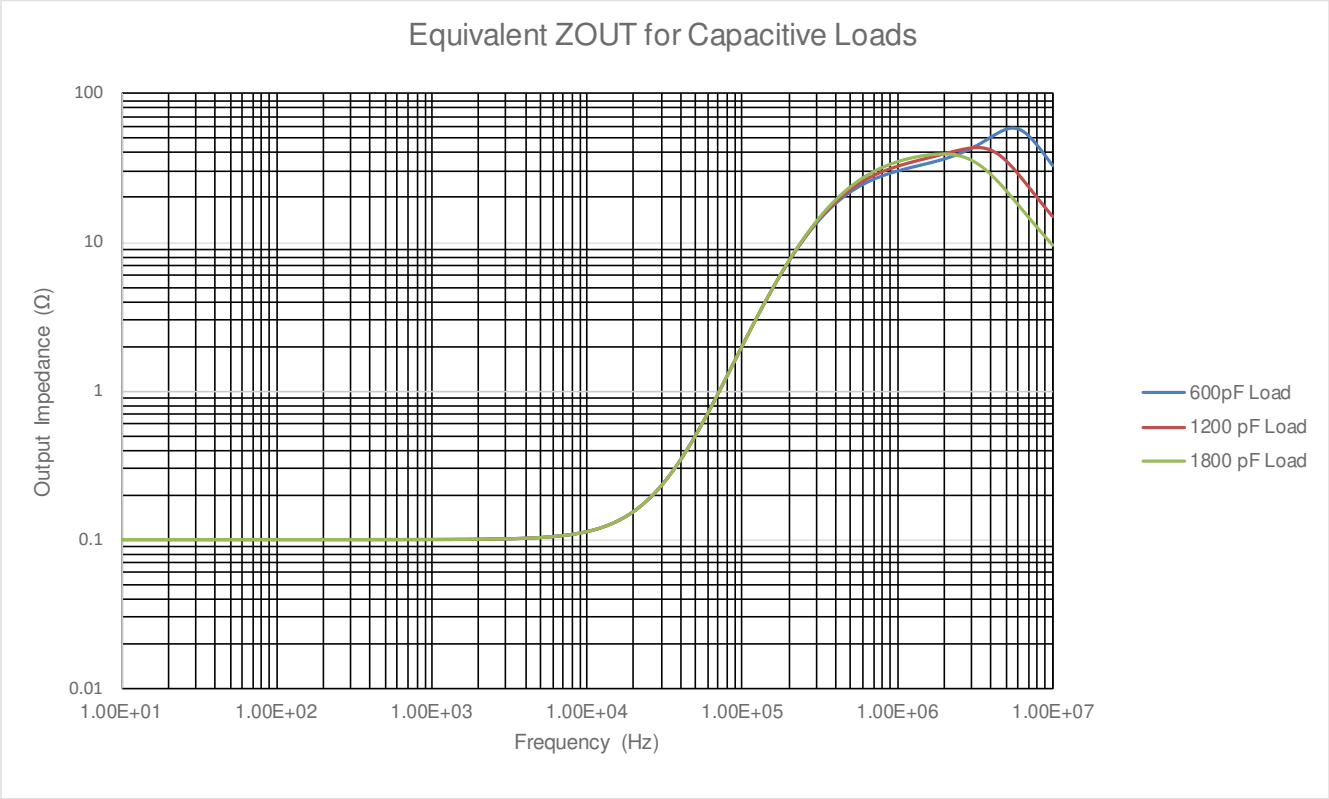

Figure 4-3. Z_{EQ} for Various C_{FILT}

The presence of these capacitors create a set of complex conjugate poles with the output impedance of the amplifier, and therefore steps need to be taken to ensure that the amplifier will remain stable over the range of frequencies.

Examining the regions where the INA293 output impedance and each capacitor close on one another, it can be seen that the output of the INA293 corresponds with a roughly singly inductive curve, due to the 20dB per decade increase of the impedance over frequency (note that the above figure exhibits impedance in ohms on the y-axis, not in dB). This system can be therefore be approximated as a second order pole approximation, where the poles of the system are given as:

$$s_{p1}, s_{p2} = -\frac{R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}} \tag{19}$$

For the value of these poles to be real, the second term of this equation must result in a positive value. Taking this term and solving the inequality of this expression, it can be shown that

$$R \geq 2 * \sqrt{\frac{L}{C}} \tag{20}$$

Or a resistance must be present that is greater than the interaction of the inductive portion of the curve with the added C_{FILT} load. The inductive portion of the curve can be approximated at each point by the traditional formula for inductance over frequency, or

$$Z_L = j\omega L \rightarrow L = \frac{Z_L}{2\pi f} \tag{21}$$

Approximating this inductance for each point on the curve, a resistor value for each case is calculated in Minimum R_{FILT} Approximations for Stability.

Table 4-3. Minimum R_{FILT} Approximations for Stability

C_{FILT} (pF)	Crossing Frequency (MHz)	$Z_{L,\ approx.}$ (Ω)	L, approx. (µH)	$R_{FILT,\ Calculated}$ (Ω)
600	4.5	55	1.95	114
1200	3	45	2.39	89
1800	2.5	40	2.55	75

This provides a general starting point for R_{FILT}, although this value may need to be adjusted based on ADC topology or settling.

4.1 INA293 With the ADC Switching Model

Figure 47 of the ADS8860 data sheet also provides an input sampling stage equivalent circuit, which provides a starting point for construction of a sampling stage circuit for simulation. Here, a series of voltage controlled switches can be implemented to effectively create a model of this topology in simulation:

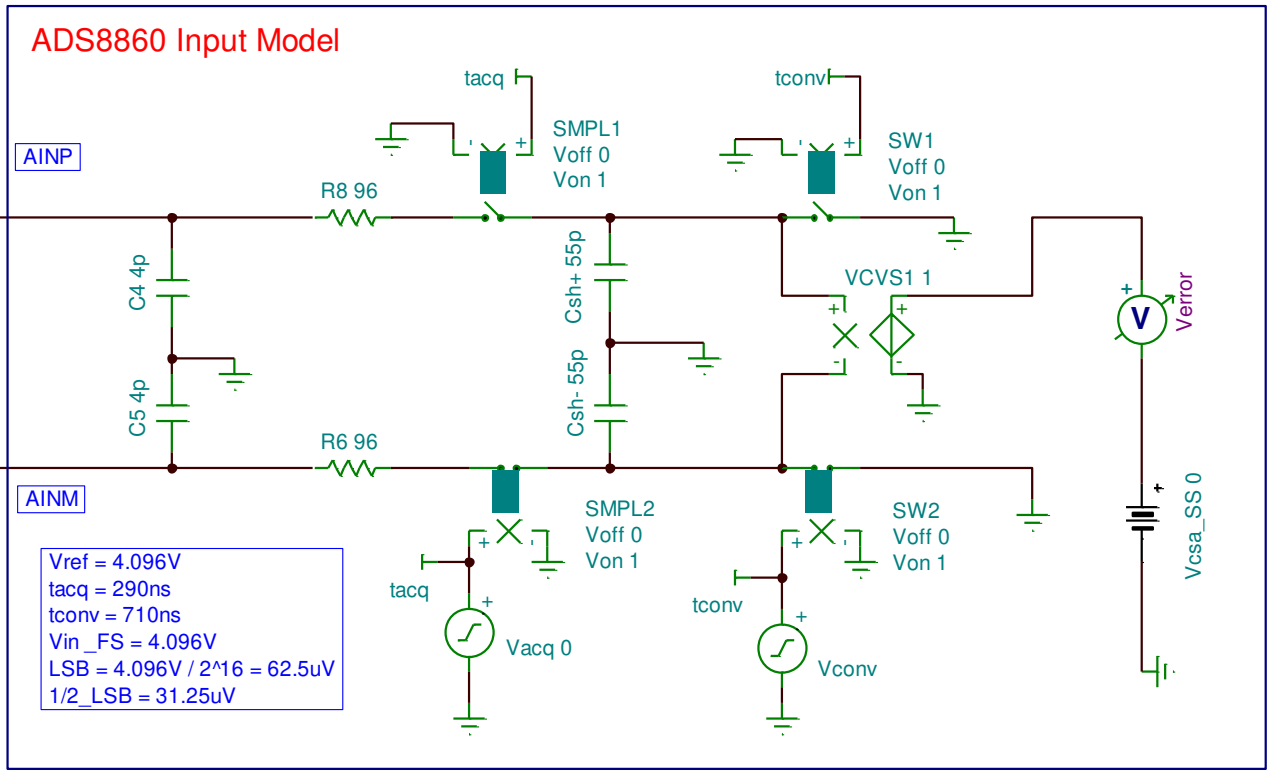

Figure 4-4. ADS8860 Switching Simulation Model

In this model, the voltage sources at the bottom effectively create pulse widths, where the left source generates the acquisition time of the device, and the right generates the conversion time. It should be noted that for this simulation, the conversion time is handled simply as a small pulse at the end of the sampling period to create a worst case voltage droop and secure a more robust testing scenario.

Next, the INA293 SPICE model, the charge bucket filter, and the ADS8860 switching model are connected together, resulting in a final simulation environment that can be used to validate stability and settling accuracy. If the device is capable of converging under this use case, it can be inferred that the device should be capable of responding to any other value inside the sample and hold time. However, prior to beginning analysis, the steady state value of the error must be calibrated. This allows the model to ignore other error contributions here, such as offset of the amplifier, and examine only the switching models ability to settle to steady state. This is achieved by performing a DC steady state analysis simulation with the model under full-scale input, steady-state output constraints. Once the steady state output is known, the value of the error reference is updated to this value so that, should the simulation perform as expected, the error shown in the simulation will converge to zero. The necessary portions to be observed and changed are indicated in Steady State Error Calibration Information:

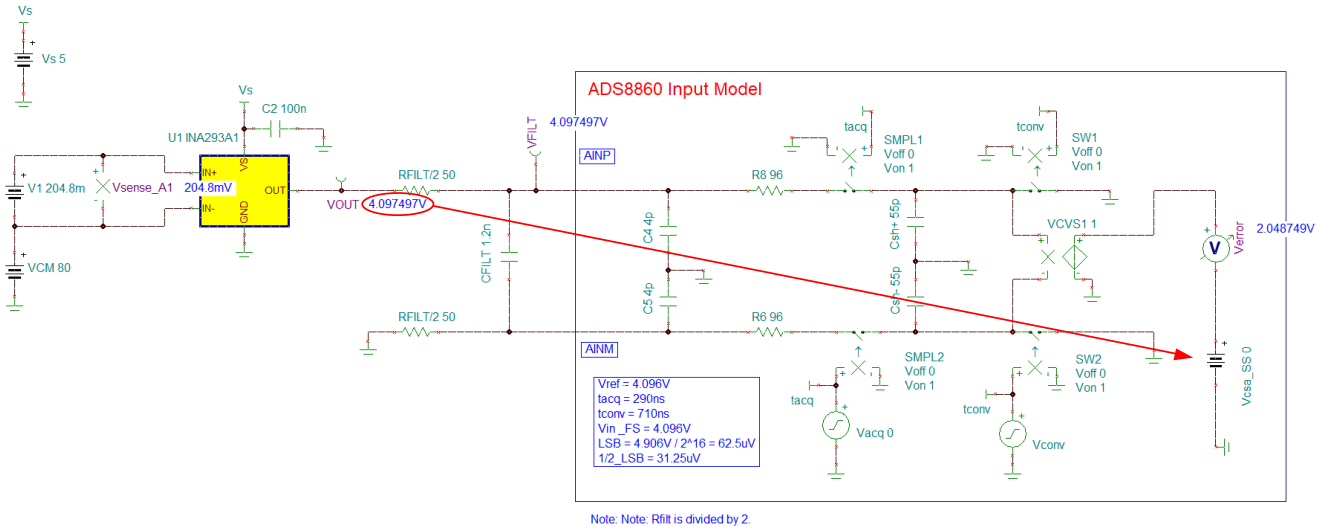

Figure 4-5. Steady State Error Calibration Information

With the system calibrated to steady state, data can now be captured. For the simulation data captured in Initial Simulation Results below, the filter is examined at the calculated C_{FILT}, 1200pF, and its corresponding $R_{FILT, MAX}$ of 59.1Ω (note that for the single ended #2 topology, this resistance is split between the resistors on each leg of the ADC). The maximum resistance was chosen here, as by earlier calculations, it was shown that resistance should be greater than 89Ω for stability purposes. The goal is to examine the response of the device under given parameters of the Analog Engineer's Calculator before making adjustments to the design. The amended schematic and its corresponding output is shown in the figures below.

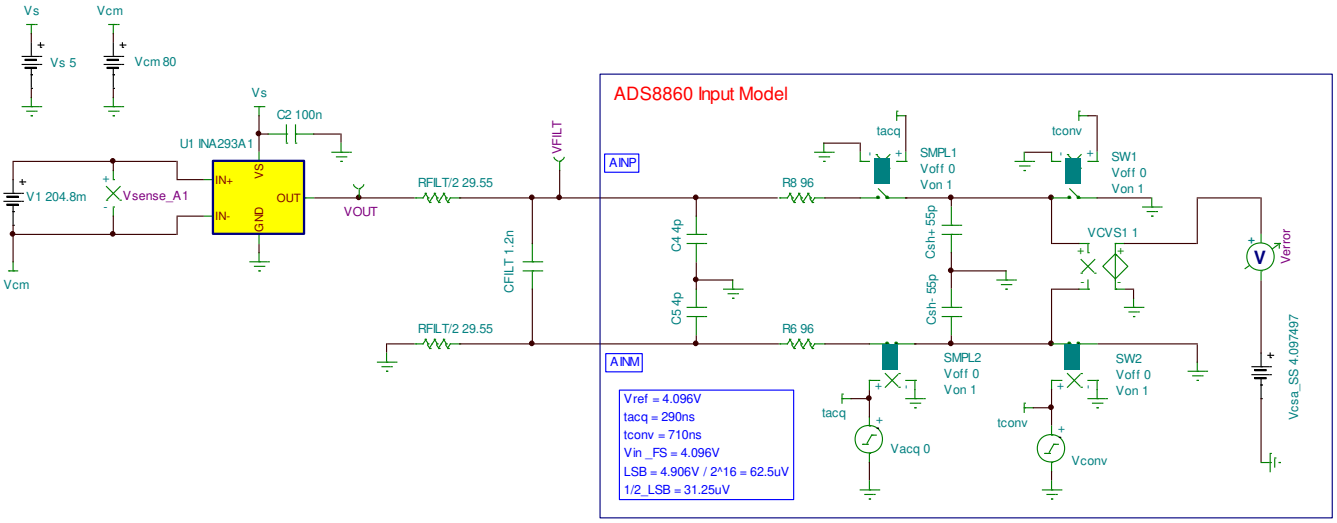

Figure 4-6. Full Initial Simulation Schematic

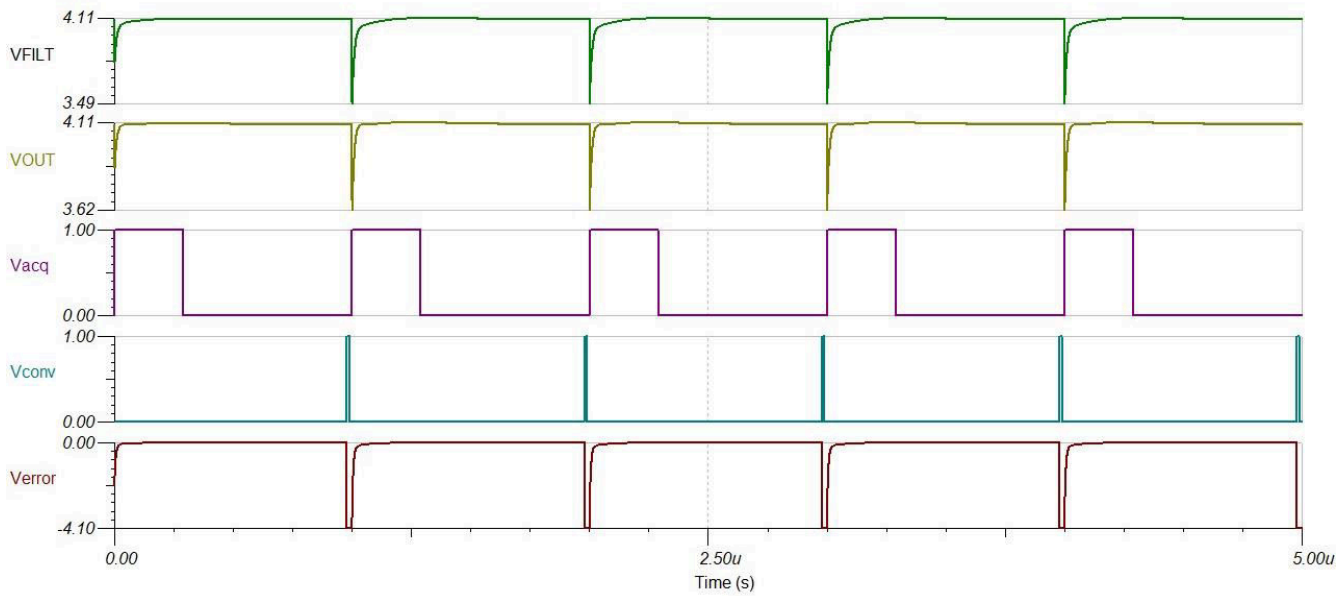

Figure 4-7. Sample and Hold Initial Waveforms

It can be seen by inspection in the initial simulation that the output is still in the process of settling in this configuration. The data shows that the output is not fully settled, and this demonstrates as observed earlier that the device cannot drive the ADS8860 in this configuration without some amount of data loss. There are several avenues to be investigated at this point: the filter values can be re-evaluated, the output of the INA293 can be buffered with a device that possesses the bandwidth to properly drive the device at this sampling rate, or, with certain devices such as the ADS8860, the sampling clock can be relaxed to extend the acquisition time to an acceptable level.

An issue also presents itself here from earlier analysis, in that a resistor value larger than 89Ω is needed to guarantee stability (for 1200pF). This means that with the calculated values of R_{FILT} by the assumptions made, for all cases shown, we risk instability in the system. This needs to be balanced, however. While a higher value of R_{FILT} helps mitigate amplifier stability issues, this resistance also adds distortion as a result of interactions with the nonlinear input impedance of the ADC. This distortion increases with the added resistance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FILT} requires balancing the stability of the driver amplifier and distortion performance of the design.

As the bandwidth needs of the system in this current configuration are greater than can be provided by the INA293, a final option exists before designing in a buffer: relaxation of the sampling clock of the ADC. While 1MSPS with this device looks unachievable, in many modern ADCs, t_{sample} is calculated as the sum of t_{acq} and t_{conv}, where t_{conv} is a fixed parameter inside the ADC that is generated by an internal clock, but the acquisition time is determined from an external clock provided to the ADC to establish the sampling rate. This means that if the device is sampled at a rate below its default sample rate, the time added to the sampling period effectively increases the time of t_{acq}, allowing the INA293 additional time to settle. From the mathematics discussed in The ADC Charge Bucket Filter, it can also be shown that relaxation of the sampling period also provides a larger selection of R_{FILT}. Furthermore, a combination of these equations can be rearranged to demonstrate that for a given bandwidth, resolution, and filter network, the acquisition time needed for proper settling is

$$t_{ACQ} > \frac{-\sqrt{17}}{2\pi \times BW} \times \ln\left(\frac{LSB}{2 \times V_{DROOP}}\right) \quad (22)$$

For the INA293, the closed loop bandwidth of the A1 variant is 1.3MHz. Using the above equation, it can be derived that with this bandwidth, the INA293 needs approximately 4.1µs to properly drive an ADC with a filter designed inside the calculated criterion. Note that the derivations for C_{FILT} are primarily based off of the sample and hold capacitance C_{SH}, and therefore do not change from the initial design. The range of R_{FILT} however, is increased as a result of this change in sample rate, and now provides selectable values inside a range that

are above the stability criterion derived earlier. For ease of clock generation, a new sampling period of 5µs is chosen, and as conversion time remains the same at 710ns, the new acquisition time is now 4.29µs.

A 200kHz sampling rate is simulated in ADS8860 Adjusted Response, f_{sample} = 200kHz. The minimum calculated RFILT of 104.4Ω is split across the charge bucket filter. The second image is a closer look at the error signal inside of a single acquisition period.

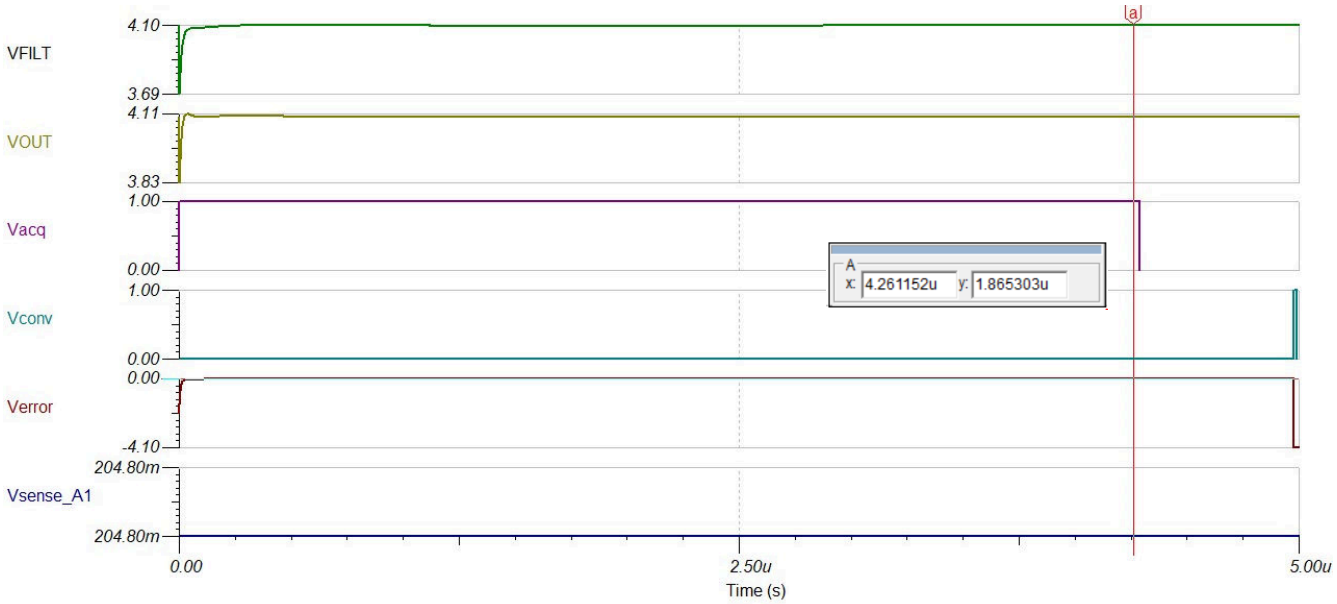

Figure 4-8. ADS8860 Adjusted Response, f_{sample} = 200kHz

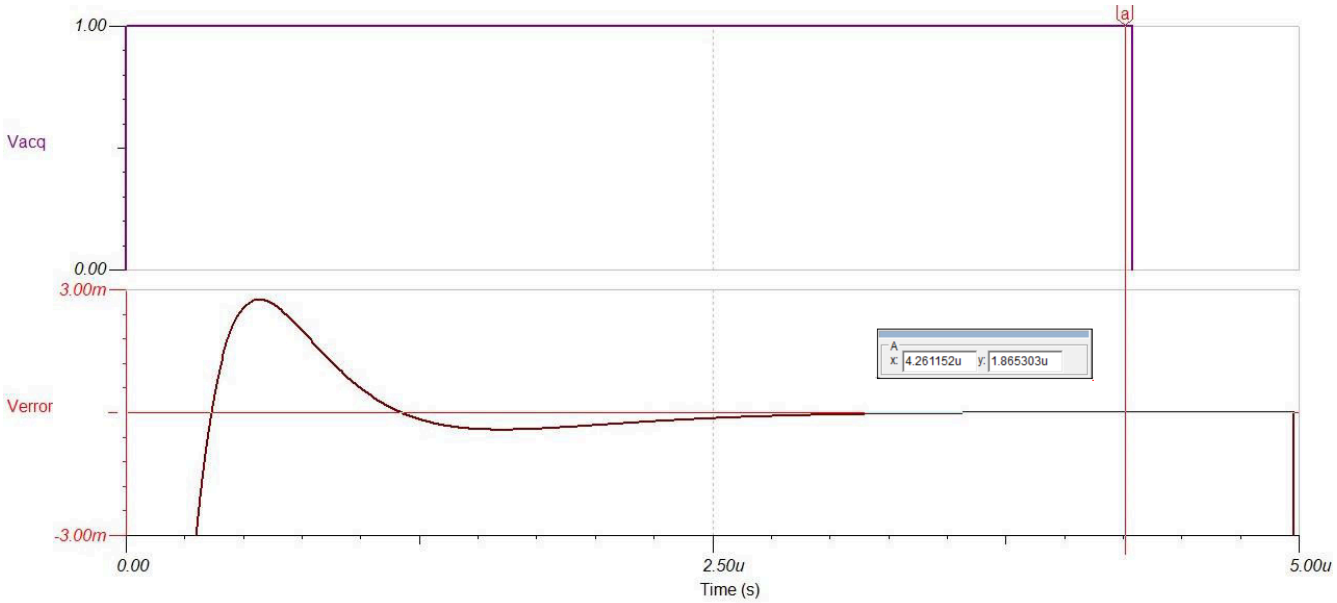

Figure 4-9. ADS8860 Error Response, fsample = 200kHz, R_{FILT} = 104.4Ω

It can now be observed that the amplifier has room to settle and converges to well inside 1/2 LSB inside the acquisition time. However, this does not complete the design. The final technique to discuss is optimization of the error response. While a range of resistances based on approximation is a good starting point, there is merit in examining the effect of this resistance over a range of values to optimize the response of the amplifiers settling. Inside the simulation, it is possible to test a range of values for R_{FILT}, and observe how the response is shaped in relation to these resistance values. A range of 50Ω to 150Ω is shown in Effects of R_{FILT} on Error Response.

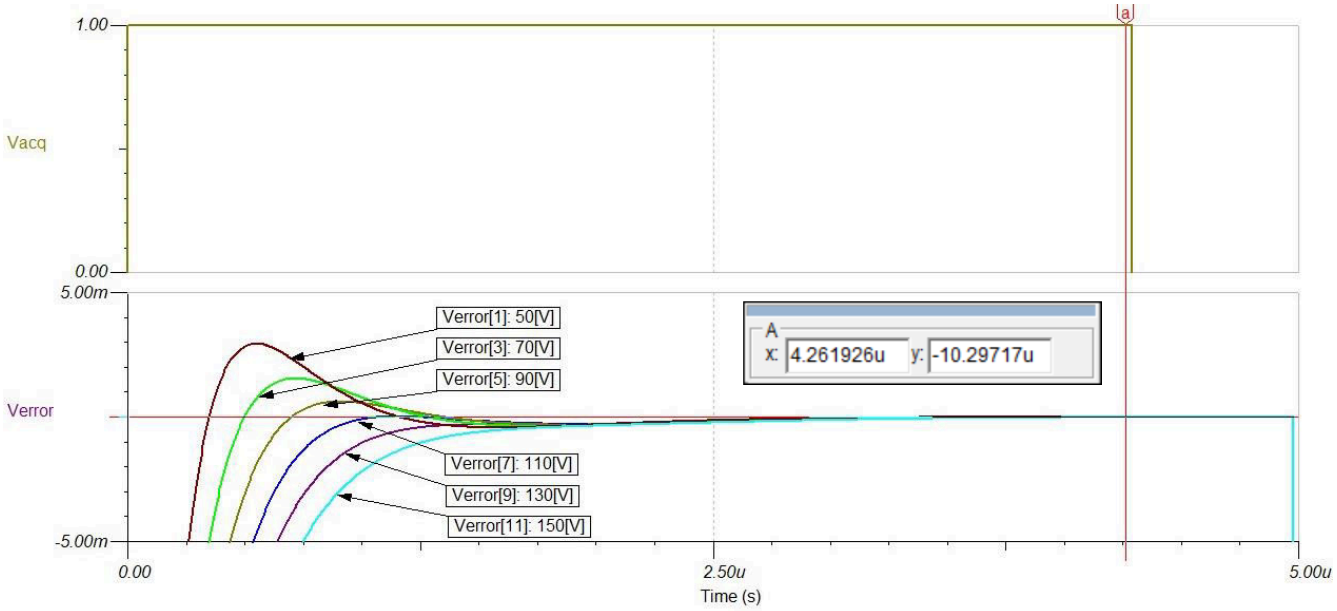

Figure 4-10. Effects of R_{FILT} on Error Response

Examining the effects of these resistances on the output impedance of the amplifier and the 1200pF capacitor, it can be observed that the impedance curve softens as additional resistance is added, beginning to converge towards a well dampened response around 130Ω:

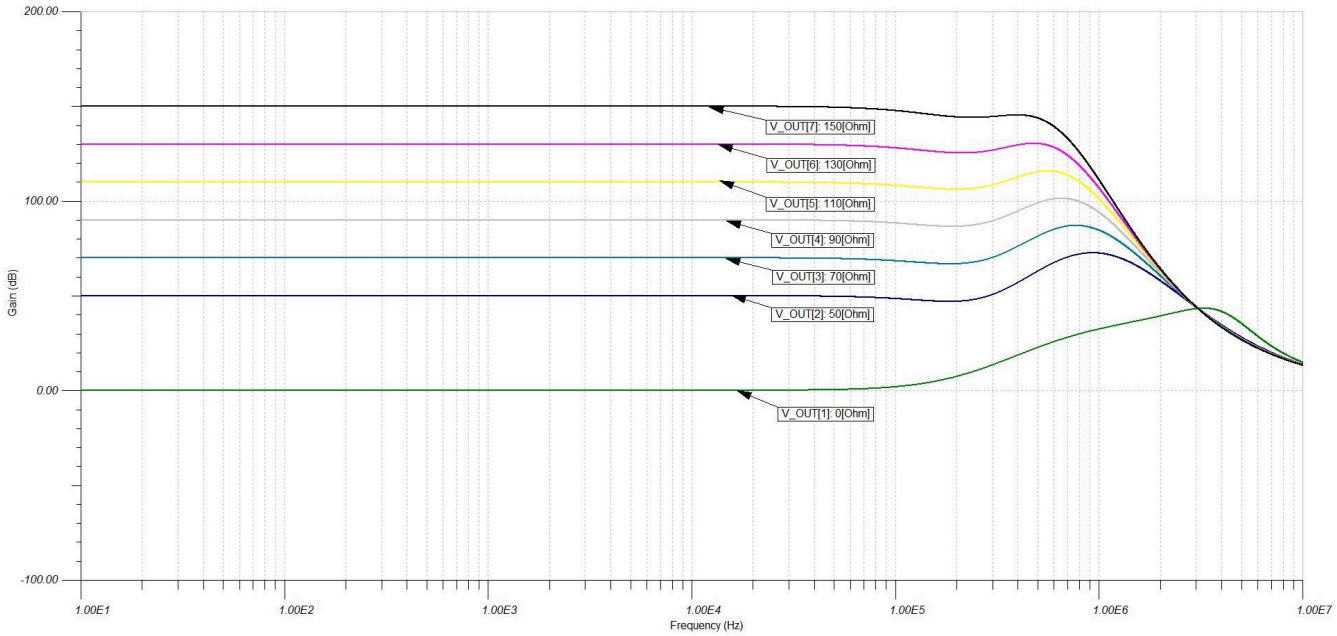

Figure 4-11. AC Response of INA293 With Various R_{FILT}

If necessary, additional iterations can be made inside of these values to further tighten resistances. However, 130Ω is chosen here, as it provides a reasonably damped response while still providing proper settling inside the acquisition window to -10.29uV. Finally, note that the final settled value is slightly higher than the previous iteration. This is due to distortion added from the increased value of resistance, but still allows the design to settle within the required range.

5 Summary

From the discussion of these various topics above, it shows that an algorithm may be established to help in the realization of designing a charge filter for a current shunt amplifier using the following steps:

1. Choose the current sense amplifier that is correct for your application.
2. Determine the digital sampling requirements of your system, and shortlist possible ADCs that may work for the intended design. Important parameters to note are default acquisition time, sample and hold capacitance, and resolution.
3. Use the bandwidth of the amplifier, resolution of the ADC, and the assumption of voltage droop to approximate the minimum needed acquisition time.
4. Either select a device with the appropriate acquisition time, or identify if the ADC chosen has the ability to extend acquisition time via the use of an external clock.
5. Determine the potential range of values for C_{FILT} based on the C_{SH} value of the chosen converter. This can quickly be achieved using the Analog Engineer's Calculator.
6. With the value of C_{FILT}, calculate the needed value of R_{FILT}.
7. Ensure that the chosen value of R_{FILT} is greater than the minimum required calcuation for stability based on the amplifiers output impedance.
8. Simulate the designed system using the created switching model to ensure proper settling inside the designed parameters. Iterative analysis of R_{FILT} can help achieve additional accuracy if necessary.

6 References

1. Texas Instruments, *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using ZOUT* application report.
2. Texas Instruments, *Analog Engineer's Circuit Cookbook: Data Converters*.
3. Texas Instruments, *Building the SAR ADC Model*.
4. Texas Instruments, *Math Behind the R-C Filter Component Selection*.

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