Application Report
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How Comparator Topology Influences Propagation Delay

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ABSTRACT

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1 Abstract

When using microprocessors, field-programmable gate arrays (FPGAs), or systems-on-a-chip (SOCs) there are power supply tolerances that must be met. Because of these power supply requirements, external monitoring of the power supply is necessary to ensure that the processor is in reset mode when the supply voltage falls below (undervoltage) or rises above (overvoltage) the specified range. Many microprocessors, FPGAs, or SOCs have internal voltage monitoring, but external voltage monitoring is often necessary for redundancy. External monitoring is often required to prevent memory from being corrupted when these events occur. When external monitoring is required, there are three types of voltage monitors available: undervoltage, overvoltage, and window (a combination of undervoltage and overvoltage). As advances in the semiconductor industry continue, silicon devices have been pushed to lower and lower power levels. With an increase in the amount of products that run off of batteries, having a supervisor with a low supply current (I_{DD}) is essential. This report aims to discuss voltage supervisors and how the move towards lower power supervisors affects the propagation delay.

1.1 Trademarks

2 Introduction

Striving towards longer battery life has pushed all devices in the system to have low supply current, which is especially true of supporting circuitry that is always on (such as supervisory circuits). Supervisory circuits are used for initialization and startup, undervoltage detection, diagnostics, and adhering to safety regulations.

An undervoltage supervisor has a single comparator with hysteresis that monitors the SENSE pin voltage through a resistor divider, as shown in Figure 1. In an undervoltage supervisor when the voltage drops below the negative threshold the $\overline{\text{RESET}}$ output is asserted (driven low).

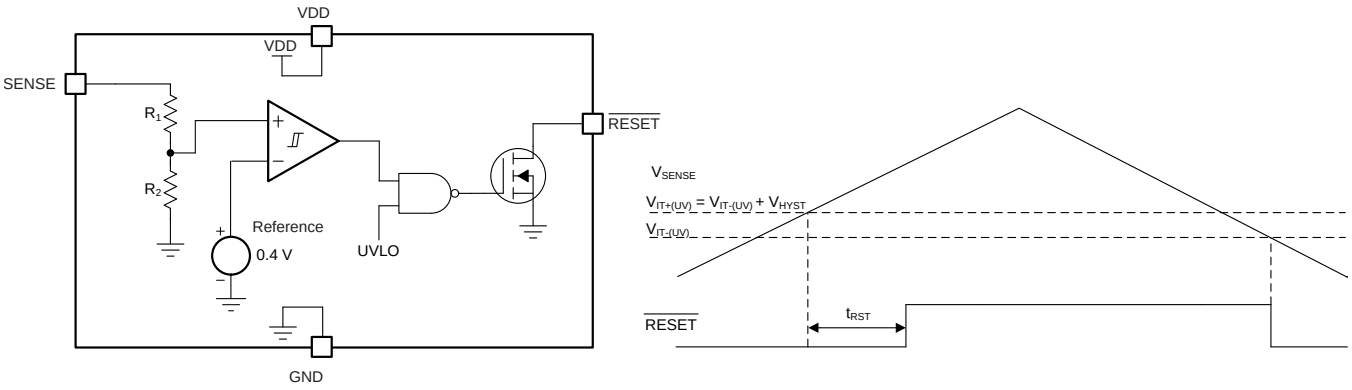

Figure 1. Undervoltage Supervisor Block Diagram and Timing Diagram

A window supervisor consists of two comparators, one monitoring the overvoltage threshold and one monitoring the undervoltage threshold. The signals from these two comparators are then ANDed together to make a $\overline{\text{RESET}}$ output, or can be used individually to create separate overvoltage (OV) and undervoltage (UV) outputs. Figure 2 shows the block diagram for a single $\overline{\text{RESET}}$ output window comparator. If the voltage on the SENSE pin drops below the negative threshold ($V_{IT-(UV)}$), then $\overline{\text{RESET}}$ is asserted (driven low). When the voltage on the SENSE pin is between the positive and negative threshold voltages, $\overline{\text{RESET}}$ deasserts after the $\overline{\text{RESET}}$ delay time, as shown in Figure 2.

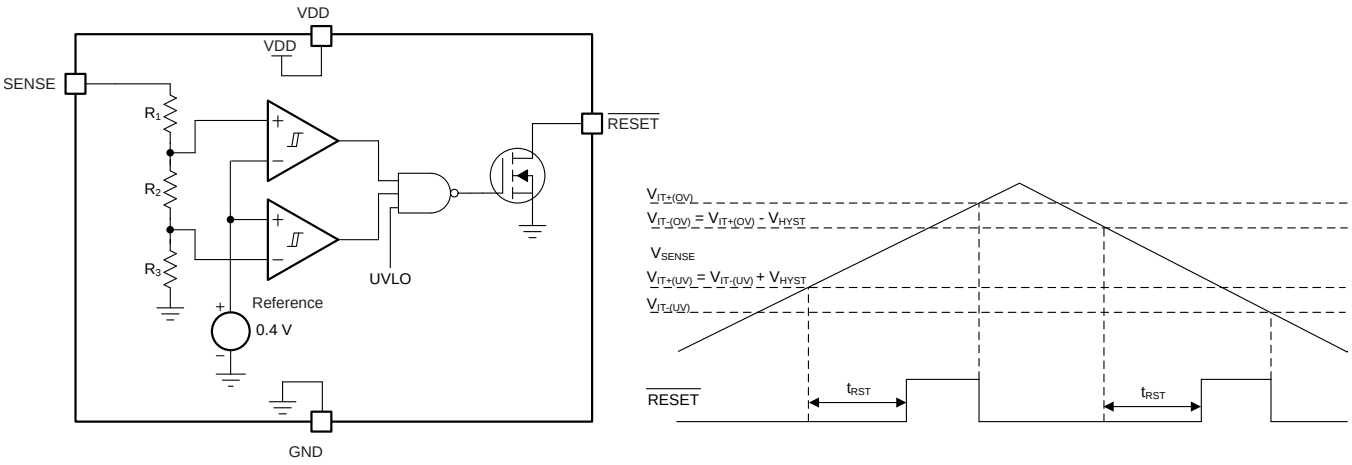

Figure 2. Window Supervisor Block Diagram and Timing Diagram

3 Understanding the Supervisor Comparator

There are four main blocks to a supervisor: the voltage reference, comparator, reset delay timing, and the output (open-drain or push-pull). Figure 1 illustrates how these blocks interact to form a supervisor. This paper primarily focuses on the comparators and how different architecture choices affect both supply current and propagation delay. There are two types of outputs for comparators, one is an active pullup current source and the other is a push-pull output. Both of these topologies will work for producing a $\overline{\text{RESET}}$ signal, but each has their limitations.

Typically supervisors use the active pullup illustrated in Figure 3, as this output offers more control over the amount of supply current that is being used. When using the active pullup output, the maximum amount of current that can be used in the output stage is the current from the current source. When using the topology in Figure 4 with a push-pull output, there can be a large increase in the I_{DD} resulting from shoot-through current. Shoot-through current is where both of the transistors are on simultaneously and current passes straight through the two transistors. Using the push-pull topology, shoot-through current occurs whenever the voltage approaches the comparator threshold. In most applications this current increase is undesirable even though faster response times may result.

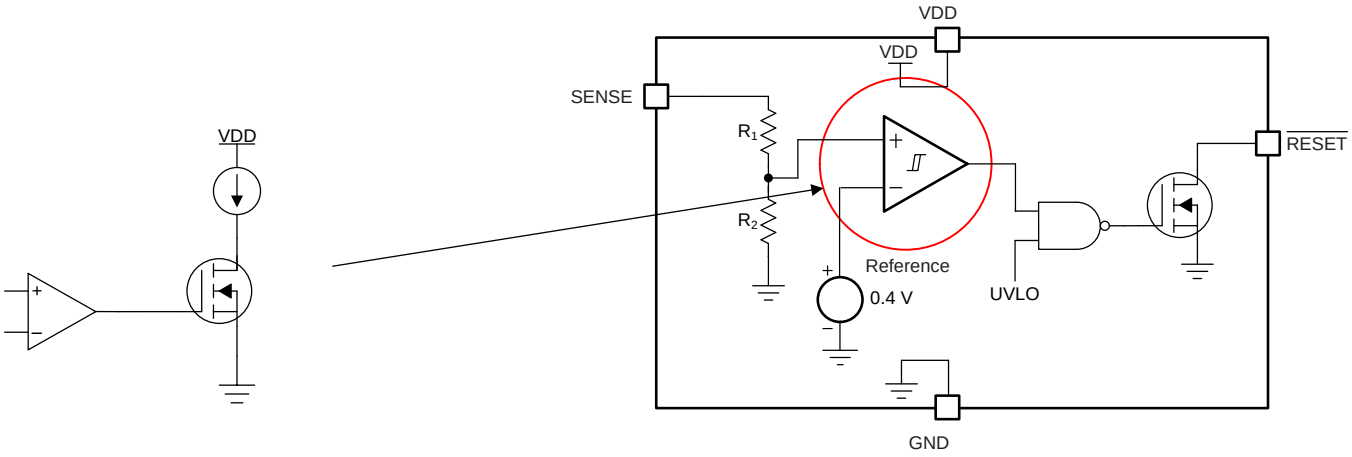

Figure 3. Comparator with Active Pullup Current Source

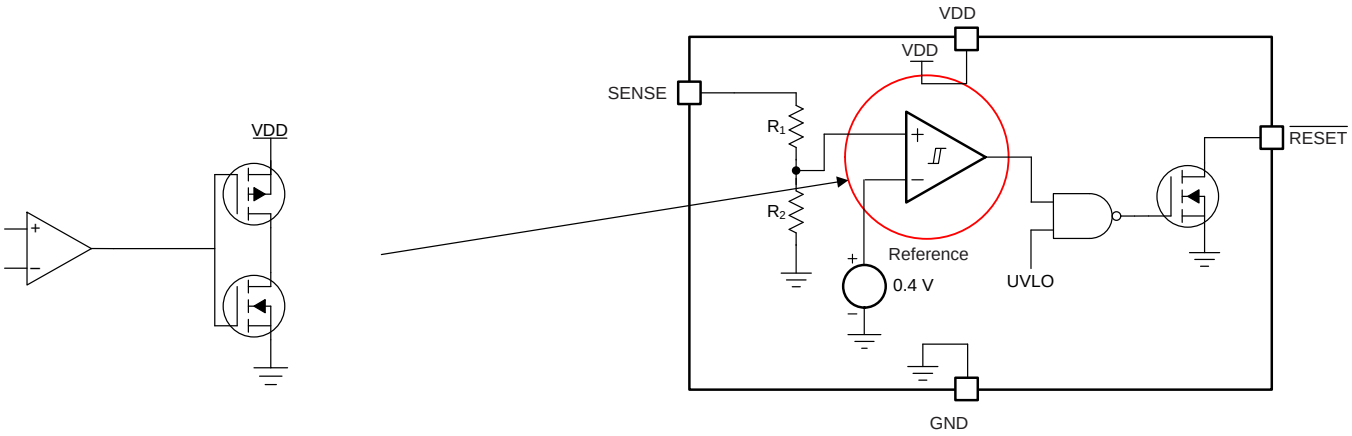

Figure 4. Comparator with Push-Pull Output

4 How Comparator Architecture Influences the System

Section 3 details why most comparators in supervisory circuits use the active pullup topology. This topology has a large impact on the system, specifically on how supply current and propagation delay is effected. The effect of comparator architecture is most evident in window comparators where there are both overvoltage and undervoltage thresholds. However, these effects can be seen in all supervisors. Figure 5 illustrates the typical architecture for window comparators. In Figure 5 there are two comparators with a PMOS differential pair that are being loaded by an NMOS current mirror. One side of the differential pair is being tied to the reference voltage and the other side is attached to the resistor divider. All the comparators in Figure 5 and Figure 6 have the active pullup discussed in Section 3. These comparators are then followed by a Schmitt trigger and inverters. A Schmitt trigger is required on the output because this is a slow changing node. If a Schmitt trigger is not used there can be a large increase in supply current when the voltage is near the threshold.

The two comparators also have a difference in the data path that contributes to the difference in propagation delay. The undervoltage comparator only has a single inverter and the overvoltage comparator has two inverters. Because of this architecture there is a difference in propagation delay between the undervoltage and overvoltage faults. This difference comes from active load and the number of inverters. Section 5 discusses why having an active pullup on the comparators produces a difference in propagation delay.

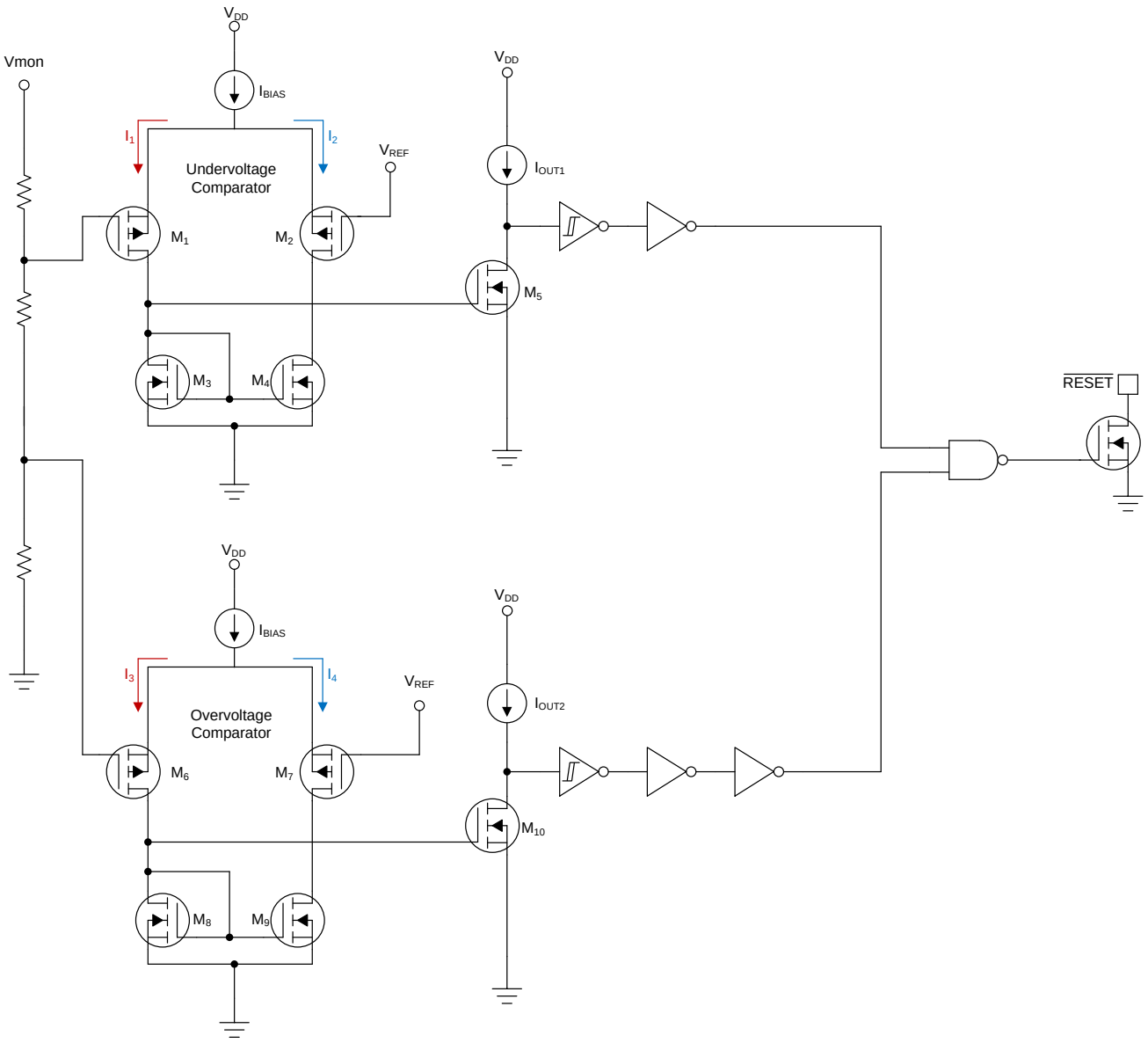

Figure 5. Window Supervisor Architecture With a Single Output

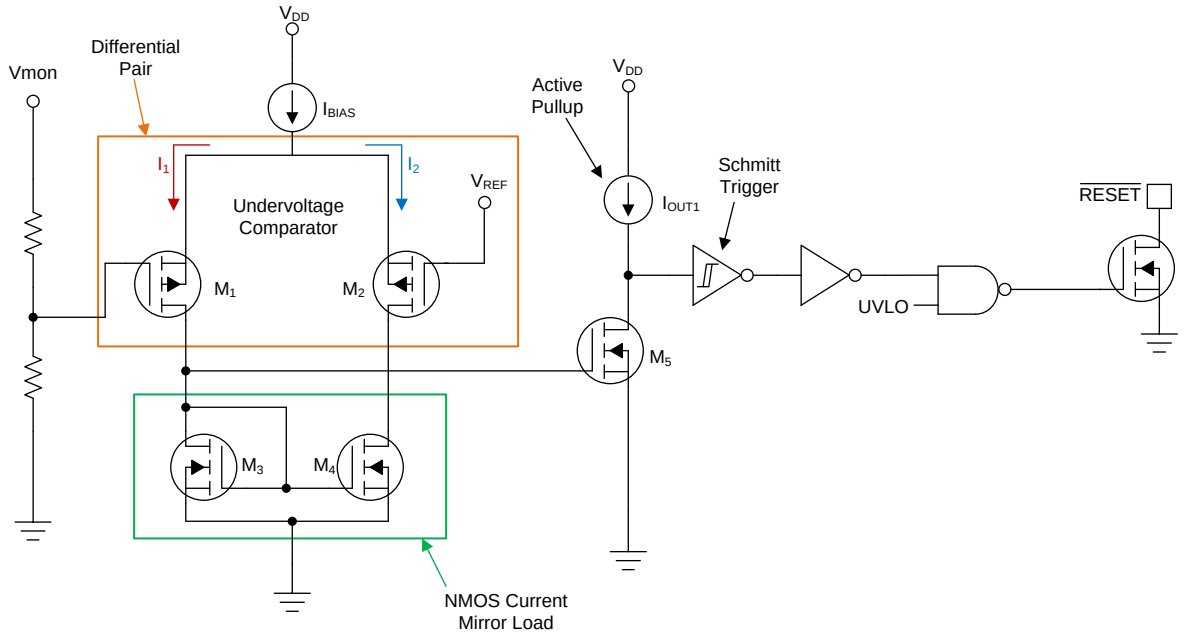

Figure 6. Undervoltage Only Supervisor Architecture

5 Difference in Propagation Delay for Window and Undervoltage Supervisors

Table 1 shows the basic states of the two comparators along with the fault condition. In Table 1, V_{UV} is the input voltage to the undervoltage comparator and V_{OV} is the input voltage to the overvoltage comparator. Table 1 shows that when $V_{UV} > V_{REF}$ and $V_{OV} < V_{REF}$, there is no fault condition; otherwise, there is a fault condition and the supervisor is in either state 2 or 3. Now using Figure 5, each of the states will be examined to show why there is a difference in the overvoltage and undervoltage propagation delay.

Table 1. Fault Condition Based on Comparator Inputs

State	V_{UV}	V_{OV}	Fault
1	V_{UV} (1) > V_{REF} (2)	V_{OV} (3) < V_{REF}	None
2	$V_{UV} < V_{REF}$	$V_{OV} < V_{REF}$	Undervoltage
3 (2)	$V_{UV} > V_{REF}$	$V_{OV} > V_{REF}$	Overvoltage

(1) V_{UV} is the input voltage to the undervoltage comparator.
(2) V_{REF} is the reference voltage that V_{UV} and V_{OV} are compared to.
(3) V_{OV} is the input voltage to the overvoltage comparator.

5.1 State 1: No Fault Condition, $\overline{RESET}$ Deasserted

In state 1 $V_{UV} > V_{REF}$ and $V_{OV} < V_{REF}$. Because of the PMOS input pair when $V_{UV} > V_{REF}$ M_2 conducts more current than M_1 ($I_2 > I_1$). When M_2 conducts more current than M_1, M_5 turns off. The active pullup then charges the parasitic capacitance of M_5, causing the drain of M_5 to rise to V_{DD}. In the overvoltage comparator $V_{OV} < V_{REF}$, M_6 then conducts more current than M_7 ($I_3 > I_4$), causing M_{10} to turn on and drag the drain of M_{10} to GND. Note that when there is no fault, M_5 is off and M_{10} is on.

5.2 State 2: Undervoltage Fault Condition, $\overline{RESET}$ Asserted

There are two times when the supervisor is in state 2, the first is during startup when either V_{DD} or V_{SENSE} is still rising, the other is when the supervisor is leaving state 1 because of a transient on V_{DD} or V_{SENSE}. The most interesting case is when leaving state 1 to enter state 2 where $V_{UV} < V_{REF}$ and $V_{OV} < V_{REF}$. When in state 1, the drain of M_5 is at V_{DD}. Figure 7 shows how the signals in the differential pair and the output stage respond to the input signal V_{UV}. Upon entering state 2 V_{UV} drops below V_{REF}, causing M_1 to start conducting more current than M_2 ($I_1 > 1_2$), which raises the voltage V_{G5}. As V_{G5} exceeds the threshold voltage of the NMOS device M_5 begins to turn on. As V_{G5} continues to rise V_{OUT1} begins to fall, and M_5 tries to pull this node to GND. When M_5 is turned on, an effective RC circuit is formed and the FET discharges the parasitic capacitances. The small resistance of the FET discharges this capacitance very quickly, causing the undervoltage trip to be much faster than the overvoltage; see Figure 12 and Figure 13.

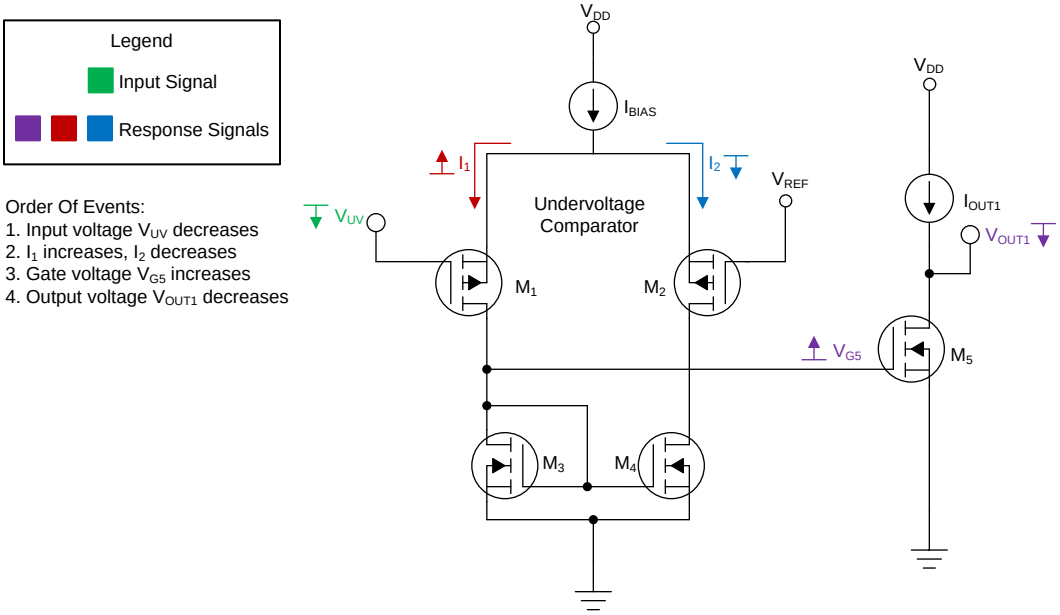

Figure 7. Undervoltage Comparator Signal Trace

5.3 State 3: Overvoltage Fault Condition, $\overline{RESET}$ Asserted

An overvoltage fault causes the comparators to leave state 1 and enter state 3, $V_{UV} > V_{REF}$ and $V_{OV} > V_{REF}$. When in state 1 the drain of M_{10} is at GND. Figure 8 shows how the signals in the differential pair and the output stage respond to the input signal V_{OV}. Upon entering state 3, V_{OV} rises above V_{REF} and M_7 starts conducting more current than M_6 ($I_4 > 1_3$), which causes V_{G10} to drop. As V_{G10} approaches the threshold voltage of the NMOS device M_{10} begins to turn off. As V_{G10} continues to fall V_{OUT2} begins to rise, and the active pullup tries to pull this node to V_{DD}. The small current source I_{OUT2} can take several microseconds to charge this node to V_{DD} because of the shoot-through current and parasitic capacitance. Because this node changes so slowly, a Schmitt trigger is required at the output to ensure there is no shoot-through current. The current source I_{OUT2} is not the only contributing factor causing the increase in propagation delay. Figure 5 also illustrates that the overvoltage comparator has a second inverter in the data path, this inverter also increases propagation delay. This extra inverter is necessary to ensure the correct logic at the output.

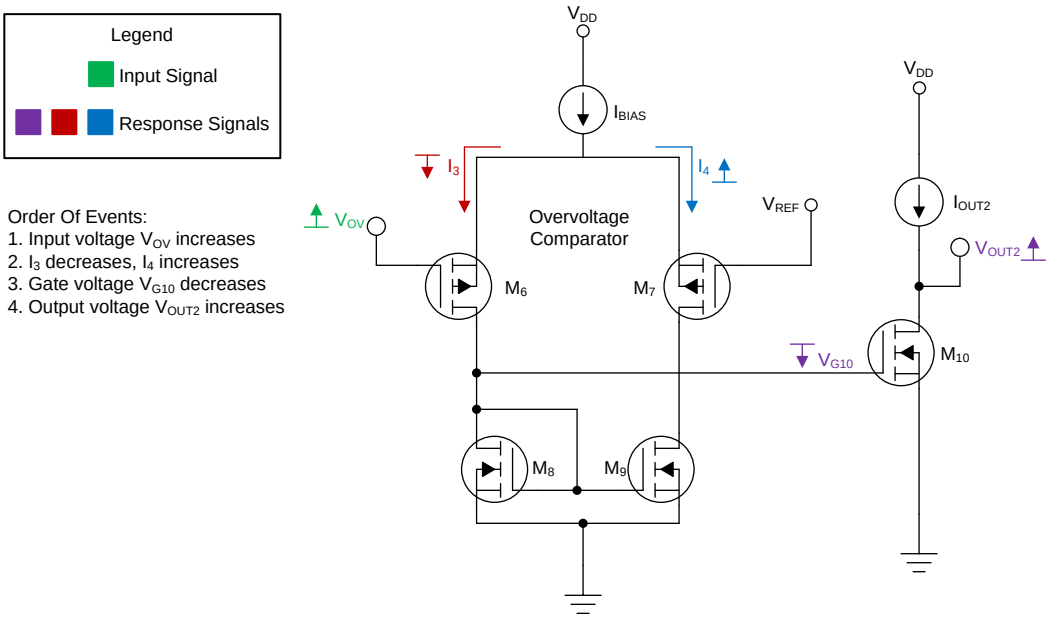

Figure 8. Overvoltage Comparator Signal Tracing

6 Analysis of Propagation Delay Differences

6.1 Measuring Propagation Delay versus Overdrive Curve

The propagation delay versus overdrive changes based on the measurement technique. There are two accepted methods for measuring the curve: the first is starting at a fixed voltage and stepping below the threshold by the required percentage. The other method is to start above the threshold by the percentage and then step below the threshold by the percentage; see Figure 9. The TPS3850 data sheet uses the second method to calculate the overdrive voltage curve. Using the second method results in a longer propagation delay than if starting at a fixed voltage and stepping above or below the threshold. The reason for this is further discussed in Figure 10. Figure 10 illustrates how the currents in the differential pair change with the overdrive voltage. When the voltage is at the trip point the currents through the two transistors are equal. However, for each measurement the voltage starts above the threshold by the overdrive voltage and then is stepped below the threshold. Starting over the threshold causes the currents to start skewed in the opposite direction of the transient. Figure 11 demonstrates that when a voltage supervisor is operated at the nominal monitored threshold one transistor in the differential pair conducts more current than the other. Then when the voltage is stepped below the threshold the amount of current through each transistor changes as M_1 begins to conduct more current than M_2 in an undervoltage supervisor.

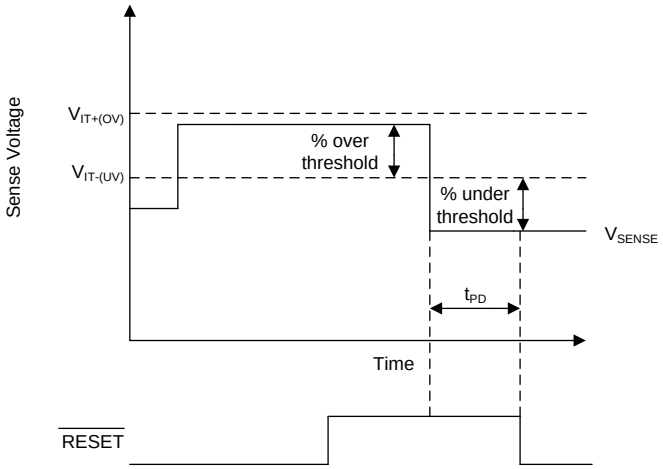

Figure 9. Measuring the Overdrive Voltage Curve

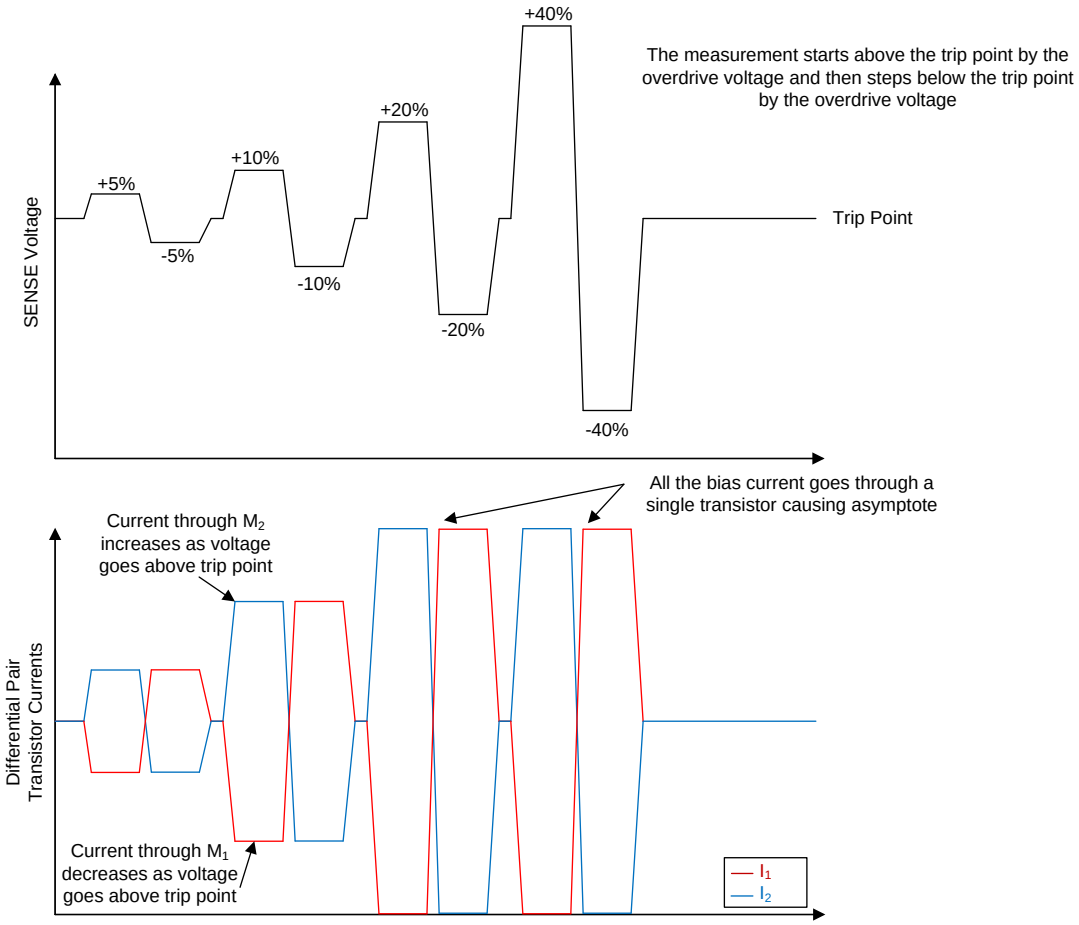

Figure 10. Current in Differential Pair for How Overdrive Voltage is Measured

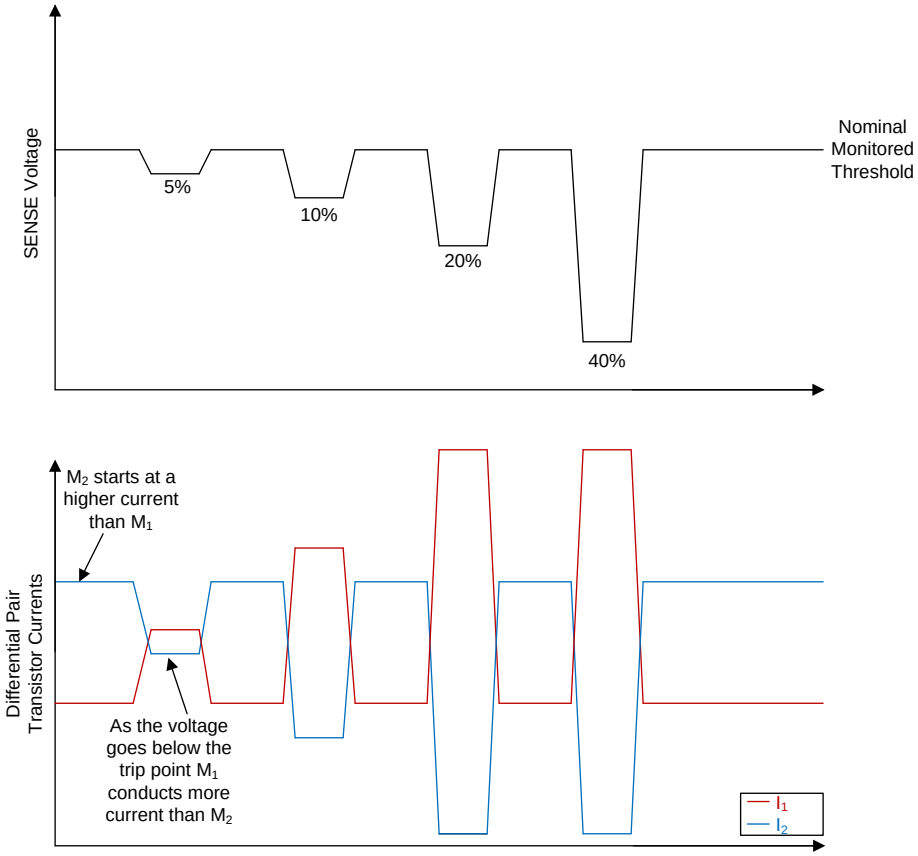

Figure 11. Differential Pair Current During Normal Use

6.2 Analyzing the Overdrive Curve

As discussed in Figure 5 the overvoltage and undervoltage comparator have different propagation delay versus overdrive curves. There are three main factors that effect the propagation delay timing: the architecture of the comparator, the monitored threshold voltage of the comparator, and the measurement technique. The overvoltage comparator takes longer to respond than the undervoltage comparator, as shown in Figure 12 and Figure 13. Figure 12 shows that the propagation delay for the undervoltage comparator is approximately 40 µs faster than the overvoltage comparator. There is also a difference in the different voltage options. When comparing a 5-V supervisor and a 1.8-V supervisor there is an obvious difference in the propagation delay curves. The 5-V part has less propagation delay for the same percentage overdrive, which is largely a result of overdrive being measured in percentages. A 4% step over the threshold is approximately three times greater in magnitude for a 5-V threshold than the 1.8-V threshold.

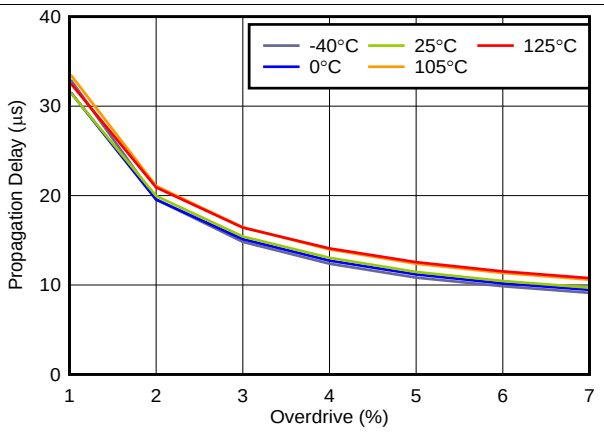

Figure 12. TPS3850 Undervoltage Propagation Delay vs Overdrive

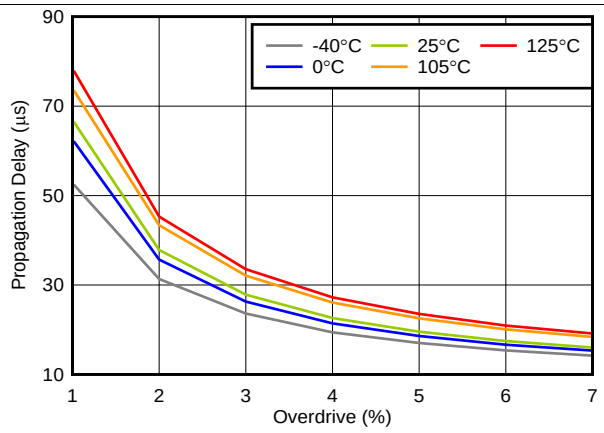

Figure 13. TPS3850 Overvoltage Propagation Delay vs Overdrive

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