Application Note

A Comparison of Fused Lead Frame and Non-Fused Lead Frame Variants of Hall Effect Current Sensors

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ABSTRACT

Texas Instruments uses a unique SOIC-10 package for the TMCS11xx family of devices where a traditional SOIC-16 style package sees eight individual leads fused into two leads. This fused lead frame is used to carry current into the package rather than two sets of four individual leads. However, there is often a need for multi-sourcing in an application, and while the parts are *pin to pin* compatible, some differences do arise in the make-up. This application note examines the Texas Instruments SOIC-10 package when used on an SOIC-16 land pattern to demonstrate that the SOIC-10 package can be used on the standard SOIC-16 footprints on a printed circuit board without cause for concern.

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Trademarks

1 Introduction

As electrification continues to sweep across various industries, manufacturing is more strained to keep up with the rapid demands needed for various products. Many manufacturers have adopted an approach of dual sourcing, where an integrated circuit is not allowed to be used by a designer unless variants are made by multiple vendors, allowing multiple supply chains to be tapped. This creates a more robust sourcing plan for the sustainment of a product, allowing the manufacturer to have backup plans in the presence of long lead times.

Finding multiple variants of a single product is not always simple. Electrical specification can vary from product to product in magnitude such that one can not function at the level the designer requires, even though the device exists in the same package and pinout, and provides the same transfer function. Thermal properties can vary. One variant can be vastly more expensive to the point that while the variant serves as a viable alternative, the variant violates the bill of materials budget to do so. All of these are challenges that the sourcing engineer must make sure are met before the sourcing engineer can declare that two products work as *functional replacements* of the other.

In the area of Hall effect sensors, one additional area of potential concern is lead frame construction. While some variants use a standard SOIC-16 package, Texas Instruments' TMCS product family uses a fused leadframe approach in SOIC-10, as a singular lead style of frame allows for resistance in the lead frame, optimizing power loss on the input side of the frame. The purpose of this application note is to examine performance and reliability concerns when using these two styles of packages as functional equivalents of one another in a design.

2 Exposure of the SOIC-10 to Board Level Reliability Testing

The main challenge presented in the use of these two packages interchangeably is the layout of the respective land patterns. Figure 2-1 shows the typical land pattern of an SOIC-10 on the left, and the SOIC-16 on the right.

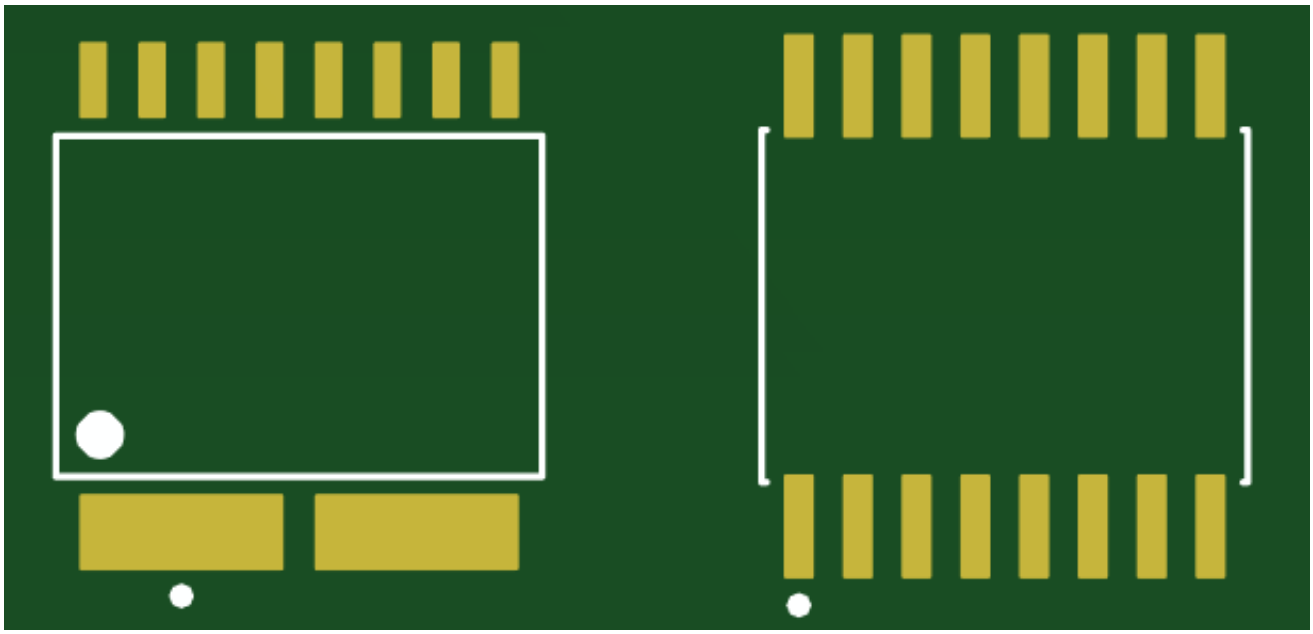

Figure 2-1. Land Patterns: SOIC-10 (Left), and SOIC-16 (Right)

As the land patterns show, while relatively similar in dimension and layout, the main solder points on the input side move from four individual solder pads, per input, to one elongated pad that the fused lead frame is then soldered to. However, in a use case where the goal is to use one device interchangeably with the other, it is simple to question whether the placement of the soldered fused leadframe on the individual pads can reduce performance. The placement of the individual leads on the elongated pad seems trivial. The four leads all share the same node of the input, and placed on the elongated solder pad results in no change to performance. However, the placement of the fused lead frame on the individual pads can cause bottlenecks in current flow resulting in additional heat.

To examine the effects of these concerns, a board level reliability experiment was conducted. For this experiment, our evaluation PCBs were populated with an SOIC-10 package onto a standard SOIC-16 footprint, shown in Figure 2-2.

Figure 2-2. SOIC-10 Package on SOIC-16 Footprint

Eight of these PCBs were connected in series with 20A of current flowing through the leadframes continuously, and placed into an oven. During this the boards were subjected to temperature cycling from -40°C to +125°C and +125°C to -40°C for 500 cycles (see Figure 2-3).

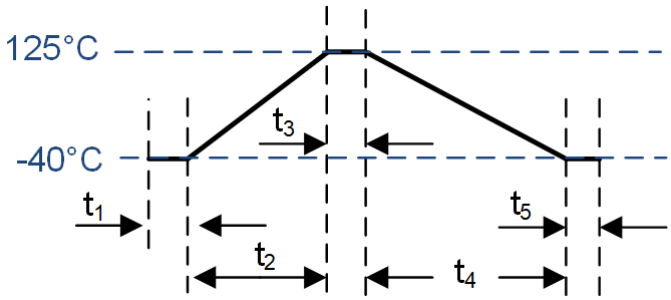

Figure 2-3. Temperature Cycling Timing Diagram

Where:

- $t_1 = t_3 = t_5 = 7$ minutes
- $t_2 = 45$ minutes
- $t_4 = 70$ minutes

The speed of the ramp up and ramp down of the temperature is limited by the oven used, a Test Equity Model 115A. The boards were left to soak at -40°C and 125°C for seven minutes before moving onto the next cycle.

Both pre- and post- testing of these 500 cycles taking place, sample cards were examined from a thermal equilibrium perspective, as well as examination of the solder joints through x-ray to examine the effects these cycles can exhibit on the devices. Further, the cards were cross sectioned to look for evidence of delamination. There were no device failures during the temperature cycling.

These devices were subject to another 500 temperature cycles to increase the total temperature cycle count to 1000 cycles. The same procedure was used as was done with the first 500 cycles and the boards were examined with no device failures occuring during the temperature cycling.

2.1 Examination of Solder Joints Through X-ray

When working with larger joints such as those on the inputs of the SOIC-10 package, the correct choice of solder is important for best performance. Texas Instruments recommends the use of a no-clean style paste, such as AIM M8 SAC Type 4 for best results. Water soluble variants can typically lead to increased voiding, which over time can reduce thermal performance due to these voids present in the joint. Figure 2-4 and Figure 2-5 show an example of no clean chemistry performance, while Figure 2-6 and Figure 2-7 demonstrate an example of water soluble chemistry performance on larger solder joints.

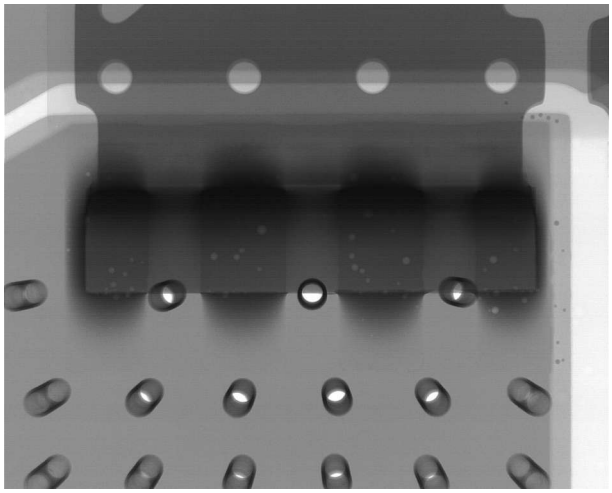

Figure 2-4. No Clean Solder Paste X-ray, Left Input Lead

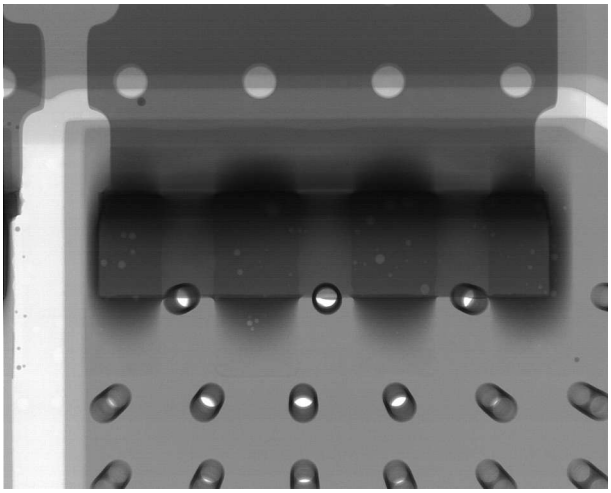

Figure 2-5. No Clean Solder Paste X-ray, Right Input Lead

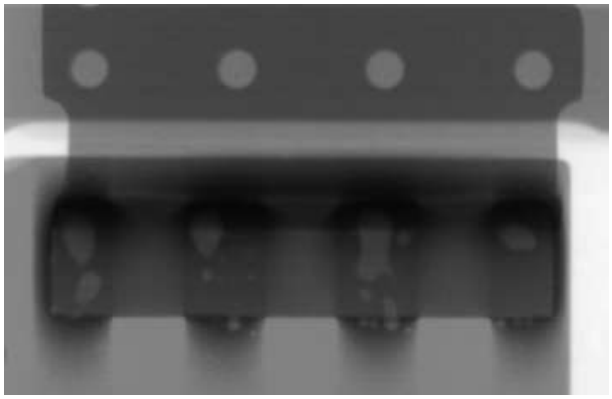

Figure 2-6. Time Zero X-rays, Left Input Lead

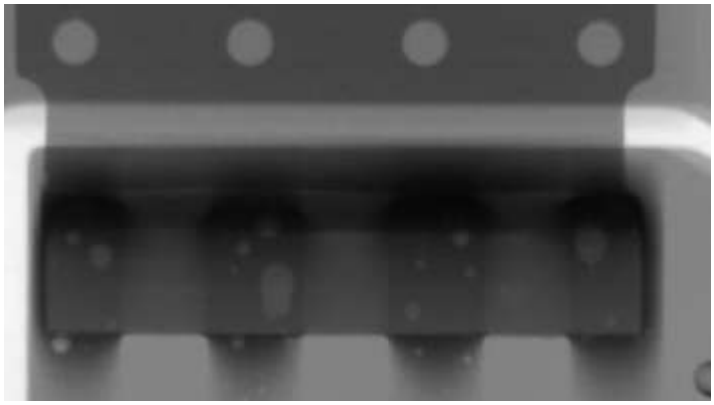

Figure 2-7. Time Zero X-rays, Right Input Lead

The solder paste chosen for this experiment is a water soluble SAC305 type 4 solder paste, and this choice was purposefully made to subject the devices under test to the worst case solder voiding scenario of an SOIC-10 package on an SOIC-16 footprint.

The solder integrity of the devices was again checked after the 500 temperature cycles outlined in Figure 2-3. Note that the device shown in Figure 2-8 and Figure 2-9 are a random sample from the tested cards, and is not a continuation of the solder voiding shown in Figure 2-6 and Figure 2-7.

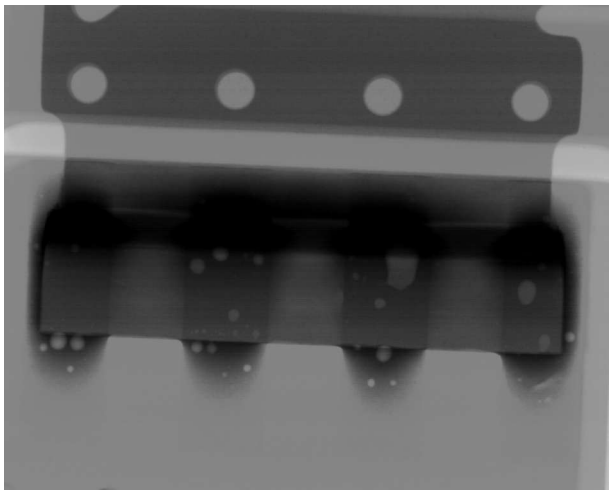

Figure 2-8. 500 Temperature Cycles X-rays, Left Lead

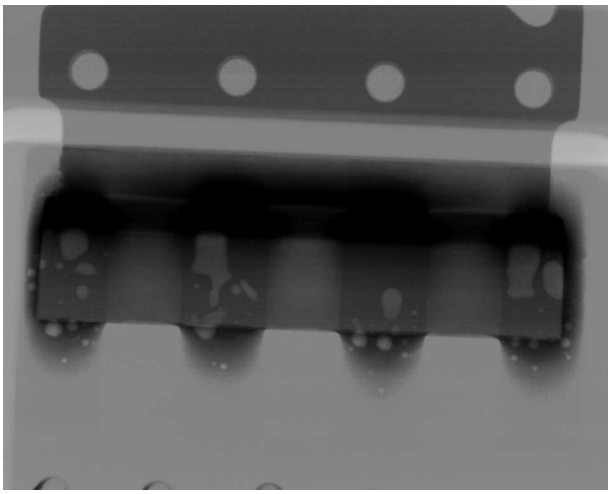

Figure 2-9. 500 Temperature Cycles X-rays, Right Lead

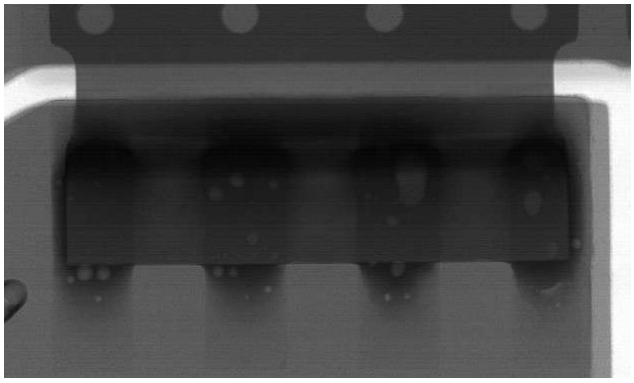

Figure 2-10. 1000 Temperature Cycles X-rays, Left Lead

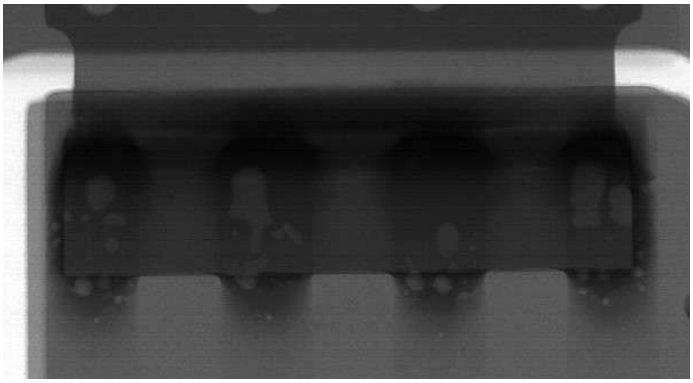

Figure 2-11. 1000 Temperature Cycles X-rays, Right Lead

The x-rays demonstrate that while there is solder voiding present on the fused leads, the quantity does not deviate from the time zero sample in any significant way. The solder voiding is comparable to the voiding that was seen before cycling, and resulted in no failures even after 1000 temperature cycles under constant DC load. This shows that temperature cycling does not cause solder voiding to get worse, regardless of presence at initial manufacturing. In general, however, a no-clean style of solder is still recommended for use in application, as this helps mitigate any additional failures due to this issue in production.

2.2 Thermal Testing

A DC thermal analysis of the devices was performed both initially, as well as after 500 and then 1000 temperature cycles to observe the thermal performance of the lead frame pre- and post-temperature cycling stress. In addition, the same test was administered to a TMCS device on the standard land pattern as a baseline, as well as a thermal test of the land pattern cross when using no-clean paste. Each of these boards were subjected to 40A of DC current flowing through the lead frame for ten minutes, and then images were captured. This was long enough in all cases for devices to reach thermal equilibrium.

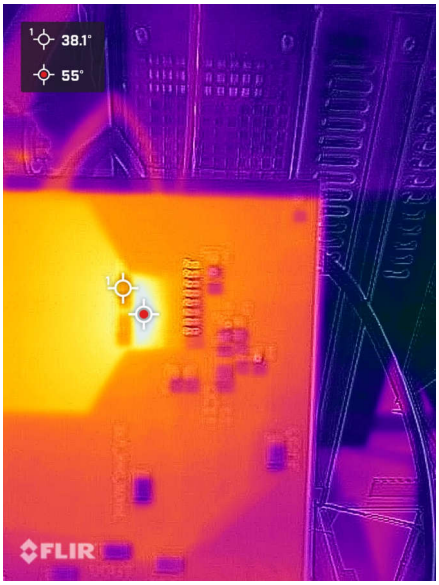

Figure 2-12. SOIC-10 on SOIC-10 Footprint, Time Zero, SAC Water Soluble Paste

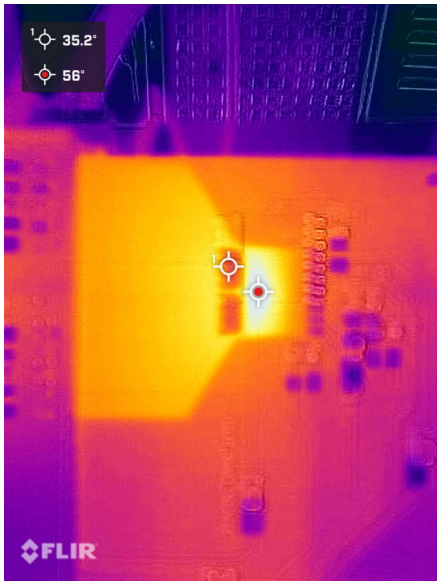

Figure 2-13. SOIC-10 on SOIC-16 Footprint, Time Zero, SAC Water Soluble Paste

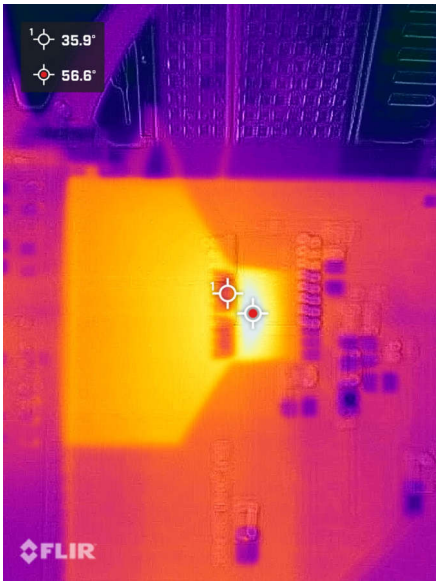

Figure 2-14. SOIC-10 on SOIC-16 Footprint, Post-500 Cycles, SAC Water Soluble Paste

Figure 2-15. SOIC-10 on SOIC-16 Footprint, Post-1000 Cycles, SAC Water Soluble Paste

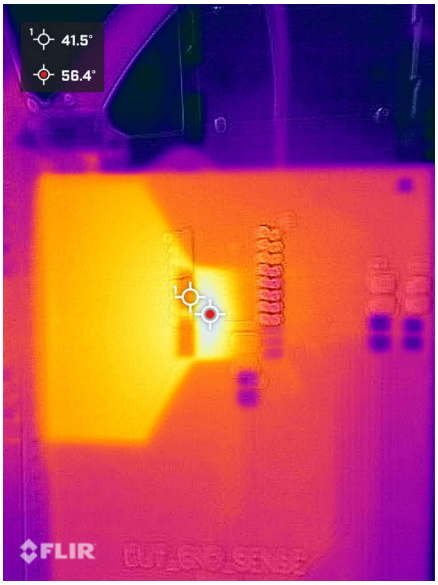

Figure 2-16. SOIC-10 on SOIC-16 Footprint, Time Zero, SAC No Clean Solder

The thermal images demonstrate that the temperature of the lead frame is comparable in all tests of the boards. From the initial test to the image post-500 temperature cycles, there is a less than a 1°C change (56°C vs. 56.6°C) in the final temperature. In comparison, the baseline board of the TMCS on the footprint exhibits a final temperature of 55°C. The SOIC-10 on SOIC-16 footprint board using no clean solder paste also settled around the same temperature as the others at 56.4°C. In summary, no drastic thermal changes were observed outside of the expectations of random process variation.

2.3 Cross Sections

As a final check, at 300, 500, and 1000 temperature cycles, sample boards were removed from the oven for cross sectional analysis. While more commonplace on multiple layer boards, delamination can occur on 2-layer boards, as well as compounding solder issues as the device leads and board expand and contract over the temperature cycles. Figure 2-17 shows worst case cross sections for a device at 300 cycles, and Figure 2-18 shows the same for 500 cycles.

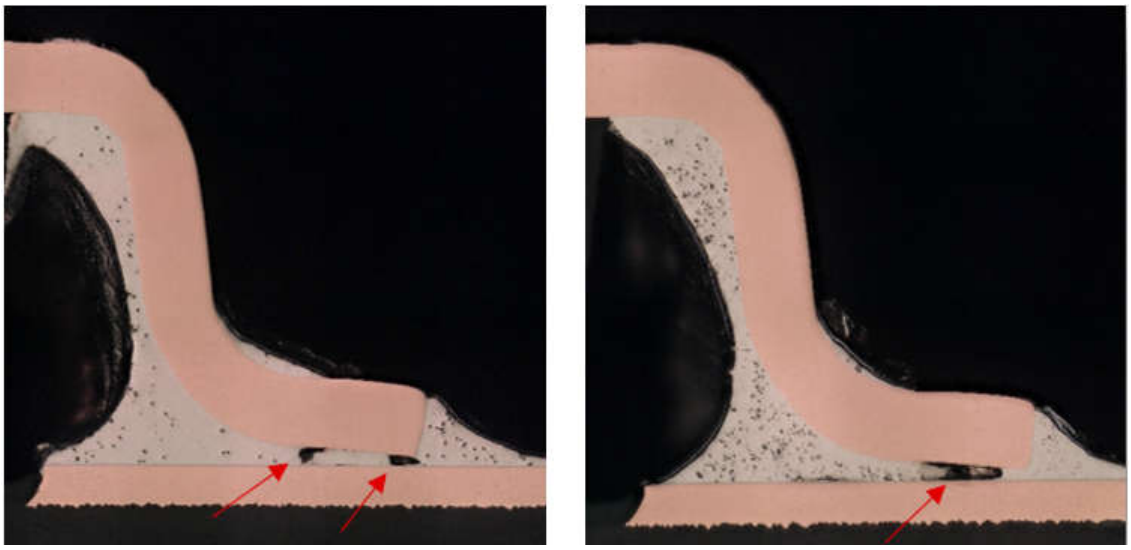

Figure 2-17. Cross Section - 300 Temperature Cycles

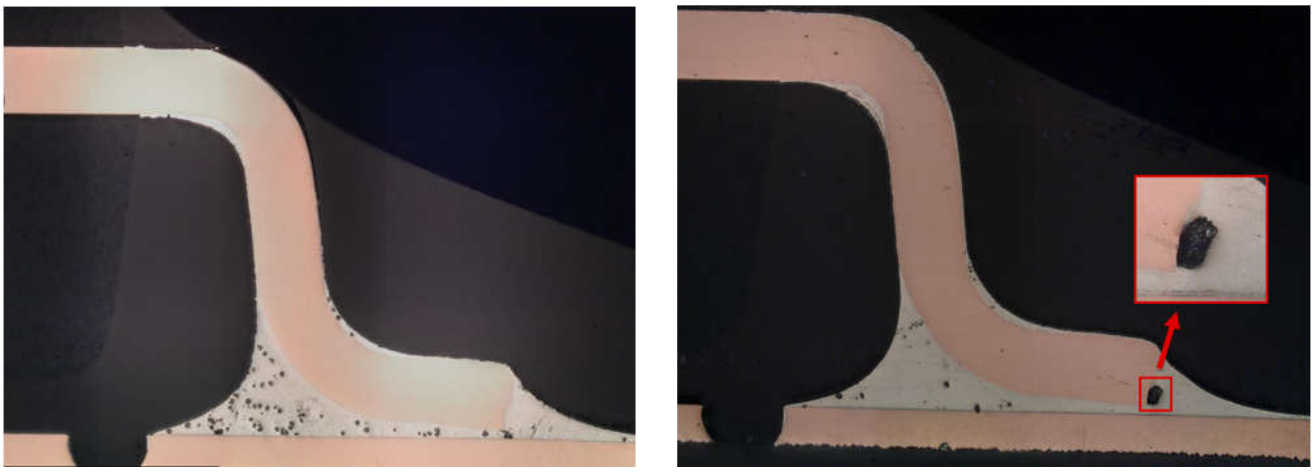

Figure 2-18. Cross Section - 500 Temperature Cycles

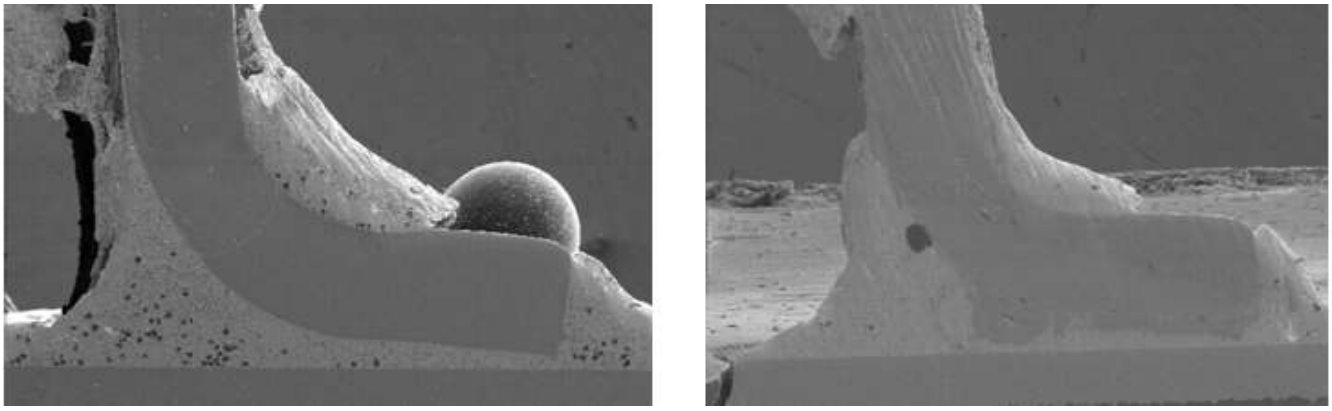

Figure 2-19. Cross Section - 1000 Temperature Cycles

As expected from the observations made during x-ray, there is evidence of solder voiding (highlighted by red arrows in the images), but even in the presence of these artifacts, none of the boards failed by abnormal heat signatures or open circuit. The cross sections show no evidence of delamination, solder adherence to the frame and PCB is still nominal, and there is no evidence of damage.

3 Summary

Correct selection of solder paste is required when using larger pads for the mitigation of solder voiding in larger solder joints. In general, a no-clean solder paste is a preferred option to optimize these joints for best performance.

In general, there are little to no risks in the use of an SOIC-10 package on an SOIC-16 footprint. Across all examinations, there is little to no observed change in device thermal performance, PCB substrate integrity, or device leadframe integrity after 1000 hours of continuous temperature stress.

4 References

- Texas Instruments, *TMCS1126 Precision 500kHz Hall-Effect Current Sensor With Reinforced Isolation Working Voltage, Overcurrent Detection and Ambient Field Rejection*, datasheet.
- Texas Instruments, *Thermal Analysis of the TMCS1123 Hall-Effect Current Sensor*, application note.

5 Revision History

Changes from Revision * (September 2025) to Revision A (March 2026)	Page
• Added text in Exposure of the SOIC-10 to Board Level Reliability Testing	2
• Added Figure 2-10 and Figure 2-11	4
• Added Figure 2-16	6
• Added Figure 2-19	8

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