Application Note

Custom Board Design and Simulation Guidelines for Processor High Speed Parallel Interfaces

Abstract

The application note includes guidelines applicable to custom board design and simulations for high speed parallel interfaces.

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Trademarks

1 Introduction

The document includes design guidelines that are applicable to custom board design simulation for high speed parallel interfaces. The interfaces support different buffer types (for example: LVCMOS, SDIO, eMMCPHY, or other buffer types, and determines the electrical characteristics) associated with the terminals (pins). Refer to the pin attributes section of the processor-specific data sheet for supported buffer types and the timing and switching characteristics section for the supported speed.

The guidelines can be used for commonly simulated peripherals including eMMC (up to HS200), MMC SD card, MMC SDIO, OSPI, QSPI, and RGMII (Ethernet interface). The simulation approach can be extended to DPI, GPMC, SPI, or other on-board peripheral interfaces. The high speed parallel interface specifications for many of the peripherals are based on JEDEC standards.

2 Board Design and Layout Guidance

2.1 General Board Design Guidance

To achieve optimal signaling (signal integrity) performance, follow the below listed general board design guidelines:

- All signals need ground reference (strongly suggest on both sides).
- Avoid crossing plane splits in the signal reference planes.
- Use widest possible trace width between the decoupling capacitors and the supply pins.
- Minimize inter-symbol interference (ISI) by matching the trace impedance (refer to SoC or attached device recommendations)
- Minimize crosstalk by isolating the sensitive signals, such as clock and strobe signals, and selection of PCB stackup.
- Avoid signal return path discontinuities by adding stitching vias whenever signals change layers and reference planes.
- Minimize supply rail noise by isolating signal traces and power traces and use of decoupling capacitors.
- Keep the signal connection stub lengths as short as possible.
- Follow spacing guidelines for clock and strobe signals to minimize crosstalk.
- Maintain a common ground (commonly called as GND) reference for all signals and capacitors (bypass, decoupling capacitors).
- There can be difference in propagation delay between microstrip trace routing and stripline trace routing. The recommendation for custom board designer is to factor the propagation delay differences while performing timing analysis or routing the traces.
- Via-Via coupling can be a significant contributor to PCB-level crosstalk. Dimension of Via and pitch of Vias is important. For high speed interfaces, consider using ground shielded Vias to minimize Via-Via coupling.
- Via stub can affect signal quality. Via back-drilling can be considered to improve signal quality based on the use case.

2.2 Board Design Guidelines to Follow for Improved Signal Integrity

There are a number of factors that contribute to signal integrity related issues. System level analysis and optimization is recommended for improving custom board level signal integrity.

A number of options can be considered to improve custom board signal integrity (signal quality). Some of the suggested options are listed below.

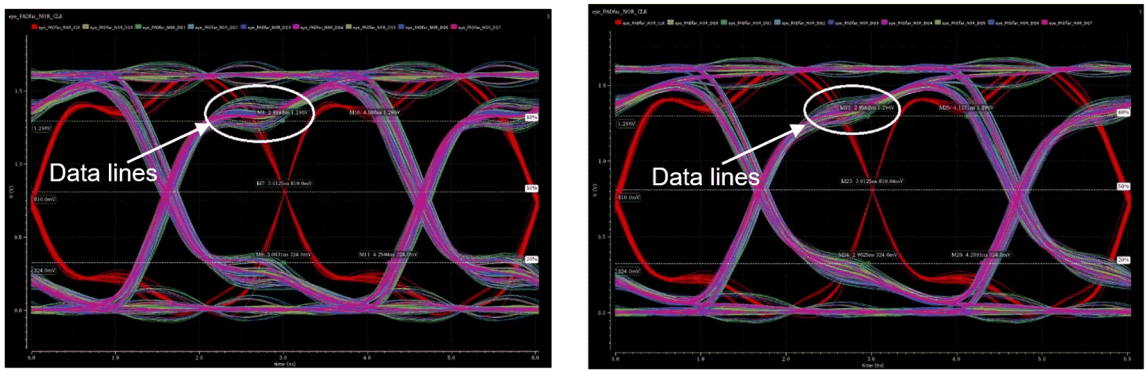
Table 2-1. Signal Quality Improvement Approach Options

Options	Recommendation	How does the recommendation help?
A	Add a series resistor	Can reduce signal reflections and improve signal quality
B	Add a capacitor (near to the load)	Can reduce the return signal reflections. Balancing capacitors added on both ends can reduce the overall reflections.
C	Increase signal trace length	Can reduce out of phase reflections from impacting the incident signal while the signal is continuing to transition.

Table 2-1. Signal Quality Improvement Approach Options (continued)

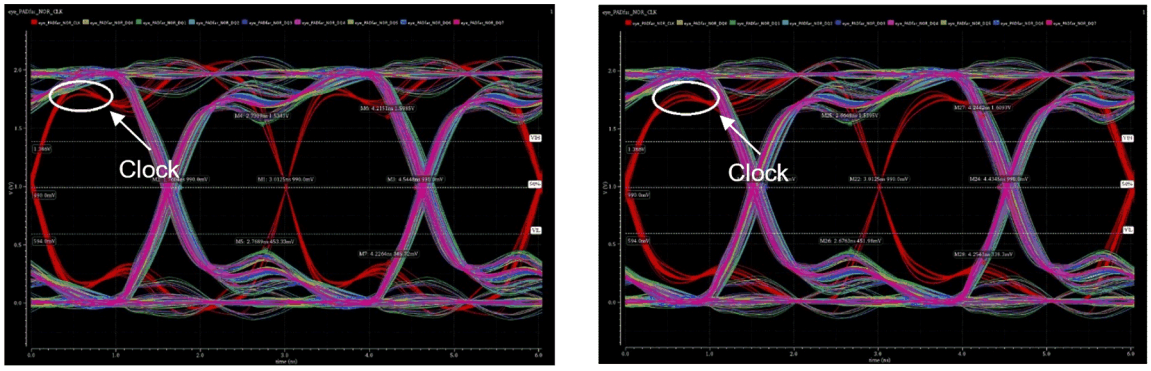
Options	Recommendation	How does the recommendation help?
D	Configure fast drive strength and use a combination of A, B, C	Improves signal rise/fall time and improves overall eye pattern (along with a combination of A, B, C to reduce signal reflections).

The following diagrams are a general guidance for signal integrity improvement:



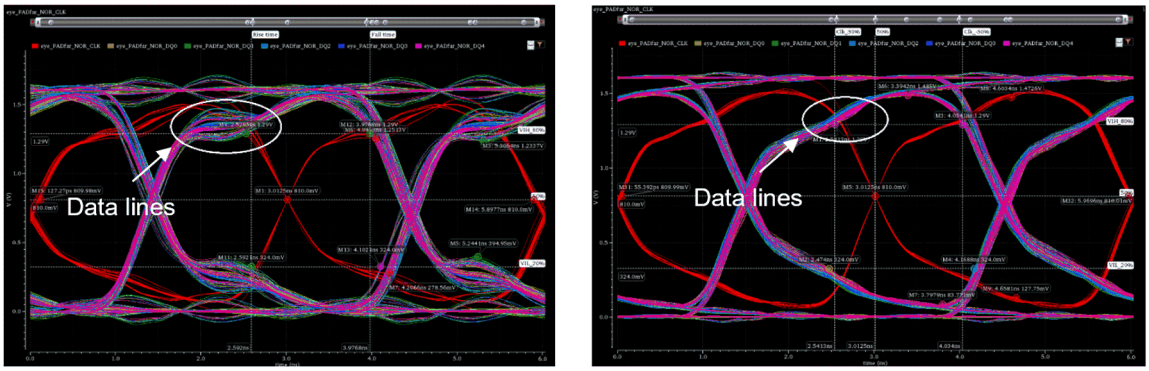
Before **After**

Figure 2-1. Series Resistor Added on the Data Lines



Before **After**

Figure 2-2. Load Capacitor Added on the Clock Line



Before **After**

Figure 2-3. Combination of Option A and Option B on the Data Lines

Notes on setup and measurement:

- Processor and Attached device (also called device) IBIS models used
- .SNP file (extracted from the custom board using extraction tool to perform SI simulation)
- Signal integrity analysis tool (2.5D)
- Eye plotting tool

Note

The eye diagrams shown in the examples have been measured at the BGA PAD of the attached device and plotted.

The analysis and examples shown are for write operations. The same guidelines can be used for simulating read operations.

2.3 Description of Custom Board Design Simulations Example

The section includes some guidelines for custom board designer to improve signal quality:

C_{LOAD} represents the total capacitive load of the attached device (measured at the input pin of the peripheral being simulated for write and SoC input pin for read).

Example: For a C_{LOAD} of ~3pF:

Option 1: Keep trace length short (~0.5 inch - 0.6 inch), adding (insert) a low value (10Ω or 22Ω) series resistor at the mid point of the signal trace.

Option 2: In case trace length is >1 inch and <5 inches, consider the below options:

A: Adding a resistor at the mid point of the trace as in option 1.

B: Adding a low value lumped capacitor (use different values 2pF, 3pF (choose available standard capacitance value nearest to the required capacitance)) close to the attached device BGA pad.

Option 3: In case Option 1 and 2 are not feasible, increase trace length to the maximum allowed length by the attached device specifications (Example: 6 inches) Adding a small lumped capacitor similar to option 2-B can be used in addition to increased trace length.

Note

The options listed above are some of the possible suggestions to improve the signal quality. Option 1 is expected to provide better overall signal quality. The custom board designer is expected to perform simulations and evaluate which of the described options works best for a specific system level use case.

3 Custom Board Design Simulations

3.1 Extraction of Board Model

The guidelines for extraction of board model listed below are intended to be used with any EDA extraction tool (are not tool-specific). Follow the steps outlined in Section 3.2 after completing extraction of s-parameter. The recommendation is to confirm the custom board design follows the below listed steps prior to running the simulations:

- For signal extractions, a 2.5D extraction tool can be used
- Follow the recommended layer thickness and PCB base material for custom board layer stackup.
- In case the required section of custom board layout is clipped prior to extraction (to reduce simulation time), the recommendation is to define the clip boundary that is >0.25 inch away from the signal and power traces.
- Use s-parameter or RLC package models (provided by the supplier) and continue with the simulation.

3.1.1 Simulations Using IBIS Model and Extracted Board Model

The guidelines for performing simulation for high speed parallel interfaces are outlined in the following section: channel (group) simulations (example: data lines) using IBIS models and extracted board model are performed with targeted data attack bit patterns, to generate signal waveforms and eye diagrams. The recommendation is to verify the simulation results for setup/hold time, slew rate, clock high and low, and other parameters defined in the attached device data sheet. Additional checks are recommended to be performed for ring back with respect to VIH/VIL voltage levels.

3.2 Simulation Setup

Setup the IBIS simulation with the following steps:

- Obtain and use the SoC IBIS model available on TI.com under SoC specific product page and request for the attached device IBIS model from the supplier (memory, EPHY). The IBIS models are expected to include package RLC model.
- Extract S-parameter file for signals on the custom board.
- Using a 3D extraction tool is preferred. Using 3D extraction tool may not be feasible due to run time limitations during simulation. If run time is a concern, the recommendation is to use a 2.5D extraction tool.
- Build the simulation netlist following the guidelines in the simulation tool used
- Set up the SoC IBIS model, board model, and attached device IBIS model (simulation deck)
- Configure the process, voltage, temperature corners that are required to be simulated.

  The recommendation is to perform simulation across all process, voltage, temperature supported by the SoC IBIS model:

  – Typical
  – Minimal
  – Maximal
- Analyze the simulations results using waveform analysis tool and use the pass/fail criteria (specifications) from attached device data sheet.

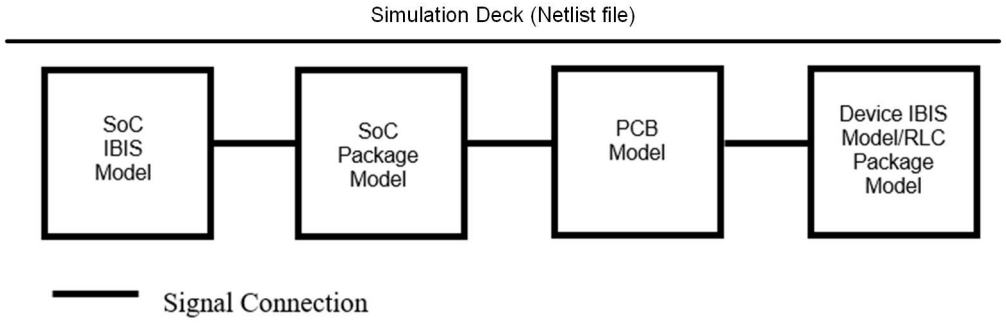


Figure 3-1. System-Level Simulation Setup Sequence

4 Custom Board Design Examples with Circuit and Examples

Board modifications include changes where additional capacitors known as delta capacitors are added on data and clock signals with respect to ground. The difference between the sum of C_Comp value and pin capacitance value of SoC and attached device included in IBIS model of SoC and attached device is the delta capacitor value (calculation is shown in the table below). Addition of delta capacitors on the signal lines and clock line can reduce signal reflections and minimize ring back violations.

Example calculation for Delta Capacitance value using C_Comp (Typical (Typ) value):

SoC IBIS Model			Attach Device (Device) IBIS Model			
C_pin (pF)	C_Comp (Typ) pF	C Total pF	C_pin (pF)	C_Comp (Typ) pF	C Total pF	C Delta pF
1.582	4.812	6.394	1.076	1.72	2.796	3.598

4.1 Simulation Terminologies

C_COMP - Buffer die pin capacitance, unique for each buffer type

Ring Back - Waveform ringing, overshoot/undershoot

4.2 OSPI Interface Simulation Examples for Different Use Cases

Example 1: The figure below shows the analysis for the baseline system. The baseline system does not meet the setup and hold time (timing) requirements as per the attached memory device data sheet and also has ring back on data lines and clock line.

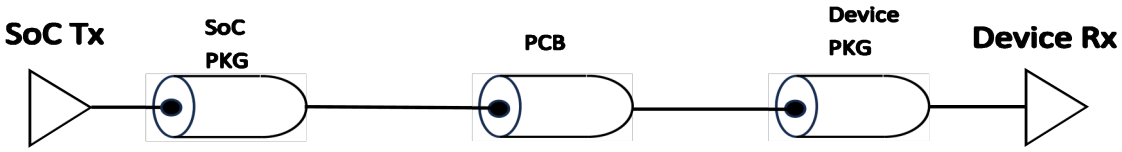


Figure 4-1. Circuit for Baseline System

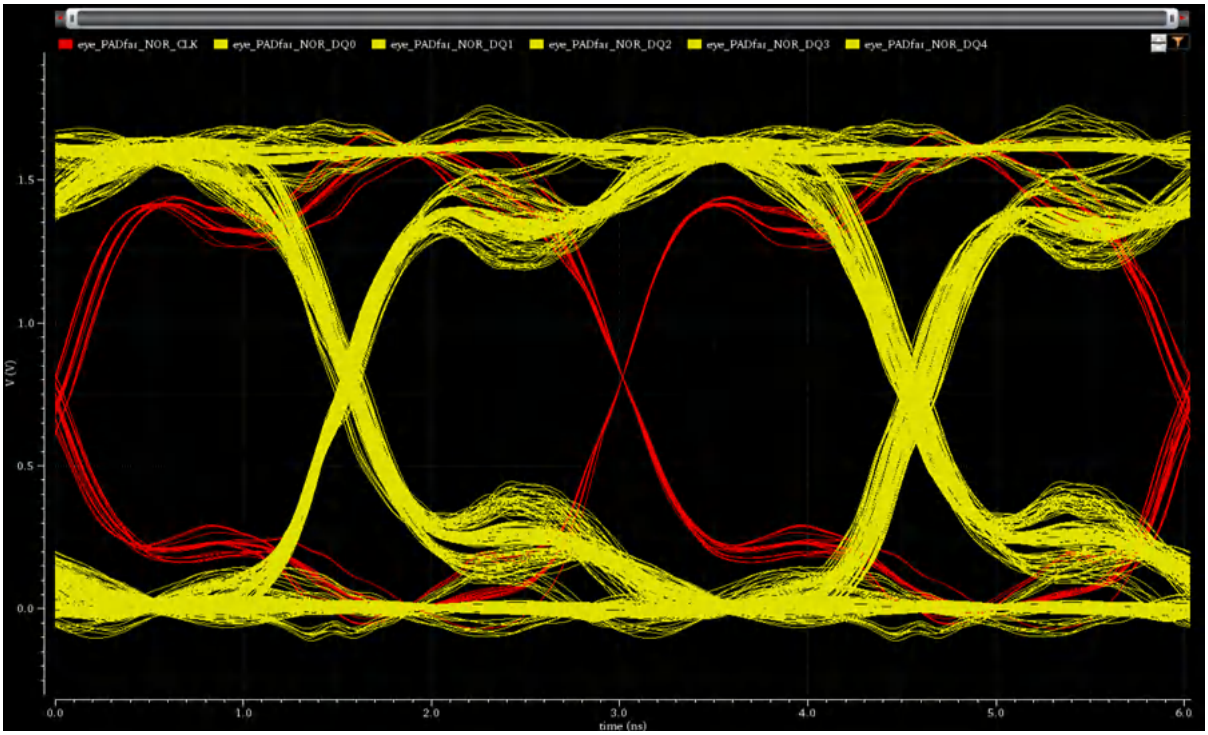


Figure 4-2. Waveform for Baseline System Analysis

Example 2: The figure below shows the analysis with a series resistor 10Ω added on the data interface signals between SoC and attached memory device placed near to SoC. The ring back on on data lines reduced improving the signal quality.

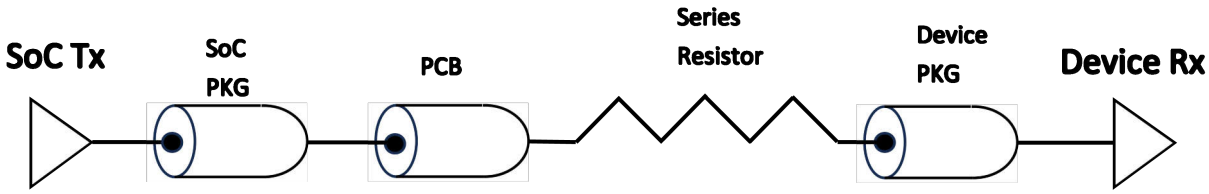


Figure 4-3. Circuit with Series Resistor Added on Data Lines for Baseline System

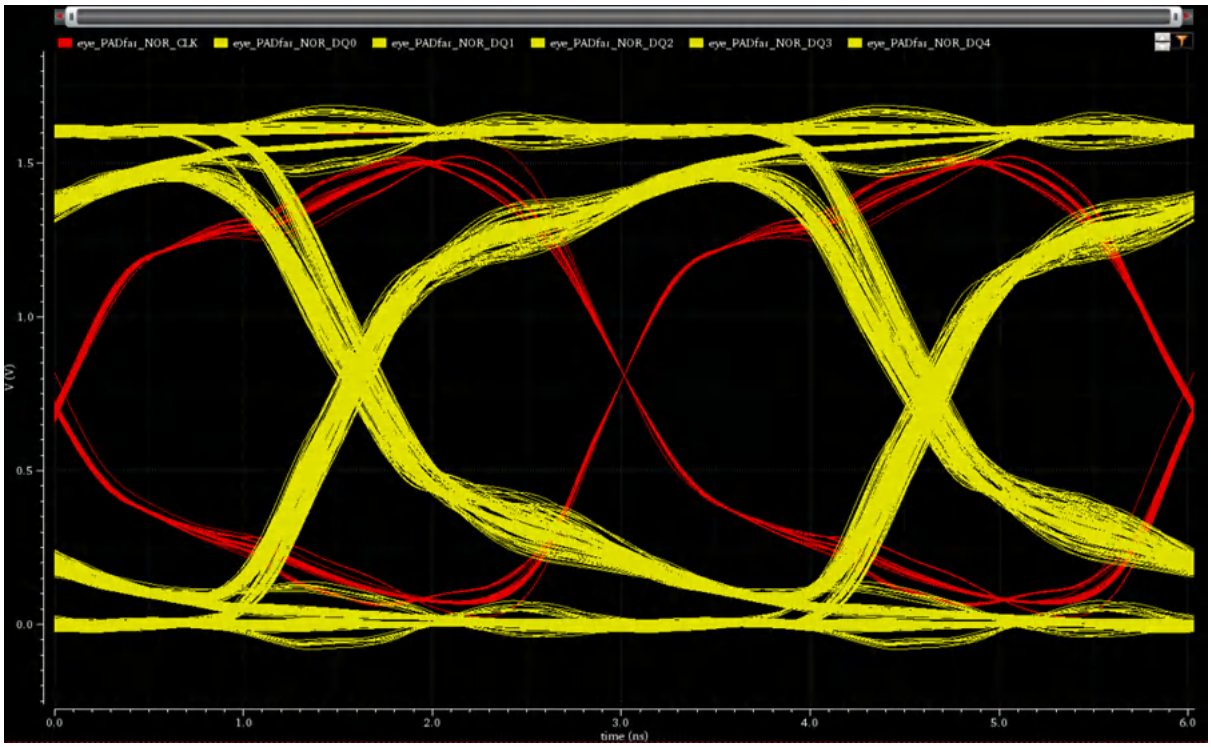


Figure 4-4. Waveform for Series Resistor Added on Data Lines for Baseline System

Example 3: The figure below shows the analysis with a series resistor 10Ω added on clock signal between SoC and attached memory device near to SoC. The ring back on clock signal is reduced improving the signal quality.

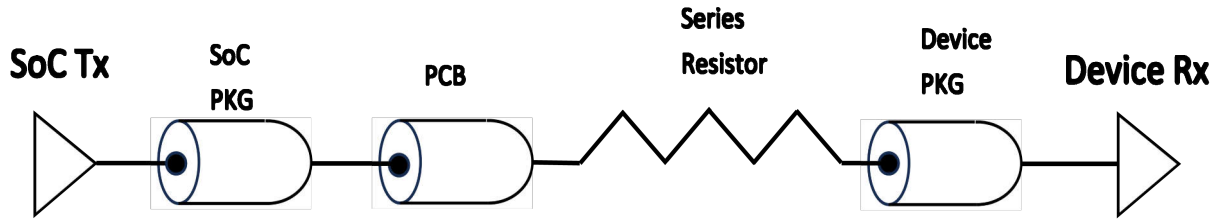


Figure 4-5. Circuit with Series Resistor Added on Clock Line for Baseline System

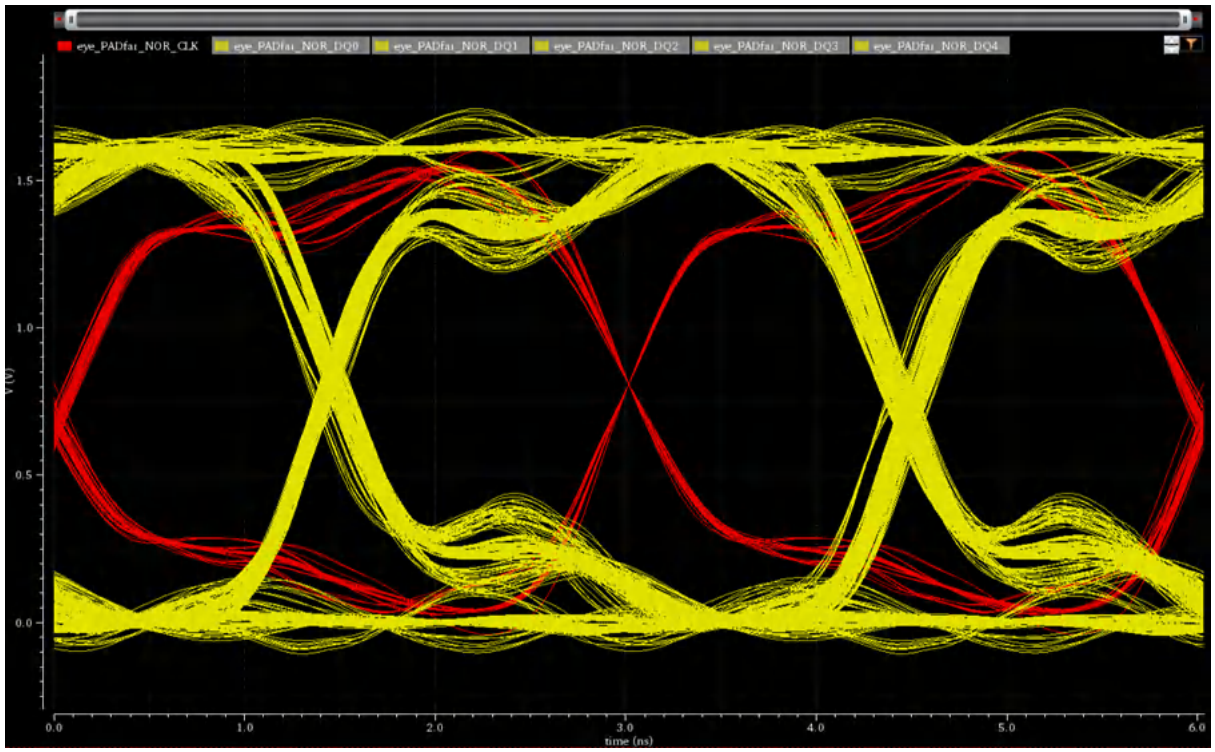


Figure 4-6. Waveform for Series Resistor Added on the Clock Signal for Baseline System

Example 4: The figure below shows the analysis with the trace length reduced to 0.5” to 0.7" for all data lines and clock line. The modified circuit meets the setup and hold time requirements as per attached memory device data sheet. The configuration has reduced signal reflections on data lines and clock line.

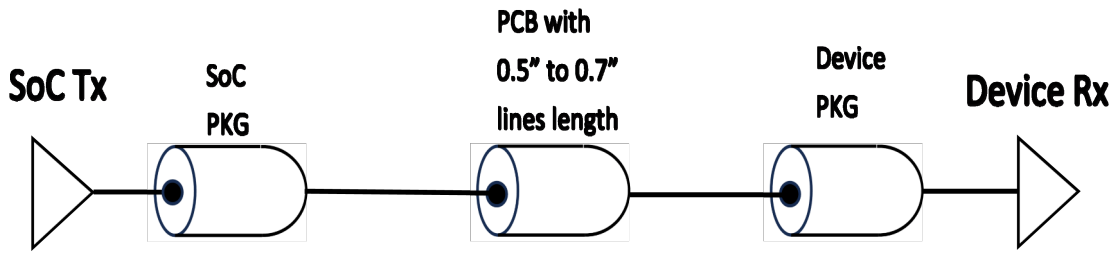


Figure 4-7. Circuit with 0.5” to 0.7” Trace Length

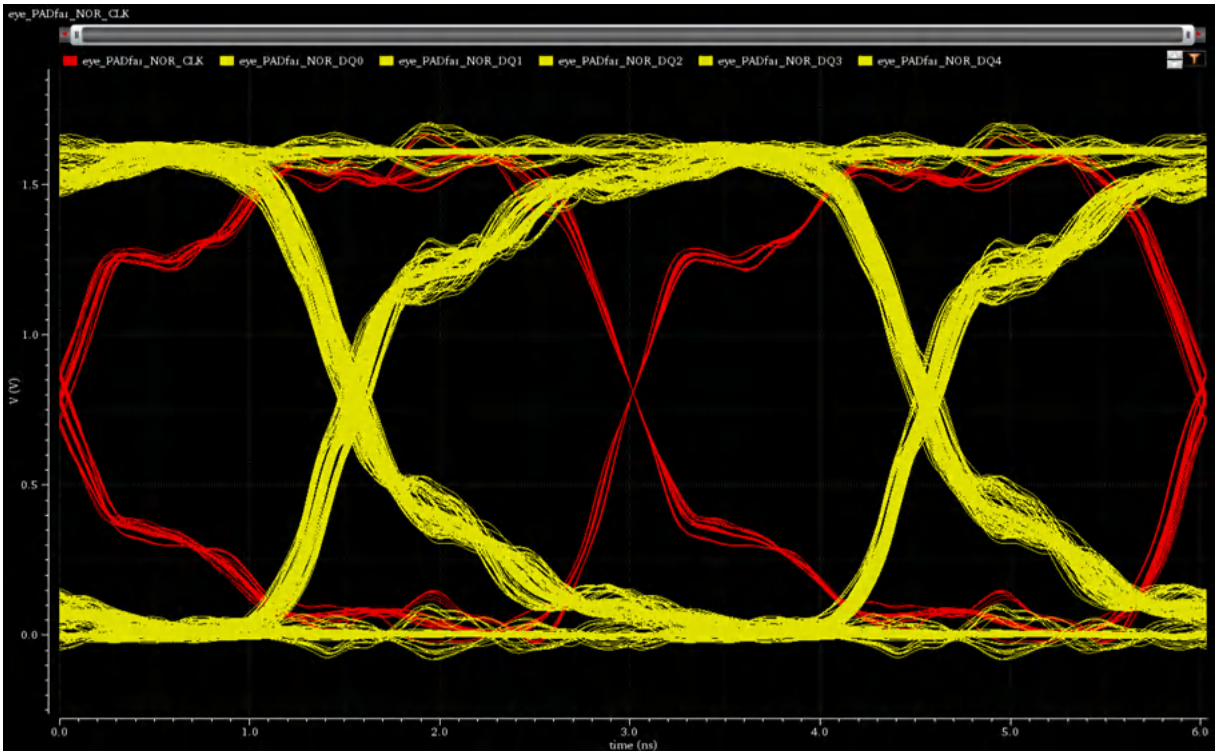


Figure 4-8. Waveform for 0.5” to 0.7" Trace Length

Example 5: The following figures show the analysis with a trace length of 0.5” to 0.7" and delta capacitors c_comp added between the SoC and the attached memory device (OSPI memory) on data lines. The delta capacitors are recommended to be added as close as possible to attached device BGA pads.

The configuration does not meet the setup time and hold time requirements (as per specification).

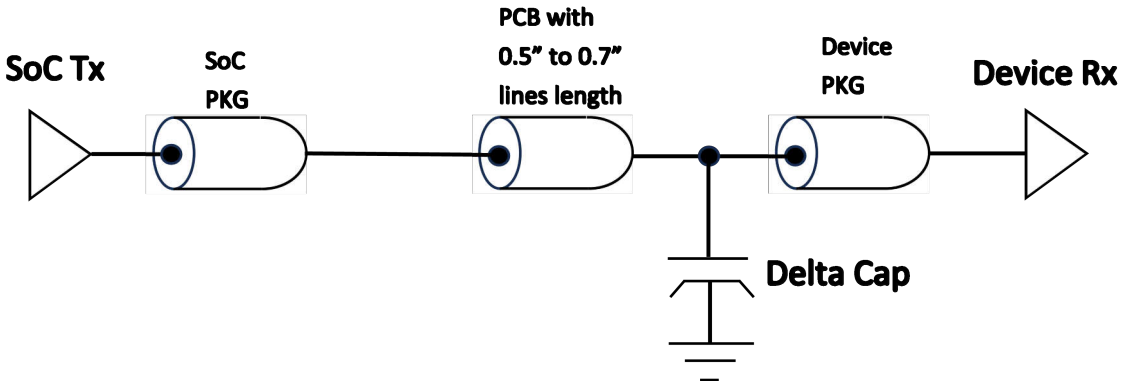


Figure 4-9. Circuit with 0.5” to 0.7" Trace Length and Delta C_Comp Capacitor Added on the PCB at the BGA pad (for data lines and clock line of attached memory) for Baseline System

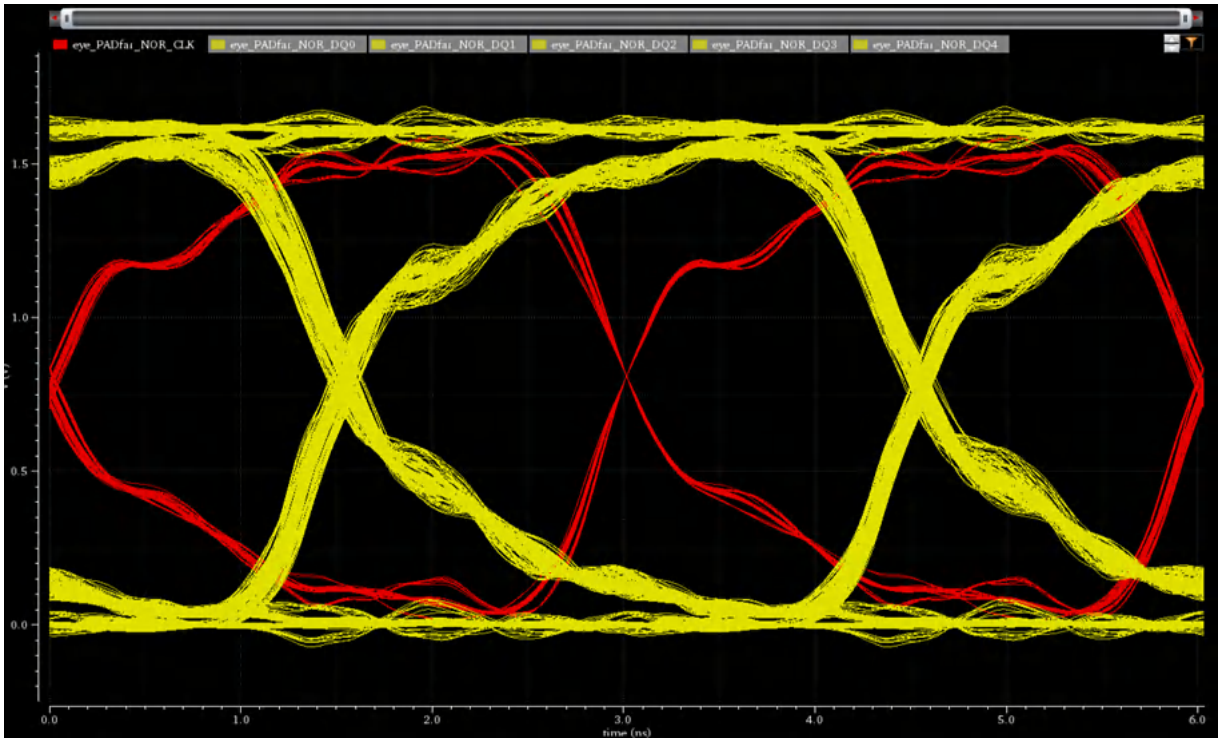


Figure 4-10. Waveform for 0.5” to 0.7" Trace Length with Delta C_Comp Capacitors Added on the PCB at the BGA pad (for the data lines and clock line of the attached memory device)

4.3 RGMII Interface Simulation Examples for Transmit Data Signals with Different Use Cases

Example 1: The figure below shows the baseline analysis. The baseline analysis meets the setup and hold time requirements as per the RGMII specifications. The waveform has reflections on Data Lines and Clock Line.

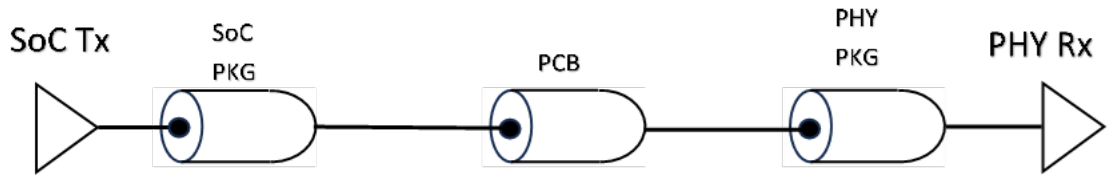


Figure 4-11. Circuit for Baseline System

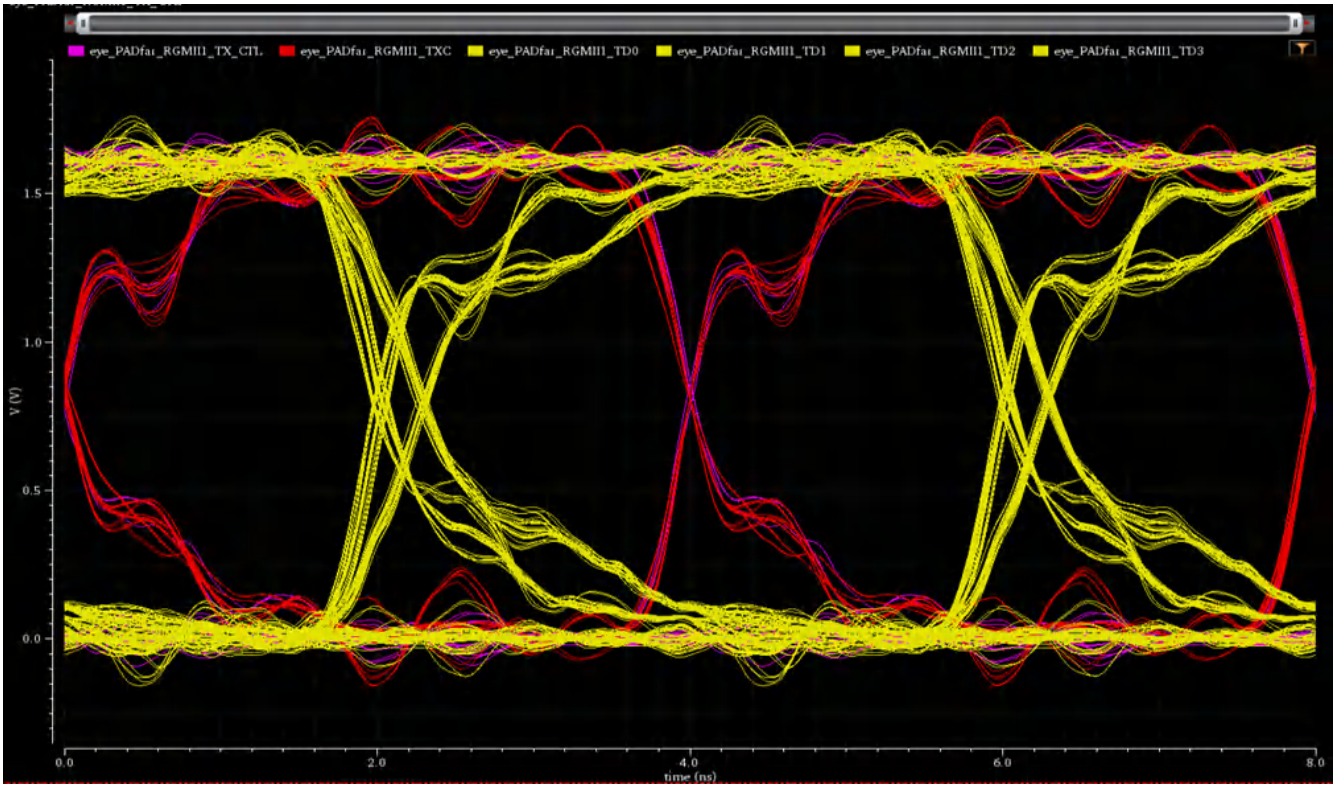


Figure 4-12. Waveform for Baseline System Analysis

Example 2: The figure below shows the analysis for delta capacitor c_comp added between SoC and attached device (EPHY) for all the transmit data (TD0, TD1, TD2, TD3) signals and transmit clock signal. The delta capacitors are recommended to be added as close as possible to attached device BGA pads. Addition of capacitors reduced signal reflections and improved the signal quality.

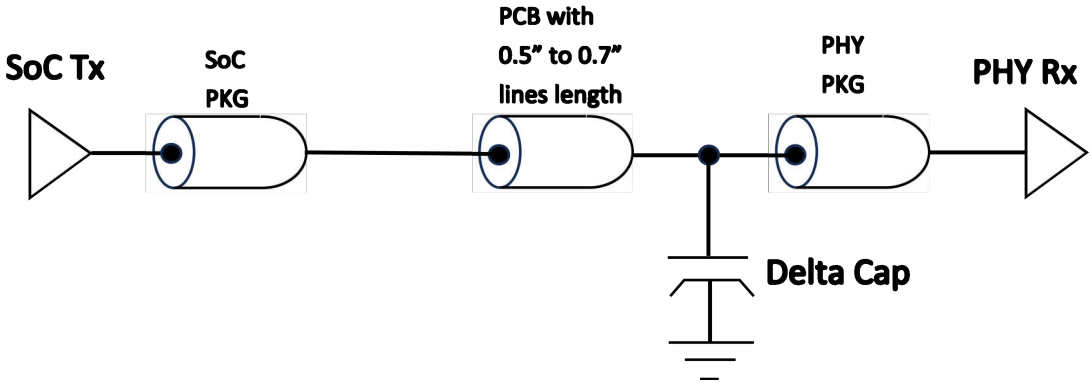


Figure 4-13. Circuit with Delta C_COMP Capacitors Added on the PCB near to the attached device BGA pad (Data Lines and Clock Line) to the Baseline System

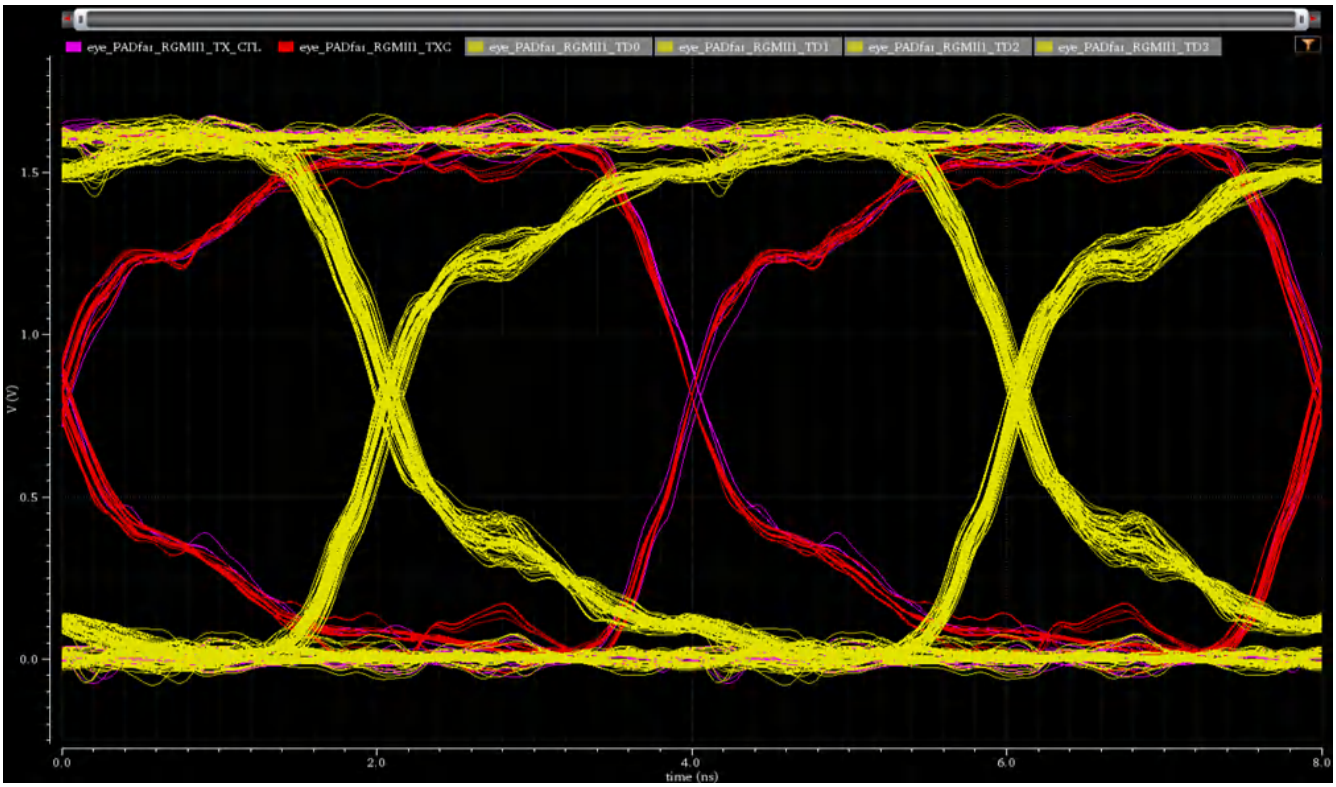


Figure 4-14. Waveform for Delta C_Comp Capacitors (4.7pF) Added on the PCB near to the attached device BGA pad Data Lines and Clock Line for Baseline System

5 Summary

The application report describes methodology to plan, route, and simulate custom board layout for implementing a successful high speed parallel interface. The recommendation for custom board designer is to simulate and evaluate the simulation option that works best for the specific system use case.

6 References

1. Texas Instruments, *AM62Px eMMC HS400 Board Design and Simulation Guidelines*, application note.
2. Reduced Gigabit Media Independent Interface (RGMII)- EIA/JESD 8-6 1995.
3. AM625 / AM623 / AM620-Q1 / AM62L / AM64x/ AM243x (ALV) / AM62Ax / AM62D-Q1 / AM62Px Board Layout – Links to documents for General High Speed Layout Guidelines
4. High-Speed Interface Layout Guidelines

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from September 30, 2025 to February 28, 2026 (from Revision * (September 2025) to Revision A (February 2026)) **Page**

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