Application Note

Precision Data Converter Selection Guide

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ABSTRACT

Selecting the right digital-to-analog converter (DAC) for an application involves several considerations relating to the device specifications. Making the right choice requires an understanding of precision DAC functional parameters and the influence on DAC performance and system capability. This guide explains key DAC specifications and how to select the right DAC for a specific system.

Table of Contents

Trademarks

1 Introduction

Before selecting a DAC, assess the absolute system requirements:

- **What are the key specifications?** – Output voltage range, current drive capability, current drive, and communication interface are important considerations.
- **Is a high resolution necessary?** – Some applications achieve sufficient performance with lower bit resolutions, reducing the DAC power and cost.
- **What is the bandwidth of the DAC?** – The minimum time needed for DAC output changes is related to output slew rate limitations and settling time.
- **What integrated features reduce system complexity?** – Integrated voltage reference, diagnostic features such as output monitoring and STATUS alarms, or integrated analog-to-digital converters (ADC) can simplify the design and reduce bill-of material (BOM).
- **What device rating does the target industry require?** – AEC-Q100 for automotive (Q1) or radiation hardened for space applications (SP).

2 Detailed Description

Access the Precision DAC parametric search page to see the parameters referenced in this guide.

2.1 Data Converter Architecture Overview

There are three precision DAC architectures:

- String
- Resistor Ladder (R-2R)
- Multiplying DAC (MDAC)

2.1.1 String DAC

The string DAC consists of 2^N resistors in series, where N is the resolution of the DAC. The resistors are connected between the positive DAC reference voltage (VREF) and the negative DAC reference voltage. This architecture provides a constant input impedance for the reference voltage and a structure best suited for low-cost, low-power designs. The code latched by the DAC closes the corresponding switch and divides the reference voltage to the desired output level before connecting directly to the output buffer. This output buffer provides low output impedance for driving loads and isolates the reference voltage source from external loading conditions.

String DACs become inefficient at greater resolutions as the number of resistors in the design increases. Each input code represents a resistor and switch, so the increase in resistors is exponential. An 8-bit string DAC only requires 256 resistors, but a 16-bit string DAC requires 65536 resistors. This architecture is inherently monotonic which means a positive code step never produces a negative change in output voltage and vice versa. Since a single code change only involves two active switches, strings DACs have low glitch energy. Figure 2-1 shows a simple diagram of the string DAC architecture.

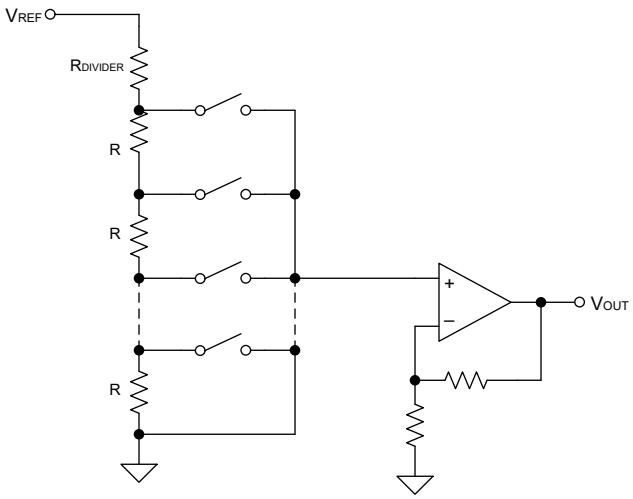

Figure 2-1. String DAC Architecture

2.1.2 R-2R DAC

The R-2R DAC (or back-DAC) architecture uses two resistor values of R and 2R to form a repeating pattern, with each 2R component of the design connected to either VREF or GND by a switch. The state of each switch depends on the latched input code to the DAC. The MSB controls the switch closest to VOUT and LSB controls the switch farthest from VOUT. The reference voltage input impedance of the R-2R architecture changes according to the digital input code. The R-2R design is commonly used for higher resolution devices, as they only require 2N resistors, where N is the resolution of the DAC. R-2R DACs provide high resolutions up to 16 or 20 bits and better noise performance. This type of DAC is not inherently monotonic.

Figure 2-2 shows a diagram of the R-2R DAC architecture.

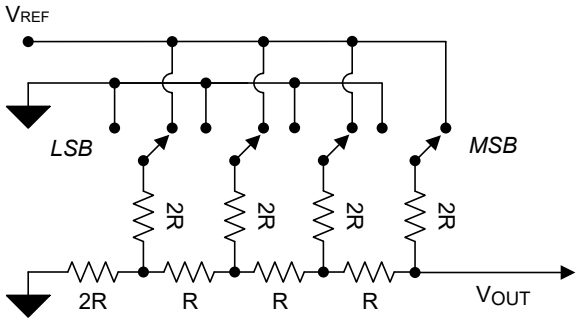

Figure 2-2. R-2R DAC Architecture

R-2R DACs have higher glitch energy as more switches are changed at once depending on the code-to-code transition. A 4-bit DAC changing its input code from 1000'b to 0111'b involves all four switches changing their state, otherwise known as a major carry transition. This type of midscale code change often produces the highest glitch energy.

Figure 2-3 shows an example of a major carry transition. At step 1 in the graph, the output voltage is settling from the previous code change. At step 2, there is a rise in the output voltage due to the major carry transition. At step 3, there is a larger voltage drop as the switches settle.

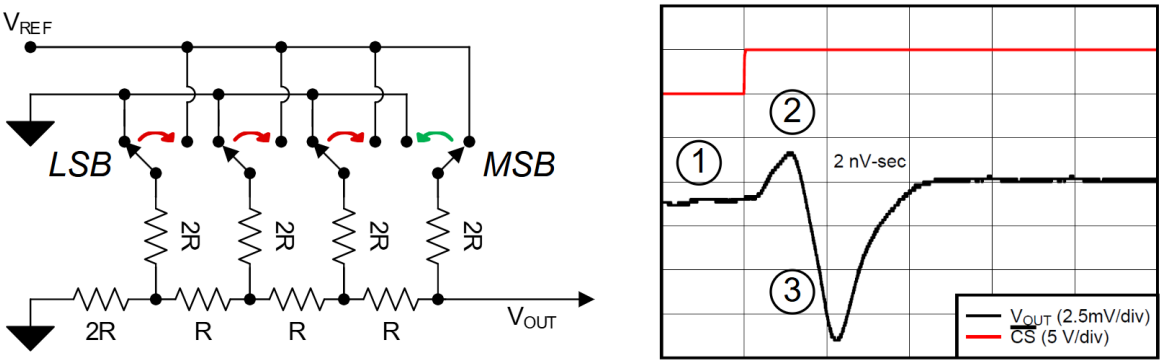

Figure 2-3. Major Carry Transition Glitch Voltage

2.1.3 Multiplying DAC

The Multiplying DAC (MDAC) shares a similar structure to R-2R DAC. The reference voltage and output swap positions to form a current-switching ladder architecture. Due to this architecture, the voltage reference input impedance is constant, allowing the reference to be dynamic. The MDAC essentially *multiplies* the reference voltage by the input code. The MDAC can utilize a reference voltage higher than the supply voltage, with the full-scale output determined by the reference voltage rather than the supply voltage. The resistor architecture uses current steering which creates faster settling times and low total harmonic distortion (THD) and noise, which are desirable traits for applications such as waveform generation.

A transimpedance amplifier (TIA) is necessary to convert the current output of the MDAC to a voltage. As the output impedance of the MDAC changes depending on the input code, a TIA with low offset voltage is necessary to avoid introducing linearity errors at the output. The final output voltage is inverted compared to the reference voltage input.

MDACs are often used in test and measurement applications but can also be implemented for other purposes such as generating AC waveforms or attenuation and mixing signals. MDACs are also used to generate a waveform from a DC input voltage. Figure 2-4 shows a simple diagram of the MDAC architecture.

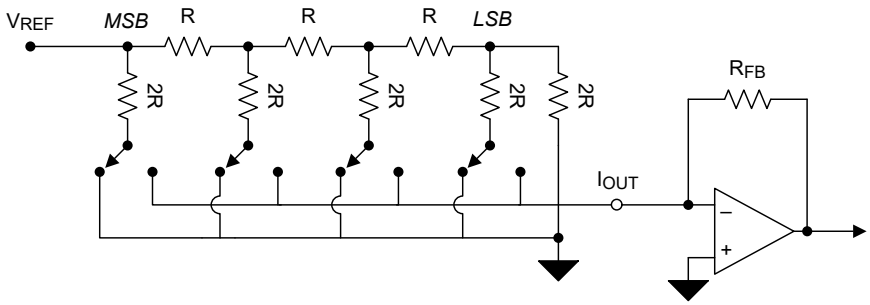

Figure 2-4. MDAC Architecture

2.2 Data Converter Parameters

The Precision Digital-to-analog converters parametric search page contains parametric filters that can assist with DAC selection. A general overview of each parameter is provided below to explain the main considerations for each column found in the search window.

2.2.1 Resolution

Resolution is the number of digital input bits used to determine the analog output signal. A "code" is a single digital input value. The total number of codes describes the number of discrete steps the DAC output can generate. In combination with the DAC's resolution, the reference voltage determines the LSB (least significant bit) weight, or output step size. The example equations below show LSB voltage calculations for different DAC resolutions.

$$V_{LSB} = \frac{A \times V_{REF}}{2^n} \quad (1)$$

For $A = 1\frac{V}{V}, V_{REF} = 5V$

8-bit DAC: $V_{LSB} = \frac{1 \times 5V}{256} = 19.531mV$

12-bit DAC: $V_{LSB} = \frac{1 \times 5V}{4096} = 1.2207mV$

16-bit DAC: $V_{LSB} = \frac{1 \times 5V}{65{,}536} = 76.294\mu V$

DACs withgreater resolutions allow for small-step voltage output control. Increasing the resolution expands the number of input codes available to the user exponentially. A 16-bit DAC has 65,536 codes while a 20-bit DAC has 1,048,576 codes. Applications such as high-quality audio conversion or medical imaging rely on DACs with greater resolution to accurately reconstruct the original sound wave from a studio recording or sensitive digital data from ultrasound and MRI machines. The total number of available input codes for different resulutions are shown below.

8-bit = 2^8 = 256 (0 to 255)

10-bit = 2^{10} = 1,024 (0 to 1,023)

12-bit = 2^{12} = 4,096 (0 to 4,095)

16-bit = 2^{16} = 65,536 (0 to 65,535)

20-bit = 2^{20} = 1,048,576 (0 to 1,048,575)

2.2.2 Reference Type

The reference voltage for a DAC can be either internal or external. External references can be shared across multiple DACs to eliminate common mode noise and to avoid additional noise coupling from the internal switching action of the DAC devices. External references are often a requirement for radiometric applications and can offer increased accuracy, lower noise, and better temperature stability.

Internal references provide a simple integrated design for DAC output control. Advantages of an internal reference include reducing the routing complexity on a board layout and improving power efficiency.

2.2.3 Number of Channels

Channel count is the number of independent DACs that are integrated into one device. Traits such as the input code or gain are applied individually for each channel or to multiple channels in a group. Increasing the channel count of the DAC increases its power consumption but reduces the system design complexity by integrating multiple controlled outputs into a single IC. Figure 2-5 shows a DAC with 2 channels as an example.

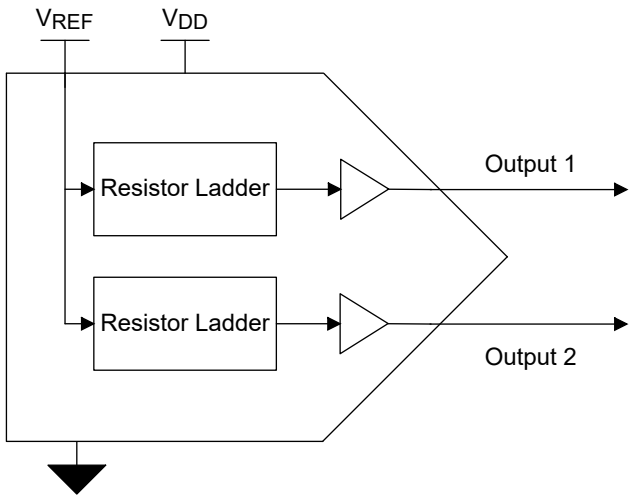

Figure 2-5. DAC with 2 Channels

2.2.4 Interface Types

The two most common interface types available for Precision DACs are SPI and I2C. Many DAC devices can accept both SPI and I2C communication.

Serial Peripheral Interface (SPI) is a 3- or 4-wire protocol that provides full-duplex communication, with hardware-based device selection through the chip select (CS) pin. SPI is advantageous in applications that require fast communication, with speeds as high as 100MHz depending on the DAC device.

Inter-Integrated Circuit (I2C) is a 2-wire protocol that provides half-duplex communication with software-based device selection through device-specific register addressing. The 2-wire structure benefits a design with limited pin count. I2C is slower than SPI, with standardized speeds of 100kHz and 400kHz (although some systems support fast+ mode I2C which operates at 1MHz). The host controller must support start, stop, and acknowledge commands, leading to a more complex design overhead.

2.2.5 Output Types

Depending on the DAC architecture, the output can be either voltage or current. Some DACs come with only one type of output while more complex DACs include both voltage and current output options.

The DAC output can be buffered or unbuffered as well. Some devices remain unbuffered to give users the option of selecting an operational amplifier tailored to their specific system requirements.

DAC outputs come in unipolar or bipolar configurations. Unipolar outputs provide either positive or negative output but cannot provide both with a single reference voltage. For a unipolar device, the binary input code is unsigned. Bipolar configurations offer both positive and negative outputs, often using signed binary codes to

select specific analog values. Bipolar outputs require both a positive and negative voltage source for the internal amplifier.

2.2.6 Integral Nonlinearity and Differential Nonlinearity

Integral Nonlinearity (INL) is the deviation of analog output values from the ideal transfer function of the DACs digital input codes, represented by a perfect line from the zero-scale code to the full-scale code. Differential Nonlinearity (DNL) is the difference between the expected 1LSB (Least Significant Bit) step of the analog output and the empirically measured step size. In the ideal case, every digital code would produce the exact voltage output derived from the transfer function of reference voltage and gain, with adjacent codes creating a consistent step size. This ideal case is shown in Figure 2-6.

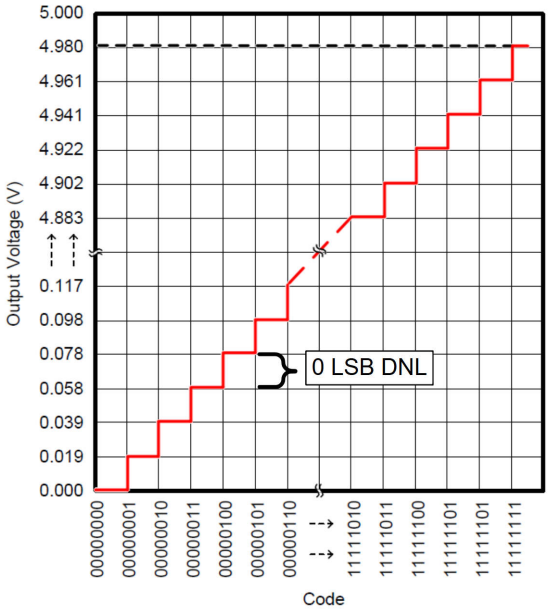

Figure 2-6. Ideal Transfer Function

In a real system, the analog output can deviate from the theoretical result of the transfer function across the full output range. Figure 2-7 shows a DNL of 0.5 LSB.

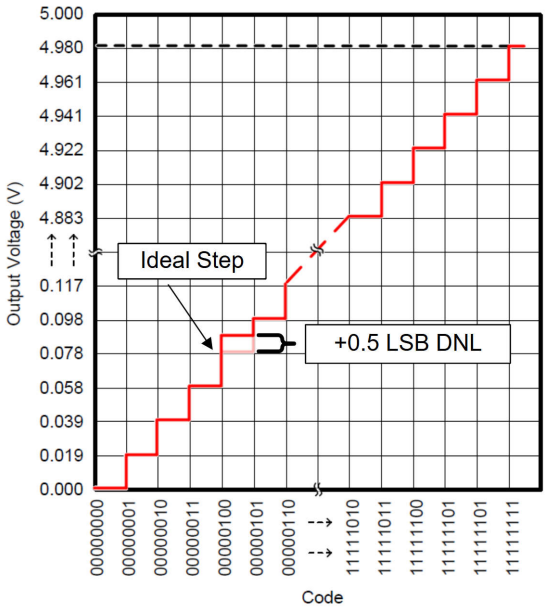

Figure 2-7. Non-ideal DNL Step

A DAC with more than 1LSB of DNL is nonmonotonic, where an increase of the DAC code results in a decrease of the analog output or vice versa. This behavior is undesirable for closed-loop applications. Figure 2-8 shows a nonmonotonic DNL step.

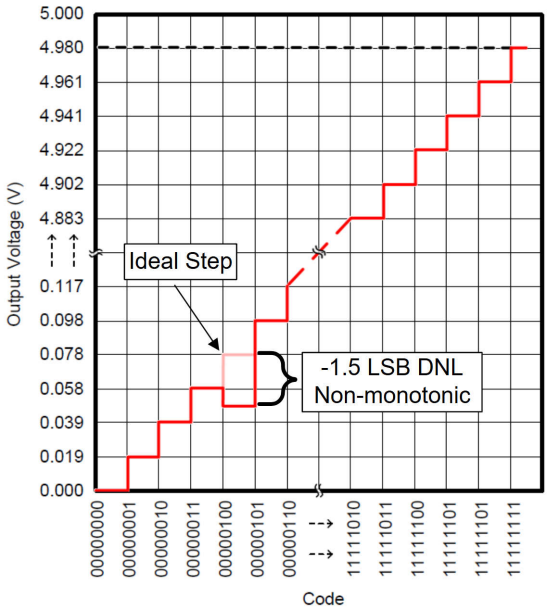

Figure 2-8. Non-monotonic DNL Step

INL is related to DNL mathematically, where the INL between two output codes is the combined sum of the DNL for each code step in the transition. Figure 2-9 shows an example of INL.

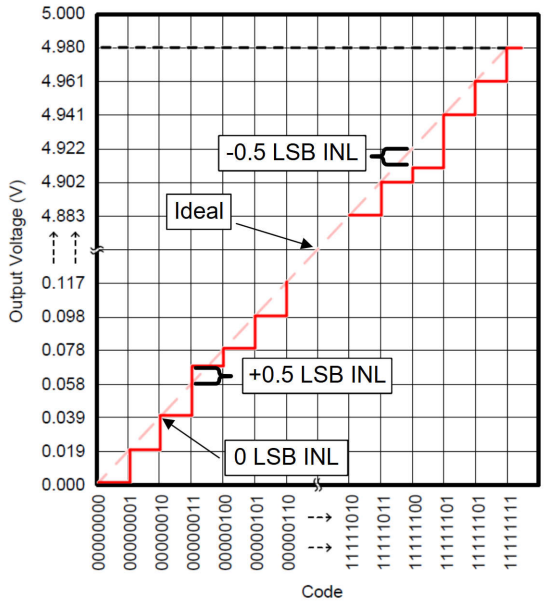

Figure 2-9. INL in the DAC Transfer Function

2.2.7 Settling Time and Update Time

The settling time of a DAC is the total time a DAC requires to transition from one output voltage to a new output voltage. The final analog value must settle within a defined threshold before this is considered a valid output (usually +/-1 LSB). The settling time begins when a new input code is initially latched by the DAC (by asserting the active-low LDAC pin for example). Greater code steps result in longer settling times due to the output buffer slew rate. Figure 2-10 shows each part of the settling process after a new input code is sent to the DAC.

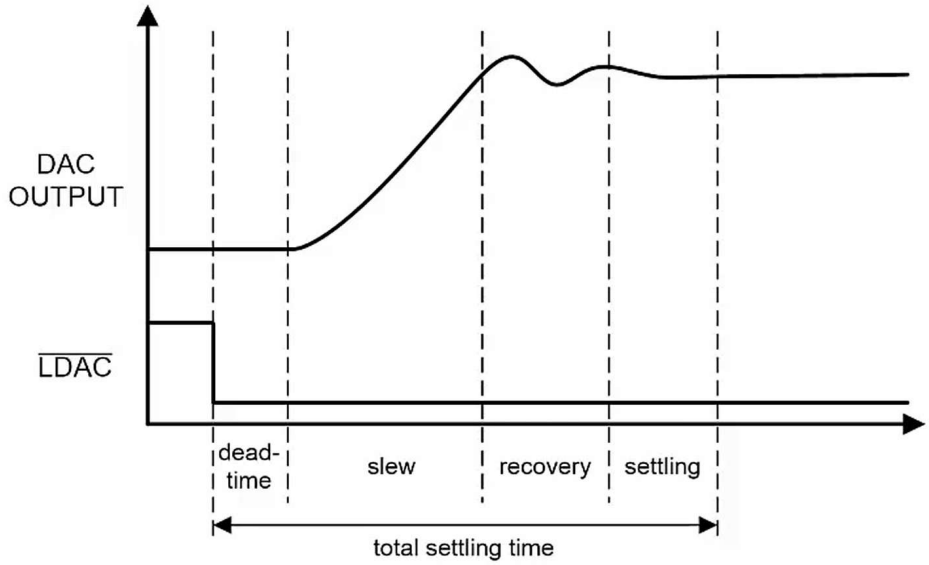

Figure 2-10. DAC Settling Time

The update time of a DAC is the minimum time that must pass before a new code can be latched into the DAC. The maximum possible number of updates within a given period represents the update rate. The settling time can limit the update rate if a selected DAC has a fast communication speed. This limitation occurs when the DAC output voltage does not have enough time to stabilize at the target voltage before the next code change is received from the host controller. Alternatively, the settling time may be faster than the timing specifications of the digital communication protocol. In this case, the total time for a single code change command to complete becomes the minimum update time.

The sample rate of a DAC is determined by taking the inverse of either the worst-case settling time or the minimum update time of the communication protocol, depending on which metric is the limiting factor.

2.2.8 Physical Properties

DACs come in many different package sizes. The physical considerations of choosing a DAC will depend on the system requirements and board area.

Certain applications require packages rated for safety or quality, depending on industry standards. TI provides Precision DACs at multiple qualification levels with AEC-Q100 Automotive (Q1), and Space (SP) rated devices.

Package specifications for a DAC can be found on the device product page, under the *Package* | *Pins* | *Size* tab in the Product Details section. For a comprehensive list of specific package types, visit the Packaging Terminology page on TI.com.

2.2.9 Notable Features

Some DACs include extra features to enhance user control options, provide additional device information, or enable host controller alert systems.

SDO – DACs with readout capability have a 4-wire SPI interface. The SDO pin can send register information back to the host and is usually controlled by an SDO-EN bit to toggle functionality on and off. Not all DACs support readback with some devices only including the SDI hardware pin for updating the DAC input register.

EEPROM – DACs with EEPROM Non-volatile memory can store programmed settings that are automatically loaded after a power cycle. This function is useful for systems that require custom settings in an isolated environment. EEPROM data retention can be anywhere from 20 to 50 years depending on the device specification, with the ability to withstand thousands of communication cycles.

HART – HART is a backward-compatible enhancement to 4-20mA instrumentation that allows two-way communication with smart, microprocessor-based field devices. DACs with HART functionality are used in factory automation and control applications. For more information about HART see A Basic Guide to the HART Protocol

Integrated Temperature Sensor – Devices with integrated temperature sensors can report the temperature at different points inside the device package. This information is either reported as a digital readback value or converted to a voltage and routed to an external monitoring pin for measurement. These sensors support programmable alerts on specific hardware pins and provide overtemperature shutdown functions. Some high-end DACs may have multiple temperature sensors per channel to monitor the internal components.

Analog Monitoring – DACs with internal ADC monitoring systems have analog input pins, allowing the devices to function as control supervisors. These DACs include programming options to set up alarm high and alarm low window thresholds. A dedicated alarm output pin sends information to the host controller based on user defined conditions. This type of monitoring enhances diagnostics for industrial control or test and measurement systems.

Flexible GPIOs – FlexIO pins can be configured as either ADC inputs, GPIOs, or sequencing signals depending on the programmed register settings of the device. Additional functionalities include alarm inputs, conversion reporting, conversion triggers, or DAC data clearing functionality.

Smart DAC – Smart DAC devices reduce the resource count in a system by providing extended features and factory programmability. These devices have integrated non-volatile memory, programmable state machine logic, pulse-width modulation generators, and custom waveform generators built in. Smart DACs eliminate the need for complicated software in systems that require minimal resources or a simple sense-measure-control feedback loop. For more information about Smart DAC applications see the Smart DAC Product Selection Guide.

3 Summary

The Precision DAC portfolio offers a diverse selection of different product features and functions. Understanding the parameters and features listed in this guide transforms the device selection process into a digestible system of choosing your highest priorities and needs.

Precision Digital-to-analog converters parametric search page shows the search page. This tool includes all the parameters mentioned in previous sections. By selecting *Columns* in the top left of the table, different parameter columns can be added or removed from the list. Columns for operating temperature range, package dimensions, typical power consumption, and GPIO count are found here. Once added to the list, each parameter in the table can be filtered for specific criteria by selecting the filter symbol under the column heading. Alternatively, selecting *All Filters* to the left of the *Columns* button will reveal a drop-down menu for every available filter. Adjusting the filter settings here will automatically add the parameter to the column list. Columns can be re-ordered by clicking and dragging the heading.

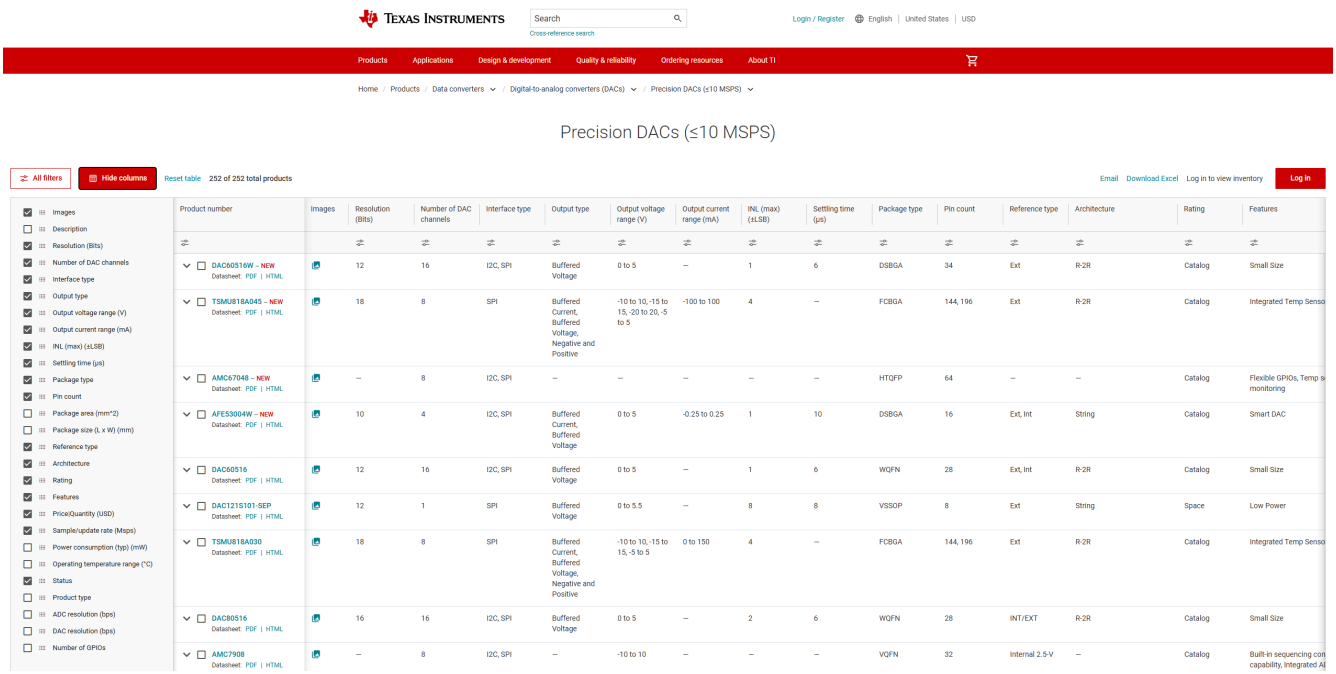

Figure 3-1. Precision Digital-to-Analog Converter Parametric Search Page

3.1 Example Devices

Examples of our device catalog and specific DAC parts can be found below.

DAC43701* – *Cost Optimized, Low Power

Even the low-cost devices can support extra features to add flexibility for the user.

- 8-bit, 10-bit, and 12-bit versions
- Includes EEPROM and Smart DAC features.
- String DAC architecture provides low glitch and stable VREF input impedance

***DAC80516* – High Channel Count, Small Package**

DAC devices can support many channels while maintaining a small package size.

- 12-bit and 16-bit versions
- R-2R architecture supports higher resolutions and multiple channels with significantly lower resistor count.
- Fast settling time of 6us which enables quicker code-to-code transitions.

***DAC8775* – Expanded Feature Set, Industrial Control**

Some DACs have an increased feature set to facilitate more complex factory automation applications.

- Adaptive Power Management which minimizes power dissipation of the chip.
- Extended monitoring functions such as CRC/Frame Error Check, Watchdog Timer, Thermal Alarm, and Open/Short Circuit protection.
- Integrated Buck-Boost converter for each channel to minimize power dissipation and provide significant system integration.
- Auto Learn Mode to sense the load current and optimize the settling time.

3.2 Other Resources

Precision Digital-to-analog converters parametric search page

Precision Labs Series: Digital-to-analog converters (DACs)

A Basic Guide to the HART Protocol

Smart DAC Product Selection Guide

Packaging Terminology

DAC E2E Forum

4 References

1. Texas Instruments, A DAC for all precision occasions, analog design journal.
2. Texas Instruments, Precision labs series: Digital-to-analog converters (DACs), video series.
3. Texas Instruments, Settling time and update rate, video series.

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Last updated 10/2025