Application Note

SYSREF Alignment Detector and SYSREF Monitor

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ABSTRACT

This application note describes the use of SYSREF Alignment detector in AFE81xx. The AFE81xx is a family of high-performance, wide-bandwidth multi-channel transceivers, integrating up to sixteen RF sampling transmitter chains, up to sixteen RF sampling receiver chains, and up to four RF sampling digitizing auxiliary chains (feedback paths). SYSREF is a reference signal which serves as reset for key functional blocks within the device and also helps to establish a common timing reference across multiple devices. To Ensure deterministic latency at the system level, it is essential for the SYSREF to be latched by the AFE input clock in a deterministic way across power-up cycles. The SYSREF Alignment detector primarily assists in aligning SYSREF edge to the AFE input clock edge without any setup and hold time violations. This is important when functioning at higher clock rates, such as when the AFE is used in external clock mode.

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Trademarks

1 Introduction

SYSREF is utilized by devices to synchronize its internal components, including dividers, signal processing blocks, and elastic buffers, thereby guaranteeing deterministic latency. It ensures that the latency across the link is deterministic and multiple devices are completely synchronized such that the outputs are phase aligned. The SYSREF signal operates at a significantly lower frequency than the input clock, and its frequency is an integer multiple of the input clock. In the AFE the SYSREF is latched on the reference clock (Fref) rise edge. The phase difference between them can lead to timing violation for SYSREF block since SYSREF can fall in between setup and hold boundaries as shown in Figure 1-1.

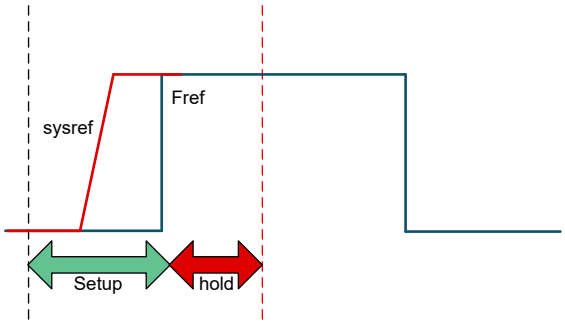

Figure 1-1. Setup Hold Window

SYSREF should always be positioned such that the timing conditions are met. The easiest way to ensure this is to make SYSREF transition coincide with reference clock (Fref) falling edge. This should be done by introducing appropriate delay in SYSREF path or Fref path, for e.g. in case AFE is receiving clock from external source then we can introduce phase in the clock source to mimic the delay. (delay = phase in degrees/360/Fref).

SYSREF Alignment Detector helps identify the relative position between SYREF and reference clock (Fref). With the device operating in external clock mode with high frequency clock such as 12GHz input clock (83ps period), precise SYSREF signal alignment becomes critical due to the extremely tight timing margins. In this mode, even small deviations in SYSREF propagation or input reference clock propagation (of the order of 30–40ps) can shift the SYSREF edge very close to the rising edge of the input clock. In contrast, in internal PLL mode, where the input clock is typically ≤500 MHz (2ns period), the available timing margin is much larger. Variations in SYSREF arrival time are less likely to push it across the clock edge boundaries, making the system more tolerant to skew and reducing the dependence on SYSREF Alignment Detector. Ultimately, for deterministic operation, the use of the SYSREF Alignment Detector is highly recommended in external clock configurations to verify proper synchronization and compliance with timing requirements.

The SYSREF Alignment Detector block receives Two inputs: clock_in (Fref) and sysref_in (SYSREF). It evaluates the relative timing of SYSREF with respect to the clock edges and generates a 10-bit SYSREF Alignment Detector readout as its output. This readout reflects the relative phase relationship of the input clock to the SYSREF signal at the point of capture near the first internal latch. By observing changes in the SYSREF Alignment Detector output while incrementally adjusting the SYSREF delay at the source, users can optimize SYSREF placement within a valid timing window.

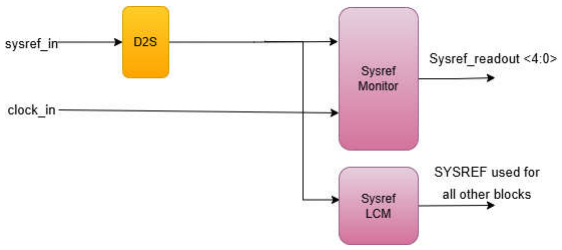

Figure 1-2. SYSREF Path Overview

2 SYSREF Alignment Detector Architecture

The output of the SYSREF Alignment detector is a 10 bit number [9:0]. Each bit signifies zone for SYSREF with respect to reference clock (Fref) rising edge as show below.

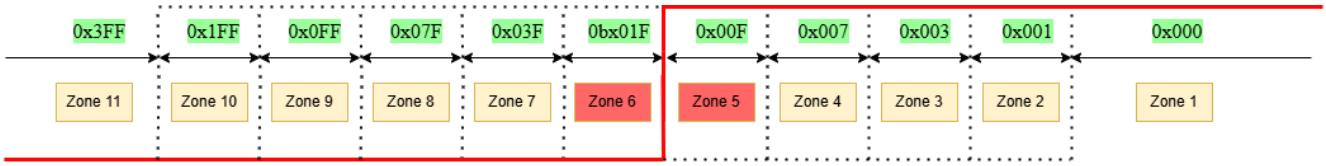

Figure 2-1. SYSREF Zone and SYSREF Alignment detector Reading Mapping

Each zone signifies the Margin available from setup and Hold violation. Table 2-1 lists the interpretation for each zone.

Table 2-1. SYSREF Alignment Detector Zone Definitions & Timing Margins

Zone Number	SYSREF Alignment Detector Reading	Explanation
Zone 1	0	This signifies that SYSREF is present before the falling edge and after the rising edge of the reference clock (Fref). This zone has minimum margin of 32ps from the timing violation. SYSREF will latch on the next rising edge of the reference clock (Fref). This is the most optimal zone.
Zone 2	1	This signifies SYSREF is present before the falling edge and after the rising edge of the reference clock (Fref). This Zone has a margin of 24-32ps from the timing violation. SYSREF will latch on the next rising edge of the reference clock (Fref)
Zone 3	3	This signifies SYSREF is present before the falling edge and after the rising edge of the reference clock (Fref). This Zone has a margin of 16-24ps from the timing violation. SYSREF will latch on the next rising edge of the reference clock (Fref)
Zone 4	7	This signifies SYSREF is present before the falling edge and after the rising edge of the reference clock (Fref). This Zone has a margin of 8-16ps from the timing violation. This is susceptible to timing violation. Ideally SYSREF will latch on the next rising edge of the reference clock (Fref)
Zone 5	15	This signifies SYSREF is present before the falling edge and after the rising edge of the reference clock (Fref). This Zone has a margin of 0-8ps from the timing violation. This is most susceptible to timing violation.
Zone 6	31	This signifies SYSREF is present before the rising edge and after the falling edge of the reference clock (Fref). This Zone has a margin of 0-8ps from the timing violation. This is most susceptible to timing violation.
Zone 7	63	This signifies SYSREF is present before the rising edge and after the falling edge of the reference clock (Fref). This Zone has a margin of 8-16ps from the timing violation. This is susceptible to timing violation. SYSREF will latch on this rising edge of the reference clock (Fref).
Zone 8	127	This signifies SYSREF is present before the rising edge and after the falling edge of the reference clock (Fref). This Zone has a margin of 16-24ps from the timing violation. SYSREF will latch on this rising edge of the reference clock (Fref).
Zone 9	255	This signifies SYSREF is present before the rising edge and after the falling edge of the reference clock (Fref). This Zone has a margin of 24-32ps from the timing violation. SYSREF will latch on this rising edge of the reference clock (Fref).
Zone 10	511	This signifies SYSREF is present before the rising edge and after the falling edge of the reference clock (Fref). This Zone has a margin of 32-40ps from the timing violation. SYSREF will latch on this rising edge of the reference clock (Fref).
Zone 11	1023	This signifies SYSREF is present before the rising edge and after the falling edge of the reference clock (Fref). This zone has minimum of 40ps margin from the timing violation. SYSREF will latch on this rising edge of the reference clock (Fref). This is the most optimal zone.

Zone 1 and Zone 11 are the safest zones for SYSREF. Based on the current reading we can either advance or delay SYSREF to get the best margin. In AFE81xx SYSREF Alignment Detector reading latches on positive edge of Fref clock and its recorded/Frozen at negative edge of clock. Effectively all readings are with respect to positive edge of Fref clock preceding the negative edge of Fref clock which falls after the SYSREF positive edge.

Note: For high frequency mode (Fref above 7.5G), Some of the zones are not valid. Refer Section 4.

We can discuss some case studies with examples of alignment strategy.

2.1 Case 1

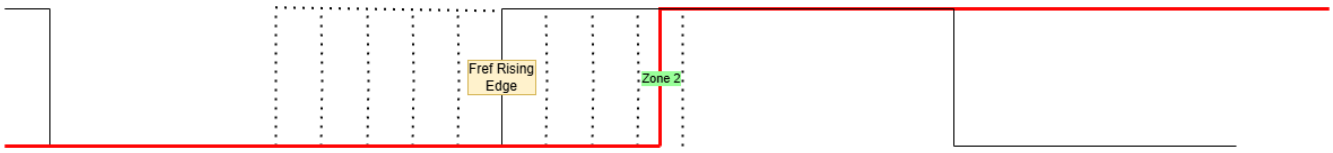

Figure 2-2. Case 1 - SYSREF in Zone 2

In this case SRSREF is in Zone 2 and SYSREF Alignment Detector reading should be 0x01. Now extrapolating this case further, we can say as we keep advancing the SYSREF with respect to clock the reading should start transitioning from 0x01 to 0x3FF. Once SYSREF Alignment Detector reads 0x3FF, we will be in zone 11. Similarly, if we delay the SYSREF then we will start transitioning to 0x000 reaching the zone 1.

2.2 Case 2

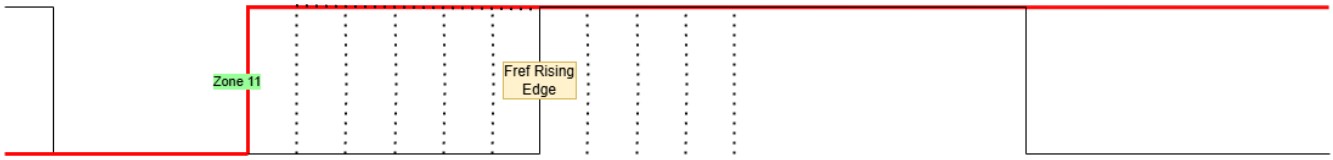

Figure 2-3. Case 2 - SYSREF in Zone 11

In this case SYSREF is advanced such that the SYSREF comes well before the reference clock rising edge, falling into zone 11. The SYSREF Alignment Detector would display 0x3FF. Now even if we advance the SYSREF further we keep seeing SYSREF Alignment Detector output to be 0x3FF until SYSREF doesn't come before the falling edge of previous reference clock (Fref).

2.3 Case 3

Figure 2-4. Case 3 - SYSREF in Zone 1

In this case when we advance the SYSREF clock so much that it even precedes the falling edge of the reference clock (Fref). This is zone 1 and SYSREF Alignment Detector would display 0. Now if we keep advancing the SYSREF further we will see all zeros at monitor output unless we advance so much that SYSREF starts coming within Zone 2. This situation becomes same as discussed in case 1 with only difference being SYSREF Alignment Detector getting latched on one clock before.

3 Software Sequence for SYSREF Alignment Detector Configuration

The AFE81xx SYSREF Alignment Detector configuration and readout is done through the device's SPI interface using a set of CAPI functions.

In bringup configuration we need to provide the input to AFE if SYSREF is AC coupled or DC coupled using "sysrefTermination" system parameter.

* Bit4 = 1 - SYSREF is DC coupled

* Bit4 = 0 - SYSREF is AC coupled

uint8_t sysrefTermination;

Following CAPI sequence is need for config and readout.

1. ti_afe81_enableSysrefmonitor(AFE81_INST_TYPE afeInst);

   This function is used to Enable the SYSREF Alignment Detector. We should Run this only once if we want to use SYSREF Alignment Detector.
2. ti_afe81_sysrefmonitorReady(AFE81_INST_TYPE afeInst)

   This function resets SYSREF Alignment Detector state machine and keeps it ready to trigger on next SYSREF pulse. SYSREF Monitor should be enabled before running this function. Give SYSREF pulse just after running this and check SYSREF Monitor output using sysrefmonitorReadout function.
3. Give SYSREF pulse just after calling sysrefmonitorReady. can use function #adcDacSync.
4. ti_afe81_sysrefmonitorReadout(AFE81_INST_TYPE afeInst, uint32_t *sysrefMonitor)
5. ti_afe81_disableSysrefmonitor(AFE81_INST_TYPE afeInst)

Returns SYSREF Alignment Detector output data. If no SYSREF is received after the latest call of sysrefmonitorReady function, then output data contains 65535 else it should be a 10-bit field.

Table 3-1. SYSREF Location Relative to FRef

0x3FF	**Valid/Best Case**
0x0FF	Advanced
0x01F	Advanced/Delayed
0x00F	Advanced/Delayed
0x001	Delayed
0x000	**Valid/Best Case**

The best setting is when we have clean transition from 0 to 0x3FF (Zone1 to Zone11) while delaying/adding delay in SYSREF and 0x3FF to 0 (Zone11 to Zone1) if advancing/reducing delay in SYSREF path. This aligns SYSREF exactly at the negative edge of the clock.

The **ti_afe81_sysrefmonitorReadout** function returns the readout of the first SYSREF pulse captured after calling **ti_afe81_sysrefmonitorReady**. To obtain updated readings, you must call **ti_afe81_sysrefmonitorReady** before each readout operation. You must disable the monitor to restore normal device operation. This is critical because sequences requiring multiple SYSREF pulses, such as Re-link, will be impacted as device will continue to receive only one pulse after the detector is enabled. For each SYSREF readout, follow the complete sequence of enabling the monitor, ready, capturing the pulse readout, and then disabling the monitor before proceeding with AFE operations. Repeat this entire five-step cycle for every measurement if you plan to perform AFE-related operations between readouts.

4 High Frequency Mode

For reference clock (Fref) above 7.5G, we run the SYSREF Alignment Detector in high frequency mode. In this mode certain zones from all 11 zones are not valid due to timing constraints.

Invalid Zones are Zone 1, Zone 2, Zone9, Zone 10 and Zone 11. Which effectively means that out of 10-bit [9:0] output of the SYSREF Alignment Detector five bits [6:2] are valid, bits[1:0] will always be 1 and [9:7] will always be 0.

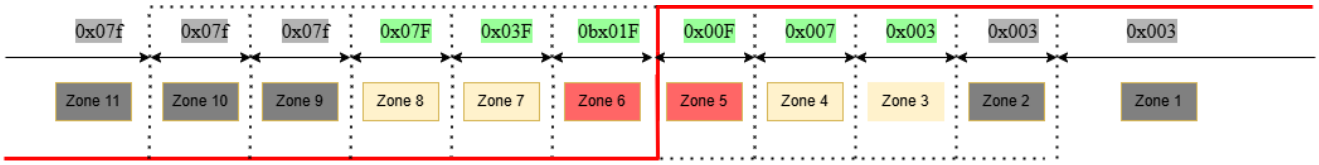

Figure 4-1. SYSREF Zones in High Frequency Mode

In high frequency Mode the best setting is when we have clean transition from 0x3 to 0x07F (Zone3 to Zone8)while delaying/adding delay in SYSREF and 0x07F to 0 (Zone8 to Zone3)) if advancing/reducing delay in SYSREF path. This will align SYSREF exactly at the negative edge of the clock.

Table 4-1. SYSREF Location Relative to FRef in High frequency mode

0x07F	**Valid/Best Case**
0x03F	Advanced
0x01F	Advanced/Delayed
0x00F	Advanced/Delayed
0x007	Delayed
0x003	**Valid/Best Case**

5 Summary

This application note describes the role of the SYSREF Alignment Detector in achieving deterministic latency across devices. It explains the internal architecture and operation of the SYSREF Alignment Detector, detailing the precise alignment of the SYSREF signal with respect to the input clock. By observing the SYSREF Alignment Detector's 10-bit readout, users can validate and optimize input clock timing to meet setup and hold timing requirements.

6 References

1. Texas Instruments, *AFE812x Octal/Quad-Channel RF Transceiver with Feedback Paths*, datasheet.
2. Texas Instruments, *AFE8104, AFE8108 7.4GHz Transceiver With 12GSPS DACs and 6GSPS ADCs*, datasheet.
3. Texas Instruments, *AFE8190 16-Channel RF Transceiver with Feedback Paths*, datasheet.

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