Application Note

Multiphase Operation of LM5125A-Q1

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ABSTRACT

Multiphase operation offers advantages such as ripple cancellation, smaller components and simpler thermal management. The LM5125A-Q1 supports multiphase operation to handle higher currents. The system achieves balanced current sharing and accurate phase shift.

This application note introduces 4-phase and 3-phase operation setups. Next, the LM5125A-Q1 multiphase phase operation related block diagram is presented. The functionalities are described for configurations as Primary or Secondary. Finally, some waveforms are shown and analyzed.

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Trademarks

1 Introduction

The LM5125A-Q1 is a stackable, dual-phase synchronous boost converter specifically designed for automotive audio amplifier applications. The output voltage is adjustable through the ATRK/DTRK pin.

To meet the increasing power demands of modern audio amplifiers, designs employing 3-phase and 4-phase operation are gaining popularity. A four-phase configuration can be readily achieved by connecting two LM5125A-Q1 devices. In this setup, the primary controller regulates the output voltage and communicates a current command (COMP) to the secondary controller. The secondary controller follows the current command and synchronizes with the primary controller with a phase shift.

This document provides a comprehensive guide to configuring and implementing 3-phase and 4-phase systems using the LM5125A-Q1, outlining the specific functionalities when the device is configured as either the primary or secondary controller.

2 LM5125A-Q1 Multiphase Operation Setup

Figure 2-1 shows the 4-phase operation diagram.

The key notes are as follows:

- Set the Primary CFG2 to Level 9, Level 10, Level 13 or Level 14; Set the Secondary CFG2 to Level 15 or Level 16.
- Tie the Secondary SYNCIN to the Primary SYNCOUT.
- Tie COMP, SS, ILIM/IMON and MODE pins of the Secondary to their respective counterparts on the Primary.
- Tie the Secondary ATRK/DTRK, DLY pin to AGND.

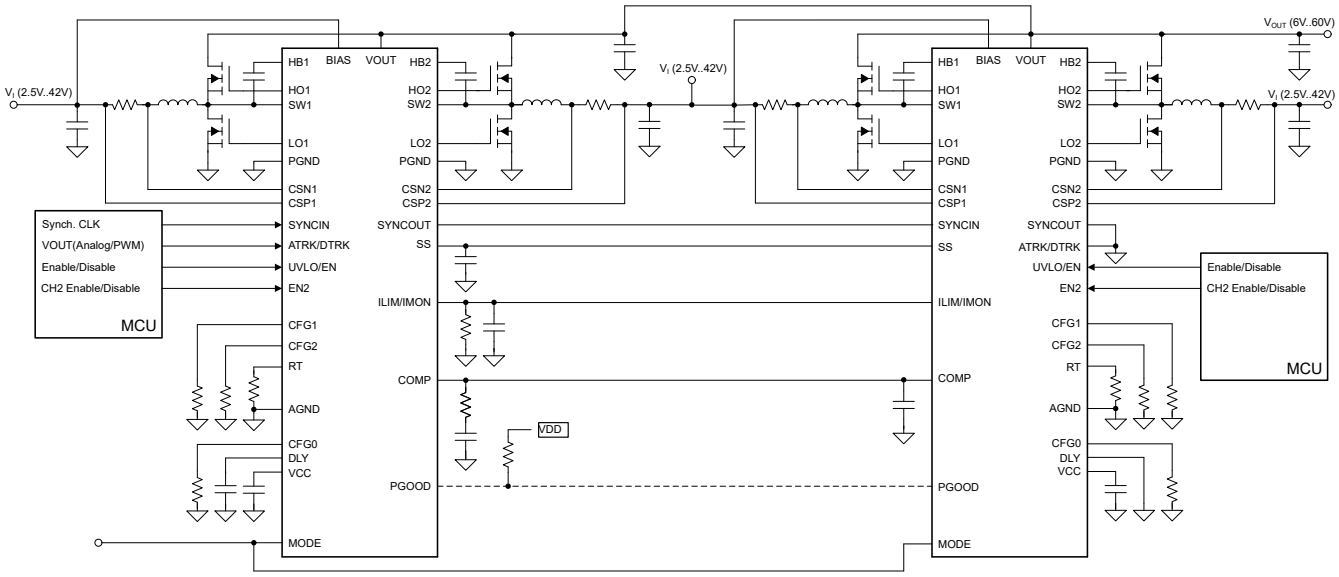

Figure 2-1. LM5125A-Q1 4-Phase Operation

Similarly, Figure 2-2 shows the 3-phase operation diagram. Compared to Figure 2-1, the difference is: Set the Primary CFG2 to Level 7, Level 8, Level 11 or Level 12. LM5126A-Q1 can also be used as the Secondary.

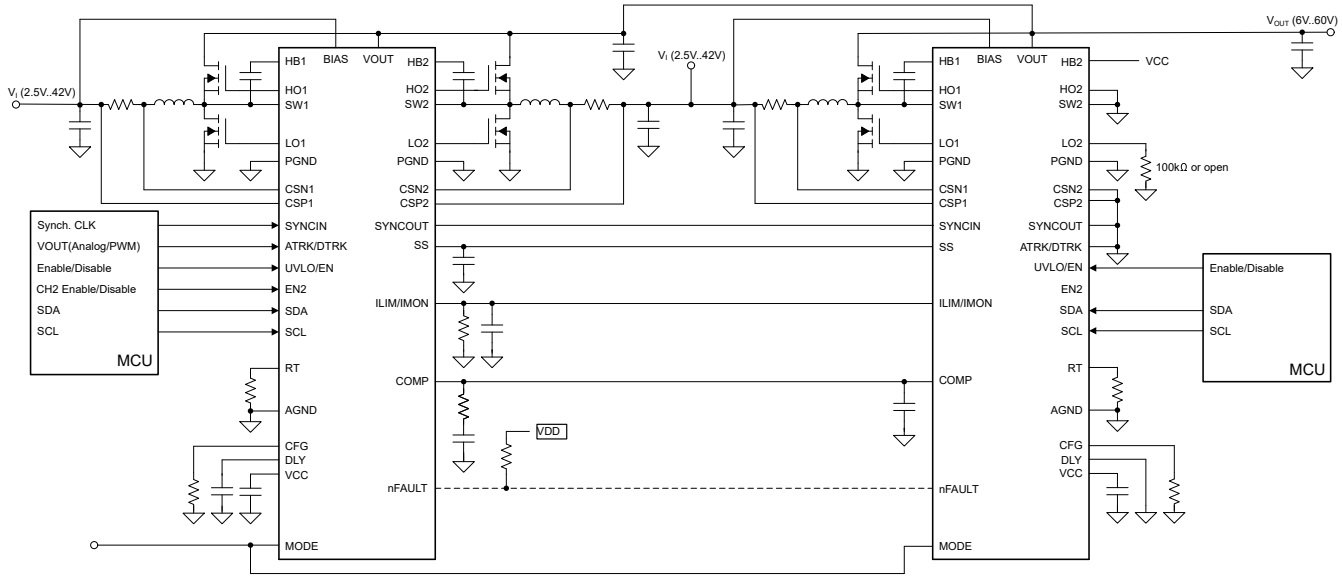

Figure 2-2. LM5125A-Q1 3-Phase Operation

3 LM5125A-Q1 Function Block Diagram

The LM5125A-Q1 multiphase operation related block diagram is shown in Figure 3-1.

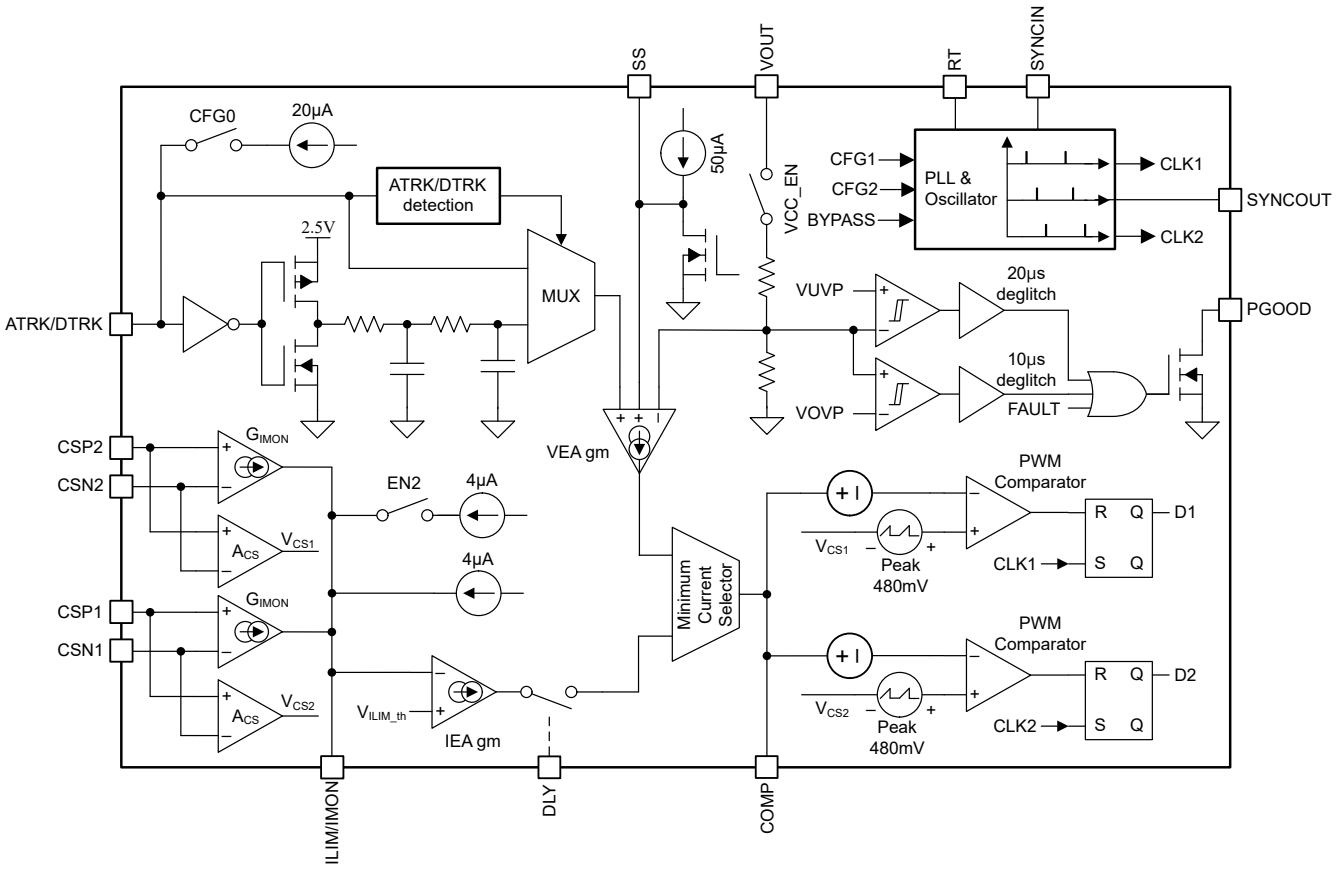

Figure 3-1. The LM5125A-Q1 Multiphase Phase Operation Related Block Diagram

The LM5125A-Q1's functionality differs when configured as Primary or Secondary. As illustrated in Figure 3-1, configuring the device as Secondary disables the following:

- OVP comparator and UVP comparator
- IEA gm and VEA gm
- Minimum Current Selector
- 50µA current source and discharge switch (connected to the SS pin)

See Table 3-1 for more information.

Table 3-1. Functionality when Configured as Primary or Secondary

Pin	Primary	Secondary
COMP	The voltage loop transconductance error amplifier (VEA gm) or the average current loop transconductance error amplifier (IEA gm) regulates the COMP pin voltage. The “Minimum Current Selector” selects the lower current. The COMP pin is the input of the PWM Comparators. Tie the compensation network between the COMP pin and AGND.	The “Minimum Current Selector” is disabled. The COMP pin receives the signal from the Primary and send the signal to the PWM Comparators. Tie to Primary COMP pin. Place the capacitor of the compensation network close the Secondary COMP pin to minimize the noise.
SS	An internal switch fully discharges the SS pin at start up, and then a 50µA current source charges the SS pin. Tie a capacitor between the SS pin and AGND.	The 50µA current source and the discharge switch are disabled. Tie to the Primary SS pin. Place a capacitor close to the Secondary SS pin to minimize noise pickup.
ILIM/IMON	Inductor current monitor and average input current limit setting pin. The ILIM/IMON pin sources a current proportional the current sense voltage of phase 1 and phase 2. When the ILIM/IMON reaches 1V, the average current loop reduces the current to limit the voltage on the ILIM/IMON pin to 1V.	The internal current sources are still active. The IEA gm is disabled. Tie to Primary ILIM/IMON pin.
ATRK/DTRK	The ATRK/DTRK pin sets the output voltage regulation target. Connect to analog tracking signal or digital tracking signal. Or, tie a resistor between the ATRK/DTRK pin and AGND, and enable the 20µA current source to program a fixed output voltage.	The VEA gm is disabled, so the ATRK/DTRK pin on the Secondary takes no effect. Tie to AGND.
DLY	Average input current limit extra delay setting pin. Tie a 10pF capacitor between the DLY pin and AGND.	The IEA gm is disabled, the DLY pin on the Secondary takes no effect.. Tie to AGND.
SYNCIN	Synchronize to the external clock input. Tie to AGND to use the internal clock. Tie to external clock input or AGND.	High: Bypass mode. Pulse: Synchronize to external clock input from the Primary. Low: Stop switching. Tie to Primary SYNCOUT.
SYNCOUT	High: Communicate bypass mode to Secondary. Pulse: Clock input for the Secondary SYNCIN. Low: Communicate stop switching to Secondary. Tie to Secondary SYNCIN.	The SYNCOUT is disabled. Tie to AGND.
PGOOD	PGOOD is pulled low under the following conditions: VOUT UVP VOUT OVP Device in SHUTDOWN state VCC regulator fault Thermal shutdown HBx fault ICL_latch fault CRC fault	PGOOD is pulled low under the following conditions: Device in SHUTDOWN state VCC regulator fault Thermal shutdown HBx fault ICL_latch fault CRC fault When the Secondary SYNCIN remains low (e.g., due to the Primary overvoltage)

4 LM5125A-Q1 Multiphase Operation Waveforms

4-phase Operation Waveform

The waveforms below were measured with using two LM5125AEVM-BST boards configured according to **Section 3.1.2 Configurations for Stacking Two EVMs** of the LM5125AEVM-BST EVM User's guide.

The primary EVM was modified by removing the SH-JP5.

The secondary EVM was modified by removing the soft-start (SS) capacitor (C8) and the compensation network (R5, C5, and C6).

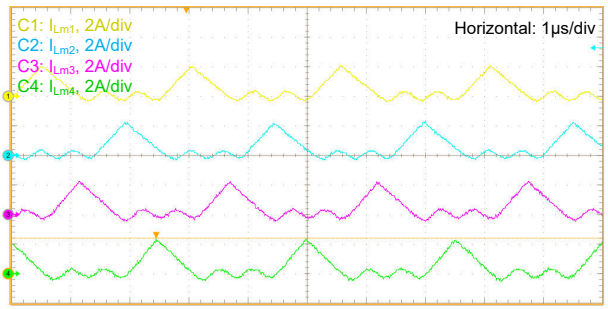

Figure 4-1. 4-phase, V_{IN} = 14V, V_{OUT} = 24V, DEM, I_{LOAD}= 1A

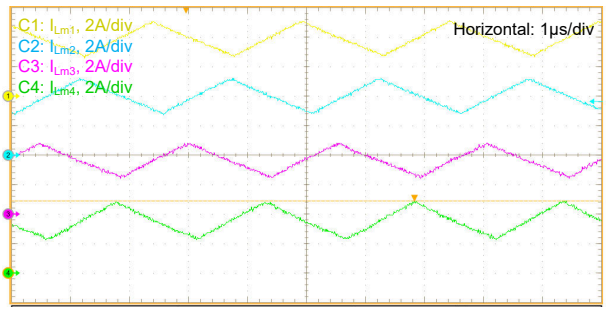

Figure 4-2. 4-phase, V_{IN} = 14V, V_{OUT} = 24V, DEM, I_{LOAD}= 20A

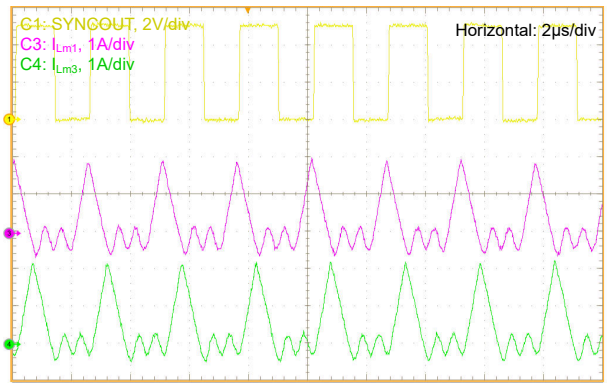

Figure 4-3. 4-phase, V_{IN} = 14V, V_{OUT} = 24V, DEM, I_{LOAD}= 1A

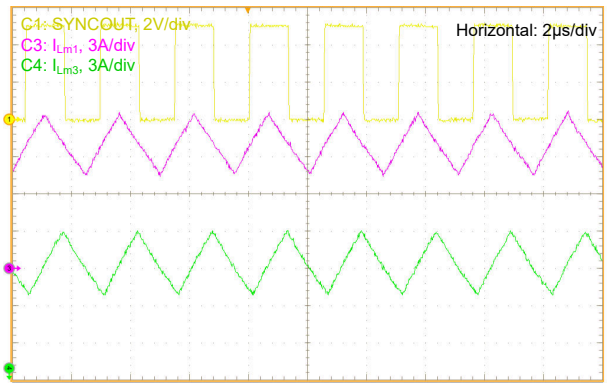

Figure 4-4. 4-phase, V_{IN} = 14V, V_{OUT} = 24V, DEM, I_{LOAD}= 20A

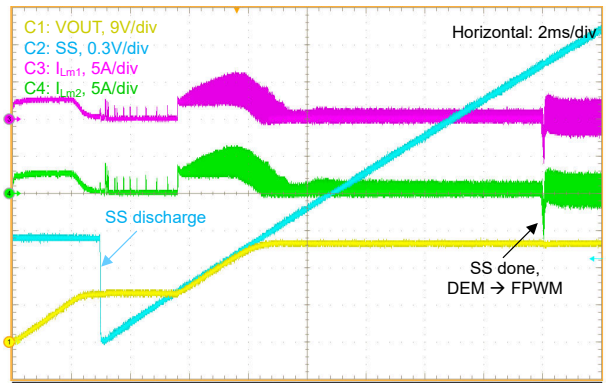

Figure 4-5. 2-phase soft start, V_{IN} = 12V, V_{OUT} = 24V, FPWM, I_{LOAD}= 0.1A

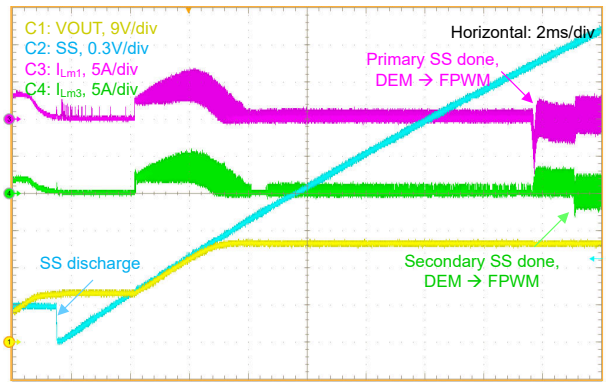

Figure 4-6. 4-phase soft start, V_{IN} = 12V, V_{OUT} = 24V, FPWM, I_{LOAD}= 0.1A

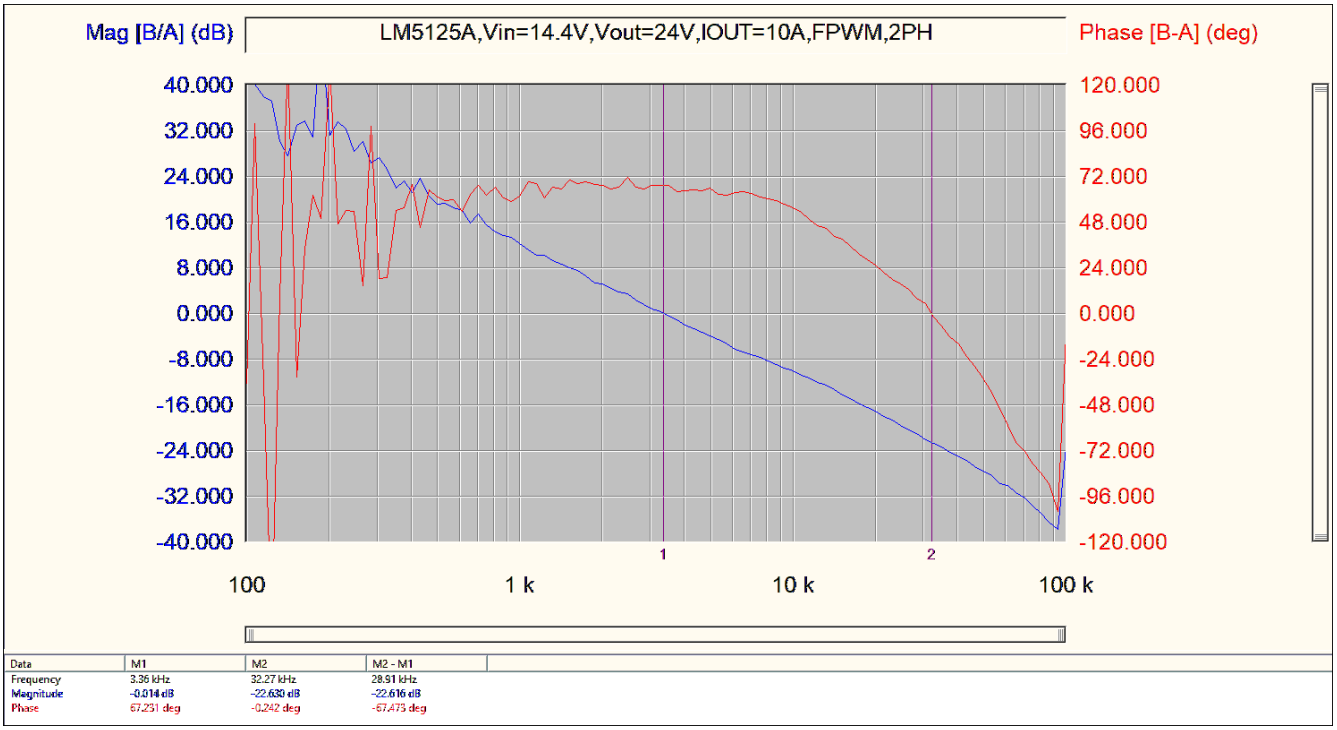

Figure 4-7. Bode plot of 2-phase setup, V_{IN} = 14.4V, V_{OUT} = 24V, I_{LOAD}= 10A

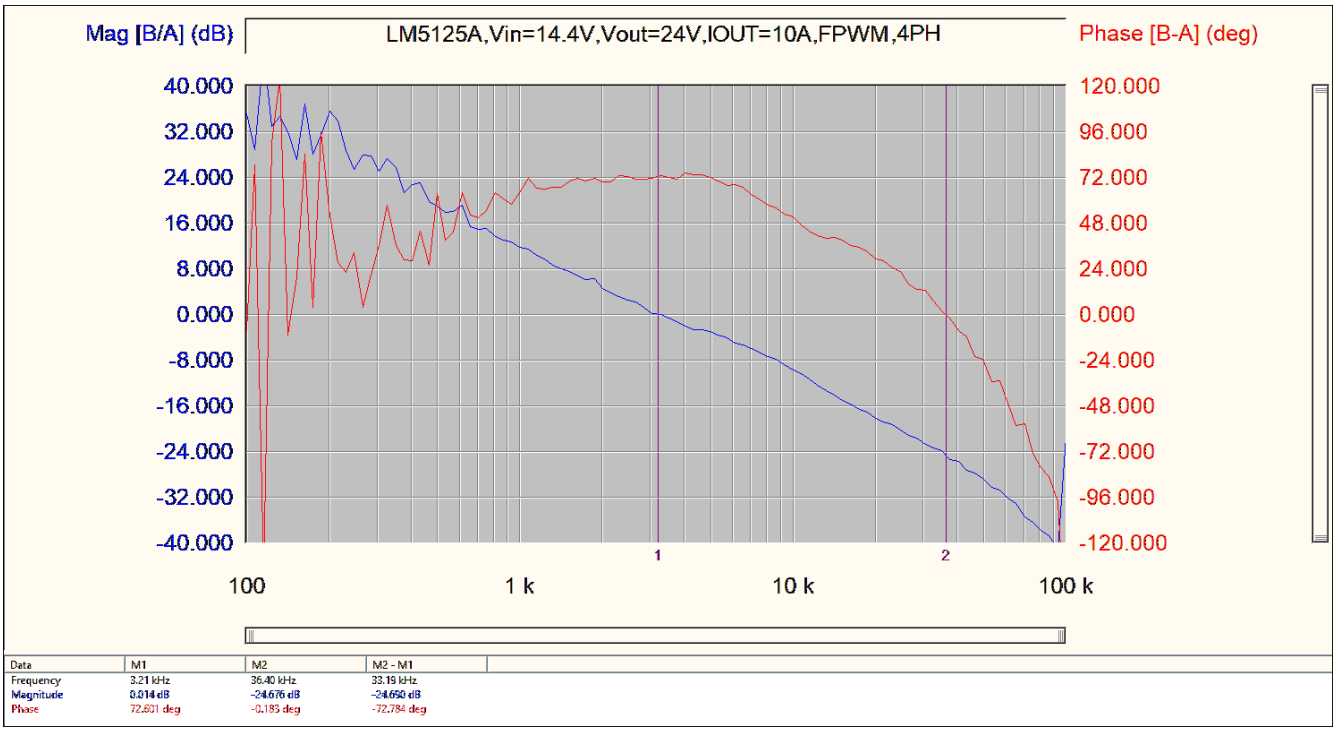

Figure 4-8. Bode plot of 4-phase setup, V_{IN} = 14.4V, V_{OUT} = 24V, I_{LOAD}= 10A

Note that the output capacitance doubles when the two EVMs are connected for a 4-phase setup. Consequently, the Bode plots for the 2-phase and 4-phase setups are very similar, which aligns with theoretical expectations.

3-phase Operation Waveform

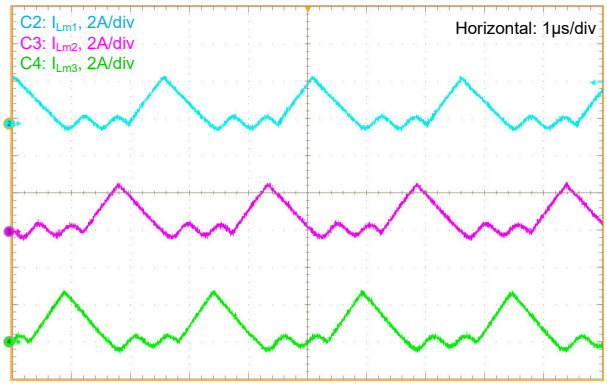

Figure 4-9. 3-phase, V_{IN} = 14V, V_{OUT} = 24V, DEM, I_{LOAD}= 1A

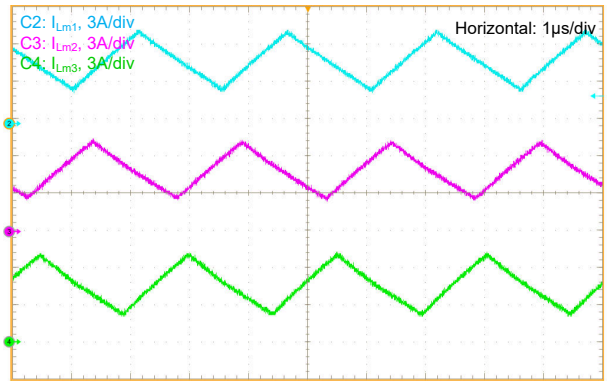

Figure 4-10. 3-phase, V_{IN} = 14V, V_{OUT} = 24V, DEM, I_{LOAD}= 8A

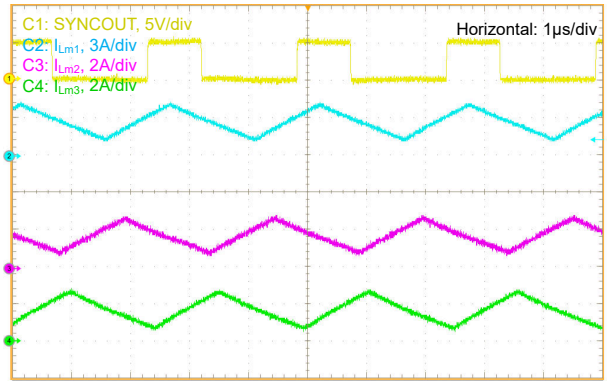

Figure 4-11. 3-phase, V_{IN} = 14V, V_{OUT} = 24V, DEM, I_{LOAD}= 1A

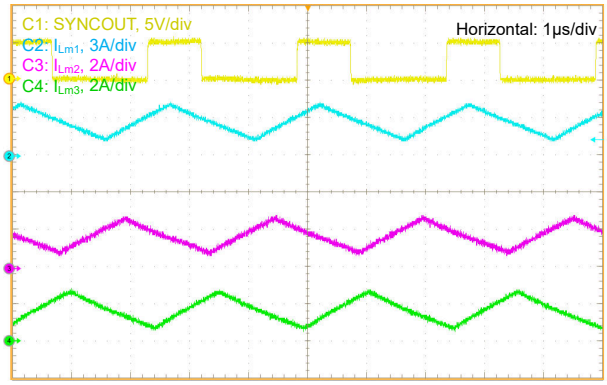

Figure 4-12. 3-phase, V_{IN} = 14V, V_{OUT} = 24V, DEM, I_{LOAD}= 8A

5 Summary

This application note introduces LM5125A-Q1 3-phase and 4-phase operation setups. Then, the LM5125A-Q1 multiphase phase operation related block diagram is presented. The functionalities are described for configurations as Primary or Secondary. Finally, some waveforms are shown and analyzed.

6 References

- Texas Instruments, LM5125A-Q1, Wide-VIN 2.2MHz dual-phase boost controller with VOUT tracking
- Texas Instruments, LM51251A-Q1, Wide-VIN 2.2MHz dual-phase boost controller with VOUT tracking and I2C
- Texas Instruments, LM5126A-Q1, Wide-VIN 2.2MHz single-phase boost controller with VOUT tracking
- Texas Instruments, LM51261A-Q1, Wide-VIN 2.2MHz single-phase boost controller with VOUT tracking and I2C

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