Application Note

Using Low-Noise Buck TPS6291X to Power CMOS Sensor

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ABSTRACT

This paper presents a design for powering CMOS image sensors using the TI TPS6291X series buck converter. By employing the TPS6291X, the system eliminates the need for a dedicated linear and low-dropout regulator (LDO) while still delivering high power supply rejection ratio (PSRR) and low output voltage ripple to meet CMOS AVDD power supply requirements, thereby reducing overall system power consumption. The AVDD requirements of CMOS sensors are discussed, and the capability of the TPS6291X is validated through experimental results covering output ripple and load transient. Furthermore, design considerations for achieving LDO-equivalent performance with the TPS62912 are presented and compared against conventional designs.

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1 Introduction

With the rapid development of short video platforms and the requirement for convenient access to video recording products, a lot of portable handheld products are blooming in the market. Handheld products are a combination of battery, mother board, and the camera module. Camera module requires a low voltage ripple, high PSRR and low noise analog power supply to provide high quality graphics in photos or video. Battery then requires high efficiency system structure to support extend use of device. From these perspectives, a high efficiency, low noise system structure is required to improve the performance of portable handheld products.

Figure 1-1 is the conventional system block diagram of CMOS power supply.

To power these three inputs, the conventional architecture employs either a buck or bypass boost converter as the primary power supply, followed by three LDOs as secondary power supplies. The selection between buck and bypass boost converters depends on the battery cell configuration. The LDOs effectively attenuate ripple and noise from the buck or boost converter, providing a clean power input for the CMOS sensor.

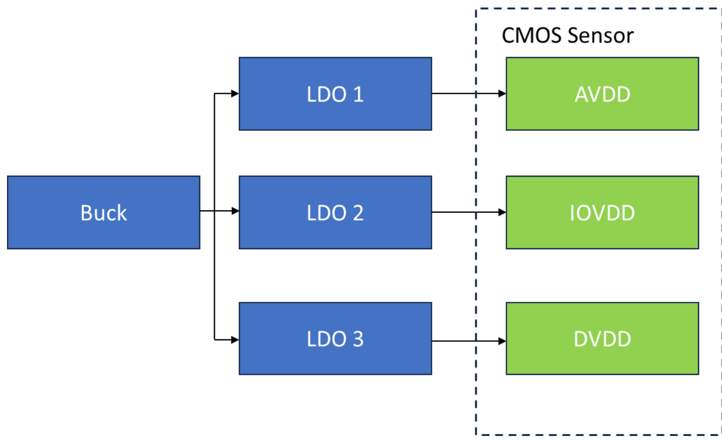

Figure 1-1. Conventional CMOS Sensor Power Supply System

This architecture is widely adopted and well-validated. However, LDOs operating in the linear region exhibit significant power dissipation due to the voltage differential between input and output.

Consequently, replacing the LDO with a buck converter can substantially reduce power consumption. Figure 1-2 demonstrates the use of the TPS62912 as an LDO replacement.

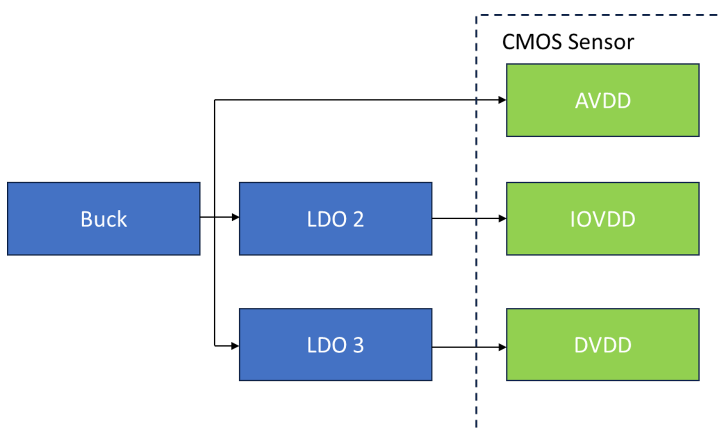

Figure 1-2. Replace LDO by Using TPS6291X

In next section, the power supply requirements of CMOS sensor are discussed and TPS62912 performances are tested and verified.

2 CMOS AVDD requirements

CMOS sensors typically require three power supplies: AVDD, DVDD, and IOVDD. AVDD powers the imaging pixel array, column analog block, and column logic block. DVDD supplies the image processing block, while IOVDD powers the CSI-2 interface and I^2C interface, among others. AVDD demands the cleanest power supply to maintain the dynamic range and signal-to-noise ratio (SNR) within the specifications provided by the CMOS sensor manufacturer.

Table 2-1 shows two common CMOS sensor power supply requirements.

Table 2-1. CMOS Sensor Power Supply Requirements

CMOS Sensor	AVDD(Typical)	DVDD(Typical)	IOVDD(Typical)
1	2.9V	1.1V	1.8V
2	2.8V	1.5V	1.8V

Based on specifications released by CMOS sensor manufacturers and product design companies, AVDD has the most stringent power supply requirements. In camera image and video quality testing, low noise is a critical performance indicator. When covering the camera with black tape and capturing a photograph, an ideal image is completely black. However, due to AVDD variations during row scanning, the brightness of each row differs, causing variations in row brightness that manifest as visible stripes in the image.

3 TPS62912 Performance and Design Considerations

Based on above section, a low-noise, low-ripple, high-PSRR Buck is needed to reduce the power consumption and improve the CMOS sensor image quality. TPS62912/3 is a low noise and low ripple buck converter that integrated ferrite bead filter compensation to support second-order LC filter to further decrease the output voltage noise and ripple.

3.1 Steady-State Operation Performance

Table 3-1 shows the specification during the test. The evaluation was conducted using the TPS62913 EVM.

Table 3-1. Test Specifications

Specification	Test Conditions	TYP	Unit
Input Voltage	Electrical Load	3.6	V
Output Voltage	SMA Probe	2.8	V
Output Current	Electrical Load	200	mA
Switching Frequency	JP2 to VIN	2.2	Mhz

The output voltage and current were configured according to CMOS AVDD requirements, with the input voltage set to 3.6V to simulate a single-cell battery power supply.

Figure 3-1 shows the output voltage. Importantly, SMA cable must be used to detect output voltage to truly reflect noise and ripple level.

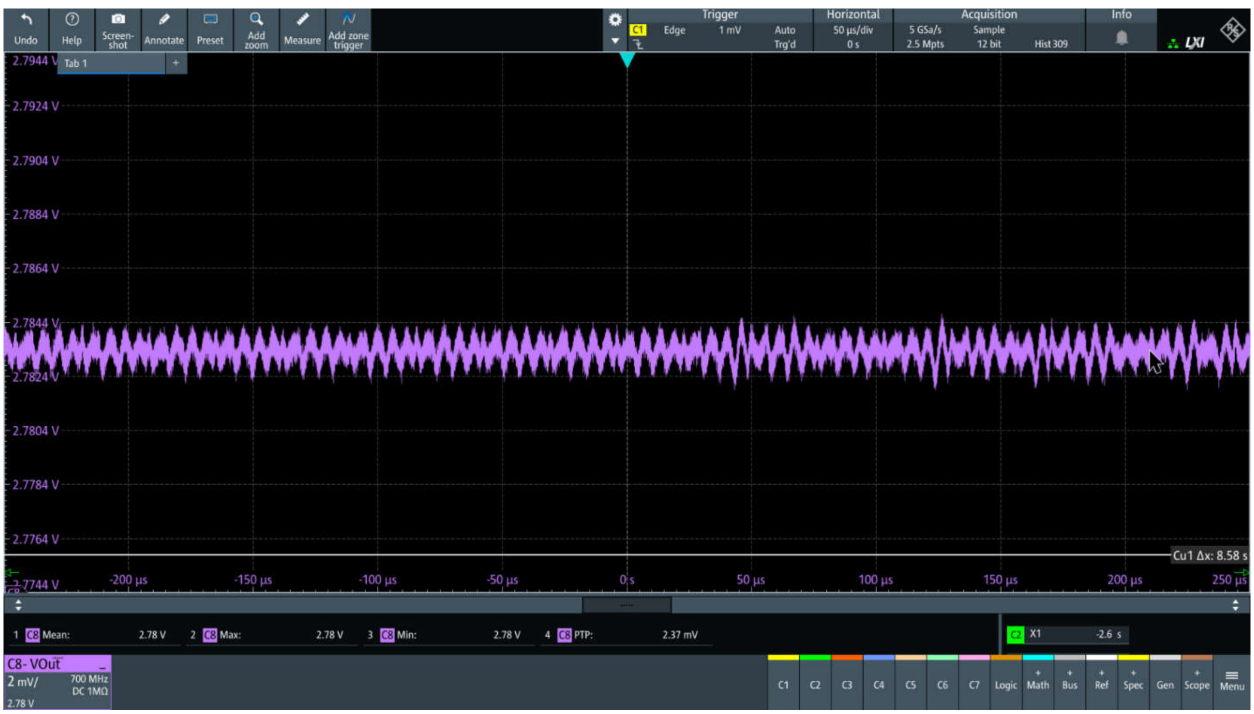

Figure 3-1. Output Voltage of TPS62913

Figure 3-1 demonstrates that the peak-to-peak voltage is approximately 2.37mV.

3.2 Output Voltage Ripple Performance With Long Cable

In practical applications, the CMOS module power supply is located on the main board and uses a FPC connector to deliver power to the CMOS sensor. This configuration introduces extended traces between the load and the buck converter IC. To further investigate the influence of long traces, an 8cm trace was added to the test setup.

Figure 3-2. Output Voltage of TPS62913 With 8cm Long Trace

Figure 3-2 shows that the spike increased to 26.12mV and the frequency corresponds to switching frequency.

Importantly, this spike does not come from the buck itself, and is primarily a measurement artifact. The long trace or FPC connector creates a large loop for power supply, noise couples into the probe during measurement.

To reduce the spike, an SMA cable with a DC blocker and AC coupling in the oscilloscope can be used to observe the actual ripple voltage level. Alternatively, an SMA cable with a decoupling capacitor placed near the test point can mitigate the measurement spike.

Figure 3-3 shows the result with 100nF or 470nF capacitor also with 8cm connection from load to TPS62913 EVM.

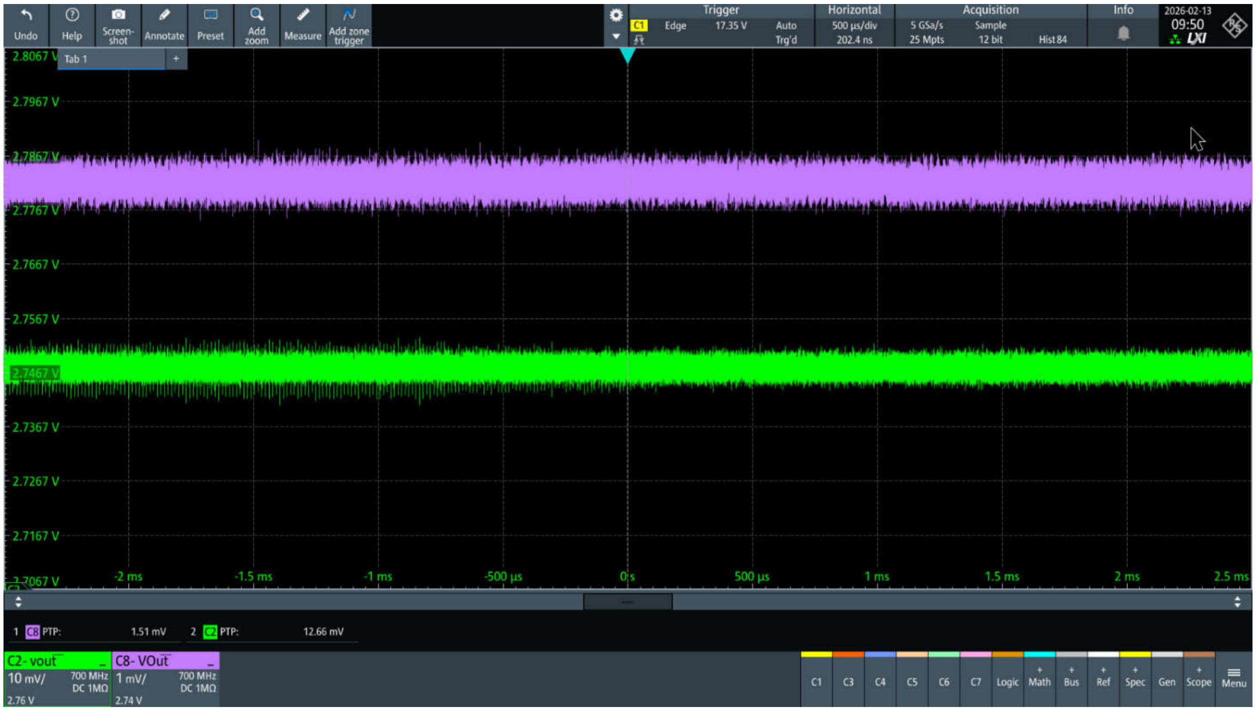

Figure 3-3. Output Voltage of TPS62913 With 8cm Long Trace With 100nF Capacitor

The purple trace represents the voltage measured at the TPS62913 EVM test point, while the green trace shows the measurement at the load side. As illustrated, the peak-to-peak voltage ripple measured at the load side decreased from 27mV to 12.6mV, representing an approximately 53% reduction.

Subsequently, the test was repeated using a 470nF capacitor. As shown in Figure 3-4, the peak-to-peak voltage ripple measured at the load side decreased from 27mV to 6.49mV, representing an approximately 70% reduction.

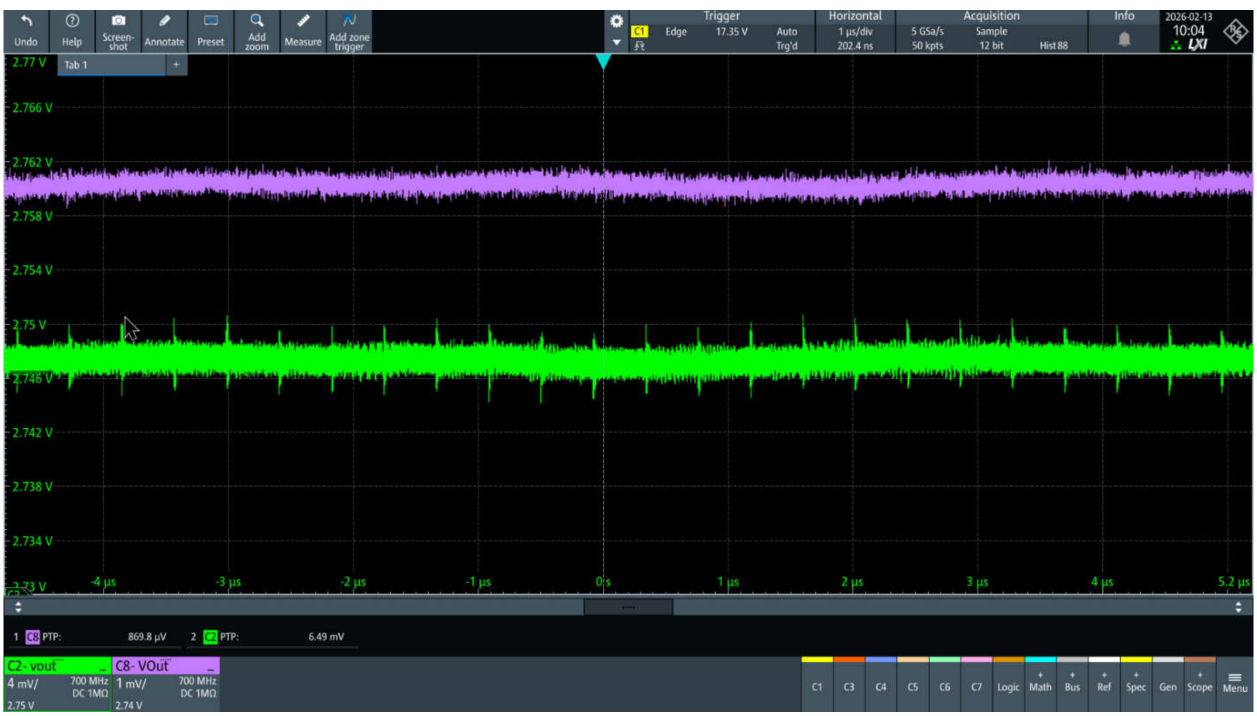

Figure 3-4. Output Voltage of TPS62913 With 8cm Long Trace With 470nF Capacitor

3.3 TPS62912 and LDO Performance Comparison in Actual Board Implementation

After addressing the measurement spike issue, the performance of the TPS62912 and LDO can be compared.

Figure 3-5 and Figure 3-6 illustrate the voltage ripple differences in the CMOS module between the buck converter and LDO under an 8K, 30-fps recording configuration.

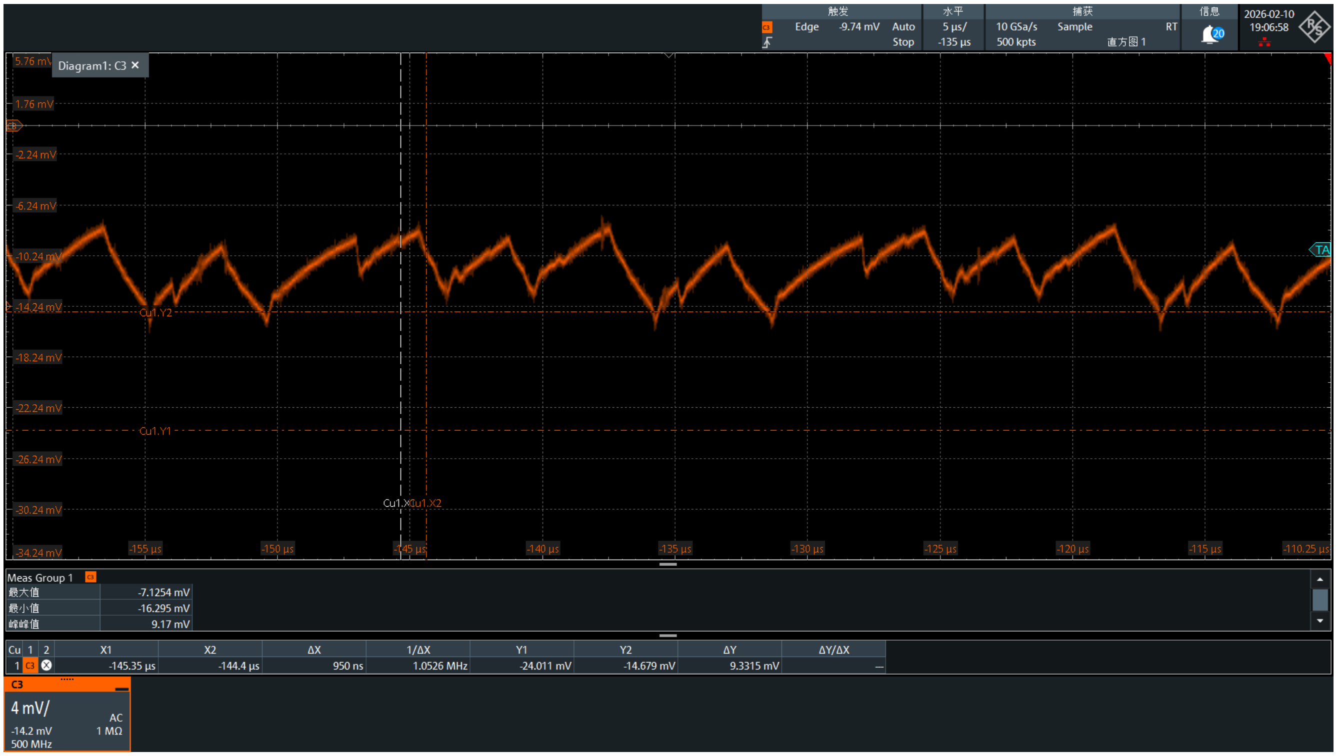

Figure 3-5. Output Voltage of LDO in 8k/30fps Recording Donfiguration

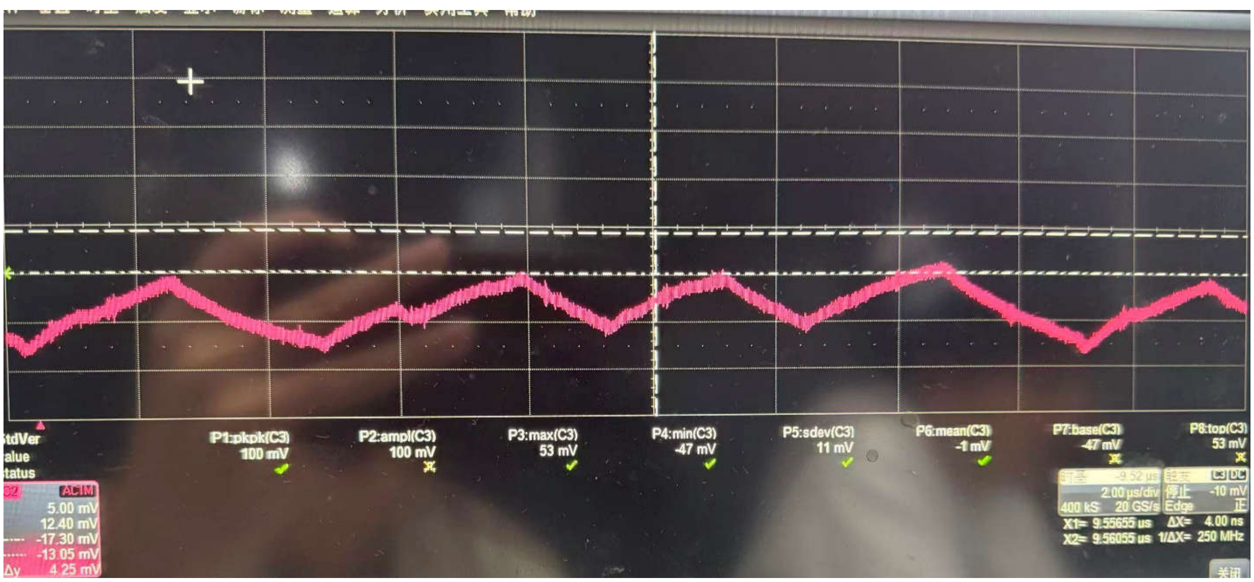

Figure 3-6. Output Voltage of Buck in 8k/30fps Recording Configuration

Compared between Figure 3-5 and Figure 3-6, the average voltage ripple and peak to peak voltage is close. Average voltage around -11.5mV and peak to peak voltage is about 9mV.

Based on these results, image quality testing was conducted to evaluate the actual performance of the buck converter and LDO. The image quality assessment employed a black frame test, which involves capturing an image in a completely dark environment to evaluate noise performance, as discussed in Section 2.

The results are as below:

Table 3-2. Row Noise Ratio Comparison Between LDO and TPS62912

Device	Row noise ratio
LDO	0.08
TPS62912	0.1

The input and output capacitors of the TPS62912 were identical to those on the EVM board. The results indicate that the TPS62912 row noise performance is inferior to that of the LDO.

As previously discussed, the average ripple and peak-to-peak voltage are comparable between the LDO and buck converter. Upon further analysis, the loop response was identified as the key performance differentiator. The LDO exhibits a faster loop response than the TPS62912.

Based on this finding, a 100pF feed-forward capacitor was added to evaluate the performance change in the TPS62912 output voltage.

Figure 3-7. Output Voltage of Buck With and Without Feedforward Capacitor

The left side shows the board without the 100pF capacitor, while the right side shows the board with the 10-pF capacitor.

By incorporating a 100pF capacitor in the feedback loop, Figure 3-7 demonstrates that while the peak-to-peak voltage remains unchanged, the response time with the 100pF capacitor is reduced to 60µs, compared to 90µs without the capacitor. More significantly, the addition of the capacitor substantially reduces the spike amplitude and produces a smoother waveform.

Based on these findings, a 100pF capacitor was added to the board and connected to the CMOS sensor for row noise retesting. Table 3-3 presents the results with the 100pF feedforward capacitor.

Table 3-3. Row Noise Ratio Comparison Between LDO and TPS62912 With 100pF Feedforward Capacitor

Device	Row noise ratio
LDO	0.0760
TPS62912	0.0764

Based on the results, feedforward capacitor can largely increase the noise performance of TPS62912 and close to LDO.

4 Design Considerations

To enable the TPS62912 single-buck design to deliver performance equivalent to an LDO, the following design considerations are summarized.

4.1 Measurement Spike Mitigation

To eliminate measurement-induced spikes, an SMA cable with a DC blocker and AC coupling provides the most accurate representation of output voltage. In the absence of a DC blocker, an SMA cable with a decoupling capacitor placed near the test point can achieve similar results.

4.2 Feedforward Capacitor for Enhanced Loop Response

CMOS sensors present loads with rapid and multiple load transients. Due to the double pole formed by the LC filter and ferrite bead, the TPS62912 exhibits a slower loop response compared to LDOs. This slower response can result in insufficient settling time before the next load transient occurs, contributing to row noise issues. The design involves improving the loop response speed by adding a feedforward capacitor to increase the crossover frequency.

5 Conclusion

The TPS6291X series, utilizing a second-order LC filter and integrated loop compensation, significantly enhances voltage ripple and noise performance. Compared to conventional buck-plus-LDO architectures, the TPS6291X can function as a single buck converter while providing low noise and output voltage ripple characteristics that satisfy load requirements. This approach offers substantial power consumption advantages over LDO-based designs.

During practical testing, measurement artifacts and loop response limitations can cause the TPS62912 to exhibit inferior performance compared to LDOs. These factors must be carefully evaluated and addressed through proper design practices.

6 Reference

- Texas Instruments, *TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter with Integrated Ferrite Bead Filter Compensation* datasheet.
- Texas Instruments, *TPS6291x Step-Down Converter Evaluation Module User's Guide*
- Texas Instruments, *Feedforward Capacitor to Improve Stability and Bandwidth with the TPS621-Family and TPS821-Family* application report.
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.