Functional Safety Information

LMK3H0102-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LMK3H0102-Q1 (RGT package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

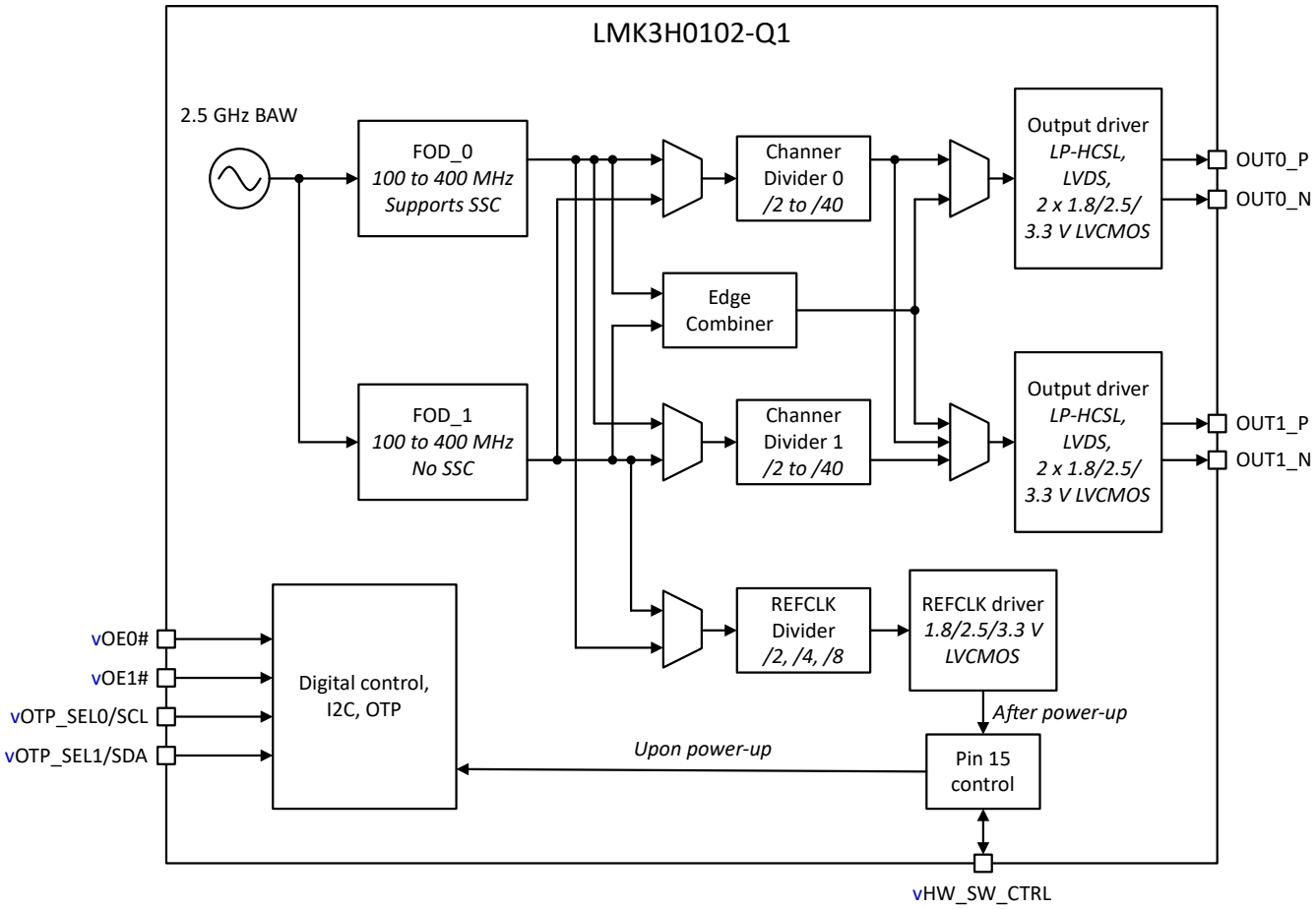

Figure 1-1. Functional Block Diagram

The LMK3H0102-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LMK3H0102-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	9
Die FIT rate	3
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 230mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LMK3H0102-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Performance degradation of output clocks	25
Incorrect output frequencies, poor timing accuracy	25
No output clocks	20
Loss of I2C communication	20
Part in an undefined state due to incorrect start up or power-on reset	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMK3H0102-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LMK3H0102-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMK3H0102-Q1 data sheet.

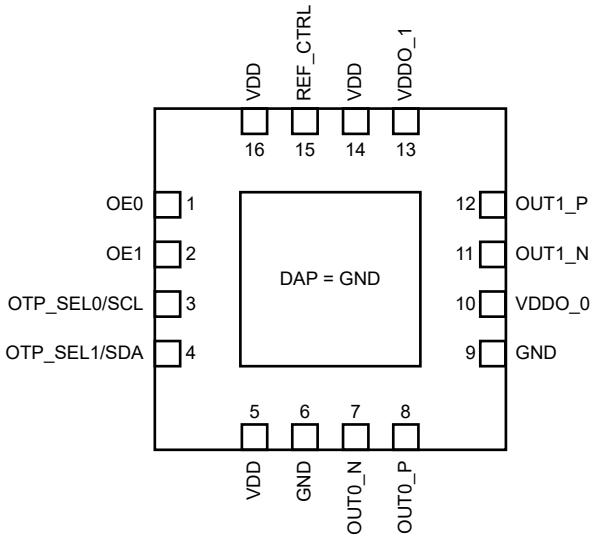

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VDD = VDDO_0 = VDDO_1 = 3.3V
- OE0 and OE1 are floating (internal pull-down enabled)
- Device is configured to I2C-Mode
- OTP_SEL0/SCL and OTP_SEL1/SDA are connected to a I2C bus
- OUT0 configured to 100MHz LP-HCSL
- OUT1 configured to 100MHz AC-LVDS
- REF_CTRL configured to 33.33MHz LVCMOS output

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OE0	1	Output OUT0 enabled. Normal operation.	D
OE1	2	Output OUT0 enabled. Normal operation.	D
OTP_SEL0/SCL	3	No I2C communication is possible.	B
OTP_SEL1/SDA	4	No I2C communication is possible.	B
VDD	5	Power-ground short can damage the device.	A
GND	6	No effect. Normal operation.	D
OUT0_N	7	Output pulled low. No output clock.	B
OUT0_P	8	Output pulled low. No output clock.	B
GND	9	No effect. Normal operation.	D
VDDO_0	10	Output OUT0 not functional.	B
OUT1_N	11	Output pulled low. No output clock.	B
OUT1_P	12	Output pulled low. No output clock.	B
VDDO_1	13	Output OUT1 not functional.	B
VDD	14	Power-ground short can damage the device.	A
REF_CTRL	15	Output pulled low. No output clock.	B
VDD	16	Power-ground short can damage the device.	A
DAP	17	No effect. Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OE0	1	Output OUT0 enabled. Normal operation.	D
OE1	2	Output OUT0 enabled. Normal operation.	D
OTP_SEL0/SCL	3	No I2C communication is possible.	B
OTP_SEL1/SDA	4	No I2C communication is possible.	B
VDD	5	With this pin open, the device has a weaker VDD connection than intended by design. Other VDD pins maintain connection. Performance degradation is possible.	C
GND	6	With this pin open, the device has a weaker ground connection than intended by design. Other ground pins maintain connection. Performance degradation is possible.	C
OUT0_N	7	Normal Operation. Device is not impacted. Load in the system does not receive the clock signal.	D
OUT0_P	8	Normal Operation. Device is not impacted. Load in the system does not receive the clock signal.	D
GND	9	With this pin open, the device has a weaker ground connection than intended by design. Other ground pins maintain connection. Performance degradation is possible.	C
VDDO_0	10	Output OUT0 not powered. No output.	B
OUT1_N	11	Normal operation. Device is not impacted. Load in the system does not receive the clock signal.	D
OUT1_P	12	Normal operation. Device is not impacted. Load in the system does not receive the clock signal.	D
VDDO_1	13	Output OUT1 not powered. No output.	B
VDD	14	With this pin open, the device has a weaker VDD connection than intended by design. Other VDD pins maintain connection. Performance degradation is possible.	C
REF_CTRL	15	Normal operation. Device is not impacted. Load in the system does not receive the clock signal.	D
VDD	16	With this pin open, the device has a weaker VDD connection than intended by design. Other VDD pins maintain connection. Performance degradation is possible.	C
DAP	17	With this pin open, the device has a weaker ground connection than intended by design. Other ground pins maintain connection. Performance degradation is possible.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OE0	1	OE1	No effect. Normal operation.	D
OE1	2	OTP_SEL0/SCL	No I2C communication is possible. Output OUT1 disabled due to I2C bus pull up.	B
OTP_SEL0/SCL	3	OTP_SEL1/SDA	No I2C communication is possible.	B
OTP_SEL1/SDA	4	VDD	Not considered. Corner pin.	D
VDD	5	GND	Power-ground short can damage the device.	A
GND	6	OUT0_N	Output pulled low. No output clock.	B
OUT0_N	7	OUT0_P	No output.	B
OUT0_P	8	GND	Not considered. Corner pin.	D
GND	9	VDDO_0	Power-ground short can damage the device.	A
VDDO_0	10	OUT1_N	Output pulled high. No output clock. Long periods of high current flow through output transistors can cause device damage.	A
OUT1_N	11	OUT1_P	No output.	B
OUT1_P	12	VDDO_1	Not considered. Corner pin.	D
VDDO_1	13	VDD	No effect. Normal operation.	D
VDD	14	REF_CTRL	Output pulled high. No output clock.	B
REF_CTRL	15	VDD	Output pulled high. No output clock.	B
VDD	16	OE0	Not considered. Corner pin.	D
DAP	17	all pins	DAP is connect to ground, behavioris the same as described in Table 4-2	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OE0	1	OE0 pulled high. Output OUT0 disabled.	B
OE1	2	OE1 pulled high. Output OUT1 disabled.	B
OTP_SEL0/SCL	3	No I2C communication is possible.	B
OTP_SEL1/SDA	4	No I2C communication is possible.	B
VDD	5	No effect. Normal operation.	D
GND	6	Power-ground short can damage the device.	A
OUT0_N	7	Output pulled high. No output clock. Long periods of high current flow through output transistors can cause device damage.	A
OUT0_P	8	Output pulled high. No output clock. Long periods of high current flow through output transistors can cause device damage.	A
GND	9	Power-ground short can damage the device.	A
VDDO_0	10	No effect in the described operation mode. Normal operation.	D
OUT1_N	11	Output pulled high. No output clock. Long periods of high current flow through output transistors can cause device damage.	A
OUT1_P	12	Output pulled high. No output clock. Long periods of high current flow through output transistors can cause device damage.	A
VDDO_1	13	No effect in the described operation mode. Normal operation.	D
VDD	14	No effect. Normal operation.	D
REF_CTRL	15	Output pulled high. No output clock.	B
VDD	16	No effect. Normal operation.	D
DAP	17	Power-ground short can damage the device.	A

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